STM32U5

ULPMark-PeripheralProfile and LPBAM use case consumption

Hello, and welcome to this presentation on the ULPMark peripheral profile, which measures the energy impact of common peripheral on deep-sleep, and highlights the benefits offered by the Low-power background autonomous mode (or LPBAM) of the STM32U5.

ULPMark overview

- Ultra-Low Power (ULP) is a major challenge for MCU design
- ST deploys creative design techniques to reduce power consumption
- EEMBC ULPMark quantifies these tradeoffs and compares different reference designs by measuring multiple aspects of MCU energy efficiency
  - Each MCU vendor can promote the score of their latest design
- At ST, we measure, certify and publish the scores of all our STM32 families
- Developers are increasingly relying on these scores rather than datasheet figures for typical power efficiency use cases.

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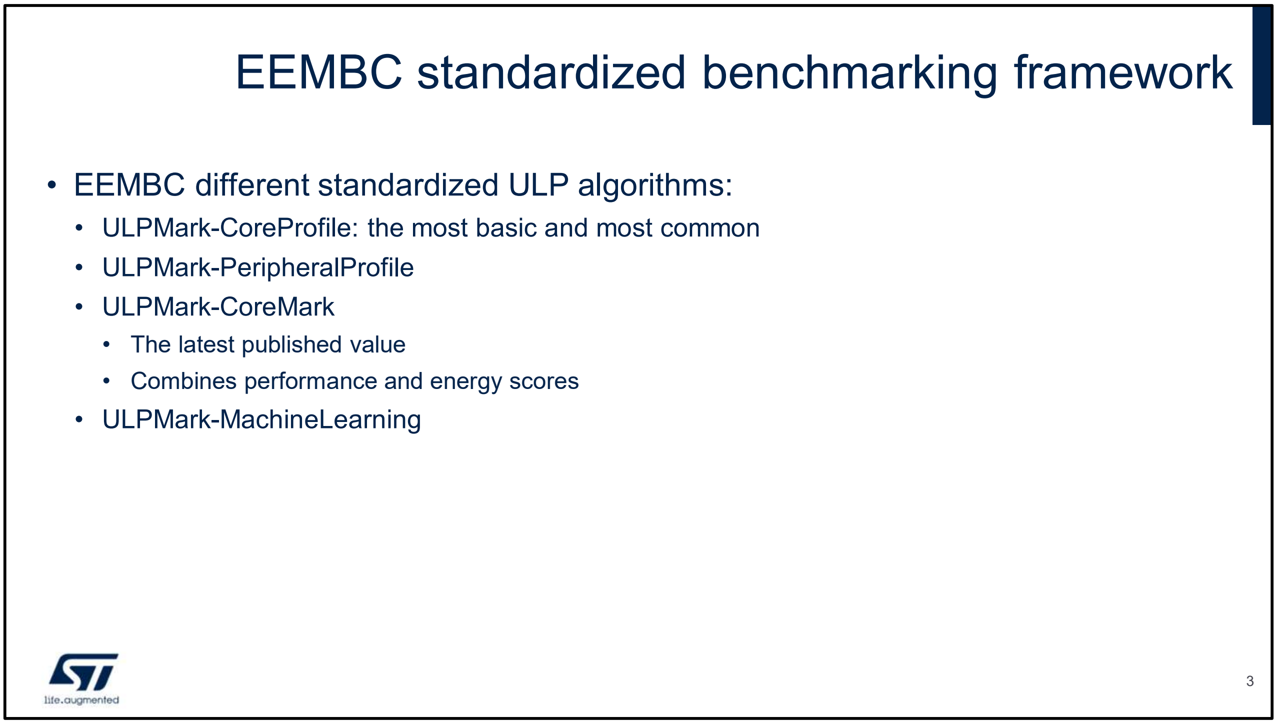
Ultra-low power (or ULP) is a major design challenge facing MCU today, as many systems are battery powered, especially in the IOT domain.
STMicroelectronics deploys creative design techniques to reduce power consumption. The STM32U5 series offers advanced power-saving microcontrollers, to meet the most demanding power/performance requirements for smart applications.
The Embedded Microprocessor Benchmark Consortium or EEMBC, develops industry-standard benchmarks for the hardware and software used in autonomous driving, mobile imaging, the Internet of Things, mobile devices, and many other applications.
The ULP subcommittee focuses on power and energy.

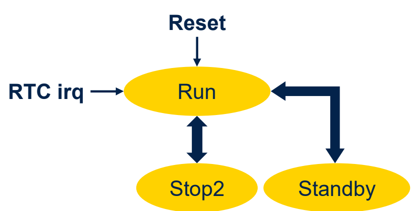
Scores that are certified have undergone a rigorous analysis by the EEMBC Certification Lab. Certification is a benefit only available to members, and guarantees that the score adheres to the official run-rules for that benchmark.
ST measures, certifies and publishes the scores of all STM32 families.
Since the ULP mark scores are an unbiased way to compare the performance of microcontrollers, developers increasingly rely on these scores rather than on metrics found in datasheets.



In 2014, the ULP team introduced the ULPMark-CoreProfile (or -CP for short). This benchmark runs an active workload for a period of time, then goes to sleep. The energy measurement during the duty cycle reflects a real-life test of embedded low power, beyond a simple sleep count.
The ULPMark-PeripheralProfile (or -PP for short) launched in 2016, examines the energy cost of four peripherals: real-time clock, pulse-width modulation, analog-to-digital conversion, and SPI communication.
ULPMark-CoreMark (or ULPMark-CM for short) launched in 2019 measures the energy of CoreMark in a consistent environment. It is EEMBC's first active-power benchmark.
For measuring the energy costs of neural-net inference in embedded devices, EEMBC offers ULPMark-ML.

ULPMark-PP benchmark

- ULPM-PP measures the power consumption of the commonly used peripherals
- PWM, ADC, SPI and RTC



Slot	ADC		PWM				SPI	RTC
	Number of samples	Conversion rate	Freq.	Period	Duty	Pulses		
1	64	1 KHz	32.768 KHz	255	10%, fixed	20		Setup & start timer
2	64	1 KHz Buffered evaluation	32.768 KHz	255	20%, Increase	40		
3	1	1 Hz	32.768 KHz	255	30%, fixed	40		
4	1	1 Hz	32.768 KHz	255	40%, fixed	100	Tx: 128 bytes	
5	1	1 Hz	32.768 KHz	255	50%, fixed	100	Check last Rx Tx: 128 bytes	
6	1	1 Hz	32.768 KHz	255	60%, fixed	100	Check last Rx Tx: 128 bytes	
7	1	1 Hz	32.768 KHz	255	70%, fixed	100	Check last Rx Tx: 128 bytes	
8	1	1 Hz	32.768 KHz	255	80%, fixed	100	Check last Rx Tx: 128 bytes	
9	1	1 Hz	1 MHz	10000	10%, increase	30	Check last Rx Tx: 128 bytes	
10	Off Check slot's 3-9 data		Off				Check last Rx	Stop & check

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ULPMark-PP focuses on the MCU's most commonly used peripherals like pulse-width modulation (PWM), analog-to-digital conversion (ADC), serial peripheral interface (SPI), and real-time clock (RTC).
This benchmark defines ten one-second activity slots, each with variable usage of ADC, SPI, PWM, RTC, allowing the MCU and peripherals to sleep after their activities have completed.
The table gives an overview of the activity in each slot. As soon as the device finishes the peripheral operation for that slot, it can enter Standby or Stop 2 mode.
This means faster peripherals will most likely score higher since they can remain off longer.
ULPMark has been redesigned since its first release in

2014. It now works with the EEMBC benchmark framework, the same one used
by IoTMark and SecureMark, with a super-thin API that enables any MCU to execute next generation EEMBC benchmarks.
In slot one, there is one processor wakeup per sample, while in slot 2, there is a unique wakeup after 64 samples.

Architecture Optimization in STM32U5

- STM32U5 architecture introduced LPBAM (Low-power Background Autonomous Mode)
  - IPs running autonomously in STOP2 mode drastically reduce consumption

	STM32U5
LPTIM mode up	**LPDMA linked-list transfer**
LPTIM mode fixed	Repetition counter
STOP2 mode	RTC **LPTIM1,3,4** **ADC4** **SPI3** **LPDMA**
Slot 2	ADC with LPDMA **in STOP2**
Slot 4/5/6/7/8	SPI with LPDMA **in STOP2**
Slot 9	PWM at 1 MHz **in STOP2**
Clock	MSIS, LSE, **MSIK**

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Several peripherals support the autonomous mode which allows it to be functional and perform DMA transfers in Stop 0, Stop 1, and Stop 2 modes. In addition, the low-power background autonomous mode (LPBAM) is supported in Stop 2 mode, allowing to build more complex use cases with autonomous peripherals, without any CPU wake-up thanks to DMA transfers.

In this autonomous mode, the Cortex-M33 core and most of the peripherals can remain inactive.

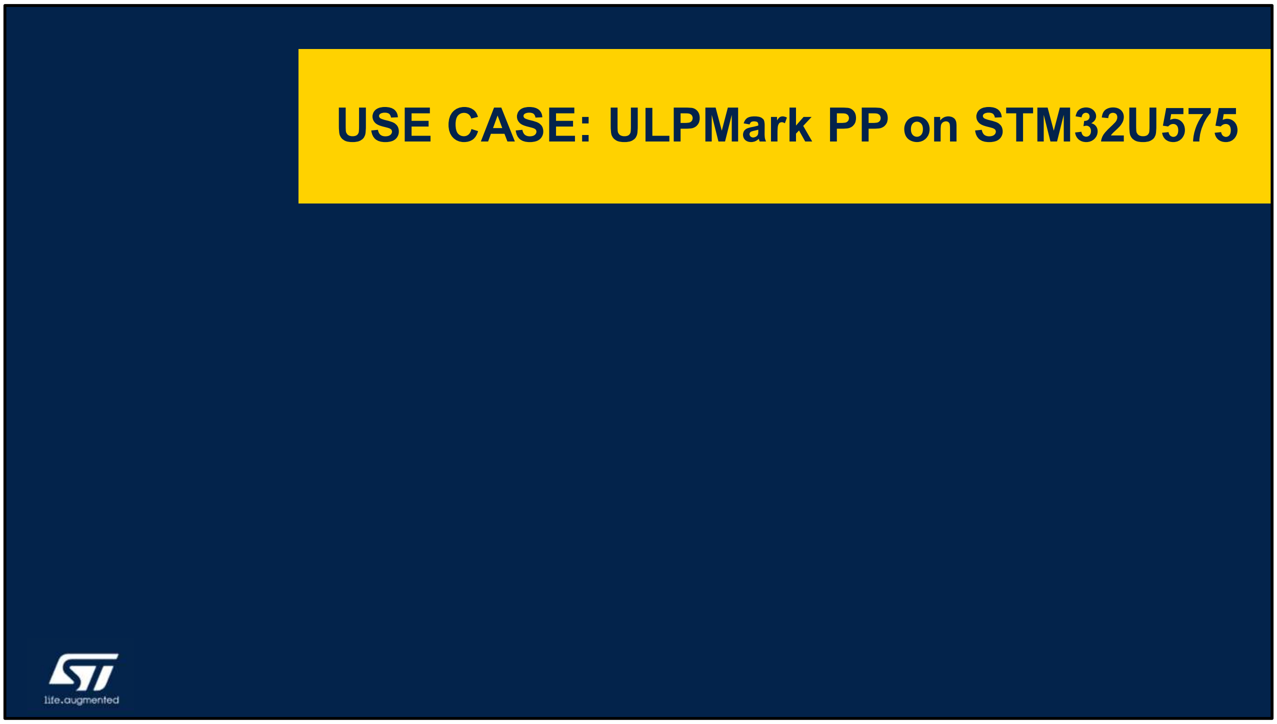
In Stop 2 mode, the CPU Domain is in retention, no dynamic activity is possible, while the Smart Run Domain (or SRD) is fully powered.

SRD autonomous peripherals are functional thanks to the LPDMA and the SRAM4.

The Low power timer can be used by STM32U5 to trigger a series of transfers performed by the LPDMA.
To periodically trigger events over a large period of time, the STM32U5 can use the repetition counter capability of the low power timer instead of the real time clock.
RTC, low power timers number 1, 3 and 4, ADC4, SPI3 and LPDMA belong to the SRD, as does SRAM4.
With respect to the ULPM-PP benchmark, STM32U5 can implement LPBAM in stop 2 mode as follows:

- ADC4 with LPDMA in slot 3
- SPI3 with LPDMA in slots 4, 5, 6, 7 and 8
- PWM in slot 9.

The MSIK oscillator present in STM32U5, generates a clock that is independent of the system clock and therefore convenient for peripherals that require a fixed clock, while the system clock may be gated off.



Now, we will move on to a practical example of consumption measurement with the ULPMark Peripheral Profile on an STM32U575. These values depend on the product .
For other references of this series, please refer to documentation of the concerned product.

Analyzing PP consumption waveform

This slide details the consumptions in the 10 one-second activity slots of the ULPMark-PP benchmark.
The STM32Cube power consumption calculator, is used to provide these metrics.
The microcontroller is in run mode at the beginning of each slot, to initialize the peripherals which are active in the current slot.
Once initialized, the peripherals collaborate to perform background tasks, while the microcontroller is in stop 2 mode.
The consumption is approximately 4 microamperes in stop 2.
In slots 1, 2,3, 9 and 10, standby mode is entered, which decreases the power consumption down to 1 micro ampere, because the microcontroller is completely idle at the end of the slot.

ULPMark-PP competition

Product	U575	L412	L552	SAML11	R5F	Apollo2
Core	**Cortex®-M33**	Cortex®-M4	Cortex®-M33	Cortex®-M23	RL78-S3 (16-bit)	Cortex®-M4
Flash	**2M**	128K	512K	32K	32K	1M
RAM	**768K**	40K	256K	8K	3K	256K
Max freq	**160**	80	110	32	24	48
STOP + RTC	**4.7uA**	900nA	3.9uA	800nA	650nA	2.8uA
ADC in STOP with 32K crystal	**Yes (LPBAM)**	No	No	Yes	Yes	No
ADC in STOP with higher clk	**Yes (LPBAM)**	No	No	No	No	No
Autonomous PWM duty cycle	**Yes (LPBAM)**	No	No	Yes	Yes	No
ULPMark-PP score	**70.8**	94	34.0	120	122	34.7
ULPMark-PP position	**#4**	#3	#6	#2	#1	#5

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This table indicates the scores of various microcontrollers:
- STM32U575, STM32L412, STM32L552 from STMicroelectronics
- SAML11 from Microchip
- R5F from Renesas
- Apollo2 from Ambiq micro.

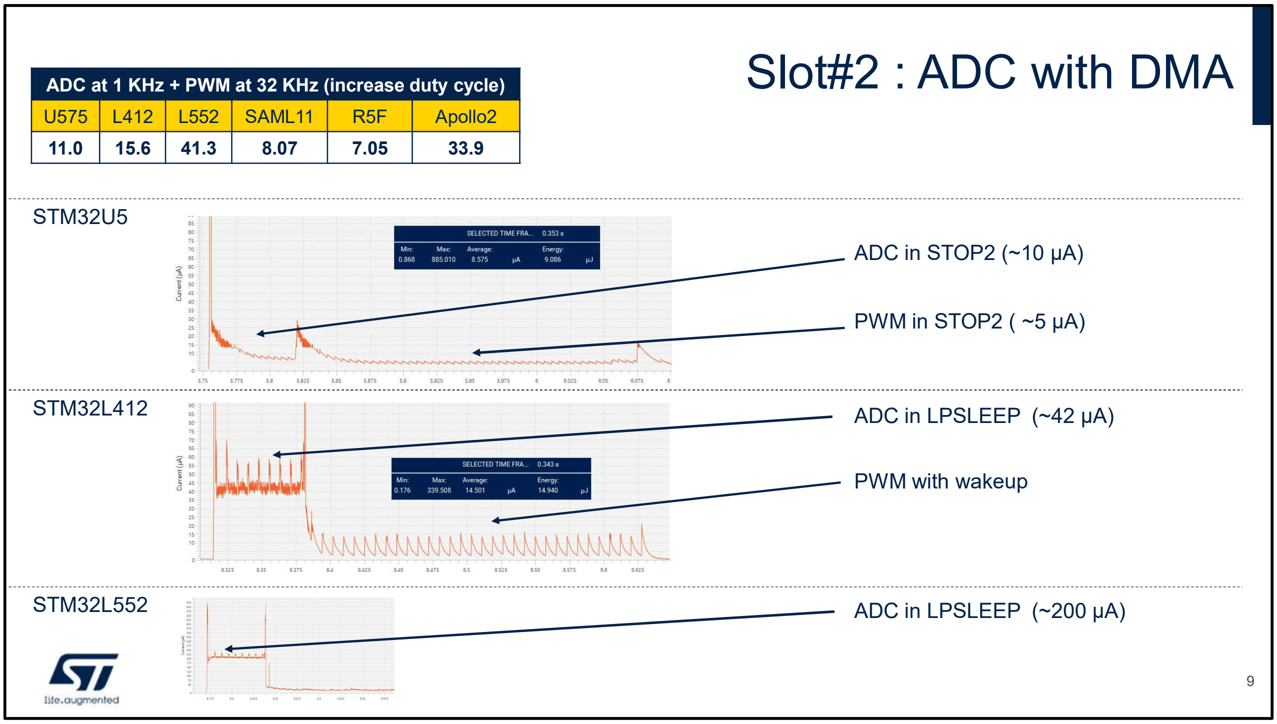
The four first rows provide general information about the microcontroller:
- Processor core
- Size of the flash memory
- Size of the SRAM
- Maximum frequency.

The fifth row indicates the consumption when stop mode is active with RTC enabled.

The sixth, seventh and eighth rows indicate whether ADC conversions can occur while the microcontroller is in stop mode. The STMU575 supports this capability through LPBAM.

The ninth row provides the ULPMark-PP score.

Although STM32U575 is the microcontroller with the largest consumption in stop with RTC active mode, it occupies the 4^{th} position in terms of ULPMark-PP, due to the LPBAM mode and the use of the LP timer to trigger the conversions rather than using the RTC.



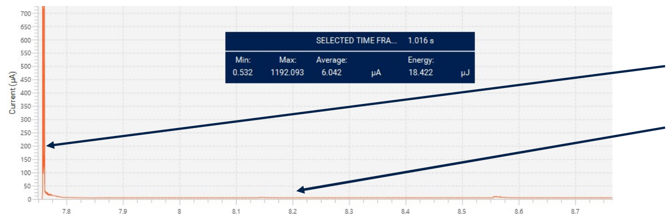
This slide details the consumption during the second slot of the ULPMark-PP benchmark.
The ADC acquires 64 samples at a frequency of 1 KHz and generates 40 PWM pulses at a frequency of 32 KHz, with a duty cycle that increases gradually from 10 to 20%.
The 64 samples acquired during the first slot are evaluated by software.
LPBAM enables the ADC and PWM to remain active while the STM32U5 microcontroller is in stop 2.
LPDMA is used to transfer samples from ADC4 to SRAM4 and to transfer duty cycle values from SRAM4 to the LP timer.
For STM32L412 and STM32L552, the core is asleep while the ADC and DMA remain active, but all other peripherals

are also active in low power sleep mode.
As a result, the consumption is higher than that of STM32U5.
For STM32L412, a wakeup of the Cortex-M4 core is required to update the duty cycle of the PWM.

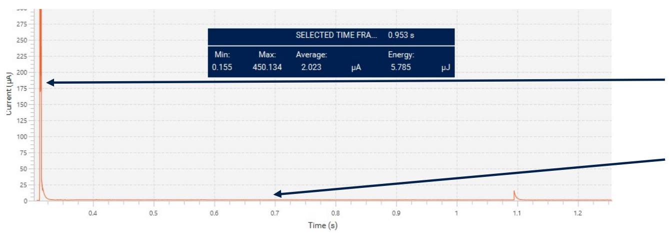
Slot#4 : SPI w/ DMA

ADC at 1 KHz + SPI 128 bytes transmission + PWM at 32 KHz							
U575			L412	L552	SAML11	R5F	Apollo2
Global	STOP3	Stby					
18.4	**10.9**	**7.3**	**4.94**	**15.0**	**7.50**	**5.63**	**10.7**

STM32U5



STM32L412



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This slide details the consumption during the fourth slot of the ULPMark-PP benchmark. Results are expressed in microjoule units.

18.4 microjoule is the total energy of Slot4, 10.9 microjoule is the energy in STOP3 and 7.3 microjoule is the energy in Standby (10.9+7.3=18.2)

The ADC acquires 1 sample at a frequency of 1 Hertz, generates 100 PWM pulses at a frequency of 32 KHz, with a fixed duty cycle of 40% and transmits 128 bytes on the SPI interface.

For STM32U5, all these operations can be performed in stop2 mode, by implementing the LPBAM. The SPI controller number 3 belongs to the Smart Run domain.

For STM32L412, transmitting data on SPI can be performed in low power sleep mode, but all peripherals remain active, not just DMA and the SPI controllers. Both microcontrollers support the generation of PWM pulses at a fixed duty cycle in stop 2 mode.

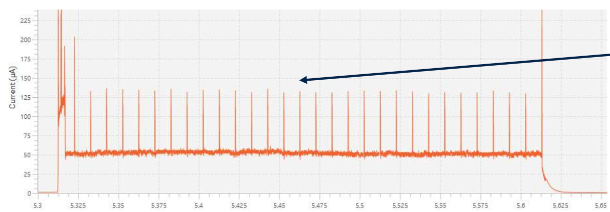
Slot#9 : PWM @ 1MHz

PWM at 1 MHz (increase duty cycle)					
U575	L412	L552	SAML11	R5F	Apollo2
12.2	46.9	140	18.9	30.5	151

STM32U5

PWM in STOP2 (~7 µA)

STM32L412



PWM in LPSLEEP with wakeup (~50 µA)

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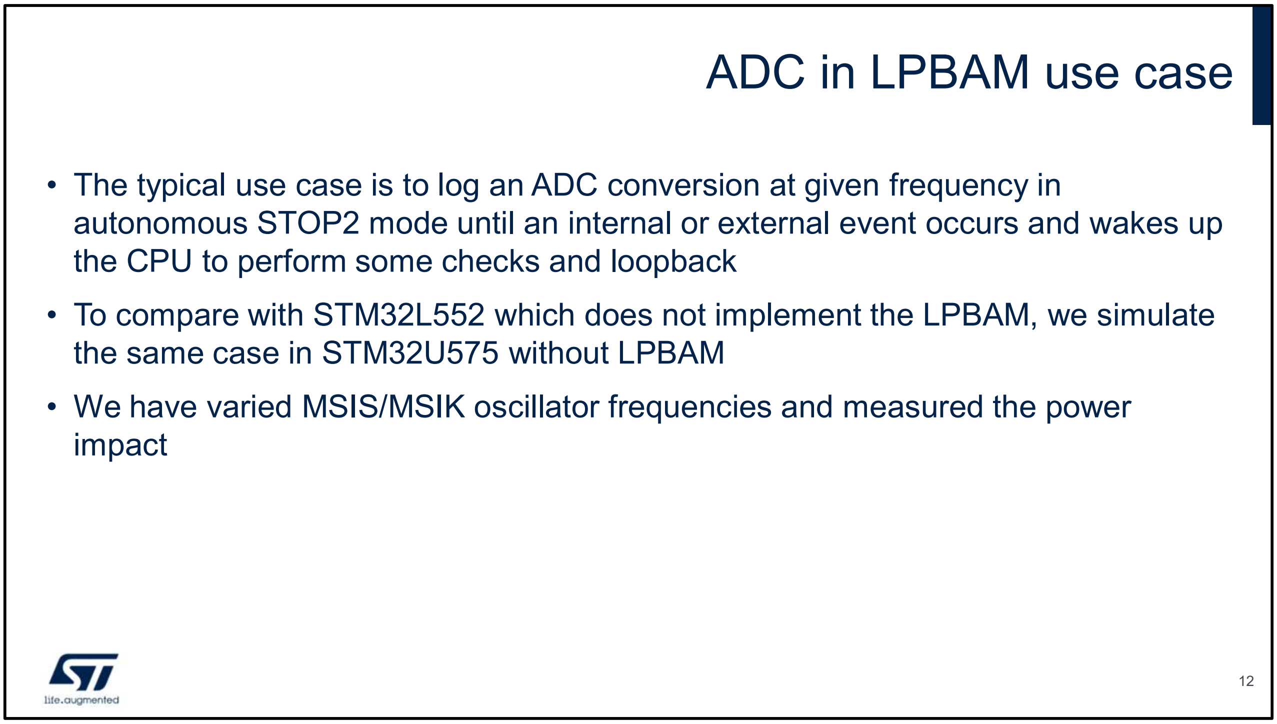
This slide details the consumption during the ninth slot of the ULPMark-PP benchmark.
The ADC acquires 1 sample at a frequency of 1 Hertz, generates 30 PWM pulses at a frequency of 1 MHz, with a duty cycle that increases gradually and transmits 128 bytes on the SPI interface, while checking the 128 bytes received in slot number 8.
The consumption of the PWM in this sequence is more than 7 times lower with STM32U5 compared to STM32L412, due to LPBAM which enables the duty cycle to be updated while the microcontroller is in stop 2 state.



The typical use case of using the ADC in a power-sensitive system consists in acquiring samples in stop 2 mode and using an event to wakeup the CPU that will process these samples.
In order to compare the performance of STM32U575 and STM32L552, two tests are performed on STM32U575: one with LPBAM and the other without LPBAM, based on the sleep and run modes.
Multiple frequencies were tested, the clock source being the Multiple-Speed Internal oscillator System (MSIS) and Kernel (MSIK).
The results of these tests are described in the next slide.

LPBAM ADC results

MSIS and MSIK frequencies	Consumption with LPBAM (µA)	Consumption with SLEEP+RUN modes (µA)
MSIS=MSIK=100 KHz	14.5	80
MSIS=MSIK=400 KHz	14.8	90
MSIS=MSIK=1 MHz	15.5	112
MSIS=4 MHz / MSIK=1 MHz	15.5	171

- At higher frequencies and using LPBAM, the consumption of STM32U575 remain almost the same, while with SLEEP+RUN mode (similar to L5 case) the consumption is doubled when MSI up from 100 KHz to 4 MHz

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It is interesting to study the impact of the MSIS and MSIK frequencies on the overall consumption when LPBAM is active and when the legacy sleep / run approach is used. When LPBAM is implemented, the variation of consumption is 6.5% when the frequency of MSIS and MSIK varies respectively from 100 KHz to 4 MHz and from 100 KHz to 1 MHz.
This demonstrates that the frequency of the oscillator has a minor impact on the consumption when LPBAM is used, because peripherals with the LPBAM capability can switch on MSIS or MSIK for transferring data. During idle time, the oscillator is switched off.
When the sleep and run approach is used, based on the processor wakeup each time a sample is acquired, the

consumption has an important relationship with the frequency of the oscillator. The reason is that all peripherals remain active in sleep mode, not just the ADC. In this case, the consumption is more than doubled when the frequency of MSIS and MSIK varies respectively from 100 KHz to 4 MHz and from 100 KHz to 1 MHz.

I2C typical use case with LPBAM

- Setup a typical use case with Temperature sensor acquisition via I2C
  - Setup LPTIM timer to trigger an I2C read sequence from external temperature sensor
  - Setup two different power modes and compare
    1. Use LPBAM so the CPU remains in Stop2 mode all the time and wakes up on DMA transfer completion or an asynchronous event
       - In this case, the LPDMA will record data from the I2C RxBuffer to SRAM4
    2. Align with the STM32L552/L412 capability:
       - From Stop2 mode, I2C is triggered by LPTIM and the CPU wakes up and transitions the system to SLEEP mode
       - In SLEEP mode, the DMA will transfer the data from the RxBuffer to SRAM4
       - Once done, the CPU is woken up by the DMA transfer complete event and puts the system in STOP2
  - Vary LPTIM frequency and get the power consumption trend
  - Do the same test with STM32L412

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Testing the power consumption when a temperature acquisition is performed from a sensor connected to I2C is a second important use case for low power performance analysis.
The low power timer is used to trigger the I2C read operation.
Two different power modes are tested:
- With LPBAM and stop 2 mode
- With a sleep and run approach, also supported by STM32L412.

In the first case, the LP timer triggers the I2C read transaction and the LPDMA transfers the received data from the I2C receive buffer to SRAM. Then an interrupt wakes up the processor.

In the second case, the LP timer wakes up the processor that transitions the system from Stop 2 to Sleep mode. Then the DMA transfers the data received from the I2C to a buffer in SRAM. Finally another interrupt wakes up the processor that transitions the system back to stop 2. Several low power timer frequencies are tested.
The results of these tests are described in the next slide.

I2C test result

	STM32U575 MSIS=MSIK=16 MHz		STM32L412 MSI=8 MHz
	LPBAM (µA)	SLEEP +STOP2 (µA)	SLEEP +STOP2 (µA)
LPTIM frequency =6 Hz	**4.46**	**9.525**	**2.05**
LPTIM frequency =60 Hz	**5.36**	**13.9**	**6.35**
LPTIM frequency =600 Hz	**15.6**	**47.7**	**40.3**

- At a low acquisition rate, the STM32U575 consumes twice as much as STM32L412
- When the frequency of the I2C read operations increases, the benefits of the STM32U575 with LPBAM become visible, with 2 to 3 times less consumption than STM32L4

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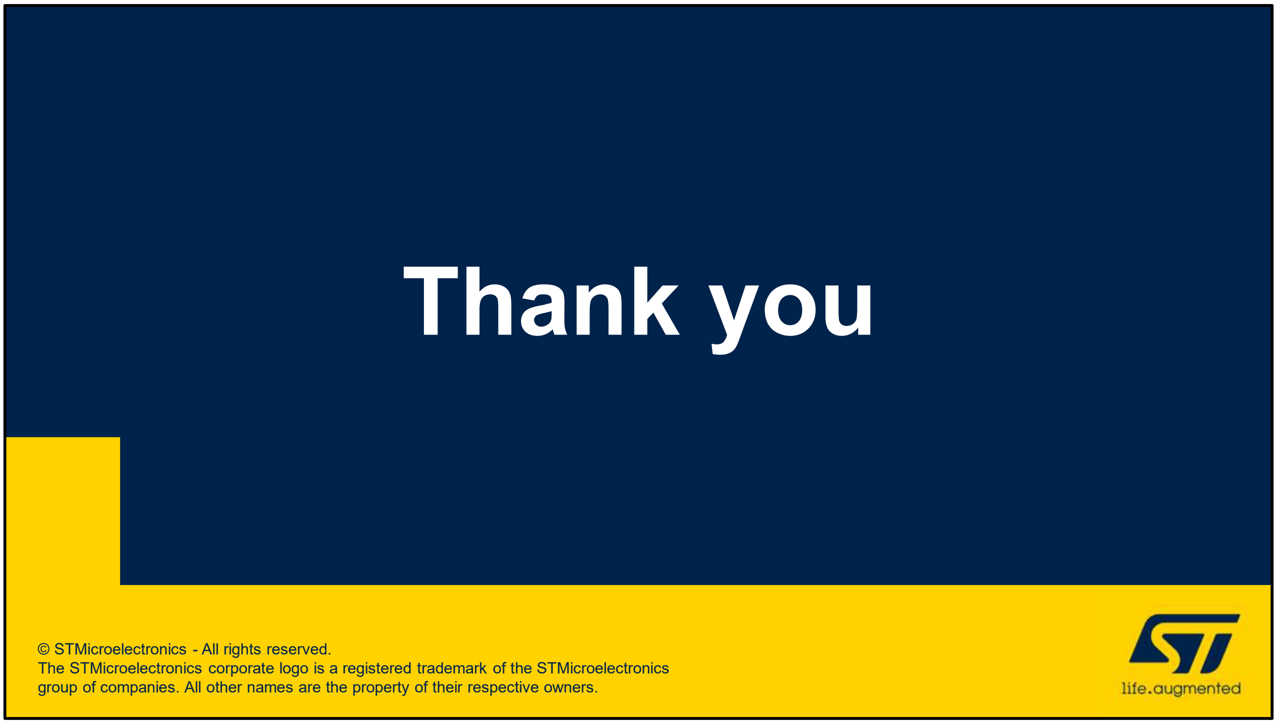
Let us first compare consumption when the LPTIM frequency is 6 Hertz. STM32U575 with LPBAM consumes more than twice as much as STM32L412 and more than four times when sleep and stop 2 modes are used.
When the LPTIM frequency is 60 Hertz, STM32U575 with LPBAM consumes 15% less than STM32L412 but consumes more than twice as much as STM32L412 when sleep and stop 2 modes are used.
When the LPTIM frequency is 600 Hertz, STM32U575 with LPBAM consumes 61% less than STM32L412 but consumes 18% more than STM32L412 when sleep and stop 2 modes are used.
Therefore, the lower the period of the I2C read operation, the higher the score of STM32U575 when LPBAM is

active.
When the traditional sleep and stop 2 approach is implemented, STM32L412 offers a lower consumption, even if the gap decreases when the frequency of I2C reads increases.



In addition to this presentation, you can refer to the following presentations:

- Power management
- Reset and clock controller.