VL53L9CX

Datasheet

3D dToF all-in-one lidar module

Features

- Fast and accurate 3D direct Time-of-Flight (dToF) camera module
  - Multizone ranging output with up to 54 x 42 separate zones and binning options
  - On-chip processing streaming 2D IR image, depth and ambient maps
  - Confidence level and reflectance maps generated in postprocessing
  - Ranging from <5 cm up to 8.8 m
  - Up to 100 Hz frame rate capability
  - On-chip histogram processing and algorithmic compensation minimize or remove the impact of cover glass crosstalk and veiling glare
- Fully integrated miniature module with wide field of view (FoV)
  - Scan by two vertical-cavity surface-emitting lasers (VCSEL) flood illumination
    - 940 nm invisible light and integrated analog driver
  - 55°x42° (71° diagonal) FoV using metasurface optical elements (MOE) on both transmitter and receiver
  - Receiving array of single photon avalanche diodes (SPADs)
  - Size: 12.8 x 6.1 x 4.6 mm
- Easy integration
  - True all-in-one module with integrated SPAD sensor and VCSEL PMIC
  - Single reflowable component
  - Interface: I3C & MIPI CSI
  - Flexible power supply options:
    - Supports dual power supply operation: 1.2 V & 3.3 V
  - Compatible with a wide range of cover glass materials

Applications

- Robotics
  - SLAM
  - Obstacle avoidance
  - Small object identification
- Augmented reality/virtual reality (AR/VR) enhancement.
  - Dual camera stereoscopy assistance thanks to 2D and depth multizone distance measurement at 60 fps
  - 3D room mapping (multizone and multiobject detection)
  - Gesture recognition and skeletal tracking
- Industrial applications
  - Content management thanks to wide FoV and multizone scanning (liquid level control, load in trucks, tanks, waste bins)
  - People mapping
- Smart homes
  - Smart buildings and smart lighting (user detection to wake up devices)
- IoT
  - User and object detection

- Mobile devices
  - Telephoto zoom camera assist. High resolution and long range allow image crop to align with telephoto camera.
  - Laser-assisted autofocus (LAF). Enhances the camera AF system speed and robustness, especially in difficult low-light or low-contrast scenes.
  - Video focus tracking. 60 Hz ranging allows optimization of continuous focus algorithm.
- Projectors
  - Keystone correction for video projectors

Description

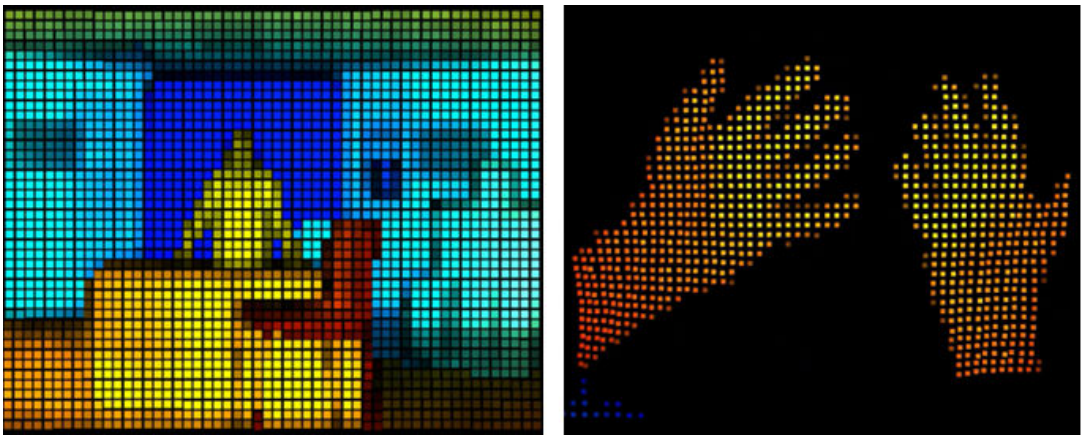
The VL53L9CX is a state of the art, dToF 3D lidar (light detection and ranging) module with market leading resolution of up to 2.3k zones enhancing the ST FlightSense product family. Housed in a miniature reflowable package, it integrates all necessary components to make it a true all-in-one and easy to integrate module. The VL53L9CX includes a SPAD array, postprocessing SoC, two VCSELs powered by a dedicated BCD VCSEL driver providing a flood illumination, physical infrared filters, metasurface optical elements (MOE), and an embedded PMIC. The module is Class 1 laser safe, offering skin protection in addition.

The use of a MOE above the VCSELs allows to project an optimized rectangular FoV onto the scene. The receiver lens focuses the reflection of this light onto the SPAD array.

Unlike conventional IR sensors, the VL53L9CX uses ST's latest generation BSI stacked direct ToF technology, which allows absolute distance measurement whatever the target color and reflectance. It provides accurate ranging from below 5 cm up to 8.8 m. The VL53L9CX can stream processed data at maximum frame rate (100 Hz), which makes it the fastest, truly integrated 3D lidar camera module on the market. Available output data: depth, 2D IR with active illumination, 2D IR without active illumination, reflectance, and confidence.

The VL53L9CX achieves the best ranging performance, including under strong ambient light conditions, with a range of cover glass materials. Multizone distance measurements are possible up to 54 x 42 zones, with a wide 55°x42° FoV, which can be reduced by software.

Figure 1. Sensor output examples



1 Acronyms and abbreviations

Table 1. Acronyms and abbreviations

Acronym/abbreviation	Definition
AF	autofocus
AOI	angle of incidence
AP_CLK	application processor clock
API	application programming interface
AR	augmented reality
BCD	bipolar CMOS-DMOS
CWL	center wavelength of the band-pass at 80% transmission
DOE	diffractive optical elements
DSS	dynamic SPAD selection
dToF	direct Time-of-Flight
ECC	error correction code
EoT	end of transmission
ESD	electrostatic discharge
FoI	field of illumination
FoV	field of view
FE	frame end
FS	frame start
FW80	bandwidth of the band-pass at 80% transmission
GPIO	general-purpose input/output
IoT	Internet of Things
I^2C	inter-integrated circuit (serial bus)
I3C	communication protocol (serial bus)
LAF	laser-assisted autofocus
LDO	low drop out
LE	line end
LP	low power
LS	line start
MIPI CSI-2	camera serial interface
MOE	metasurface optical elements
NVM	nonvolatile memory
PCB	printed circuit board
PLL	phase-locked loop
PMIC	power management integrated circuit
POR	power on reset
PVT	process, voltage, and temperature
RAM	random-access memory
ROI	region of interest
SCL	serial clock line

Acronym/abbreviation	Definition
SDA	serial data line
SOT	start of transmission
SPAD	single photon avalanche diode
TNR	temporal noise reduction (algorithm running in processing pipeline)
ToF	Time-of-Flight
UI	user interface
VCSEL	vertical-cavity surface-emitting laser
VR	virtual reality

2 Overview

2.1 Technical specifications

Table 2. Technical specifications

Feature	Details
Package	OLGA
Size	12.83 x 6.10 x 4.64 mm
Ranging	50 to 8800 mm per zone
Operating voltage	AVDD: 2.8 V or 3.3 V / VBAT: 2.8 V to 4.8 V DVDD: 1.2 V / IOVDD: 1.8 V and 1.2 V
Operating temperature	-30°C to 70°C
Sample rate	Up to 100 Hz
Infrared emitter	2 VCSEL emitters (940 nm)
Communication interface	I^2C: 1 MHz serial bus (Add. 0x52) / I3C: 12.5 MHz
Output interface	MIPI CSI-2: 1 Gbps / I3C: 12.5 Mbps

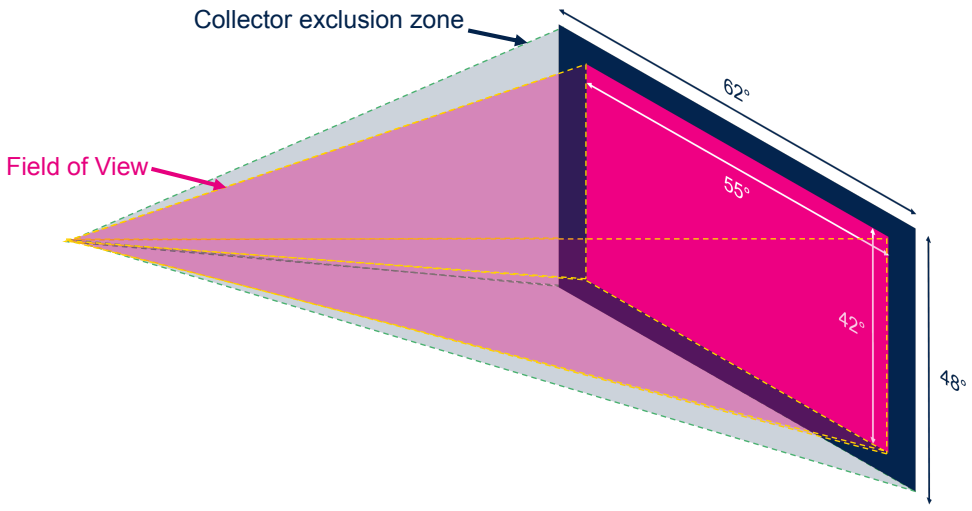
2.2 Field of view

The Rx (or collector) exclusion zone includes all module assembly tolerances. It is used to define the cover glass dimensions. The cover glass opening must be equal to or wider than the exclusion zone.

Table 3. FoV angles

	Horizontal	Vertical
Field of view	55°	42°
Collector exclusion zone	62°	48°

Figure 2. Field of view and exclusion zone description (not to scale)



2.3 Field of illumination

The relative emitted signal power of the two VCSELs field of illumination (FoI) depends on the FoI angles. The final field of illumination correspond to:

Table 4. FoI angles

	Horizontal divergence	Vertical divergence
FoI	57.6°	43°
Illuminator exclusion zone	64°	51°

2.4 Bandpass filter

A bandpass filter is placed over the Rx lens. The table below shows the bandpass filter characteristics under room temperature (25°C).

Figure 3. Bandpass spectral definitions

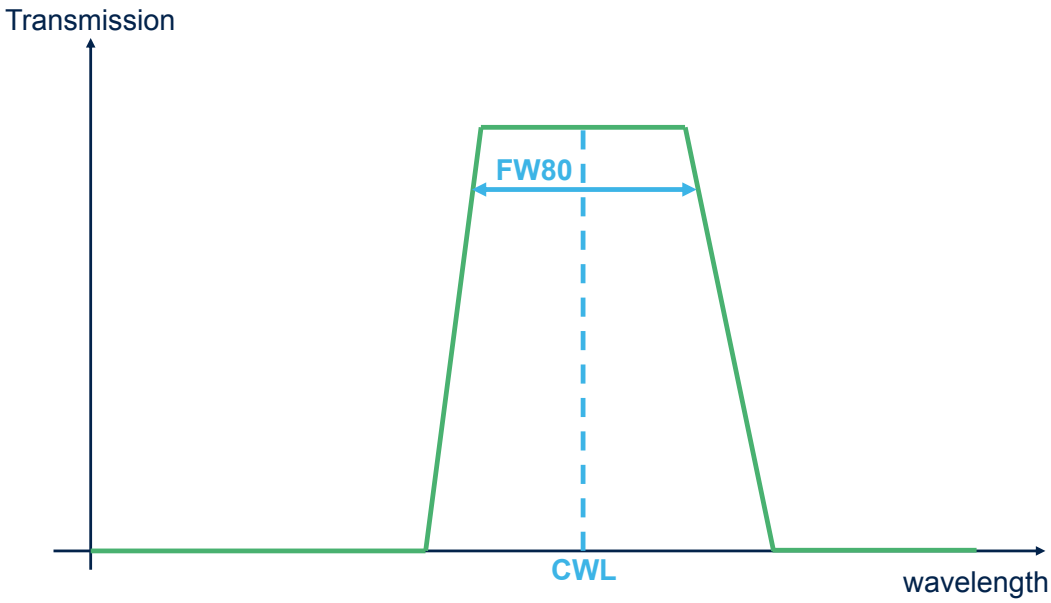


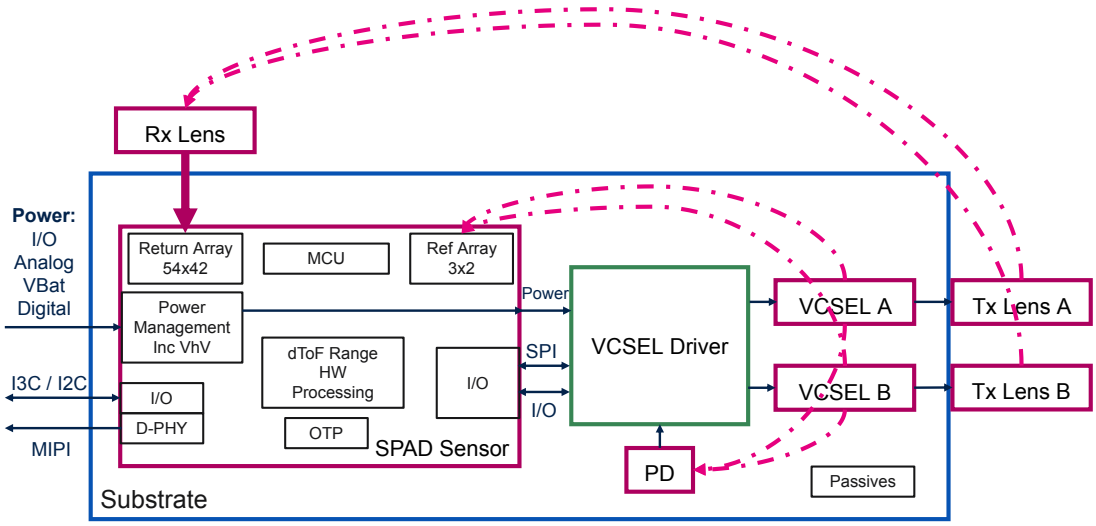
Table 5. Bandpass filter characteristics

Band	Wavelengths (nm)	Transmission	AOI
FW80	32	80%	0°
	30		34°
CWL	950	> 93% (average)	0°
	934.5		34°

2.5 System block diagram

The block diagram below shows the VL53L9CX system architecture.

Figure 4. Block diagram



2.6 Module pinout

The figure below shows the module footprint pad positions (bottom view).

Figure 5. Module pinout (bottom view)

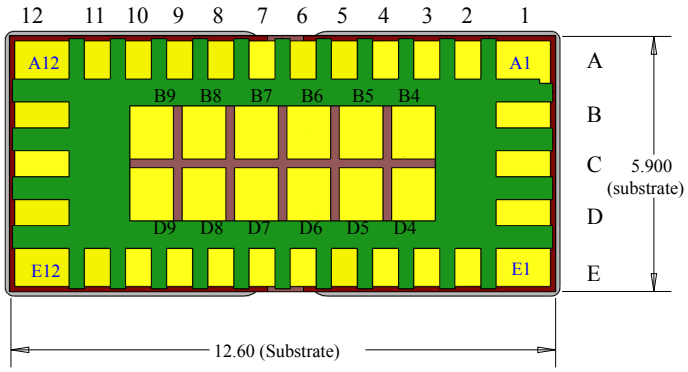


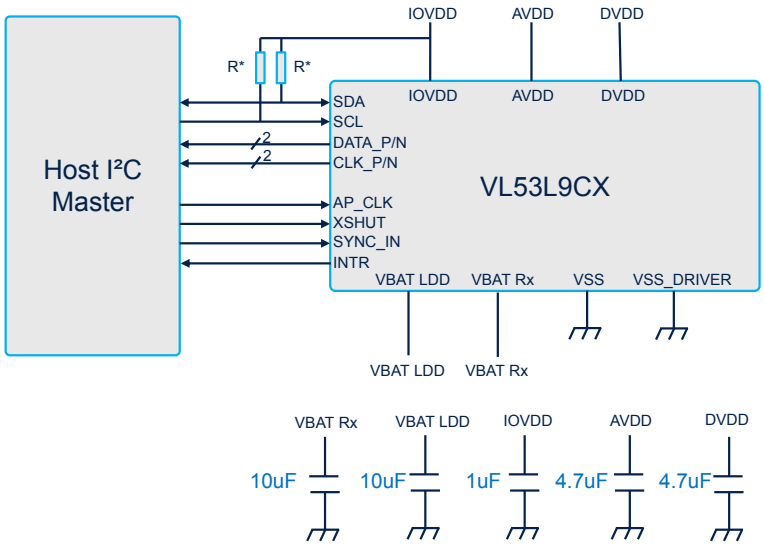
Table 6. VL53L9CX pin description

Pin number	Name	Type	Description
A1	VSS	Ground	Ground
A2	VSS_DRIVER		
A3			
A4	VSS		
A5	DATA_P	Digital output	MIPI CSI-2: Data lane
A6	DATA_N		
A7	VSS	Ground	Ground
A8	CLK_P	Digital output	MIPI CSI-2: Clock lane (min: 100 MHz, max 500 MHz)
A9	CLK_N		
A10	INTR	Digital input output (I/O)	Interrupt output, used to signal interruptions
A11	SCL	Digital input	I^2C or I3C control interface
A12	SDA	Digital input output (I/O)	I^2C or I3C control interface
B1	VBAT_LDD	Power	Laser driver boost supply (2.8 V to 4.8 V)
B4-B9	VSS	Ground	Thermal pad (see Section 2.9.1: Thermal dissipation)
B12	XSHUT	Digital input	Enable the signal. Drive to logic 1 to enable the device
C1	VSS	Ground	Ground
C12	DVDD	Power	1.2 V digital supply
D1	VBAT_RX	Power	SPAD boost supply (2.8 V to 4.8 V)
D4-D9	VSS	Ground	Thermal pad (see Section 2.9.1: Thermal dissipation)
D12	SYNC_IN	Digital input output (I/O)	Synchronization input, used to synchronize the device. Drive to logic 0 to trigger a new frame
E1	VSS	Ground	Ground
E2			
E3	RSVD1	Reserved	Do not connect
E4	VSS	Ground	Ground
E5	VSS	Ground	Ground
E6	AVDD	Power	2.8 V or 3.3 V analog supply
E7			
E8	IOVDD	Power	1.8 V or 1.2 V I/O supply
E9	VSS	Ground	Ground
E10			
E11	AP_CLK	Clock	Device clock (6 MHz to 27 MHz)
E12	RSVD2	Reserved (Internal I/O)	Do not connect

2.7 Application schematic

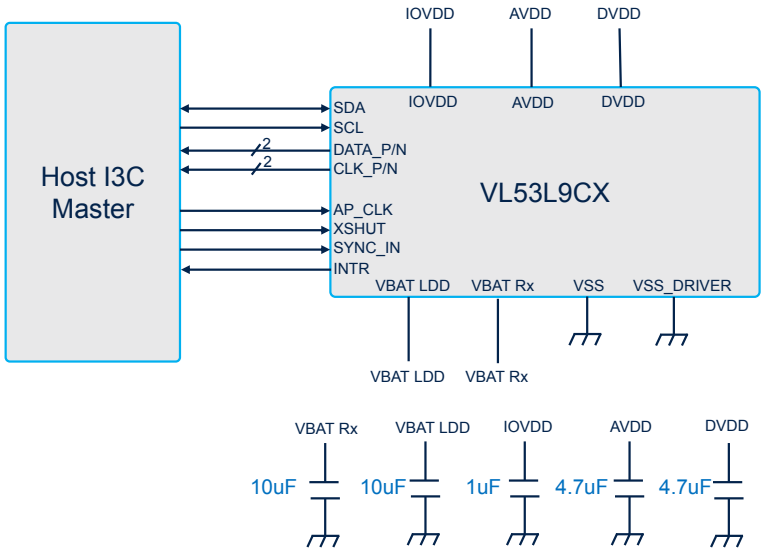
The application schematics below show examples for connecting to a host.

Figure 6. Application schematic with an I²C host



Note: Use appropriate pull-up resistors when the communication interface is I²C. 2.2K Ω is a typical value for a device connected on an I²C interface at 1 Mbps.

Figure 7. Application schematic with I3C host



Note: The device is connected to the host with an I3C interface. The serial communication signals (SDA/SCL) do not require pull-up resistors.

Note: Capacitors on the external supplies (AVDD, DVDD, VBAT, and IOVDD) should be placed as close as possible to the module pins.

Note: IOVDD must be set to ensure the host and the VL53L9CX operate at the same voltage levels for all IOs and communication interface.

Note: AVDD supports 3V3 supply. It is possible to use the same supply to power VBAT and AVDD.

Note: MIPI CSI-2 is not mandatory. It is possible to control and read the data using the communication interface (either I3C or I^2C), but the maximum frame rate decreases depending on the sensor resolution and the interface.

2.8 Substrate trace impedances

The following signals must be routed with balanced, controlled-impedance, differential traces. This is required for high-speed signaling.

Table 7. Signals and their differential impedance values

Signal name	Differential impedance (ohms)	Tolerance (ohms)
CLK_P CLK_N DATA_P DATA_N	• 100 Ω for differential impedance • 50 Ω for signal impedance • Intra- and inter-lane routing length @ 1 Gbps	To be as close as possible to stated values. Important to have the same values for CLK_P/CLK_N and DATA_P/DATA_N

2.9 PCB guidelines

2.9.1 Thermal dissipation

ToF sensors are precision sensors manufactured on a mixed analog and digital semiconductor CMOS process. ToF sensors are sensitive to temperature variation. They function over a temperature range of -30 to 70°C.

Note: The VL53L9CX sensor contains an onchip temperature monitor used for automatic temperature compensation.

The ranging error/noise of ToF sensors increases with a rise in junction temperature. Proximity to heat sources must be avoided.

Recommendations

- Identify heating components in the application based on their maximum power consumption as they may impact ToF sensor performance.
- Place the ToF module as far as possible from heat-generating components. However, ignore this step if the heat-generating component does not impact the ToF sensor usage.
- Consider using a good PCB layout design to increase ToF heat dissipation (Section 2.9.2: PCB layer).
- Assume the thermal power dissipation is evenly distributed amongst the thermal pads when calculating the system Rth.

Thermal pad soldering recommendations:

- A large open zone on the solder mask.
- 12 independent central pads on the PCB (B4 to B9 and D4 to D9).
- 12 welding rod tips

Note: For more details about thermal dissipation and system thermal resistance, refer to technical note (TN1579): Thermal guidelines when using the VL53L9CX.

2.9.2 PCB layer

Recommendations

- Maximize the copper cover on the PCB/FPC to increase the thermal conductivity of the board.
- Use wide tracking for all signals particularly for the power and ground signals:
  - Track and connect them into adjacent power planes where possible. The power rail width should meet the peak current requirement.
- Surround the signals and power rails with GND.
- Ensure there is a complete GND layer below the module.
- Add as many thermal vias as possible to the thermal pad module. This maximizes the thermal conductivity into adjacent power planes.
- Add heat sinking to the chassis or frames to distribute heat away from the device.

2.10 Power management

2.10.1 Supply limit and guard bands

The table below shows the module supply limits and guard bands.

Table 8. Supply limits

Supply	Voltage (V)	Tolerance
IOVDD (1)	1.2 or 1.8	± 10%
AVDD (2)	2.8 or 3.3	± 5%
DVDD	1.2	± 5%
VBAT (3)	Between 2.8 and 4.8	—

1. *IOVDD can be either 1.2 V or 1.8 V. The application configures the driver to specify the supply configuration (the default configuration is 1.8 V).*
2. *AVDD can be either 2.8 V or 3.3 V. The application configures the driver to specify the supply configuration (the default configuration is 2.8 V).*
3. *VBAT supports any voltage in the range of 2.8 V and 4.8 V. No configuration is expected at application level for VBAT.*

2.11 Clock

An application clock (AP_CLK) is required with the same voltage level as the IOVDD level. The device supports various values in the range of 6 to 27 MHz with a maximum jitter of 200 ps. The driver provides the exact frequency value to the firmware during the boot sequence. Accuracy is expected to be ± 100 ppm to ensure optimal performance.

3 Functional description

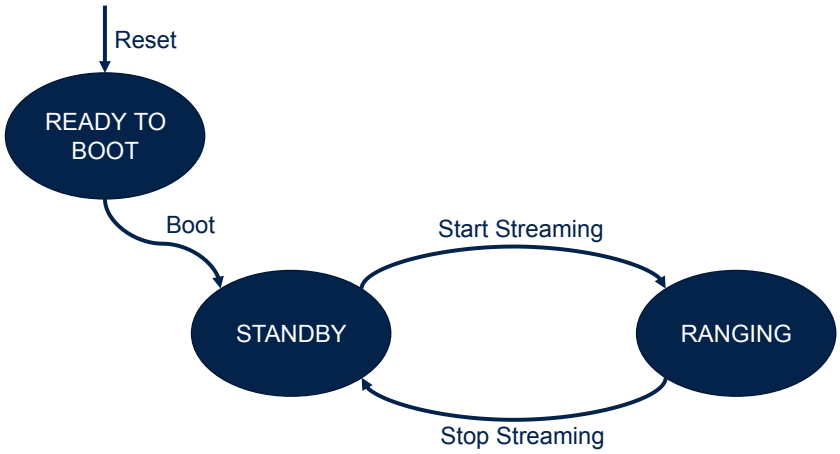
3.1 Device operating modes

Device state machine

The sensor has three operating modes:

- Ready to boot
- Standby
- Ranging

Figure 8. State machine



Once the VL53L9CX is powered, it is in the state "READY TO BOOT". The firmware reads OTP and configures the control interface. During this state, the host can configure the sensor (for example the value of an external clock) and boot the device.

During the boot, the firmware configures the clock tree knowing the external clock frequency, and loads all the calibration settings read in OTP.

The host can set the ranging configuration in standby mode and start the streaming.

Power up sequences

The VL53L9CX requires at least three power supplies to power up and two others in streaming (VBAT_RX, VBAT_LDD).

- DVDD - Digital core supply
- AVDD - Analog core supply
- IOVDD - I/O voltage supply

To power up the device, the three supplies above could be applied in any order. The two extra supplies below are used to power the boost functions of the SPAD array and the laser driver.

- VBAT_Rx - SPAD boost supply
- VBAT_LDD - VCSEL boost supply

Device ranging modes

Two ranging modes can be configured:

- Precision ranging mode (below 5 cm to 8.8 m)
- Ambient ranging mode (from 45 cm to 8.5 m)

Precision mode is optimized for close and accurate distance measurement.

Ambient mode is optimized for ranging under IR light conditions.

Output interfaces

The default is the output interface MIPI CSI-2. However, the user can choose to get data over the control interface.

Note: STMicroelectronics recommends using a I3C host for increased bandwidth. It is possible to read data in I²C mode but the achievable frame rate is lower depending on the finale map resolutions.

Trigger modes

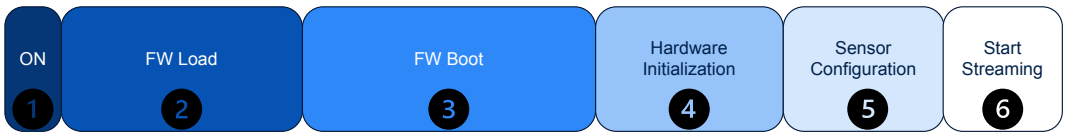
Three trigger modes are available:

- Autonomous mode (the device generates its own trigger signal)
- External sync mode (the device uses the SYNC_IN pin to trigger new frames)
- Manual mode (the device wait for a trigger command in the UI to start a new frame exposition)

Time to first range

The time to the first range data being available is dependent upon the platform resources, the host bus interface speed, the frame rate and results configuration. However, the same sequence is applicable in all cases as shown below.

Figure 9. Boot sequence (not to scale)



1. Add power, AP clock, XSHUT, and read device ID.
2. Load the firmware in memory.
3. Call the firmware boot command and wait for boot complete.
4. Hardware specific configuration.
5. Device configuration.
6. Call the firmware start streaming command.

In addition to the three supplies, the device requires an AP_CLK to be enabled and the XSHUT pin to be at a high level.

3.2 Device features

Resolution and return array dimension

The sensor resolution is the number of zones in X and Y dimension. It depends on the ratio selected and the binning configuration. This means that a zone is a 2x2 macro SPAD. The events are combined together. The final output resolutions are:

- 54 x 42 (Binning 2)
- 24 x 20 (Binning 4)
- 18 x 14 (Binning 6)
- 12 x 10 (Binning 8)
- 8 x 6 (Binning 12)
- 4 x 4 (Binning 24)

Dynamic SPAD selection

The device firmware implements a dynamic SPAD selection algorithm (DSS) which keeps the signal rate in a range to ensure good accuracy.

Power modes

Different levels of power mode can be configured during the ranging to allow power saving specially when the frame rate is low.

Note: Low power and ultralow power modes disable circuitry in between frames to save power.

3.3 Profile examples

The following table lists examples of profiles the application can configure.

Table 9. Profile examples

Profile	Purpose	Resolution	Ranging mode	Frame rate	Exposure	Power mode	Max ranging	Typical power consumption
Gaming	High frame rate	54x42	Precision (no DSS)	100 fps	4 ms	Regular	5 m	420 mW (5 klx)
Room mapping	Long ranging in private home	54x42	Ambient	30 fps	6 ms	ULP	8 m	200 mW (5 klx)
AR glasses	High IR ambient application	54x42	Ambient	20 fps	16 ms	LP	3 m	600 mW (100 klx)
Autofocus	Low noise and latency photo assist	24x20	Precision	15 fps	5 ms	ULP	8.8 m	80 mW (Indoor)
Wake on approach	Very low power detection	12x10	Ambient	1 fps	2 ms	ULP	8.5 m	12.5 mW (Dark)
Content/ Volume calculation	On battery smart object	54x42	Precision	1 frame per hour	5 ms	Regular	8.8 m	2 mW (Dark)

3.4 Host algorithms

STMicroelectronics recommends that the customer use the software processing pipeline provided.

4 Control interfaces

4.1 I²C interface

This section specifies the I²C interface. This interface uses 1.8 V or 1.2 V I/Os with two signals: serial data line (SDA) and serial clock line (SCL). The I²C is used to control data transfer. Each device connected to the bus uses a unique address, and a simple host/client relationship exists.

Both SDA and SCL lines are connected to a positive power supply through pull-up resistors, which are located on the host platform. Lines are only actively driven low. A high condition occurs when lines float and the pull-up resistors pull lines up. When no data are transmitted, both lines are high. See Section 8: Ranging performances for electrical and timing information.

The host device performs a clock signal generation and initiates data transfer. The I²C bus has a maximum speed of 1 MHz (I²C fast mode+ mode).

I²C sensor address

The sensor address can also be modified during standby by writing a control register.

The sensor I²C address at power up can be programmed into the NVM by the user (see product application notes for details). In this case, the new address is effective 1 ms after reset.

If nothing is specified in the NVM, the default address at power up is 0x52 (8-bit address, or 0x29 7-bit address).

Control interface

Information is packed in 8-bit packets (bytes), followed by an acknowledge bit. Ad for device acknowledge, and Ah for host acknowledge (baseband or hardware accelerator whichever is the I²C bus host). Internal data are produced by sampling the SDA at a rising edge of the SCL. The external data must be stable during the high period of the SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

A message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition without a preceding stop condition) followed by another message. The first byte contains the device address on 7 bits and 1 bit that provides the data direction. If the least significant bit is low, the message is a host write to the device. If the least significant bit is set too high, then the message is a host read from the client.

All serial interface communications with the sensor must begin with a start condition. The device acknowledges receipt of a valid address by driving the SDA wire low. The state of the read/write bit (LSB of the address byte) is stored and the next byte of data, sampled from the SDA, can be interpreted. During a write sequence, the second and third bytes received provide a 16-bit index (big-endian), which points to one of the internal 32-bit registers (little-endian).

Read/write support

After each data byte is received by the client, an acknowledge is generated. The data are stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index are read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of the SCL.

At the end of each byte, in both read and write sequences, an acknowledge is issued by the receiving device (that is, the device for a write and the host for a read).

Only the bus host can terminate a message. It is stopped either by issuing a stop condition, or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The device supports multibyte registers read and write. Below are examples of 32-bit register and bytes array read and write.

Figure 10. Register write

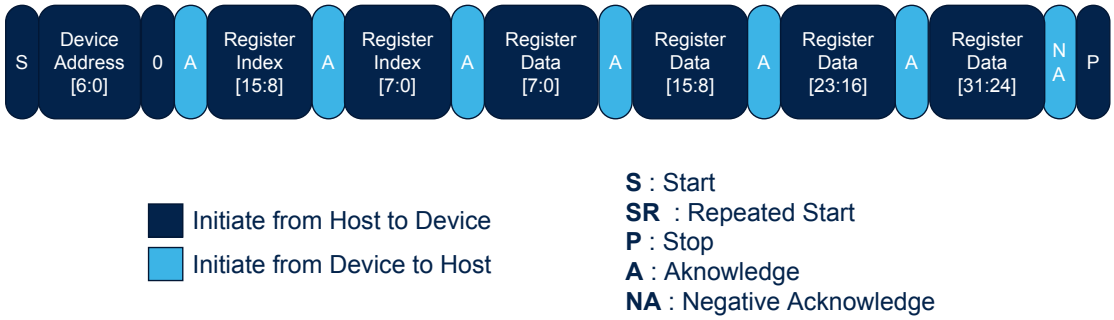
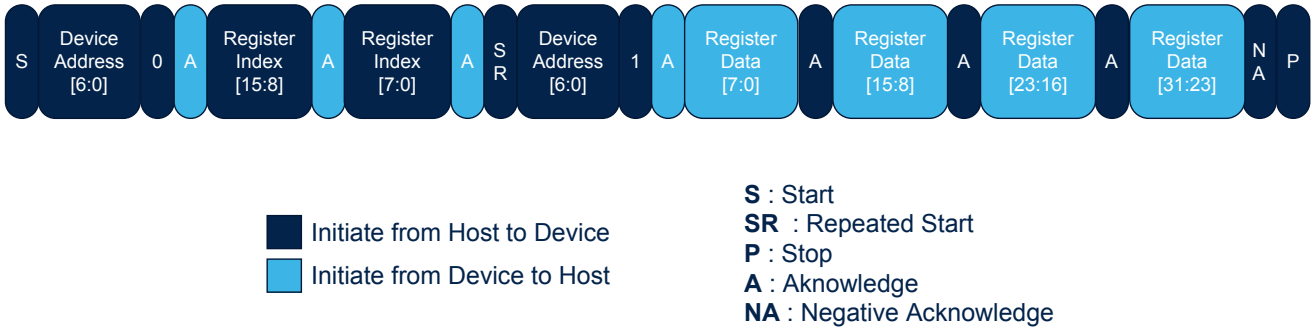


Figure 11. Register read



The interface also supports autoincrement indexing. After the first data byte is transferred, the index is automatically incremented by 1. The host can therefore send data bytes continuously to the client until the client fails to provide an acknowledge, or the host terminates the write communication with a stop condition. If the autoincrement feature is used, the host does not have to send address indexes with the data bytes.

Figure 12. Multibytes write

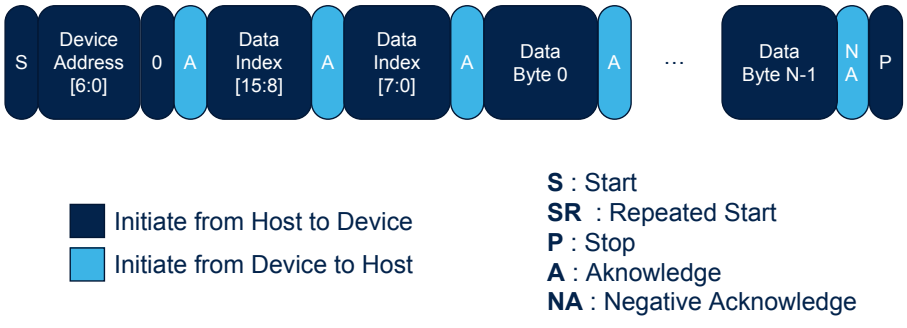
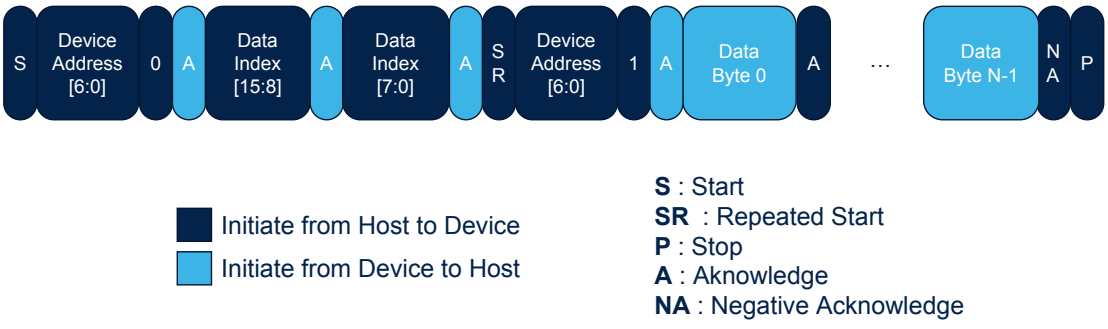


Figure 13. Multibytes read



4.2 MIPI I3C^{SM} client interface

The device interface includes a MIPI I3C^{SM} SDR only client interface (compliant with release 1.0 of the specification) with MIPI I3C^{SM} SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for a single byte
- Multiple read and write
- In-band interrupt request
- Error detection and recovery methods (S0-S6)

Note: Refer to I^{2}C/MIPI I3C^{SM} coexistence for details concerning the choice of the interface when powering up the device.

MIPI I3C^{SM} CCC commands

The list of MIPI I3C^{SM} CCC commands supported by the device is detailed in the following table.

Table 10. MIPI I3C^{SM} CCC commands

Command	Code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address
ENEC	0x80 / 0x00		Client activity control (direct and broadcast)
DISEC	0x81 / 0x01		Client activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
ENTAS1	0x83 / 0x03		Enter activity state (direct and broadcast)
ENTAS2	0x84 / 0x04		Enter activity state (direct and broadcast)
ENTAS3	0x85 / 0x05		Enter activity state (direct and broadcast)
SETXTIME	0x98 / 0x28		Timing information exchange
GETXTIME	0x99	0x07 0x00 0x05 0x92	Timing information exchange
RSTDAA	0x86 / 0x06		Reset the assigned dynamic address (direct and broadcast)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B		Get maximum write length during private write
GETMRL	0x8C		Get maximum read length during private read
GETPID	0x8D		Device ID register
GETBCR	0x8E		Bus characteristics register
GETDCR	0x8F		MIPI I3C^{SM} device characteristics register
GETSTATUS	0x90		Status register
GETMXDS	0x94		Return max data speed

I²C/MIPI I3C^{SM} coexistence

SDA and SCL lines are common to both I²C and MIPI I3C^{SM}.

The host can be connected to both I²C and MIPI I3C^{SM}. In this configuration the serial communication signals (SCL/SDA) must not have pull-up resistors, refer to Section 2.7: Application schematic.

MIPI I3C^{SM} known limitations

DAA sequence

DAA sequence is done at low speed (<= 1MHz), VL53L9CX enables automatically the I3C mode once the dynamic address is assigned by the host. The host can increase the I3C frequency to 12.5 MHz after the DAA sequence.

Burst mode

To perform a multibytes access, the index should be aligned on a word, and a fast clock must be enabled during access.

During STANDBY and BOOT stages, the VL53L9CX uses the external clock to save power. If the application has to read bursts of data, the application should command the FW to use the fast clock during the read (Refer to the software guidelines for more information).

Consecutive Write/Read

The device does not support consecutive write and read operations on the same register with a repeated start between the write and read.

The user must stop the sequence and restart a new read after the write. This write+read operation are used by the driver to initiate a firmware command. The write command in the register (0x400) and read back the command register to verify the command execution. To perform this operation the driver must use a START/WRITE/STOP sequence followed by a START/READ/STOP sequence.

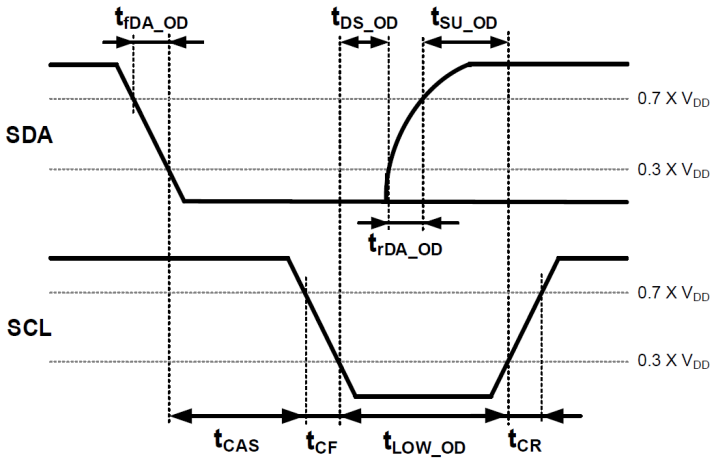
Communication error

If a communication error occurs and the device responds with NACK to all subsequent transactions, the host has to generate a STOP to escape this state.

Timing specification

Maximum T_{LOW}_OD = 500 ns

Figure 14. I3C START timing



Static address 0x00 in I²C

The device does not support 0x00 static address.

Empty transaction

Start condition with stop immediately after is not supported.

4.3 CCI compliance

The device is CCI (I²C) compliant as described in MIPI CSI-2 specification v1.1, with some limitations described below.

Multibyte register read and write.

As detailed in Section 4.1: I²C interface, data is LSB first. It is the same for multibyte register access.

Table 11. Register and bit position

Register address (M)	Bit position [31:0]
M	[7:0]
M + 1	[15:8]
M + 2	[23:16]
M + 3	[31:24]

The device is also compliant with CCI (I3C), with the same limitation on multibyte registers.

4.4 Device registers

The registers are grouped according to function, with each group occupying a preallocated region of the address space. This scheme is purely a conceptual feature and is not related to the actual hardware implementation. All registers can be found at the 7-bit I²C device address.

There are read-only registers that contain device status information, for example, design revision details.

A read and write instruction from an unused register location and a read and write instruction from a reserved address may return any value.

A write instruction to a reserved or unused register location is not allowed and the effect of such a write is undefined. It is the responsibility of the host system to only write to register locations that are defined.

5 Output interface

The host can select to output the data using the MIPI CSI-2 interface or using the I3C (or I^2C interface if desired) interface. This chapter describes how to read and process the data.

5.1 Frame content

For an active output interface, the data buffers are always packed in four arrays:

- Range array
- Amplitude array
- Ambient array
- DSS array

The array size depends on the mode, the frame ratio, and the binning. The table below summarizes the array size.

Note: Refer to the postprocessing technical note (TN1596) for more details of the data formatting, processing, and filter functions.

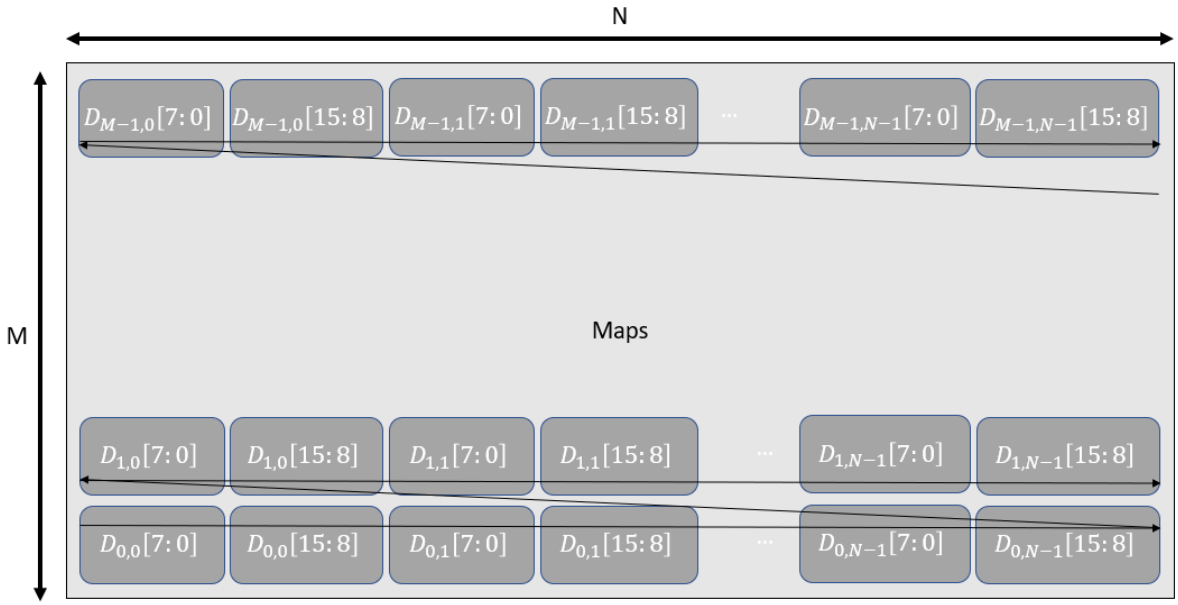
Table 12. Array size summary

Mode	Array resolution	Number of arrays	Binning	Data size (in bytes)	Array size (in bytes)	Minimal CSI frame dimension (in bytes) (1)
Ranging	54 x 42	4 (2)	2	2 (3)	14742	14842
	24 x 20 (4)		4		3744	3844
	18 x 14		6		1638	1738
	12 x 10		8		780	880
	8 x 6 (4)		12		416	516
	4 x 4 (4)		24		104	204

1. *Including the status Line dimension (100 bytes).*
2. *Depth map, amplitude map, ambient map, DSS map.*
3. *Depth, amplitude, and ambient data are coded in 2 bytes (UINT16) and DSS data is encoded on 4 bits per zone (two zones per byte from 0 to 7).*
4. *Static cropping enables matching the final array resolution.*

Multibyte data is stored in little-endian (LSB first) and starts from row 0, column 0. Sorted column by column, and then row by row. The figure below shows the data order for an N x M resolution array.

Figure 15. Data order for N x M resolution array



Sensor status data (status line)

Sensor status data provides static or dynamic information during the streaming. The list below provides details about the information present in sensor status data.

- Frame counter
- Temperature: Sensor and laser driver
- Reference array data: Channel 1 & 2, step long & short, distance & amplitude
- CSI-2 frame dimension: width and height
- Static settings: mode, format, power, synchro
- Dynamic setting: step number, context, binning, DSS mode
- Error code
- FW error status
- LDD error status
- Crop information
- Number of shots

5.2 MIPI CSI-2 interface

The CSI-2 interface outputs the data on one single lane at maximum 1 Gbps and minimum 200 Mbps.

CSI-2 functional layer

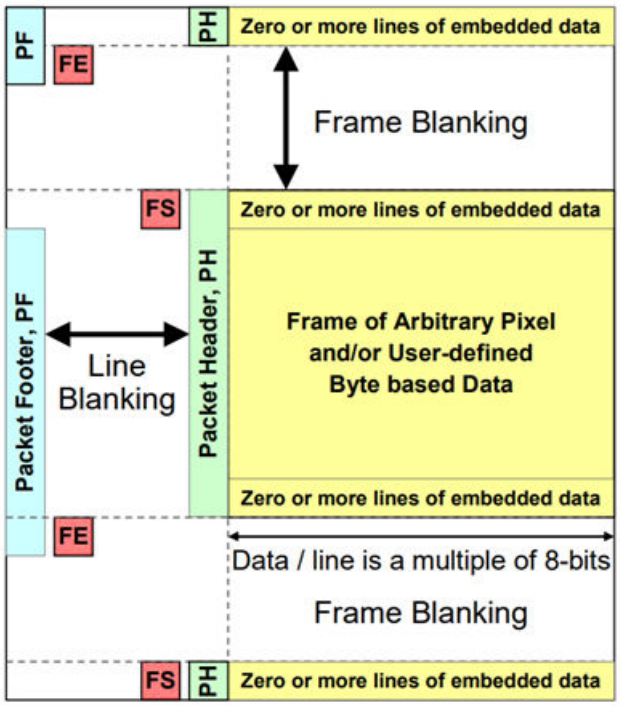
The physical layer includes:

- 1 clock lane @ 500 MHz
- 1 data lane @ 1 Gbps

CSI-2 frame format

The figure below illustrates the frame format.

Figure 16. CSI-2 frame format



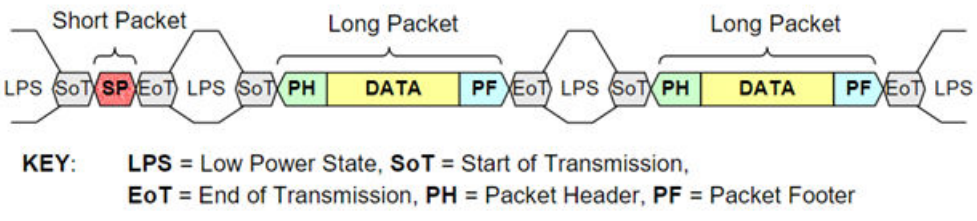
The CSI-2 uses MIPI D-PHY as the physical layer with two power levels:

- High-speed (HS)
- Low power (LP)

During high-speed power level, two types of packets are transmitted surrounded by start of transmission (SoT) and end of transmission (EoT) signaling:

- Short packet
- Long packet

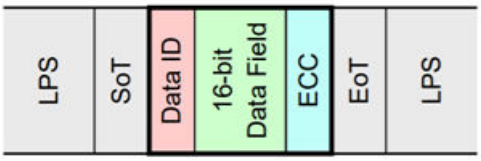
Figure 17. Packet example



Short packet format

- Data ID (DI) - 8 bits: Contains the virtual channel identifier and the data type code. Data type code denotes the format/content of the application specific payload data. Used by the application specific layer. The data type used to transmit the data is *0x30 (user-defined format)*
- 16-bit data field can be:
  - **Frame start (FS) / Frame end (FE) packets**: Frame count number
  - **Line start (LS) / Line end (LE) packet** (OPTIONAL): Line number
  - **Generic short packet code** (OPTIONAL): An arbitrary data value

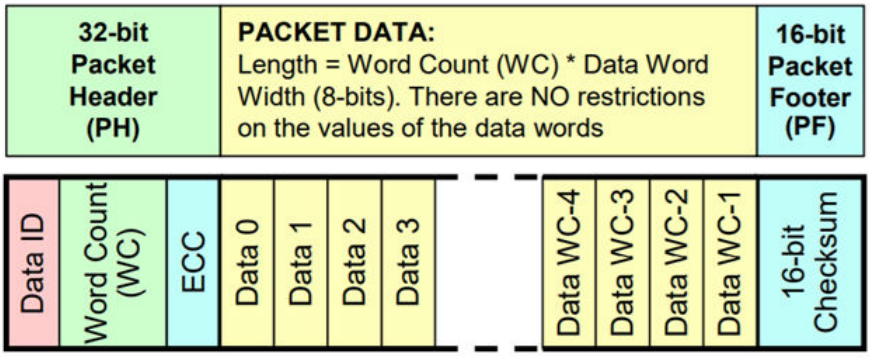
Figure 18. Short packet format example



Long packet format

- **Data ID (DI) - 8 bits**: Contains the virtual channel identifier and the data type code. Data type code denotes the format/content of the application specific payload data. Used by the application specific layer. The data type used to transmit the data is *0x30 (user-defined format)*
- **Word count (WC) - 16 bits:** Rx reads the next WC data words independent of their values. Rx uses the WC value to determine the end of the packet. Word count value is transmitted least significant byte first.
- **Error correction code (ECC) – 8 bits**: ECC code for the packet header. Allows 1-bit errors with the packet header to be corrected and 2-bit errors to be detected (common code with display).

Figure 19. Long packet format example



Frame format

The device allows the user to adapt the CSI-2 frame format. The user can configure the data and embedded data types, and frame width and height. Embedded data and data share the same width/height configuration.

Warning: *The total bytes transmitted must be greater or equal to the total active bytes. Otherwise, an error is raised.*

Configuration and guideline

The host application should have the following configuration:

- ISL data type: 0x12
- Frame data type: 0x2a
- Frame width: 100
- Frame height: Enough lines to output all the data depending on the mode and binning configuration
- Virtual channel: 0 (all data use the same virtual channel)
- Data rate: 1Gbps

The figure below shows the packet format for the configuration above.

5.3 I3C output interface

When using the I3C (or I^2C) to output the data, the host uses the communication interface to read the array of data and acknowledge the frame. The data is not updated until the host acknowledges the frame.

Note: The final frame rate depends on the host capability to read and acknowledge the frame in the allotted time to achieve the expected frame rate.

The frame data and sensor status are available from the user interface.

6 Thermal characteristics

6.1 Absolute maximum rating (T_{STG})

The storage temperature (T_{STG}) is the ambient temperature at which the device can be stored with no voltage applied.

Caution: *Stresses above those listed in the following table may cause permanent damage to the device. These are stress ratings only. Functional operation of the device is not implied at these or any other conditions above those indicated in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Table 13. Absolute maximum rating conditions

Parameter	Min	Max	Unit
Storage temperature (T_{STG})	-40	125	°C

6.2 Ambient operating temperature

The ambient operating temperature is the temperature at which the device may be powered and can operate without any damage.

Device performances are tested under typical conditions unless otherwise noted. The device is operational across the recommended temperature range. Performances vary with temperature changes.

Table 14. Recommended operating temperature

Parameter	Min	Typical	Max	Unit
Ambient operating temperature	-30	23	70	°C

Note: To prevent damage, the sensor has security features that stop the streaming and report firmware errors in case the sensor junction temperature goes outside the range -35°C to 105°C.

7 Electrical characteristics

7.1 Absolute maximum ratings

Caution: *Stresses above those listed in the table below may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*

Table 15. Absolute maximum ratings

Parameter	Maximum	Unit
AVDD	3.63	V
DVDD	1.26	
IOVDD	1.98	
VBAT_RX	4.8	
VBAT_LDD	4.8	

7.2 Recommended operating conditions

Table 16. Recommended operating conditions

Parameter	Minimum	Typical	Maximum	Unit
AVDD 2V8	2.65	2.8	2.95	V
AVDD 3V3	3.13	3.3	3.45	
DVDD	1.16	1.2	1.26	
IOVDD 1V2	1.08	1.2	1.32	
IOVDD 1V8	1.62	1.8	1.98	
VBAT_RX	2.8	–	4.8	
VBAT_LDD	2.8	–	4.8	

Note: Supplies may be considered as independent or shared when the level is identical.

7.3 Electrostatic discharge (ESD)

The VL53L9CX is compliant with the ESD values presented in the following table.

Table 17. ESD performance

Parameter	Specification	Conditions
Human body model	JEDEC JS001-2024	± 2kV
Charged body model	JEDEC JS002-2025	± 500 V
Latch up	JEDEC JESD78F-2023	± 150mA

7.4 Current consumption

The current consumption values are given in the table below.

- Typical values are quoted for nominal voltage, process, and temperature (23°C).
- Maximum values are quoted for the worst-case conditions (process, voltage, and temperature).

Table 18. Current consumption

Device state	AVDD		DVDD		IOVDD		VBAT - LDD		VBAT - Rx	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
HW Standby	0.75 µA	5.1 µA	2.5 mA	25 mA	1 µA	32 µA	1 µA	20 µA	1 µA	10 µA
Ready to Boot	0.75 µA	5.1 µA	8 mA	25 mA	15 µA	80 µA	1 µA	20 µA	1 µA	10 µA
Standby	150 µA	200 µA	8 mA	25 mA	50 µA	250 µA	1 µA	16 µA	1 µA	10 µA
Ranging	20 mA	40 mA	50 mA	120 mA	5 mA	10 mA	110 mA	250 mA	20 mA	250 mA

Note: Max currents are measured with a profile streaming at 30 fps with 25 ms exposure duration and 25 W/m² direct illumination. Typical currents have been measured with profiles streaming at 30 fps.

Note: Peak currents at module level may be 50% higher than maximum values. Use appropriate decoupling capacitors to smooth the peaks. Refer to Section 2.7: Application schematic.

7.5 Digital input and output

Table 19. I²C, XSHUT, INTR, and SYNC_IN digital I/O electrical characteristics

Symbol	Parameter	IOVDD	Min.	Max.	Unit
V^{IL}	Low-level input voltage	1V2 / 1V8		0.3 x IOVDD	V
V^{IH}	High-level input voltage		0.7 x IOVDD		
V^{OL}	Low-level output voltage (I_{OUT} = 0.1 mA)			0.2 x IOVDD	
V^{OH}	High-level output voltage (I_{OUT} = 0.1 mA)		0.8 x IOVDD		

Note: The I_{OUT} is not applicable for open drain pins.

Table 20. AP_CLK electrical characteristics (Max 27 MHz)

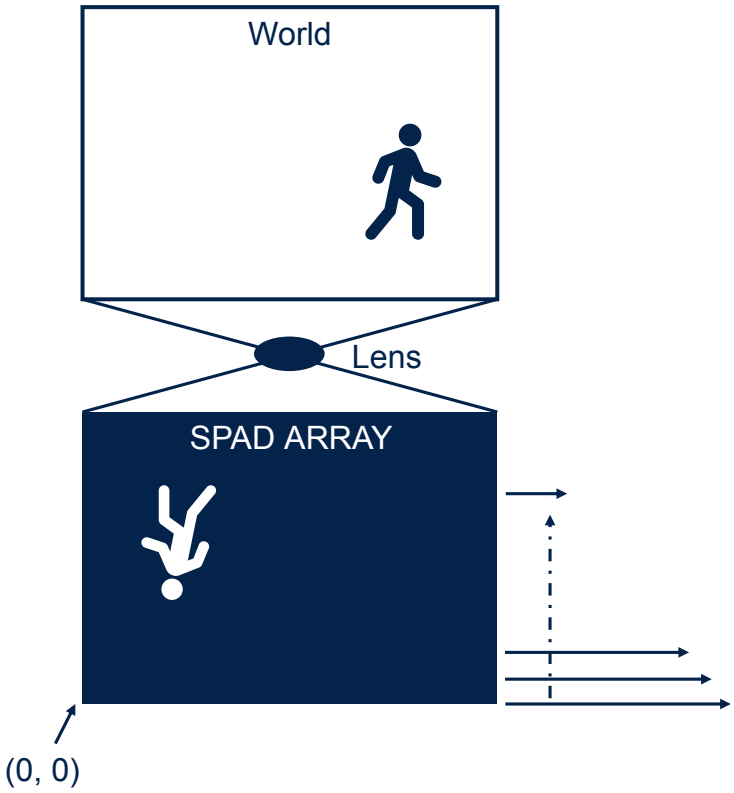
Symbol	Parameter	IOVDD	Min.	Max.	Unit
V^{IL}	Low-level input voltage	1V2 / 1V8		0.1 x IOVDD	V
V^{IH}	High-level input voltage		0.9 x IOVDD		

8 Ranging performances

8.1 Array orientation

The VL53L9CX module includes a lens over the Rx aperture, which flips (horizontally and vertically) the captured image of the target. Consequently, the bottom left of the SPAD array (see Figure 20. Effective array orientation), is illuminated by a target. This target is located at the top right-hand side of the scene.

Figure 20. Effective array orientation



8.2 Test conditions

The following criteria and test conditions apply to all the characterization results detailed in this section unless specified otherwise:

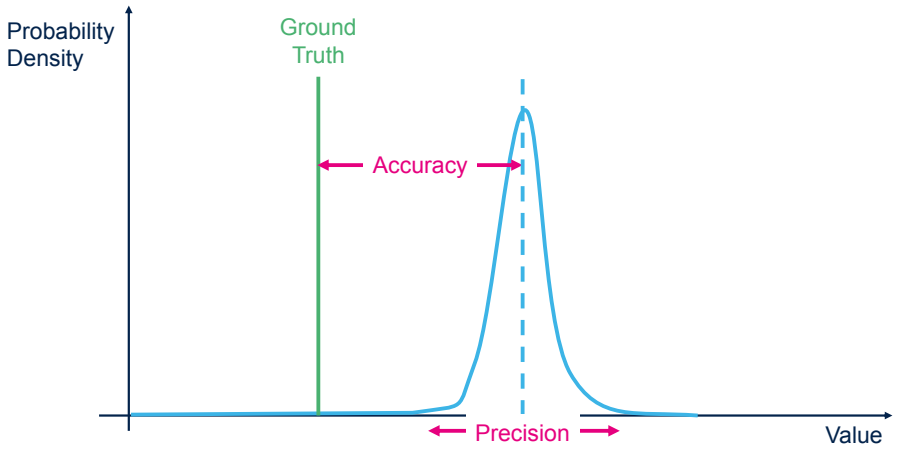
- The target is perpendicular to the module. The radial to perpendicular conversion is applied, except for the per ROI performance. In such conditions, the ROI is perpendicular to the target and measures are kept in radial.
- Targets used are gray 17% (17% reflectance in visible, 12% reflectance in infrared), and light gray 62% (62% reflectance in visible, 58% reflectance in infrared).
- AVDD is 2.8 V, IOVDD is 1.8 V, DVDD is 1.2 V, and VBAT is 3.3 V.
- The nominal ambient temperature is 23°C.
- Maximum range capability is based on a 99% detection rate. The detection rate is a statistical value indicating the worst-case percentage of measurements that return a valid range. For example, taking 1000 measurements with a 99% detection rate, gives 990 valid distances. The 10 other distances may be outside the specification, or flagged with an invalid target status.
- Tests are performed in the dark and with target illumination (940 nm) with 5 klx (1.25 W/m²) and 40 klx (10 W/m²) equivalent daylight.
- All tests are performed without cover glass (unless specified).
- Accuracy, noise, and maximum distance results are typical performances on a typical sensor.
- The module relies on default calibration data.
- The module is controlled through the API using the default driver setting with the profile configuration describe in Table 21. Profile settings.

Table 21. Profile settings

Profile	Precision mode 54x42	Ambient mode 54x42	Precision mode 24x20	Ambient mode 24x20
Resolution	54 x 42	54 x 42	24 x 20	24 x 20
Frame rate (Hz)	30	30	30	30
Exposure (ms)	4 (0 W/m²) 10 (1.25 W/m²)	4 (0 W/m²) 16 (10 W/m²)	4 (0 W/m²) 6 (1.25 W/m²)	4 (0 W/m²) 8 (10 W/m²)
Ranging mode	Precision	Ambient	Precision	Ambient
Power mode	Regular	Regular	Ultralow power	Regular
DSS	Enable	Enable	Enable	Enable

The figure below illustrates the difference between accuracy and precision used in the following chapter.

Figure 21. Accuracy and precision

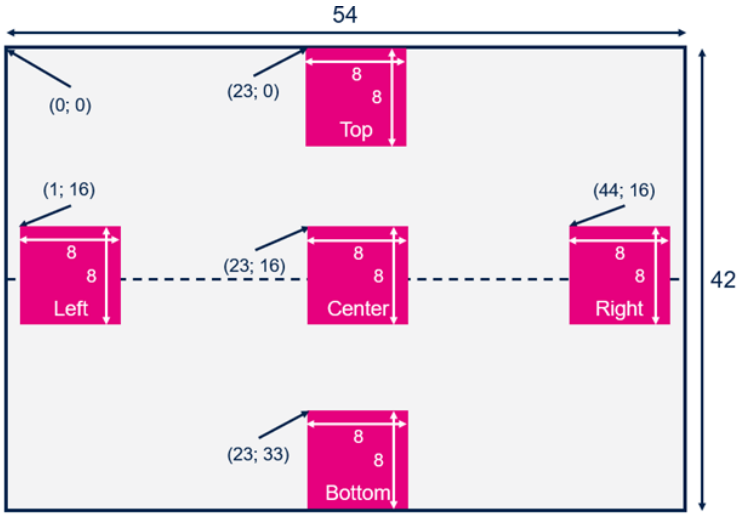


8.3 ROI description

The performance analysis is performed on five different ROIs (region of interest). The localization of the ROIs is described in the figure below. In full resolution the ROIs are 8x8 zones and 4x4 in low resolutions (24x20).

Edges refers to top, bottom, left and right ROIs.

Figure 22. ROI localization on return array



The formulas described in the following sections are computed on the depthmap (D[*t, i, j*]). Where

- *t* is the frame number of a series of frames along time
- *i* is the pixel row
- *j* is the pixel column

$$D_{perp[t,i,j]} = \frac{D[t,i,j]}{\left(\sqrt{\frac{(i-i_c)^2+(j-j_c)^2}{f^2 \cdot \left(1+\propto\left[(i-i_c)^2+(j-j_c)^2\right]\right)^2}}+1\right)}$$

Where:

- *f* is focal length (in pixel)
- α is the distortion coefficient (in pix^{-2})
- *(ic, jc)* are the coordinates of the optical center

8.4 Performance results

8.4.1 Minimum and maximum distance

For minimum ranging capabilities when ranging with different profiles, refer to Section 8.2: Test conditions.

Table 22. Minimum ranging capabilities

Ranging mode	Zone	Minimum ranging distance
Ambient mode	Full frame	450 mm
Precision mode	Full frame	50 mm

For maximum ranging capabilities under different condition with TNR enabled, refer to Section 8.2: Test conditions.

Table 23. **Maximum ranging capabilities (radial distance) for “precision mode 54x42” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure	Outdoor cloudy (1.25 W/m²) 10 ms exposure
Gray 17%	Center	8.8 m	8.0 m
	Edges	8.8 m	8.0 m
Gray 62%	Center	8.8 m	8.8 m
	Edges	8.8 m	8.8 m

Table 24. **Maximum ranging capabilities (radial distance) for “ambient mode 54x42” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure	Outdoor sunny (10 W/m²) 16 ms exposure
Gray 17%	Center	8.5 m	6.0 m
	Edges	8.5 m	6.0 m
Gray 62%	Center	8.5 m	7.0 m
	Edges	8.5 m	7.0 m

Table 25. **Maximum ranging capabilities (radial distance) for “precision mode 24x20” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure	Outdoor cloudy (1.25 W/m²) 6 ms exposure
Gray 17%	Center	8.8 m	8.8 m
	Edges	8.8 m	8.8 m
Gray 62%	Center	8.8 m	8.8 m
	Edges	8.8 m	8.8 m

Table 26. **Maximum ranging capabilities (radial distance) for “ambient mode 24x20” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure	Outdoor sunny (10 W/m²) 8 ms exposure
Gray 17%	Center	8.5 m	7.5 m
	Edges	8.5 m	7.5 m
Gray 62%	Center	8.5 m	7.6 m
	Edges	8.5 m	7.6 m

8.4.2 Ranging accuracy

This section describes the expected ranging accuracy with different profiles with the VL53L9CX. Refer to Section 8.2: Test conditions. The accuracy is defined as the error versus the ground truth.

Error is reported in absolute for short distances and relative for long distances.

$$Absolute \quad error = AVG_{t,\ i,\ j}\left[\left|D_{perp}[t,\quad i,\quad j] - ground \quad truth\right|\right]$$

$$Relative \quad error = \frac{AVG_{t,\ i,\ j}\left[\left|D_{perp}[t,\quad i,\quad j] - ground \quad truth\right|\right]}{ground \quad truth}$$

Note: Self-heating or a change in ambient temperature increases silicon temperature. This can result in an offset drift of maximum ±0.1mm/deg drift.

Table 27. Accuracy for "precision mode 54x42" profile

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor cloudy (1.25 W/m²) 10 ms exposure	
		Short (<1 m)	Long (>= 1 m)	Short (<1 m)	Long (>= 1 m)
Gray 17%	Center	< 8 mm	< 0.5%	< 7 mm	< 0.5%
	Edges		< 0.5%		< 0.5%
Gray 62%	Center	< 8 mm	< 0.3%	< 7 mm	< 0.4%
	Edges		< 0.3%		< 0.4%

Table 28. Accuracy for "ambient mode 54x42" profile

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor sunny (10 W/m²) 16 ms exposure	
		Short (<1 m)	Long (>= 1 m)	Short (<1 m)	Long (>= 1 m)
Gray 17%	Center	< 10 mm	< 0.8%	< 8 mm	< 0.7%
	Edges		< 0.8%		< 0.7%
Gray 62%	Center	< 8 mm	< 0.7%	< 6 mm	< 1.5%
	Edges		< 0.7%		< 1.5%

Table 29. Accuracy for "precision mode 24x20" profile

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor cloudy (1.25 W/m²) 6 ms exposure	
		Short (<1 m)	Long (>= 1 m)	Short (<1 m)	Long (>= 1 m)
Gray 17%	Center	< 8 mm	< 0.4%	< 9 mm	< 0.4%
	Edges		< 0.4%		< 0.4%
Gray 62%	Center	< 6 mm	< 0.3%	< 8 mm	< 0.3%
	Edges		< 0.3%		< 0.3%

Table 30. **Accuracy for "ambient mode 24x20" profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor sunny (10 W/m²) 8 ms exposure	
		Short (<1 m)	Long (>= 1 m)	Short (<1 m)	Long (>= 1 m)
Gray 17%	Center	< 12 mm	< 0.8%	< 8 mm	< 0.5%
	Edges		< 0.8%		< 0.5%
Gray 62%	Center	< 10 mm	< 0.8%	< 6 mm	< 1.8%
	Edges		< 0.8%		< 1.8%

8.4.3 Ranging precision and noise

This section describes the expected ranging precision with different profiles with the VL53L9CX. Refer to Section 8.2: Test conditions. Ranging precision and noise has been computed with TNR enabled. The precision is defined as the temporal noise.

Noise is reported in absolute for short distances, and precision in relative for long distances.

Depthmap is described by *D[t, i, j,]*

- *t:* frame number of a series of frames along time
- *i:* pixel row
- *j:* pixel column

$$Temporal \quad noise = AVG_{i,\ j}[STD_t[D(t, \quad i, \quad j)]]$$

$$Temporal \quad noise = \frac{1}{N_r} \cdot \frac{1}{N_c} \left(\sum_{(i, \quad j) \in [1; \quad N_r] \times [1; N_c]} \left(\sqrt{\frac{1}{N_f} \sum_{t=1}^{N_f} \left(D(t, \quad i, \quad j) - \frac{1}{N_f} \sum_{t=1}^{N_f} D(t, \quad i, \quad j) \right)^2} \right) \right)$$

Where:

- N_r: number of rows
- N_c: number of columns
- N_f: number of frames

Table 31. **Precision for "precision mode 54x42" profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor cloudy (1.25 W/m²) 10 ms exposure	
		Short (< 2 m)	Long (>= 2 m)	Short (< 2 m)	Long (>= 2 m)
Gray 17%	Center	< 1 mm	< 0.07%	< 1.2 mm	< 0.2%
	Edges	< 1 mm	< 0.07%	< 1.2 mm	< 0.02%
Gray 62%	Center	< 1 mm	< 0.05%	< 0.7 mm	< 0.08%
	Edges	< 1 mm	< 0.05%	< 0.7 mm	< 0.08%

Table 32. **Precision for “ambient mode 54x42” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor sunny (10 W/m²) 16 ms exposure	
		Short (< 2 m)	Long (>= 2 m)	Short (< 2 m)	Long (>= 2 m)
Gray 17%	Center	< 1.2 mm	< 0.07%	< 2.5 mm	< 0.6%
	Edges	< 1.2 mm	< 0.07%	< 2.5 mm	< 0.6%
Gray 62%	Center	< 1.2 mm	< 0.04%	< 1.75 mm	< 0.25%
	Edges	< 1.2 mm	< 0.04%	< 1.75 mm	< 0.5%

Table 33. **Precision for “precision mode 24x20” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor cloudy (1.25 W/m²) 6 ms exposure	
		Short (< 2 m)	Long (>= 2 m)	Short (< 2 m)	Long (>= 2 m)
Gray 17%	Center	< 0.8 mm	< 0.035%	< 0.8 mm	< 0.12%
	Edges	< 0.8 mm	< 0.035%	< 0.8 mm	< 0.12%
Gray 62%	Center	< 0.6 mm	< 0.03%	< 0.6 mm	< 0.05%
	Edges	< 0.6 mm	< 0.03%	< 0.6 mm	< 0.05%

Table 34. **Precision for “ambient mode 24x20” profile**

Target reflectance	Zone	Indoor (0 W/m²) 4 ms exposure		Outdoor sunny (10 W/m²) 8 ms exposure	
		Short (< 2 m)	Long (>= 2 m)	Short (< 2 m)	Long (>= 2 m)
Gray 17%	Center	< 0.8 mm	< 0.04%	< 1.8 mm	< 0.3%
	Edges	< 0.8 mm	< 0.04%	< 1.8 mm	< 0.5%
Gray 62%	Center	< 1.0 mm	< 0.03%	< 1.2 mm	< 0.2%
	Edges	< 1.0 mm	< 0.03%	< 1.2 mm	< 0.2%

8.4.4 Ranging uniformity

Ranging uniformity is measured after calibration and radial to perpendicular conversion with different target at different distances. Uniformity is evaluated by computing the depth fixed pattern noise in the dark (0 klx).

$$FPN = STDij\left[AVGt\left[D_{perp}[t,i,j]\right]\right]$$

Table 35. **Uniformity**

Target reflectance	Profile	150 mm	500 mm	1000 mm
Gray 17%	Precision mode 54x42	< 4 mm	< 3.5 mm	< 4.5 mm
	Ambient mode 54x42	-	< 4.5 mm	< 4 mm
	Precision mode 24x20	< 3.5 mm	< 3.5 mm	< 5 mm
	Ambient mode 24x20	-	< 4.5 mm	< 5.5 mm
Gray 62%	Precision mode 54x42	< 4 mm	< 3.5 mm	< 4.5 mm
	Ambient mode 54x42	-	< 4.5 mm	< 5 mm
	Precision mode 24x20	< 3.5 mm	< 3.5 mm	< 5 mm
	Ambient mode 24x20	-	< 4.5 mm	< 5.5 mm

8.4.5 Power consumption in ranging

Typical power consumption is measured with the default profile configuration, under different ambient light conditions. Power consumption table below shows typical power consumption with the profiles and exposure described in Table 21. Profile settings.

Table 36. Power consumption

Target reflectance	Profile	Indoor (0 W/m²)	Outdoor cloudy (1.25 W/m²)	Outdoor sunny (10 W/m²)	Unit
Gray 17%	Precision mode 54x42	235 (max: 250)	370 (max: 400)	—	mW
	Ambient mode 54x42	225 (max: 240)	—	560 (max: 625)	
	Precision mode 24x20	145 (max: 150)	180 (max: 310)	—	
	Ambient mode 24x20	225 (max: 240)	—	343 (max: 375)	
Gray 62%	Precision mode 54x42	235 (max: 250)	390 (max: 435)	—	mW
	Ambient mode 54x42	225 (max: 240)	—	645 (max: 820)	
	Precision mode 24x20	145 (max: 150)	190 (max: 320)	—	
	Ambient mode 24x20	225 (max: 240)	—	375 (max: 470)	

9 Outline drawings

VL53L9CX is a dToF module (12.83 mm x 6.10 mm x 4.64 mm) composed of two parts. The receiver (Rx) is a SPAD array (on the left). The right part of the transmitter is composed of two VCSELs and an associated driver managing the active illumination. There is an optical barrier between the Rx and the Tx, which minimizes the crosstalk between both parts, and improves the accuracy of the data. The figures below illustrate the VL53L9CX module.

Note: These module drawings are based on DM01164348 rev 3.0.

Figure 23. Module outline (1 of 2)

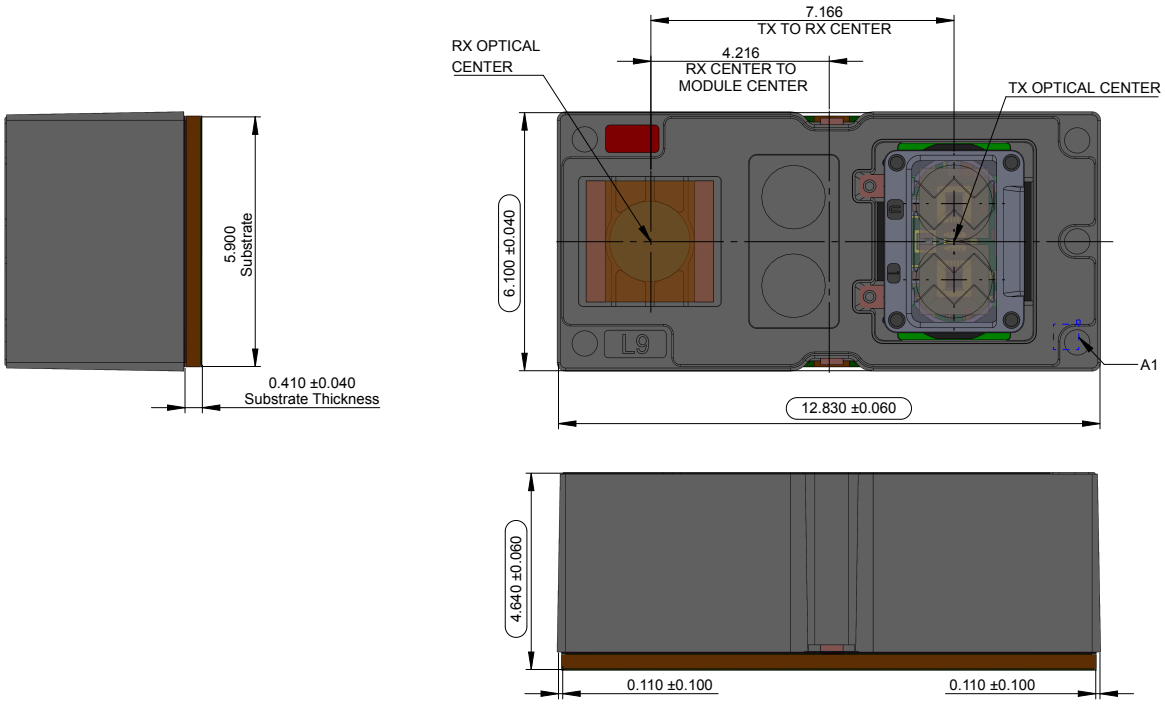


Figure 24. **Module outline (2 of 2)**

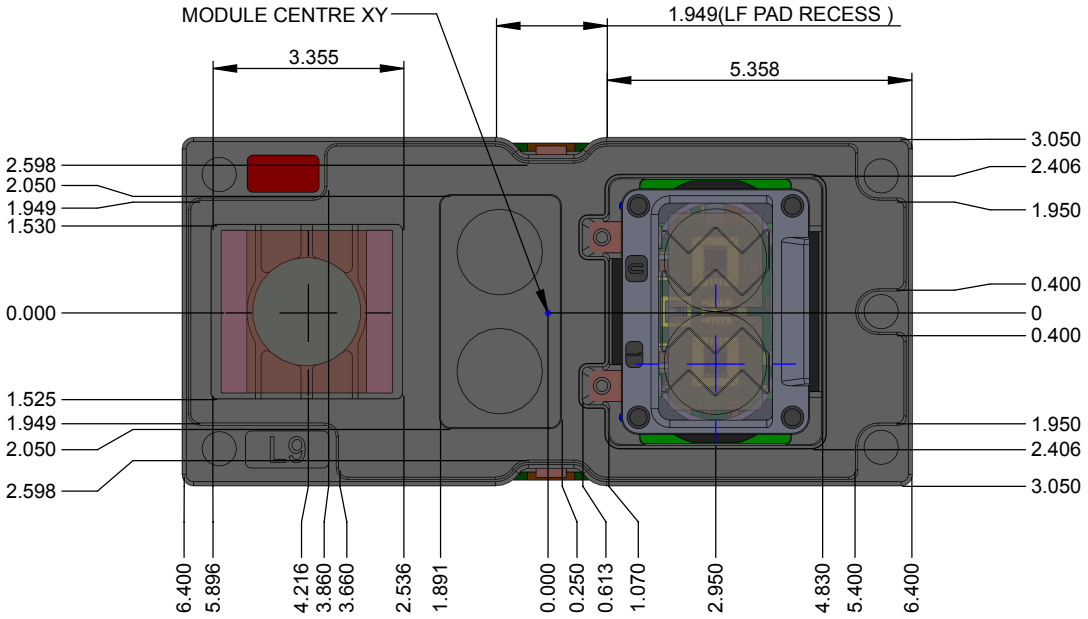


Figure 25. **Substrate pads (bottom view)**

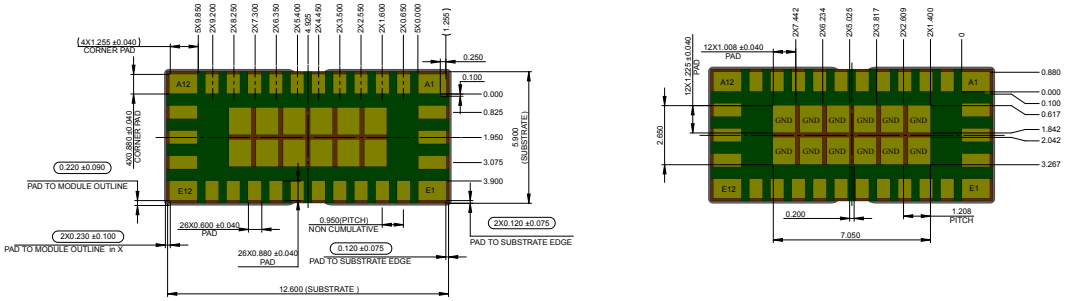


Figure 26. **Field of view**

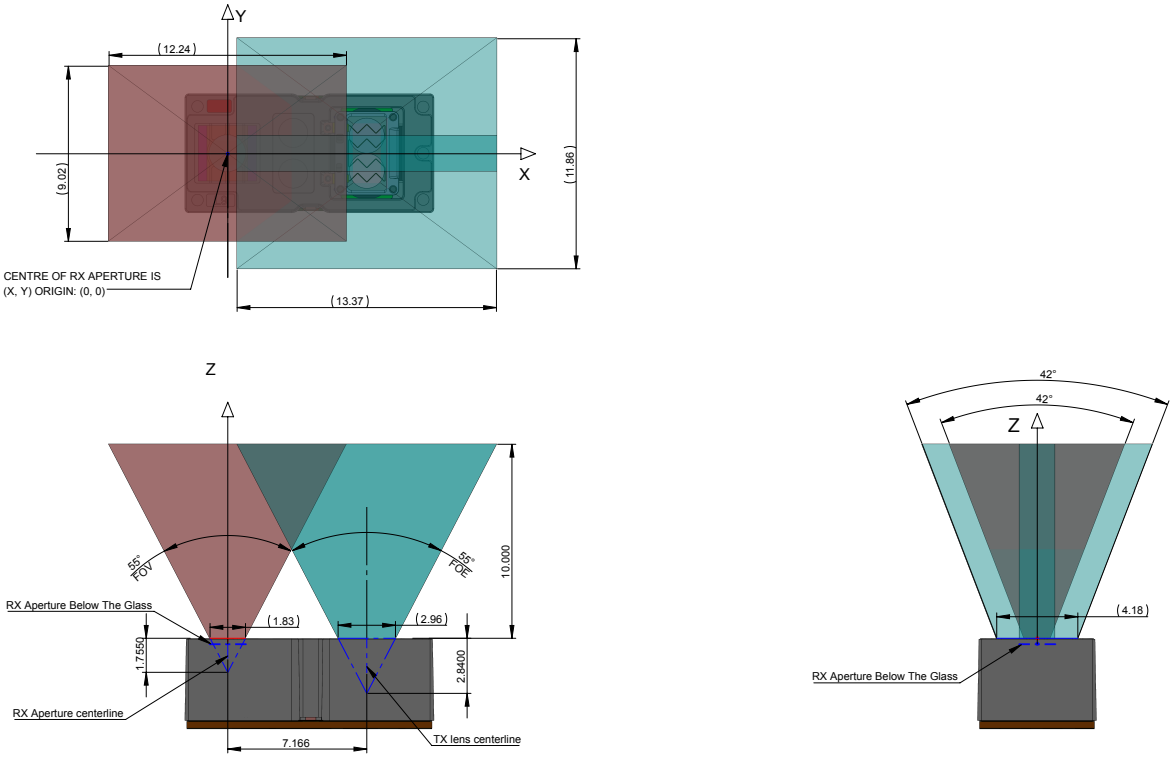
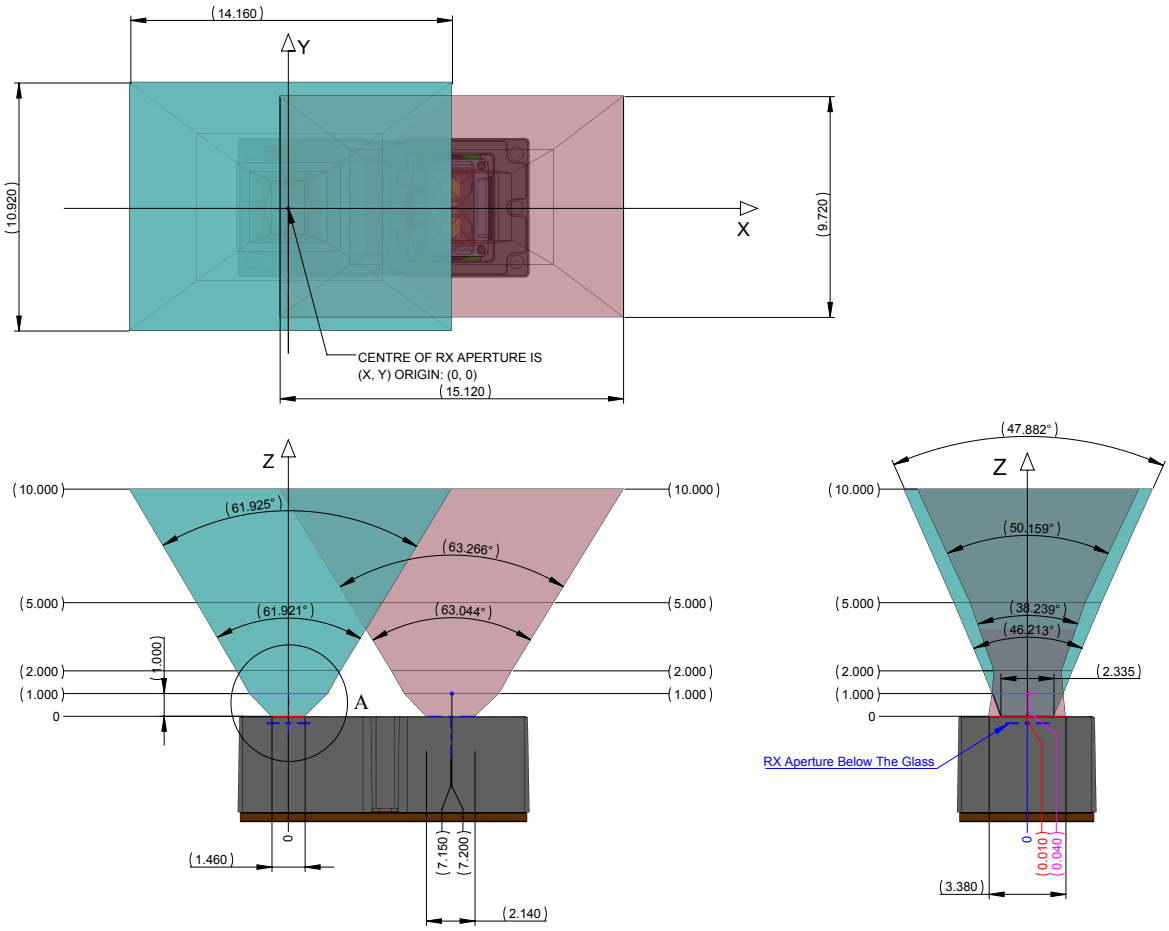


Figure 27. **Exclusion cones**



Exclusion cones are defined as an area slightly larger than the FoV that is recommended to exclude casing or shielding that may affect the FoV. Not all signals are dissipated at the edge of the FoV. Therefore, it is recommended in enclosures with thick walls, to apply an additional keep-out area. This avoids creating false targets from signal reflections from the cavity wall of the product enclosure.

Exclusion cones should be considered for the design of both the cover glass and the application apertures. Cover glass integration guides and aperture calculator tools are available on st.com.

Table 37. **Rx and Tx exclusion zones**

Rx exclusion zone rectangle					Tx exclusion zone rectangle				
Z	Centroid coordinates		Edge length along axis		Z	Centroid coordinates		Edge length along axis	
	X	Y	X	Y		X	Y	X	Y
0	0.01	0.01	1.46	2.34	0	7.15	0.01	2.14	3.38
1	0.04	0.04	3.44	3.12	1	7.20	0.04	4.16	3.12
2	0.04	0.04	4.56	3.92	2	7.20	0.04	5.28	2.96
5	0.08	0.04	8.16	6.48	5	7.20	0.04	8.96	5.04
10	0.12	0.06	14.16	10.92	10	7.20	0.06	15.12	9.72
100	1.00	0.25	129.00	97.50	100	7.25	0.25	132.50	98.50
1000	10.00	4.00	1308.00	992.00	1000	12.00	4.00	1320.00	992.00

10 Laser safety

This product contains a laser emitter and corresponding drive circuitry. The laser output is designed to meet Class 1 laser safety limits under all reasonably foreseeable conditions including single faults in compliance with IEC 60825-1:2014.

Do not increase the laser output power by any means. Do not use any optics to focus the laser beam.

Caution: *Use of controls, adjustments, or procedures other than those specified herein may result in hazardous radiation exposure.*

Figure 28. Class 1 laser label

This product complies with:

- IEC 60825-1:2014
- 21 CFR 1040.10 and 1040.11, except for conformance with IEC 60825-1:2014 as described in the laser notice number 56, dated May 8, 2019.
- EN 60825-1:2014 including EN 60825-1:2014/A11:2021
- EN 50689:2021, however STMicroelectronics does not guarantee compliance with the requirement of clause 5 from EN50689 regarding child appealing products. If designing a child appealing product, contact STMicroelectronics' technical application support.

11 Packing and labeling

11.1 Product marking

There are two types of product marking:

- The first is on the backside of the module, as shown in Section 9: Outline drawings.
- The second is on the corner of the module cap.

Product marking on the backside of the module

This is a two-zone product marking. The first marking is the silicon product code. The second is the internal tracking code.

Product marking on the corner of the module cap

A 2D product marking code is applied on the corner of the module cap.

11.2 Inner box labeling

The labeling follows the STMicroelectronics' standard packing acceptance specification. The following information is on the inner box label:

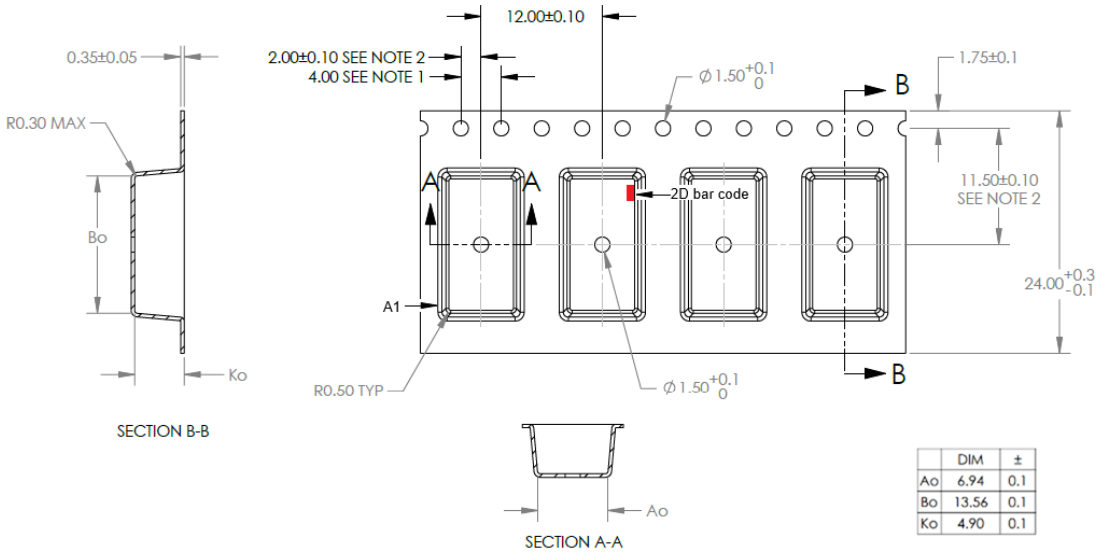
- Assembly site
- Sales type
- Quantity
- Trace code
- Marking
- Bulk ID number

11.3 Packing

The module is shipped in a tape and reel format (see Section 14: Ordering information). At customer/subcontractor level, it is recommended to mount the VL53L9CX in a clean environment to ensure no contamination of the module laser cavity.

11.4 Tape outline drawing

Figure 29. Carrier tape outline



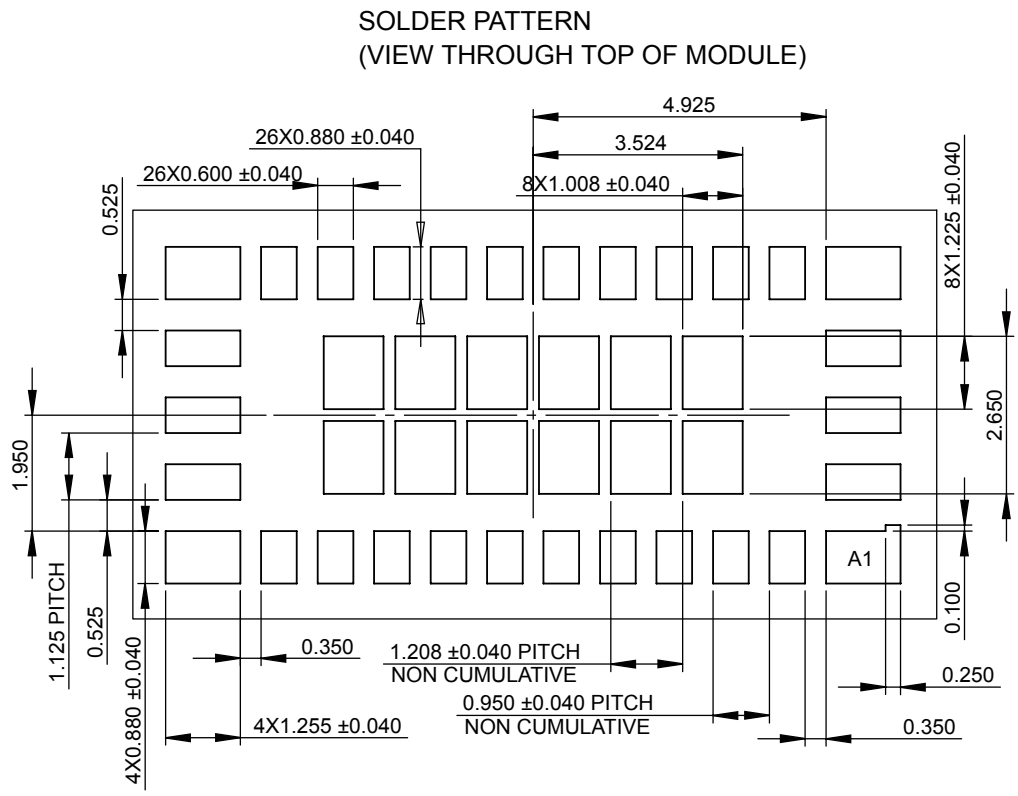
Note:

1. *10 sprocket hole pitch cumulative tolerance ±0.2*
2. *Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.*
3. *A0 and B0 are measured on a place at the distance "R" above the bottom of the pocket.*
4. *A1 pad is bottom left inside the carrier tape.*

12 Handling, moisture and reflow precautions

12.1 Recommended solder pad dimensions

Figure 30. Solder pattern



Note: To avoid issues with solder voids it is recommended that the large thermal pad in the center of the footprint is created with tented vias or split into multiple smaller pads.

12.2 Shock precautions

Sensor modules house numerous internal components that are susceptible to shock damage. If a unit is subject to excessive shock, is dropped on the floor, or a tray/reel of units is dropped on the floor, it must be rejected, even if no apparent damage is visible.

12.3 Part handling

Handling must be done with non-marring ESD safe carbon, plastic, or Teflon™ tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process until a protective cover glass is mounted.

12.4 Compression force

A maximum compressive load of 25 N should be applied on the module.

12.5 Moisture sensitivity level

Moisture sensitivity is level 3 (MSL) as described in IPC/JEDEC J-STD-020-F - 2022.

For devices that are classified to the levels defined in JEDEC J-STD-020-F - 2022, JEDEC J-STD-033-D - 2018 provides:

- Manufacturers and users with standardized methods for handling, packing, and shipping.
- Standardized methods for using moisture/reflow and process sensitive devices.

12.6 PB-free solder reflow process

The table and figure below show the recommended and maximum values for the solder profile.

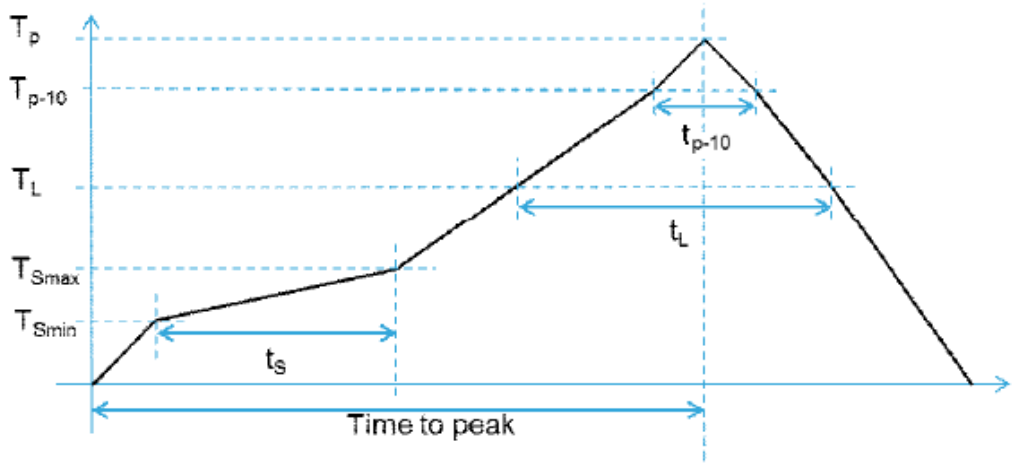
Customers must tune the reflow profile based on the PCB, solder paste, and material used. The product reflow must follow the JEDEC J-STD-020 standard. The illustration below is provided for as an example.

If a different reflow profile is required, especially a profile with a peak of 245°C, the customer is responsible for qualifying the new profile. In all cases, the profile must be within the maximum limits specified in the table below.

Table 38. Recommended solder profile

Profile feature	Pb-free assembly
Preheat/Soak Temperature min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	245°C
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Figure 31. Solder profile



Note: The component should be limited to a maximum of four passes through this solder profile.

Note: As the VL53L9CX package is not sealed, only a dry reflow process should be used (such as convection reflow). Vapor phase reflow is not suitable for this type of optical component.

Note: The VL53L9CX is an optical component and as such, it should be treated with care. This includes using a 'no-wash' assembly process.

Solder profile

The VL53L9CX module can withstand five reflows.

- One reflow during ST production
- Up to four reflows at customer product assembly

13 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

14 Ordering information

The VL53L9CX is currently available in the format below. More detailed information is available on request.

Table 39. Order codes

Order code	Package	Packing	Minimum order quantity
VL53L9CXV0VE/1	Optical LGA	Tape and reel	1000

Revision history

Table 40. **Document revision history**

Date	Version	Changes
18-May-2026	5	First public release.
15-Jun-2026	6	Updated: Table 19. I²C, XSHUT, INTR, and SYNC_IN digital I/O electrical characteristics
10-Jul-2026	7	Updated Table 18. Current consumption. Table 19 and Table 20: Modified V^{H} by V^{IH} and V^{L} by V^{IL}.

Contents

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