

EMI/EMC and Co-Existence Simulation Methodology for High Performance Digital, Mixed Signal and RF Wireless Products

Design complexity of high-performance electronics systems, including chip-package-board and mechanical surrounding, has dramatically increased in the past years ^{[1][2]}. Due to the growing integration of high-speed digital features (HDMI2.0, USB3.1, LP/DDR4, CPU, etc.), reaching compliance with EMI/EMC standards (Electro-Magnetic Interferences and Compatibility) has become challenging. Moreover EM co-existence issues with RF wireless/analog interfaces (WiFi, Bluetooth, ZigBee, etc.) can potentially occur, causing integrity problems and bandwidth reduction. In some cases, fixing the EMI/EMC issues requires a re-design of the product and delays mass-production.

Based on our experiences in domains such as consumer, mobile, imaging and automotive product development, this paper presents the challenges and the achievements in the development of a new simulation methodology to estimate, investigate and address radiated EMI/EMC/Co-existence issues. The first part of this paper introduces examples of radio-frequency interferences which can occur and EMI/EMC standards. Then the Ansys EMI/transient co-simulation flow and methodology are presented based on a real case study. Importance of correlations with measurements is highlighted, as it enables further evaluation EM mitigation techniques.

1. Complexity to Achieve EMI/EMC Standards and Avoid Co-Existence Issues

A. Introduction on EM Co-Existence

Modern electronic systems offer very often a strong integration of features (see Figure 1) such as high-speed digital links (DDR, USB3.1, HDMI2.0, etc.) and sensitive analog/RF functions (WiFi 802.11 or Bluetooth). Proper co-existence of all platform functionalities has to be ensured. Digital interfaces are often considered as potential EMI aggressors and can be activated simultaneously with RF wireless systems. The challenge is then to ensure that in a complete system, each individual RF wireless system behaves at the same level of RF performances as in standalone.

HDMI2.0 and (LP)DDR3/4 standards are high-density and high-speed interfaces, which can generate potentially many possible co-existence issues. Common-Mode (CM) and Differential-Mode (DM) excitations of lanes (especially for differential clocks) can generate strong EMI.

Receiver systems should be capable to process very small signals characterized by the reference sensitivity at the antenna. For instance, a WiFi receiver can operate signals as low as -82dBm or -155dBm/Hz. This is required by IEEE for 6Mbps throughput and 20MHz BandWidth [BW]) in order to maintain a satisfying PER (Packet Error Rate) of 10%. In addition, the WiFi receiver systems operate in both ISM 2.4GHz and 5GHz bands. If a WiFi antenna is placed quite close to any of potential EMI aggressors, WiFi sensitivity can be affected and RF throughput can be significantly degraded. Due to coupling complexity and possibilities on a full system (see Figure 2), investigations of co-existence issues are often difficult and time-consuming.

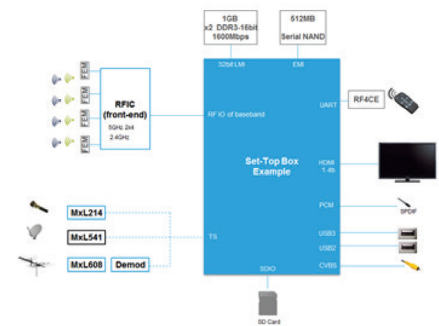


Figure 1. Example of a Set-Top Box with WiFi and other high-speed interfaces and IP's: HDMI, DDR3.

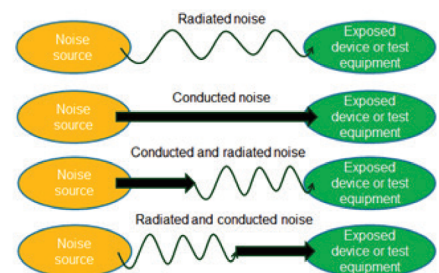


Figure 2. Complexity of EM noise propagation and coupling.

/ B. EMI/EMC Standards

Consumer electronic devices or systems such as mobiles or Set-Top boxes have to comply with EMI/EMC standards. In Europe, all domestic products should follow CISPR22 class "B" recommendations. In the revision 5.2 2006-03 [3], EMI measurements are done below 1GHz at 10m using a resolution bandwidth (RBW) of 120KHz and peak electrical field radiation should remain below 30 or 37dBuV/m. Above 1GHz, at 3m and for a RBW of 1MHz, peak radiations should not exceed 70 or 74dBuV/m. Regarding EM compatibility, additional tests are done including ESD discharges or checks of product immunity against conducted or radiated stimulus. In North America and Asia, EMI/EMC standards are different (ex. FCC standard as on Figure 3 [4]), but products should comply to the appropriate standard whenever required.

In order to avoid re-design and delay in mass-production, it is advised to start preparing EM and co-existence aspects early at the beginning of the product design. This includes considering all mitigation techniques and implementation guidelines on architecture, technology, product sizing and layout design.

/ 2. EMI-Transient Co-Simulation Methodology

/ A. Importance of Understanding EMI Theory

Before starting to use the tools, it is essential to make sure that we have sufficient understanding of the EMI theory on the device that is being analyzed. For a digital differential pairs, there are several current excitations and interconnect loops that generate EMI (Figure 4):

- Differential-mode (DM) excitation and loop.
- Common-mode (CM) excitation and loop.
- Crosstalk current and loop.

Some equations detailed in [5] helps to estimate radiated EM field. On a digital interface example, at 148.5MHz, the H field dominates the E field and a model of a long-differential wire in near-field conditions can be used:

$$H \text{ (mA/m)} = 0.16 \cdot C \cdot I \cdot \frac{S}{D^2}$$

I is the excitation current in mA, S is the loop separation distance in m and D is the measurement distance in m. C is a coefficient coming from the structure's ground planes underneath (0.45 in this case). Validity of this equation is limited by the complexity of the structure, but still good approximation can be done as shown in Figure 5.

Academic approach is useful to understand in our case that:

- Magnetic Near-field decreases with 1/D².
- DM radiations are proportional to the DM currents, which are bounded by the standard.
- CM radiations are proportional to the CM currents, which are essentially defined by the quality of the balancing/symmetry of P/N drivers and passive interconnect.
- CM or DM radiations are proportional to the areas of the loops (s or h), which are set by the PCB/Connector technology and design strategies.

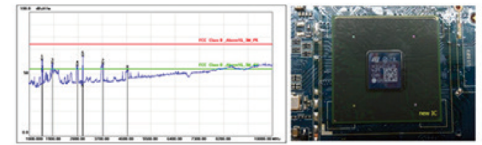


Figure 3. FCC above 1GHz EM emission test for a SOC.

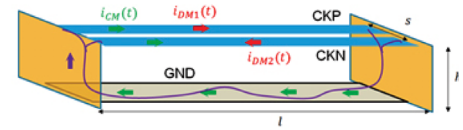


Figure 4. PCB differential pair with loop geometries and currents.

D (mm)	H (mA/m) Simulated @148.5MHz	H (mA/m) Formula @148.5MHz
0.15	5310	6390
6.50	3.5	3.3

Figure 5. Estimated and simulated H fields show good correlation.

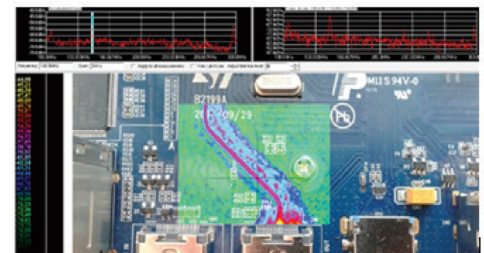


Figure 6. Magnetic near-field map of a digital interface with four differential pairs (three data lanes and one clock).

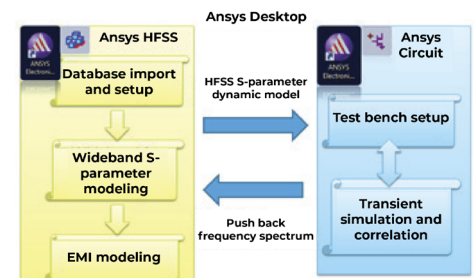


Figure 7. Ansys EMI flow as used within STMicroelectronics.

/ B. Overview of the Simulation Methodology With Correlations

The methodology described hereafter was verified and approved after successful comparison of simulation and measurement results on a digital high-speed interface case (Figure 6).

The EMI simulation flow uses the Ansys tools suite [6] with:

- HFSS, a 3D FEM full-wave electromagnetic solver, to model the structure and calculate the EM fields.
- Ansys Circuit, an electrical spice-like solver, to do transient simulation using HFSS model and realistic excitation patterns. Results of the simulation are back-annotated in HFSS to compute final EM fields.

Both time and frequency domain simulations done within the two tools above are required to reproduce a real-case EMI fields. Automation around exchange of data (S parameter model and frequency spectrum at port level) is ensured by the Ansys EMI flow as depicted Figure 7.

The methodology development consists in finding the best settings to obtain results within expected accuracy and limit the simulation time.

In this perspective, it is essential to reduce the model complexity in HFSS (Figure 8). Investigations have been led to define the appropriate cut-out clearance rules. Then essential simulation parameters include the bounding box type and size around the structure, the port types, the frequency sweep for the wideband S-parameter modeling, the meshing settings and the convergence criteria.

The HFSS S-parameter model is linked inside the Circuit environment and it is instantiated in the schematic (Figure 9). Note that by default the S-parameter model is converted automatically in a spice-like model. The port excitations are set by drivers in IBIS format, using pseudo random bit sequence (PRBS) to reproduce a real use-case. Before running the simulation, the schematic should be complete including models with adequate accuracy. Moreover parameters such as transient step and stop time are very important since they are used to generate the frequency spectrum at port levels through the FFT. Resolution bandwidth (RBW) is linked to StopTime and bandwidth (BW) can be limited by the time step. For instance, a 15 bits length PRBS creates sub-harmonics every 45.32KHz. As the smallest frequency needed in this context is the frequency of the first sub-harmonic, the sampling frequency of the time-domain excitation must be smaller. A quarter of the first sub-harmonic value gives a good compromise between this constraint and the transient simulation duration (SamplingFrequency=11.33KHz => stopTime = 88.33µs).

After the transient simulation, eye diagram correlations are advised to build confidence in the setup:

The next step is to push back the excitation into HFSS in order to re-calculate the EMI fields. As underline above, the parameter used for the FFT (BW, RBW, windowing, etc.) have to be carefully chosen to match the measurement setup. Simulation and measurement of EMI are focused on the magnetic field which dominates the electrical field in our case. Near-field conditions are also considered to avoid being affected by external environment (fan, casing, etc.). This means that the distance D between the emitter and the scan is less than $\lambda/(2\pi)$, where λ is the maximum wavelength. The EMI victim being the WiFi interface, the bandwidth is 0-6Ghz and λ is therefore 8mm. For flexibility and investigation purposes, 2 EMI scan plans above the structure have been set at D=0.15mm and D=6.5mm.

/ C. EMI Evaluation Criteria and Post-Processing

The methodology described hereafter was verified and approved after successful comparison of simulation and measurement results on a digital high-speed.

On our case, the H field dominates the E field. So to define quality criteria and evaluate risks of interferences with RF interfaces, we select the H field average as the metric:

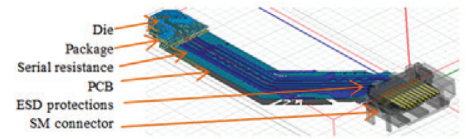


Figure 8. Simulation in HFSS 3D structure.

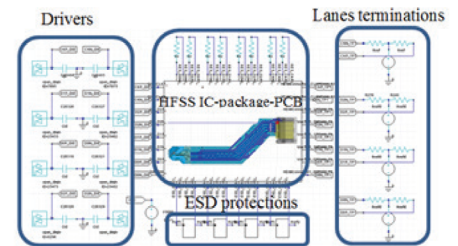


Figure 9. Schematic in the Circuit environment with the HFSS model.

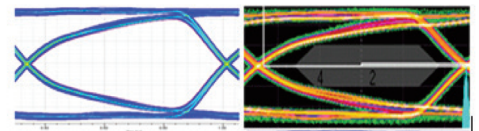


Figure 10. Good correlations between the simulation (left) and the measurements (right) in time domain.

$$H_{av} \left(\frac{\text{dBmA}}{\text{m}} \right) = \frac{1}{\text{Scan area}} \iint_{\text{Scan area}} \text{Peak (H, phase)} + 60\text{dB}$$

H_{av} takes into account the average radiation rather than maximum radiation and it uses the maximum field in A/m on full phase sweep $[0^\circ ; 360^\circ]$. This formula can be set through the HFSS calculator. Frequency sweep plot of the average magnetic field (Figure 12) is our reference for further investigation on EM mitigation techniques:

On our case, about 15% of the H-field is coming from the connector, 82% from the PCB and only 3% of the package. Nevertheless, the connector being about 5mm above the PCB routing, its impact on EMI can be consequently higher, depending on the RF antenna placement. Connector type, which is here a surface mounted shielded connector, also plays an important role.

3. Investigations on EMI Mitigation Techniques

A. Functional Techniques To Mitigate EMI Risks

The functional techniques can be very efficient with limited impact on product cost, if there are engineered at the beginning of the project. SR (Slew Rate) control is a well-known technique. A SR going from 5 to 8% of UI (Unit Interval) gives in average 3 dB of mitigation on clock frequency spectrum. Radiated magnetic field is decreased accordingly. However SR control impacts jitter and since most high-speed link interfaces have stringent jitter requirements, this solution has often limitations. Spread spectrum clock (SSC) is also another common way to mitigate the EMI which is defined in many high-speed link standards [9] [10]. It is achieved through frequency modulation and generally limited by clock PPM tolerance and jitter. EMI decreases by up to 10dB on the 3rd harmonic and 15dB on the 5th harmonic.

Data scrambling is meant to spread and lower frequency spectrum by avoiding repetitive bit sequences. Several methods exist today and some of them are used in standards. Mitigation on EMI can go up to 20dB [9] [10].

B. Physical Layout Techniques To Mitigate EMI Risks

As discussed previously, CM noise can be a major contributor to EMI. Common-mode filters (ECMF) are developed by STMicroelectronics and packaged within PCB ESD protection. The coupled inductances of the ECMF are filtering out all in-phase signals and letting differential signals go through. As an example, the ECMF04-4HSWM10 is cutting the CM noise between 1 and 6GHz by 15dB [7]. ECMF location is key for signal integrity and EMI mitigation efficiency. Placement close to SOC is preferred (option 3), as shown on Figure 14, Figure 15 and Figure 16.

EMI reduction occurs mainly on even harmonics coming from common-mode noise (10th, 16th, 34th, 36th, 38th and 40th harmonics). Additional EMI simulation scan are clearly showing that well-placed ECMF is blocking CM noise and limiting the radiations.

PCB buried routing strategy and mechanical shielding are also known EMI mitigation technics (Figure 17).

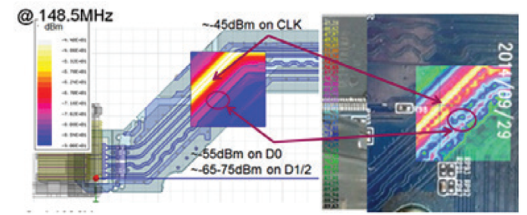


Figure 11. Simulation (left) and measurement (right) of the near-field magnetic field at D=0.15mm.

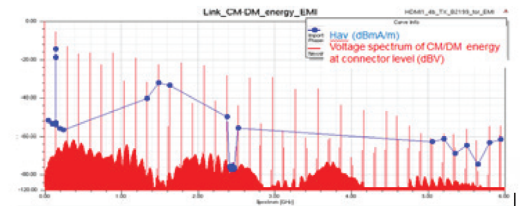


Figure 12. Cumulated clock CM/DM frequency spectrum at TP1 in red and for D=0.15mm.

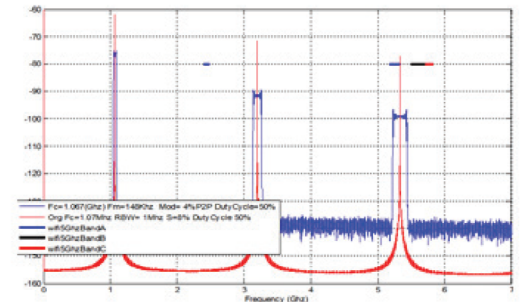


Figure 13. Example of SSC.

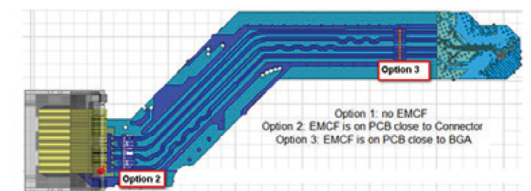


Figure 14. three options of location of the ECMF.

Since consumer boards are using very often through-hole (TH) vias, which can affect the SI margins and EMI performances, we recommend back-drilling of the sensitive vias for low cost applications containing a limited density of high speed signals. PCB over-cost is limited compared to laser drilled vias (10% versus up to 50%). During the buried routing PCB design, it is essential to pay attention to the resonances. This means that distances from die bumps to major discontinuities that would match $\lambda/4$ of sensitive frequency bands should be avoided (λ being the wavelength corresponding to a WiFi channel band for instance).

Shielding is also commonly used in consumer or mobile implementations as designed on Figure 17. Similarly to buried PCB routing, designers have to be very cautious in the shield design. Checking the cavity and the aperture resonance frequencies is recommended [5]. Experience in simulation and in real cases shows that a resonance occurring at the wrong frequency can make the EMI worse with shield than without shield. Since near-field is dominated by magnetic radiations, the shield absorption effect will set the overall shielding efficiency. 1mm copper shielding with small aperture (10x0.6mm) is used for simulations and results are shown on Figure 18 and Figure 19.

For shielding, gain on average H-field goes from 15 to 20dB, except at a shield resonance frequency (2.4GHz-2.5GHz) where gain is only about 6dB. For buried PCB routing, gain goes from 5 to 15dB, except at routing resonance (2.4GHz-2.5GHz) where radiations gain is only about 2/3dB. Correlations between theoretical formulas and simulation are good, even if discrepancies are occurring at the resonance frequencies. Due to the 3D complexity of the structure, it can hardly be predicted and a simulation tool becomes then mandatory.

4. Conclusions

The EMI/Transient flow proposed by Ansys is suitable for advanced EMI investigations. Correlations with measurements and theoretical equations are good and it enabled the development of a reliable and valuable EMI simulation flow and methodology [7].

In many cases, shielding when properly designed provides an excellent efficiency for a low cost. Filtering using ECMF [9] is also really useful and efficient on even clock harmonics, especially for implementations that suffers from high CM noise. Tuning the placement and the orientation of the RF interface versus the digital aggressor is another EMI mitigation method. For EM fields dominated by magnetic radiations, EMI falls off as in near-field and as $1/D$ in far-field. This means that if the spacing between the aggressor and victims is multiplied by 2, radiations will be decreased by 12dB in near-field and 6dB in far-field. Perpendicular orientation of the antenna versus the aggressor can also decrease the coupling. Moreover, it is advised to investigate the functional techniques which can also be very efficient despite the constraints coming from the signal integrity specifications and the lack of mechanism in standards.

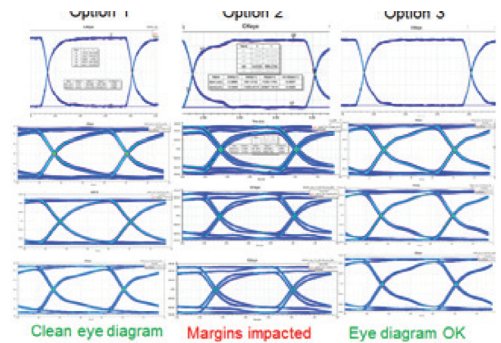


Figure 15. SI simulations of clock/D0/D1/D2.

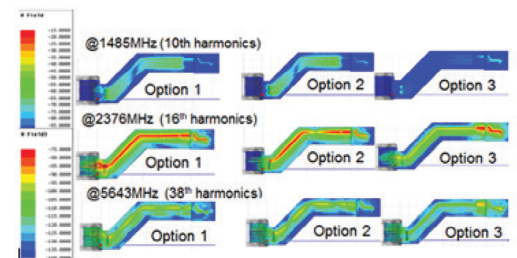


Figure 16. H near-field simulation map (dBm).

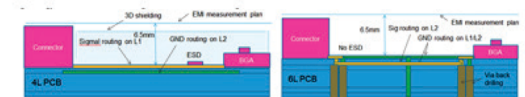


Figure 17. Cross-section of top layer PCB routing with shielding versus buried PCB routing.

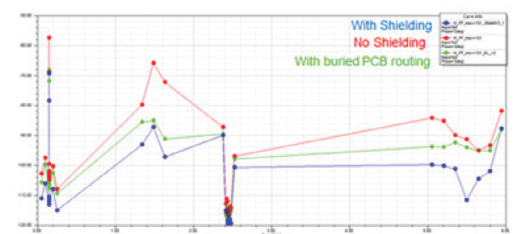


Figure 18. Average H-field in dB(mA/m) at D=6.5mm with default DUT, shielding and buried routing.

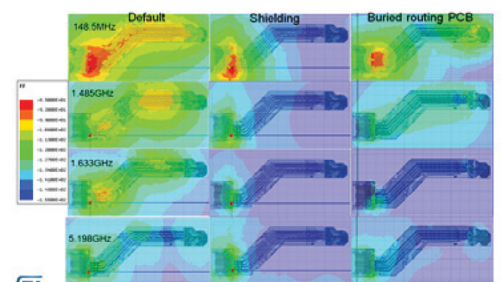


Figure 19. H-field (dBm) map at D=6.5mm.

/ Acknowledgments

We would like to thank Felipe Castro from Ansys for his valuable support. We are also thankful for the support from our colleagues in Co-design and Validation teams as well as all colleagues involved in reviews.

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