Programming guide

Introduction

This guide provides guidelines to develop a driver for VL53L9CX.

1 Application modes

The VL53L9CX is an all-in-one module that is versatile and can adapt to different platforms or different needs.

1.1 Control interface

The module has an I3C interface. As an I3C interface, it is backward compatible with I²C interfaces. The switch to I3C occurs automatically when the dynamic address assignment phase is detected.

Figure 1. I²C host

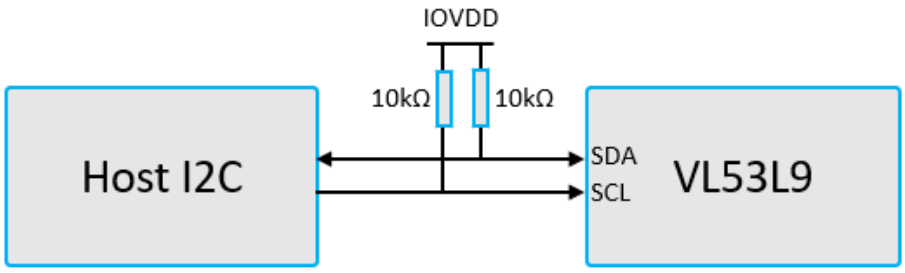
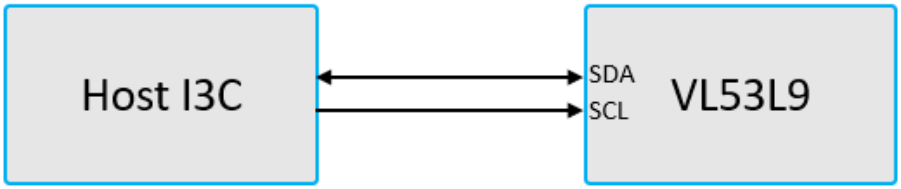


Figure 2. I3C host



The I3C interface allows a data rate of up to 10 Mbit/s, which is 10 times faster than an I²C interface.

Note: However, when the device is in standby mode, it will be necessary to change the operating clock of the device to perform I3C reads of multiple bytes (see Section 2.5.3: Device calibration for more detail).

1.2 Streaming interface

There are two ways to retrieve ranging data. The MIPI CSI-2 interface allows streaming data at a rate of up to 1 Gbps. It is also possible to bypass the MIPI interface and directly read the data in memory using the control interface (I²C/I3C). In both cases, the interface data rate must be taken into account, as it may limit performance depending on the target application.

Table 1. Performance depending on the streaming interface

Resolution	Data size (Bytes)	MIPI	I3C		I²C	
		Max FPS	Read (ms)	Max FPS	Read (ms)	Max FPS
54 x 42	14900	> 60	20	30	200	4
24 x 20	3900	> 60	5	60	50	20
18 x 14	1800	> 60	2.5	> 60	25	30
12 x 10	900	> 60	1.2	> 60	12	60

1.3 Synchronization interfaces

The VL53L9CX has two GPIOs. The first GPIO (INTR) is configured as an output and is used to notify frames (notification on falling edge event). The second GPIO (SYNC_IN) is configured as an input and allows the product to synchronize with another device (trigger on falling edge event).

The device, when controlled in I3C, can also notify the frames using the IBI (inbound interrupt) function (refer to Section 2.7.1: Frame signaling).

2 VL53L9CX firmware

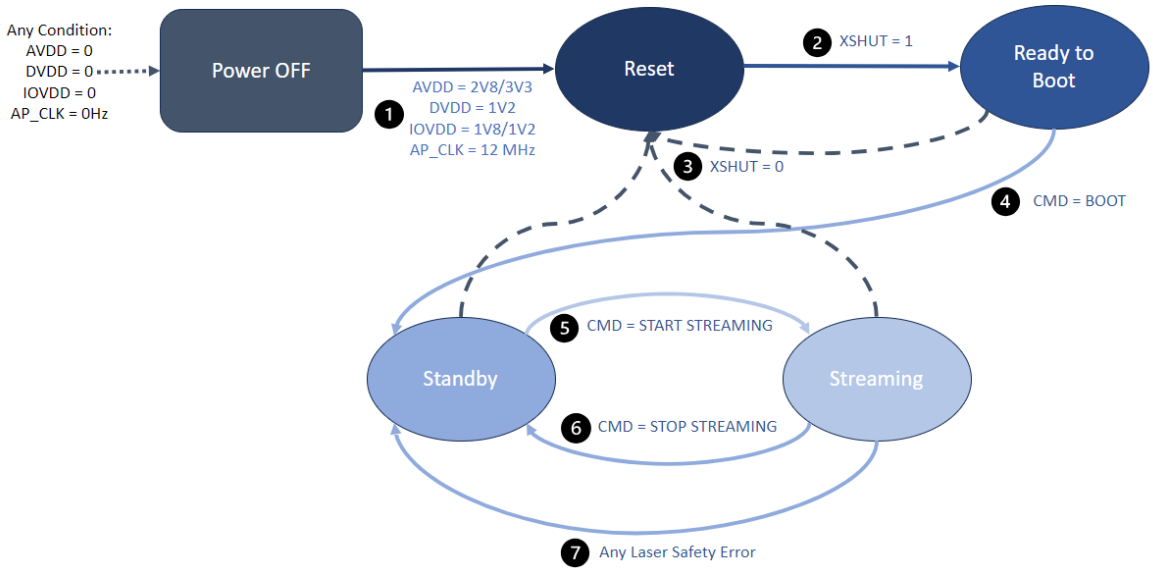
The device includes firmware that manages real-time sensor programming as well as communication with the laser driver.

A part of the firmware is embedded in the product (in ROM) and another part must be loaded at boot time (in RAM).

2.1 Firmware state machine

The diagram below shows the state machine of the device as well as the different possible transitions between these states.

Figure 3. Device state machine



2.2 T1 windowing

The memory mapping is dynamic. Windows number four, five, and six are reprogrammed depending on the firmware state. The following table describes the different configurations.

2.2.1 Registers windowing (all state)

Table 2. Registers windowing

Window	Name	R/W	I3C address	T1 interco address	Size (Bytes)
0	STATUS	RO	0x0000	UI	0x0400
1	CONTROL	RWX	0x0400	UI command	0x0004
2	SETTINGS	RW	0x042C	UI settings	0x0C00
3	OTP_MIRROR	RW	0x06E8	UI OTP mirror	0x0800
7	HW registers	RW	0xD000	0x800000	0x3000

2.2.2 Patch windowing (only in ready to boot)

Table 3. Patch windowing

Window	Name	R/W	I3C address	T1 interco address	Size (Bytes)
4	RAM patch	RW	0x1800	0x60000 (xp70 0x420000)	0x8000
5	Patch registers	RO	0xA000	0x7FE00 (xp70 0x43FE00)	0x0200
6	—	—	—	—	—

2.2.3 Frame buffer windowing (only in standby)

Table 4. Frame buffer windowing

Window	Name	R/W	I3C address	T1 interco address	Size (Bytes)
4	Frame Buffer	RO	0x1800	0x803000	0xB800
5	—	—	—	0x80B000	—
6	—	—	—	0x813000	—

2.2.4 Ranging map windowing (only in streaming)

Table 5. Ranging data windowing

Window	Name	R/W	I3C address	Size (Bytes)
4	Distance/DSS LUTs	RO	0x1800	Buffer size
5	Amplitude	RO	0x1800 + buffer size	Buffer size
6	Ambient	RO	0x1800 + buffer size	Buffer size

2.3 User interface

The firmware embedded in the device manages the low-level configuration. It also handles the real-time configuration of hardware blocks as well as communication with external components such as the laser driver. The firmware defines and provides a user interface (UI) for the driver to interface with the firmware.

The UI is divided into four blocks (STATUS, CONTROL, SETTINGS, OTP) described in the Table 2. Registers windowing.

The Section 2.3.1: User interface – Status section describes the *User interface version 2.2*.

2.3.1 User interface – Status section

The Table 6. Revision status UI describes the revision information of the device accessible through the UI. This information can be used by the driver to verify the version of the module, firmware, and UI to adapt its operation. This section is in read only as it is essentially information provided to the driver.

Table 6. Revision status UI

Register name	Address	Reset value	Bits	Field name	R/W	Description
DEVICE_MODEL_ID	0x0000	0x53334C39	31:0	VALUE	R	Device identification in ASCII (S3L9)
DEVICE_REVISION	0x0004	0xA	31:24	LOGIC_FE_REVISION	R	C40 die front end revision
		0x0	23:16	LOGIC_BE_REVISION	R	C40 die back-end revision
		0xA	15:12	FE_REVISION	R	Front end revision
		0x0	11:8	BE_REVISION	R	Back-end revision
		0x0	7:0	OPTICAL_REVISION	R	Optical revision
UI_REVISION	0x0008	0x2	15:8	MAJOR	R	Major UI revision
		0x2	7:0	MINOR	R	Minor UI revision
ROM_REVISION	0x000A	0x0	15:8	MAJOR	R	Major ROM code revision
		0x0	7:0	MINOR	R	Minor ROM code revision
PATCH_REVISION	0x000C	0x0	15:8	MAJOR	R	Major FWP revision
		0x0	7:0	MINOR	R	Minor FWP revision

The Table 7. Sensor status UI (Status line) describes the status registers of the sensor, which are also streamed in each frame in the status line (ISL).

Table 7. Sensor status UI (Status line)

Register name	Address	Reset value	Bits	Field name	R/W	Description
FRAME_COUNTER	0x0028	0x0	31:0	VALUE	R	Frame number
TEMPERATURE	0x002C	0x0	15:0	VALUE	R	Device temperature (signed from -40 to 150°C)
LDD_TEMPERATURE	0x002E	0x0	15:0	VALUE	R	Laser driver temperature
LDD_POWER_CH0_n	0x0030 + n*0x2 (where n = 0 to 6)	0x0	15:0	VALUE	R	Channel 0 laser driver power for each step
LDD_POWER_CH1_n	0x003E + n*0x2 (where n = 0 to 6)	0x0	15:0	VALUE	R	Channel 1 laser driver power for each step
REF_STEP4_5_CH1	0x004C	0x0	31:16	DISTANCE	R	Reference array step 4 or 5 channel 1 distance
			15:0	AMPLITUDE	R	Reference array step 4 or 5 channel 1 amplitude
REF_ STEP4_5_CH2	0x0050	0x0	31:16	DISTANCE	R	Reference array step 4 or 5 channel 2 distance
			15:0	AMPLITUDE	R	Reference array step 4 or 5 channel 2 amplitude
REF_STEPC_CH1	0x0054	0x0	31:16	DISTANCE	R	Reference array stepC channel 1 distance
			15:0	AMPLITUDE	R	Reference array stepC channel 1 amplitude
REF_ STEPC _CH2	0x0058	0x0	31:16	DISTANCE	R	Reference array stepC channel 2 distance
			15:0	AMPLITUDE	R	Reference array stepC channel 2 amplitude
CURRENT_FRAME_WIDTH	0x005C	0x0	15:0	VALUE	R	current frame width

Register name	Address	Reset value	Bits	Field name	R/W	Description
CURRENT_FRAME_HEIGHT	0x005E	0x0	15:0	VALUE	R	Current frame height
CURRENT_STATIC_SETTINGS	0x0060	0x0	7:6	MODE	R	Current acquisition mode
			5:4	FORMAT	R	Current format
			3:2	POWER_MODE	R	Current power mode
			1:0	SYNCHRO	R	Current synchro
AMBIENT_ATTENUATION	0x0061	0x0	3:0	VALUE	R	Ambient attenuation: copy of ALGO_SCALE.AMB_ATT CABDT register
CURRENT_DYNAMIC_SETTINGS	0x0062	0x0	15:12	STEP_NUMBER	R	Current number of steps
			11:11	CONTEXT	R	Current context
			10:6	BINNING	R	Current binning
			5:4	DSS_MODE	R	Current DSS mode
ERROR_CODE	0x0064	0x0	15:0	VALUE	R	Firmware error code (Table 17. Firmware error codes)
ERROR_STATUS	0x0066	0x0	7:0	VALUE	R	Internal FW error (Table 16. Firmware error status)
LDD_ERROR_STATUS_n	0x0067 + n*0x1 (where n = 0 to 4)	0x0	7:0	VALUE	R	Error status returned by the laser driver when receiving fault (Table 18. Laser driver error status)
CURRENT_FRAME_PERIOD	0x006C	0x0	31:0	VALUE	R	Current frame period
CROP_DSS_STATUS	0x0070	0x0	28:25	DEFAULT_DSS_LUT	R	Lut used when DSS disabled
		0x0	24:24	CROP_ENABLE	R	Enable bit of crop
		0x0	23:18	CROP_Y_OFF_STAT	R	Y offset from 0.0 output picture of crop in zone unit
		0x0	17:12	CROP_X_OFF_STAT	R	X offset from 0.0 output picture of crop in zone unit
		0x0	11:6	CROP_Y_SIZE_STAT	R	Y size of crop in zone unit
		0x0	5:0	CROP_X_SIZE_STAT	R	X size of crop in zone unit
NB_SHOT_STEP_1	0x0074	0x0	7:0	VALUE	R	Number of shots for step 1 LSB
	0x0075	0x0	7:0	VALUE	R	Number of shots for step 1 middle
	0x0076	0x0	7:0	VALUE	R	Number of shots for step 1 MSB
NB_SHOT_STEP_4_5	0x0077	0x0	7:0	VALUE	R	Number of shots for step 4/5 LSB Step4 for 6 steps mode Step5 for 7 steps mode
	0x0078	0x0	7:0	VALUE	R	Number of shots for step 4/5 middle Step4 for 6 steps mode Step5 for 7 steps mode
	0x0079	0x0	7:0	VALUE	R	Number of shots for step 4/5 MSB Step4 for 6 steps mode Step5 for 7 steps mode
NB_SHOT_STEP_6	0x007A	0x0	7:0	VALUE	R	Number of shots for step 6 LSB
	0x007B	0x0	7:0	VALUE	R	Number of shots for step 6 middle

Register name	Address	Reset value	Bits	Field name	R/W	Description
NB_SHOT_STEP_6	0x007C	0x0	7:0	VALUE	R	Number of shots for step 6 MSB
NB_SHOT_STEP_7	0x007D	0x0	7:0	VALUE	R	Number of shots for step 7 LSB
	0x007E	0x0	7:0	VALUE	R	Number of shots for step 7 middle
	0x007F	0x0	7:0	VALUE	R	Number of shots for step 7 MSB

Table 8. Firmware status UI

Register name	Address	Reset value	Bits	Field name	R/W	Description
SYSTEM_FSM	0x008C	0x0	7:0	VALUE	R	Sensor system FSM status: 0x00: (FSM_NONE) 0x01: (FSM_READY_TO_BOOT) 0x02: (FSM_STANDBY) 0x03: (FSM_STREAMING)
COMMAND_ERROR	0x008D	0x0	7:0	VALUE	R	Sensor system FSM status: 0x00: (CMD_ERROR_NONE) 0x01: (CMD_ERROR_FORBIDDEN) 0x02: (CMD_ERROR_INVALID)
FRAME_READY	0x008E	0x0	0:0	VALUE	R	Frame is ready to access through I3C
XSTART	0x008F	0x0	7:0	VALUE	R	Xstart computed by FW
YSTART	0x0090	0x0	7:0	VALUE	R	Ystart computed by FW
FINAL_WIDTH	0x0091	0x0	7:0	VALUE	R	Image width after binning
FINAL_HEIGHT	0x0092	0x0	7:0	VALUE	R	Image height after binning

2.3.2 User interface – Control section

The driver or the user can interact with the firmware using commands. The table below lists when each command can be called. This control register is used to interact with the firmware and change the state machine.

Table 9. Command register

Register name	Address	Reset value	Bits	Field name	R/W	Description
COMMAND	0x0400	0x0	7:0	VALUE	R/W	Firmware command

Table 10. Firmware commands

Code	Command	Info	Ready to boot	Standby	Streaming
1	Boot	Request firmware patch setup	✔		
2	Start streaming	Request starts streaming		✔	
3	Stop streaming	Request stop streaming			✔
4	Read temperature	Read thermal sensor value		✔	
5	Trigger next frame	Trigger next frame in manual mode			✔
6	Acknowledge frame	Acknowledge frame read back through I3C			✔

Code	Command	Info	Ready to boot	Standby	Streaming
7	Switch to Fast clock	Turn on the PLL and switch the system clock to the fast clock	✔	✔	
8	Switch to ext clock	Switching the system clock to the external clock and turn-off the PLL	✔	✔	
9	OTP custom write	Write OTP custom from OTP_CUSTOM mirror page		✔	
10	DSS LUT map	Map DSS LUT buffer instead of OUT buffer			✔
11	DSS LUT unmap	Remap OUT buffer (default)			✔
12	Fast restart	Request to restart streaming			✔

The sequence to call a firmware command is:

```
WRITE CMD
WAIT COMMAND == 0x00 (Command executed)
```

2.3.3 User interface – Settings section

The settings section of the UI allows configuring the device. It has been divided into several subsections. Each subsection corresponds to a mode of operation or a state of the state machine. All configurations needed during the "ready to boot" state are in the BOOT_SETTINGS section. The device configuration registers, which prepare the profiles, are in the STANDBY_SETTINGS section.

Table 11. Boot settings UI

Register name	Address	Reset value	Bits	Field name	R/W	Description
EXT_CLOCK	0x042C	0xB71B00	31:0	VALUE	R/W	External clock frequency in Hz (from 6 MHz to 27 MHz)
INSTALL_PATCH	0x0430	0x0	0:0	VALUE	R/W	Flag to be set to install PATCH on BOOT command.
SPI_FORMAT	0x0431	0x0	0:0	VALUE	R/W	SPI format: 0x00: (SPI_HALF_DUPLEX) 0x01: (SPI_FULL_DUPLEX)
LDD_OTP_CRC	0x0434	0x0	31:0	VALUE	R/W	CRC of laser driver OTP
VDDA_CFG	0x0438	0x0	7:0	VALUE	R/W	Voltage for VDDA: 0x0: (VDDA_2_8V) 0x1: (VDDA_3_3V)
VDDIO_CFG	0x0439	0x1	7:0	VALUE	R/W	Voltage for VDDIO: 0x0: (VDDIO_1_2V) 0x1: (VDDIO_1_8V)

There are two programmable contexts. Each of these contexts can be configured in long-range mode (six steps) or precision range mode (seven steps). The driver selects the context to apply during streaming. The composite mode alternates between the two contexts with a programmable repetition for each of the contexts.

Note: Composite mode is only possible if the two contexts share the same resolution when the DSS is active. Composite mode, in which two different resolutions are mixed with DSS (dynamic SPAD selection) enabled, is not supported by the product.

Table 12. **Standby settings UI**

	Register name	Address	Reset value	Bits	Field name	R/W	Description
Global settings	CSI2_DATA_RATE	0x0460	0x3B9ACA00	31:0	VALUE	R/W	MIPI CSI-2 data rate in bit per second (100 Mbps to 1 Gbps)
	CSI2_VIRTUAL_CHANNEL	0x0464	0x0	1:0	VALUE	R/W	ISL and data virtual channel over
	CSI2_ISL_DATA_TYPE	0x0465	0x0	6:6	FORCE_ISL_WIDTH	R/W	If 0: ISL width is equal CSI2_FRAME_WIDTH (default) If 1: ISL width is equal to SENSOR_STATUS page size
			0x12	5:0	VALUE	R/W	ISL data type over CSI-2
	CSI2_FRAME_DATA_TYPE	0x0466	0x2A	5:0	VALUE	R/W	FRAME data type over CSI-2
	DPHY_PLL_SSCG_MODE	0x0467	0x0	1:0	VALUE	R/W	DPHY PLL spread spectrum mode: 0x00: (SSCG_DISABLED) 0x01: (SSCG_DOWNSPREAD) 0x02: (SSCG_CENTERSPREAD)
	DPHY_PLL_SSCG_MOD_PERIOD	0x0468	0x0	12:0	VALUE	R/W	DPHY PLL spread spectrum modulation period
	DPHY_PLL_SSCG_INC_STEP	0x046A	0x0	15:0	VALUE	R/W	DPHY PLL spread spectrum increment step
	RANGING_FREQ	0x046C	0x7D0	15:0	VALUE	R/W	Ranging frequency in MHz (from 1000 to 2000 MHz)
	RANGING_PLL_SSCG_MODE	0x0470	0x0	1:0	VALUE	R/W	Ranging PLL spread spectrum mode: 0x01: (SSCG_SINEWAVE) 0x02: (SSCG_TRIANGLE)
	RANGING_PLL_SSCG_FREQ	0x0474	0x0	15:0	VALUE	R/W	Ranging PLL spread spectrum FREQ
	RANGING_PLL_SSCG_DEPTH	0x0476	0x0	15:0	VALUE	R/W	Ranging PLL spread spectrum DEPTH
	RANGING_PLL_SSCG_RAND	0x0478	0x0	15:0	VALUE	R/W	Ranging PLL spread spectrum RAND
	CONTEXT_SELECTION	0x047A	0x0	1:0	VALUE	R/W	Context selection: 0x00: (ALWAYS_CONTEXT1) 0x01: (ALWAYS_CONTEXT2) 0x02: (COMPOSITE)
	MODE	0x047B	0x0	1:0	VALUE	R/W	Operating mode: 0x00: (MODE_RANGING) 0x01: (MODE_HISTOGRAM) 0x01: (MODE_HOST_CONTROL) 0x03: (MODE_INTENSITY)
	SYNCHRO	0x047C	0x0	1:0	VALUE	R/W	Synchronization mode: 0x00: (SYNC_SLAVE) 0x01: (SYNC_MANUAL) 0x02: (SYNC_AUTONOMOUS)
	FORMAT	0x047D	0x0	1:0	VALUE	R/W	Frame format: 0x00: (SQUARE) 0x01: (WIDE) 0x02: (FULL)
	FRAME_PERIOD	0x0480	0x80E8	31:0	VALUE	R/W	Frame period in µs. from 10000 us to 1000000 (1 s).
	OUTPUT_IF	0x0484	0x0	0:0	VALUE	R/W	Output interface selection: 0x00: (CSI-2) 0x01: (I3C)

	Register name	Address	Reset value	Bits	Field name	R/W	Description
Global settings	CSI2_FRAME_WIDTH	0x0486	0x6C	15:0	VALUE	R/W	CSI-2 frame width (54*2 by default))
	CSI2_FRAME_HEIGHT	0x0488	0x7E	15:0	VALUE	R/W	CSI-2 frame height (42*3 by default)
	FRAME_SIGNALING_MODE	0x048A	0x0	0:0	VALUE	R/W	Frame signaling mode. 0x00: (I3C_IBI) In band interrupt in I3C, no signaling in CSI-2 0x01: (INTR_PAD) INTR PAD signaling (both in I3C and CSI-2)
	INTR_OUTPUT_MODE	0x048B	0x0	0:0	VALUE	R/W	INTR PAD mode: 0x0: (CMOS) 0x1: (OPEN_DRAIN)
	POWER_MODE	0x048C	0x0	1:0	VALUE	R/W	Power mode selection: 0x00: (REGULAR) 0x01: (LOW_POWER) 0x02: (ULTRA_LOW_POWER)
	OTP_ADDRESS	0x0492	0x0	10:0	VALUE	R/W	Address to read/write in the OTP or start address form multiple read/write
	OTP_SIZE	0x0494	0x0	10:0	VALUE	R/W	Number of 32-byte words to read/ write from/to OTP in multiple access.
	CAL_REF_OFFSET	0x0496	0x0	7:0	VALUE	R/W	Reference array ranging window offset vs T0 for the calibration phase in bins
	CAL_RTN_OFFSET	0x0497	0x20	7:0	VALUE	R/W	Return array ranging window offset vs T0 offset for the calibration phase in bins
	CAL_PROG_OFFSET_1_TO_5	0x0498	0x0	15:0	VALUE	R/W	offset applied to laser pulse position vs ranging windows for steps 1 to 5 (signed value) in bins/4
	CAL_PROG_OFFSET_6	0x049A	0x4	15:0	VALUE	R/W	offset applied to laser pulse position vs ranging windows for steps 6 (signed value) in bins/4
	CAL_TARGET_LD	0x049C	0x0	15:0	VALUE	R/W	Target for the laser pulse within reference windows in bins. Used to set t_start_ldd if CALIBRATION_DISABLE == 1
	HISTO_BIN_START	0x049E	0x0	7:0	VALUE	R/W	1st bin to start histogram (in bin)
	HISTO_BIN_STOP	0x049F	0x1F	7:0	VALUE	R/W	Last bin used in histogram (in bin)
	HISTO_BIN_WIDTH	0x04A0	0x0	2:0	VALUE	R/W	The bin width for histogram. bin_width = 2^VALUE. From 0->1 ns to 4->16 ns
	CROP_PARAMS	0x04A4	0x0	24:24	CROP_ENABLE	R/W	Enable bit to crop
			0x0	23:18	CROP_Y_OFFSET	R/W	Y offset from 0.0 output picture to crop in zone unit
			0x0	17:12	CROP_X_OFFSET	R/W	X offset from 0.0 output picture to crop in zone unit
			0x0	11:6	CROP_Y_SIZE	R/W	Y size to crop in zone unit
			0x0	5:0	CROP_X_SIZE	R/W	X size to crop in zone unit
Context 1 settings	BINNING	0x04C4	0x2	4:0	VALUE	R/W	Binning factor
	DSS_MODE	0x04C5	0x2	7:0	VALUE	R/W	DSS mode: 0x00: (DSS_DISABLE) 0x01: (DSS_LONG) 0x02: (DSS_SHORT)
	REPEAT	0x04C6	0x0	7:0	VALUE	R/W	Only in COMPOSITE mode, number of context 1 repetitions

	Register name	Address	Reset value	Bits	Field name	R/W	Description
Context 2 settings	BINNING	0x04C8	0x2	4:0	VALUE	R/W	Binning factor
	DSS_MODE	0x04C9	0x1	7:0	VALUE	R/W	DSS mode: 0x00: (DSS_DISABLE) 0x01: (DSS_LONG) 0x02: (DSS_SHORT)
	REPEAT	0x04CA	0x0	7:0	VALUE	R/W	Only in COMPOSITE mode, number of context 2 repetitions

The Table 13. Streaming settings UI describes the configuration registers accessible during streaming. Indeed, certain configurations such as exposure time can be adjusted during streaming.

Table 13. Streaming settings UI

	Register name	Address	Reset value	Bits	Field name	R/W	Description
Context 1 settings	STEP_NUMBER	0x04CC	0x7	3:0	VALUE	R/W	Number of measure steps (6 or 7)
	VCSEL_CONFIG_CH0_STEP_n	0x04CD + n*0x1 (where n = 0 to 7)	0x20	5:0	VALUE	R/W	Step laser driver configuration selection for channel 0
	VCSEL_CONFIG_CH1_STEP_n	0x04D5 + n*0x1 (where n = 0 to 7)	0x20	5:0	VALUE	R/W	Step laser driver configuration selection for channel 1
	BLANKING_STEP_n	0x04DE + n*0x2 (where n = 0 to 7)	0x0	9:0	VALUE	R/W	Step blanking (ranging clock cycles)
	MAX_DITHERING_STEP_n	0x04EE + n*0x1 (where n = 0 to 7)	0x0	4:0	VALUE	R/W	Step max dithering (ranging clock cycles)
	PULSE_WIDTH_SHORT	0x04F6	0x15	7:0	VALUE	R/W	Laser pulse width for short window (used by DSS). The unit is 1/16ns (21 for 1.3 ns)
	PULSE_WIDTH_LONG	0x04F7	0x15	7:0	VALUE	R/W	Laser pulse width for long window (used by DSS). The unit is 1/16ns (42 for 2.6 ns)
	DISTANCE_REF_LONG_OFFSET	0x04F8	0x60	6:0	VALUE	R/W	Distance offset for REF long-distance computation signed from -64 to 63. No impact on pulse position.
	DISTANCE_RTN_LONG_OFFSET	0x04F9	0x0	6:0	VALUE	R/W	Distance offset for RTN long-distance computation is signed from -64 to 63. No impact on pulse position.
	DISTANCE_RTN_SHORT_OFFSET	0x04FA	0x0	6:0	VALUE	R/W	Distance offset for RTN short distance computation signed from -64 to 63. No impact on pulse position.
	DISTANCE_SWITCHOVER	0x04FC	0xC8	15:0	VALUE	R/W	Distance threshold for short/ long distance final choice
	NB_SHOT_STEP_n	0x0500 + n*0x4 (where n = 0 to 7)	0x0	23:0	VALUE	R/W	Step number of shot
	GROUP_HOLD	0x0520	0x0	1:0	VALUE	R/W	0x00: (HOLD_OFF) Page update complete 0x01: (HOLD_ON) Page update ongoing
Context 2 settings	STEP_NUMBER	0x054C	0x6	3:0	VALUE	R/W	Number of measure steps (6 or 7)

	Register name	Address	Reset value	Bits	Field name	R/W	Description
Context 2 settings	VCSEL_CONFIG_CH0_STEP_n	0x054D + n*0x1 (where n = 0 to 7)	0x20	5:0	VALUE	R/W	Step laser driver configuration selection for channel 0
	VCSEL_CONFIG_CH1_STEP_n	0x0555 + n*0x1 (where n = 0 to 7)	0x20	5:0	VALUE	R/W	Step laser driver configuration selection for channel 1
	BLANKING_STEP_n	0x055E + n*0x2 (where n = 0 to 7)	0x0	9:0	VALUE	R/W	Step blanking (ranging clock cycles)
	MAX_DITHERING_STEP_n	0x056E + n*0x1 (where n = 0 to 7)	0x0	4:0	VALUE	R/W	Step max dithering (ranging clock cycles)
	PULSE_WIDTH_SHORT	0x0576	0x2A	7:0	VALUE	R/W	Laser pulse width for short window (used by DSS). The unit is 1/16ns (21 for 1.3 ns)
	PULSE_WIDTH_LONG	0x0577	0x2A	7:0	VALUE	R/W	Laser pulse width for long window (used by DSS). The unit is 1/16ns (42 for 2.6 ns)
	DISTANCE_REF_LONG_OFFSET	0x0578	0x60	6:0	VALUE	R/W	Distance offset for REF long-distance computation signed from -64 to 63. No impact on pulse position.
	DISTANCE_RTN_LONG_OFFSET	0x0579	0x0	6:0	VALUE	R/W	Distance offset for RTN long-distance computation is signed from -64 to 63. No impact on pulse position.
	DISTANCE_RTN_SHORT_OFFSET	0x057A	0x2	6:0	VALUE	R/W	Distance offset for RTN short distance computation signed from -64 to 63. No impact on pulse position.
	DISTANCE_SWITCHOVER	0x057C	0x1F4	15:0	VALUE	R/W	Distance threshold for short/ long distance final choice
	NB_SHOT_STEP_n	0x0580 + n*0x4 (where n = 0 to 7)	0x0	23:0	VALUE	R/W	Step number of shot
	GROUP_HOLD	0x05A0	0x0	1:0	VALUE	R/W	0x00: (HOLD_OFF) Page update complete 0x01: (HOLD_ON) Page update ongoing

Table 14. Debug settings UI

Register name	Address	Reset value	Bits	Field name	R/W	Description
LDD_FW_BYPASS	0x05D4	0x0	1:0	VALUE	R/W	Disable accesses to laser driver during streaming
INTENSITY_SPAD_SELECT	0x05D5	0x4	7:0	VALUE	R/W	SPAD selection in intensity mode: 0x00: (SPAD_0) spad id 0 enabled only 0x01: (SPAD_1) spad id 1 enabled only 0x02: (SPAD_2) spad id 2 enabled only 0x03: (SPAD_3) spad id 3 enabled only 0x04: (AUTO) Automatic cycling from SPAD_0 to SPAD_3
DSS_DEFAULT_INIT_LUT	0x05D6	0x0	7:0	VALUE	R/W	DEFAULT LUT index nb for DSS start
SHORT_DSS_OR_TREE_LIMIT	0x05D8	0x290	31:0	VALUE	R/W	or_tree_pk_rate_limit: typically, 80e6. In FP 656<= 80e6/121900

Register name	Address	Reset value	Bits	Field name	R/W	Description
SHORT_DSS_RATE_SWITCH_LO	0x05DC	0x668	31:0	VALUE	R/W	rate_switch low: typically, 200e6. In FP 1640<=200e6/121900
SHORT_DSS_RATE_SWITCH_HI	0x05E0	0x668	31:0	VALUE	R/W	rate_switch high: typically, 200e6. In FP 1640<=200e6/121900
SHORT_DSS_AMB_WEIGHT	0x05E4	0x10	7:0	VALUE	R/W	ambient_weight: typically, 1. In FP 16<=1*16
SHORT_DSS_RATE_GAIN	0x05E5	0x8	7:0	VALUE	R/W	signal_rate_gain: typically, 1.3. (In fixed point 21<= 1.3*16)
SHORT_DSS_COEF_n	0x05E6+ n*0x2 (where n = 0 to 9)	0x0	15:0	VALUE	R/W	LUT index
SHORT_DSS_INDEX_NB	0x05FA	0x8	7:0	VALUE	R/W	Nb of LUT indexes (8, 9 or 10)
SHORT_DSS_LUT_n	0x05FB+ n*0x1 (where n = 0 to 39)	0x0	7:0	VALUE	R/W	LUT pattern (2*2 pixel => 16 spads). Boolean bits: 3 2 1 0. The 4 MSB are not used
SHORT_DSS_EFF_SPAD_n	0x0624+ n*0x2 (where n = 0 to 9)	0x0	15:0	VALUE	R/W	Effective SPAD value per LUT used for internal DSS computation
LONG_DSS_OR_TREE_LIMIT	0x0658	0x290	31:0	VALUE	R/W	or_tree_pk_rate_limit: typically 80e6. In FP 656<= 80e6/121900
LONG_DSS_RATE_SWITCH_LO	0x065C	0x668	31:0	VALUE	R/W	rate_switch low: typically, 200e6. In FP 1640<=200e6/121900
LONG_DSS_RATE_SWITCH_HI	0x0660	0x668	31:0	VALUE	R/W	rate_switch high: typically, 200e6. In FP 1640<=200e6/121900
LONG_DSS_AMB_WEIGHT	0x0664	0x10	7:0	VALUE	R/W	ambient_weight: typically, 1. In FP 16<=1*16
LONG_DSS_RATE_GAIN	0x0665	0x8	7:0	VALUE	R/W	signal_rate_gain: typically, 1.3. (In fixed point 21<= 1.3*16)
LONG_DSS_COEF_n	0x0666+ n*0x2 (where n = 0 to 9)	0x0	15:0	VALUE	R/W	LUT index
LONG_DSS_INDEX_NB	0x067A	0x8	7:0	VALUE	R/W	Nb of LUT indexes (8, 9 or 10)
LONG_DSS_LUT_n	0x067B+ n*0x1 (where n = 0 to 39)	0x0	7:0	VALUE	R/W	LUT pattern (2*2 pixel => 16 spads). Boolean bits: 3 2 1 0. The 4 MSB are not used
LONG_DSS_EFF_SPAD_n	0x06A4+ n*0x2 (where n = 0 to 9)	0x0	15:0	VALUE	R/W	Effective SPAD value per LUT used for internal DSS computation
CALIBRATION_DISABLE	0x06D5	0x0	1:0	VALUE	R/W	Disable calibration phase at start of stream
LINEAR_COMPENS_CH1	0x06D6	0x2	7:0	VALUE	R/W	Linear compensation LDD offset added to step5 and 6 channel 1. (Signed value in quarter of bin)
LINEAR_COMPENS_CH2	0x06D7	0x2	7:0	VALUE	R/W	Linear compensation LDD offset added to step5 and 6 channel 2. (Signed value in quarter of bin)

2.3.4 User interface – OTP section

The firmware makes a copy of the content of the device's OTP, then provides the driver with certain information that could be useful when decoding the data.

Table 15. OTP mirror UI

Register name	Address	Reset value	Bits	Field name	R/W	Description
NVM_MODULE_ID	0x06E8	0x0	31:0	VALUE	R/W	Identifiers
GLOBAL_DISTANCE_OFFSET	0x06EC	0x0	15:0	VALUE	R/W	Global distance offset on 16LSB
DISTANCE_OFFSET_0_n	0x06F0+ n*0x1 (where n = 0 to 944)	0x0	7:0	VALUE	R/W	Per pixel distance relative offsets map. (6 bits signed)
DSS_LUT_n	0x0AB0+ n*0x1 (where n = 0 to 39)	0x0	7:0	VALUE	R/W	DSS LUT with a maximum of 10 indexes (8 by default) 1 byte per MPIX of the 2x2 aperture pattern
DEFECT_SPAD_n	0x0AE0+ n*0x2 (where n = 0 to 19)	0x0	15:9	DEFECT_X	R/W	32 bits per index (1 byte per MPIX of the 2x2 aperture pattern) X coordinate
		0x0	8:2	DEFECT_Y	R/W	Y coordinate
		0x0	1:0	DEFECT_SPAD_NB	R/W	Spad number
OPTICAL_OFFSET_X	0x0B08	0x0	1:0	VALUE	R/W	X offset of the optical center
OPTICAL_OFFSET_Y	0x0B09	0x0	1:0	VALUE	R/W	Y offset of the optical center
RESIDUAL_OFFSET_X	0x0B0A	0x0	7:0	VALUE	R/W	X residual offset between what is programmed and real optical center (S2.1 in SPAD unit-> step of 0.5)
RESIDUAL_OFFSET_Y	0x0B0B	0x0	7:0	VALUE	R/W	Y residual offset between what is programmed and real optical center (S2.1 in SPAD unit-> step of 0.5)
CAL_TEMP_DEGC	0x0B0C	0x0	6:0	VALUE	R/W	Measured temperature during calibration for traceability (in °C)
TEMP_SENSOR_VALUE	0x0B0D	0x0	4:0	VALUE	R/W	Thermal sensor correction value (to copy in DCORRECT)
AUTO_VHV_TRIM_VOLTAGE	0x0B10	0x0	9:0	VALUE	R/W	AUTO VHV found voltage at 60°C at EWS (in U5.5 V)
AUTO_VHV_TRIM_TEMP	0x0B12	0x0	7:0	VALUE	R/W	Temperature sensor reading (in °C) during AUTO VHV at EWS
BG_TRIM_IBIAS	0x0B14	0x0	5:0	VALUE	R/W	BG IBias trimming (in S5.0)
BG_TRIM_VREF	0x0B15	0x0	5:0	VALUE	R/W	BG VRef trimming (in S5.0)
TEMP_TO_DAC_GAIN	0x0B16	0x0	15:0	VALUE	R/W	Temperature to DAC setting gain (Q8.8)
AUTO_VHV_IDAC_SEL_FMT	0x0B18	0x0	7:0	VALUE	R/W	AUTO VHV found HV BOOST DAC setting at FMT
AUTO_VHV_TEMP_FMT	0x0B19	0x0	7:0	VALUE	R/W	Temperature sensor reading (in °C) during AUTO VHV at FMT
TEMP_TO_DAC_OFFSET	0x0B1B	0x0	7:0	VALUE	R/W	Temperature to DAC setting offset (S8)

Register name	Address	Reset value	Bits	Field name	R/W	Description
REF_ARRAY_CHECK	0x0B1C	0x0	31:0	VALUE	R/W	“Reference arrays check” lower thresholds for checking reference array counts do not go below this threshold (in number of events)
REF_ARRAY_SPAD_EN	0x0B20	0x0	23:0	VALUE	R/W	Reference array SPAD enables (1 bit per SPAD)
RAD2PERP_FOV_GAIN	0x0B24	0x0	7:0	VALUE	R/W	Rad2Perp Field-of-View gain (U1.7)
DISTANCE_OFFSET_30_n	0x0B28+ n*0x1 (where n = 0 to 314)	0x0	7:0	VALUE	R/W	Per pixel distance relative offsets map. (6 bits signed)
CAL_AMP_COEFF_n	0x0C80+ n*0x1 (where n = 0 to 34)	0x0	7:0	VALUE	R/W	7x5 amplitude coefficient grid captured at FMT DMAX from 0x0 (bottom left), 0x1, 0x2… to …4x4, 4x5, 4x6 8 bits unsigned
CAL_AMP_SCALER	0x0CA3	0x0	7:0	VALUE	R/W	Scaler to encode full amplitude 8 bits unsigned
CAL_AMP_DISTANCE	0x0CA4	0x0	15:0	VALUE	R/W	Distance in mm at which amplitude calibration was captured 16 bits unsigned
CAL_AMP_EXPO	0x0CA6	0x0	15:0	VALUE	R/W	Exposure number in final step in FMT use case
CAL_AMP_REFLECTANCE	0x0CA8	0x0	7:0	VALUE	R/W	Reflectance in % in which amplitude calibration was captured 8 bits unsigned
I2C_SLAVE_ID	0x0CE8	0x0	6:0	VALUE	R/W	I²C follower address
I3C_INSTANCE_ID	0x0CEC	0x0	3:0	VALUE	R/W	I3C PID
DISTANCE_OFFSET_40_n	0x0D18+ n*0x1 (where n = 0 to 440)	0x0	7:0	VALUE	R/W	Per pixel distance relative offsets map. (6 bits signed)

2.4 Device errors management

The firmware handles errors reported by the hardware or external components. Faults related to laser emission are directly checked by the VCSEL driver. In case of an error or fault, the laser driver immediately stops the laser emission and reports an error to the firmware. The firmware then stops the streaming and reports the type of error encountered in the UI. The laser driver switches to safe mode. It is the driver's responsibility to reboot the device and to restart the streaming when a laser safety error occurs.

2.4.1 Firmware errors

The firmware may report an error either while a driver command is being executed or during streaming. In such cases, the firmware sets the sticky bits in the error status register, allowing multiple errors to be reported. If bit 7 of `ERROR_STATUS` is set, the error code provides additional information about the most recent error encountered by the firmware.

Table 16. Firmware error status

Register name	Address	Bit	Details
ERROR_STATUS	0x0066	0	VHV overvoltage
		1	VHV undervoltage
		2	SPAD supply overload
		3	Current limit
		4	Start of frame outside blanking
		5	PLL lock
		6	Ref array check status
		7	Internal firmware error

The Table 17. Firmware error codes describes the firmware error codes (register 0x0064). If the firmware raises more than one error this is the last error that is reported.

Table 17. Firmware error codes

Code	Name	Details
0x0000	TOP_ERROR_NO_ERROR	No error
0x0001	TOP_ERROR_UI	User interface
0x0002	TOP_ERROR_STREAMING	Streaming
0x0003	TOP_ERROR_DSS_TIMEOUT	DSS timeout
0x0004	TOP_ERROR_SYSTEM_FAULT	System fault
0x0005	TOP_ERROR_ADDR_MONITOR	Address monitor
0x0006	TOP_ERROR_OIF	Output interface
0x0007	TOP_ERROR_UI_DSS	DSS user interface
0x0008	TOP_ERROR_LDD_TIMEOUT	LDD timeout
0x0009	TOP_ERROR_LDD_NULL_PTR	LDD null pointer
0x000A	TOP_ERROR_LDD_SPI	LDD SPI
0x000B	TOP_ERROR_LDD_OTP_CRC	LDD OTP CRC
0x000C	TOP_ERROR_LDD_NULL_SIZE	LDD null size
0x000D	TOP_ERROR_LDD_SAFETY	LDD safety
0x0200	WINDOWING_ERROR_VERSION	Windowing version
0x0201	WINDOWING_ERROR_ROLLOVER	Windowing rollover
0x0202	WINDOWING_ERROR_OVERLAP	Windowing overlap
0x0203	WINDOWING_ERROR_LOCK	Windowing lock
0x0400	THERMALSENSOR_TIMEOUT_ERROR	Thermal sensor timeout
0x0401	THERMALSENSOR_DATAREADY_ERROR	Thermal sensor data ready
0x0500	SPI2S3_ERROR_TIMEOUT	SPI2S3 timeout
0x0501	SPI2S3_ERROR_SPI_CLOCK	SPI2S3 SPI clock
0x0502	SPI2S3_ERROR_NO_SLAVE	SPI2S3 no follower
0x0503	SPI2S3_ERROR_FLASH_NOT_PRESENT	SPI2S3 flash not present
0x0504	SPI2S3_ERROR_FLASH_READ_ID	SPI2S3 flashes read ID
0x0505	SPI2S3_ERROR_FLASH_READ_STATUS	SPI2S3 flashes read status
0x0506	SPI2S3_ERROR_FLASH_ERASE	SPI2S3 flash erase

Code	Name	Details
0x0507	SPI2S3_ERROR_FLASH_READ	SPI2S3 flashes read
0x0508	SPI2S3_ERROR_FLASH_WRITE	SPI2S3 flash write
0x0509	SPI2S3_ERROR_FLASH_VERIFY	SPI2S3 flash verify
0x050A	SPI2S3_ERROR_FLASH_WRITE_ENABLE	SPI2S3 flash write enable
0x050B	SPI2S3_ERROR_FLASH_WRITE_DISABLE	SPI2S3 flash write disable
0x050C	SPI2S3_ERROR_INTERRUPT_MODFIE_NOT_SET	SPI2S3 interrupt MODFIE not sets
0x050D	SPI2S3_ERROR_INTERRUPT_TIFREIE_NOT_SET	SPI2S3 interrupt TIFREIE not sets
0x050E	SPI2S3_ERROR_INTERRUPT_CRCIE_NOT_SET	SPI2S3 interrupt CRCIE not sets
0x050F	SPI2S3_ERROR_INTERRUPT_OVRIE_NOT_	SPI2S3 interrupt OVRIE not sets
0x0510	SPI2S3_ERROR_INTERRUPT_UDRIE_NOT_SET	SPI2S3 interrupt UDRIE not sets
0x0511	SPI2S3_ERROR_INTERRUPT_TXTFIE_NOT_SET	SPI2S3 interrupt TXTFIE not sets
0x0512	SPI2S3_ERROR_INTERRUPT_EOTIE_NOT_SET	SPI2S3 interrupt EOTIE not sets
0x0513	SPI2S3_ERROR_INTERRUPT_DXPIE_NOT_SET	SPI2S3 interrupt TXPIE not sets
0x0514	SPI2S3_ERROR_INTERRUPT_TXPIE_NOT_SET	SPI2S3 interrupt SUSPC not sets
0x0515	SPI2S3_ERROR_INTERRUPT_RXPIE_NOT_SET	SPI2S3 interrupt RXPIE not sets
0x0516	SPI2S3_ERROR_INTERRUPT_SUSPC_NOT_CLEAR	SPI2S3 interrupt SUSPCs not clear
0x0517	SPI2S3_ERROR_INTERRUPT_MODFC_NOT_CLEAR	SPI2S3 interrupt MODFC not clear
0x0518	SPI2S3_ERROR_INTERRUPT_TIFREC_NOT_CLEAR	SPI2S3 interrupt TIFREC not clear
0x0519	SPI2S3_ERROR_INTERRUPT_CRCEC_NOT_CLEAR	SPI2S3 interrupt CRCEC not clear
0x051A	SPI2S3_ERROR_INTERRUPT_OVRC_NOT_CLEAR	SPI2S3 interrupt OVRC not clear
0x051B	SPI2S3_ERROR_INTERRUPT_UDRC_NOT_CLEAR	SPI2S3 interrupt UDRC not clear
0x051C	SPI2S3_ERROR_INTERRUPT_TXTFC_NOT_CLEAR	SPI2S3 interrupt TXTFC not clear
0x051D	SPI2S3_ERROR_INTERRUPT_EOTC_NOT_CLEAR	SPI2S3 interrupt EOTC not clear
0x0600	CLKCHANGER_ERROR_VERSION	Clock changer version
0x0800	ISLGEN2_ERROR_VERSION	ISL generator version
0x0801	ISLGEN2_ERROR_INVALID_CFG	ISL generator invalid configuration
0x0802	ISLGEN2_ERROR_MISSED_TRIGGER	ISL generator missed trigger
0x0803	ISLGEN2_ERROR_TOO_MANY_ENTRIES	ISL generator too many entries
0x0804	ISLGEN2_ERROR_MEMORY_LOCKED	ISL generator memory locked
0x0900	CSI2TX_ERROR_VERSION	CCSI2TX version
0x0901	CSI2TX_ERROR_PKT_TOO_LONG	CSI2TX packet too long
0x0902	CSI2TX_ERROR_PKT_TOO_SHORT	CSI2TX packet too short
0x0903	CSI2TX_ERROR_UNDERFLOW	CSI2TX underflow
0x0904	CSI2TX_ERROR_LANE_DESYNC	CSI2TX Lane desync
0x0A00	NVM_ERROR_READ_CORRECTED_ECC	NVM read corrected ECC
0x0A01	NVM_ERROR_CLK_FREQ	NVM clock frequency
0x0A02	NVM_ERROR_NULL_PTR	NVM null pointer
0x0A03	NVM_ERROR_ADDRESS_TOO_FAR	NVM address too far
0x0A04	NVM_ERROR_SIZE_TOO_BIG	NVM size too large
0x0A05	NVM_ERROR_READ_TIMEOUT	NVM read timeout
0x0A06	NVM_ERROR_READ_ECC_FAIL	NVM read ECC fail

Code	Name	Details
0x0A07	NVM_ERROR_WRITE_TIMEOUT	NVM writes timeout
0x0A08	NVM_ERROR_WRITE_FAIL	NVM Writes fail
0x0A09	NVM_ERROR_PROG_ON_NON_VIRGIN_WORD	NVM not virgin word programming
0x0B00	FRAMEMERGER_ERROR_VERSION	Frame merger version
0x0C00	I3CSLAVELITE_ERROR_VERSION	I3C version
0x0E00	STATSDATAFETCHER_ERROR_FETCHING	Data fetcher fetching
0x0E01	STATSDATAFETCHER_ERROR_RDCMD_NB	Data fetcher read command
0x0F00	CABDT_ERROR_LDD_FAULT	CABDT LDD fault (*check laser driver error*)
0x0F01	CABDT_ERROR_FRAME_REQ	CABDT frame sequencer
0x0F02	CABDT_ERROR_FSM_STEP	CABDT FSM step
0x0F03	CABDT_ERROR_NULL_PTR	CABDT null pointer
0x0F04	CABDT_ERROR_CONFIG	CABDT config
0x0F05	CABDT_ERROR_VHV_TIMEOUT	CABDT VHV timeout
0x0F06	CABDT_ERROR_DSS_TIMEOUT	CABDT DSS timeout
0x1000	CRM_ERROR_TOFPLL_LOCK_TIMEOUT	CRM TOFPLL lock timeout
0x1001	CRM_ERROR_PHYPLL_LOCK_TIMEOUT	CRM PHYPLL lock timeout
0x1002	CRM_ERROR_INVALID_CONFIG	CRM invalid config
0x1003	CRM_ERROR_INVALID_RATIO	CRM invalid ratio
0x1004	CRM_ERROR_PHYPLL_EXT_CLK	CRM PHYPLL ext clock
0x1005	CRM_ERROR_PHYPLL_VCO_RANGE	CRM PHYPLL vco range
0x1006	CRM_ERROR_PHYPLL_MULT_RANGE	CRM PHYPLL mult range
0x1007	CRM_ERROR_LDO_TIMEOUT	CRM LDO timeout
0x1008	CRM_ERROR_BG_TIMEOUT	CRM BG timeout
0x1009	CRM_ERROR_INVALID_EXT_CLOCK_FREQ	CRM invalid external clock frequency
0x1300	PATCH_ERROR_PATCH_CODE_TOO_LARGE	Patch code too large
0x1301	PATCH_ERROR_TOO_MANY_PATCHES	Patch too many patches
0x1302	PATCH_ERROR_TOO_MANY_HOOKS	Patch too many hooks
0x1303	PATCH_ERROR_BAD_CRC	Patch bad CRC
0x1304	PATCH_ERROR_BAD_PATCH_ADDR	Patch bad patch address
0x1305	PATCH_ERROR_BAD_MD5SUM	Patch bad MD5SUM
0xFF00	LASERDRIVER_ERROR_TIMEOUT	Laser driver timeout
0xFF01	LASERDRIVER_ERROR_NULL_PTR	Laser driver null pointer
0xFF02	LASERDRIVER_ERROR_SPI	Laser driver SPI
0xFF03	LASERDRIVER_ERROR_OTP_CRC	Laser driver OTP CRC
0xFF04	LASERDRIVER_ERROR_NULL_SIZE	Laser driver null size
0xFF05	LASERDRIVER_ERROR_LDD_SAFETY	Laser driver LDD SAFETY

2.4.2 Laser driver errors

The laser driver manages safety errors. All threshold and configurations are stored in the laser driver OTP. If an error occurs, the laser driver stops the laser emission and reports an error on an internal I/O to the firmware. The firmware reads the ldd error status information (sticky bits) and reports this information in the user interface and in the status line. The streaming stops automatically.

Table 18. **Laser driver error status**

Register name	Bit	Name	Details
LDD_ERROR_STATUS_1	0	flag_skin_safety_error	PD value above upper limit
	1	flag_dif_removal_error	PD value above below limit
	2	flag_power_high_error	Power too high
	3	flag_temp_high_error	Temperature too high
	4	flag_temp_low_error	Temperature too low
	5	flag_ton_error	APC gate too long
	6	flag_toff_error	APC gate too short
LDD_ERROR_STATUS_2	0	flag_max_pulse_num_error	Too many pulses
	1	flag_freq_cross_check_error	Frequency error
	2	flag_bandgap_ok_error	Bandgap issue
	3	flag_ldvcc_too_high_error	LDVCC too high
	4	flag_ldvcc_too_low_error	LDVCC too low
	5	flag_ldvcc_short_to_gnd_error	LDVCC shorted to GND
	6	flag_ldout_short_to_ldvcc_ch0_error	LDOUT shorted to LDVCC channel 0
	7	flag_ldout_short_to_ldgnd_ch0_error	LDOUT shorted to LDGND channel 0
LDD_ERROR_STATUS_3	0	flag_oc_det_error	Overcurrent error
	1	flag_oc_det_self_test_error	Overcurrent self-test error
	2	flag_trace_short_to_vdda_error	Trace shorted to VDDA
	3	flag_trace_short_to_vddio_error	Trace shorted to VDDIO
	4	flag_trace_short_to_gnd_error	Trace shorted to GND
	5	flag_trace_open_error	Trace open
	6	flag_trace_self_test_error	Trace self-test error
	7	flag_als_det_error	ALS detection
LDD_ERROR_STATUS_4	0	flag_vddio_under_error	VDDIO under voltage
	1	flag_vdda_under_error	VDDA under voltage
	2	flag_vddio_over_error	VDDIO over voltage
	3	flag_vdda_over_error	VDDA over voltage
	4	flag_watchdog_ch0_error	Watchdog Channel 0
	5	flag_crc_check_error	CRC check
	6	flag_oc_clamp_error	Overcurrent clamp
	7	flag_lvds_hiz_error	LVDS short/open
LDD_ERROR_STATUS_5	0	flag_ldout_short_to_ldvcc_ch1_error	LDOUT shorted to LDVCC channel 1
	1	flag_ldout_short_to_ldgnd_ch1_error	LDOUT shorted to LDGND channel 1
	2	flag_watchdog_ch1_error	Watchdog Channel 1

2.4.3 Other errors

Communication errors are managed at platform level.

2.5 Sensor power up and configuration guidelines

2.5.1 Device power-on

There are three necessary conditions for the device to exit its POWER_OFF state:

1. The three power supplies (AVDD, DVDD, IOVDD) must be activated.
2. The reset pin (XSHUT) must be in the high state (IOVDD level).
3. The external clock must be active.

Once the three conditions are met, which can be done in any order, the sensor switches to the "READY_TO_BOOT" state. If at any point, one of the three conditions becomes invalid, the sensor returns to the off state (or RESET for the XSHUT pin). See Figure 3. Device state machine.

After the boot phase, the device enters STANDBY state.

2.5.2 Device boot

When the system enters the READ_TO_BOOT state, the firmware reads the OTP content and automatically applies any user-programmed configuration:

- I²C address
- I3C instance identifier

Behavior

- If an I²C address is programmed, the new I²C address becomes effective.
- If an I3C instance identifier is programmed, it is used during the dynamic address assignment phase.

Firmware start-up check

The driver performs the following actions to confirm that the firmware has started correctly:

- Read the DEVICE_ID word at register address 0x0000
- Verify that the expected value is 0x53334C39 (corresponding to "S3L9" in ASCII)

When the system enters the READY_TO_BOOT state, the driver must perform the following configuration steps:

1. Set the external clock frequency, this allows the firmware to configure all internal clocks required for correct sensor operation.
2. Update the power-supply configuration, if needed
   If AVDD and IOVDD are different from the default values:
   – AVDD = 2.8 V
   – IOVDD = 1.8 V
   Then the driver must update the corresponding configuration in the UI.
3. Load the firmware patch
   – Write the firmware patch to memory
   – Indicate in the UI that the patch must be loaded during boot
   – Issue the boot command. See Table 11. Boot settings UI

Below is a pseudo code that the driver must implement to boot the device:

```
CHECK DEVICE_ID == 0x53334C39 WRITE EXT_CLOCK with Clock value ( in HZ)
WRITE VDDA_CFG if different VDDA is 3v3 (default value 2v8)
WRITE VDDIO_CFG if different VDDIO is 1v2 (default value 1v8) WRITE FW PATCH in memory (0x180
0)
WRITE I AND register NSTALL_PATCH to 1
WRITE BOOT (1) in COMMAND REGISTER
```

2.5.3 Device calibration

The firmware patch is applied during boot. All internal clocks are configured, and the user interface is updated. The versions of the firmware, patch, and user interface are updated and can be read and verified by the driver. The firmware has read the content of the OTP and made available information such as calibration offsets, optical center, and lens normalization parameters.

Important: *In I3C, when the driver accesses data blocks via the control interface, the data rate is too high for the device that operates at a slow frequency. To ensure proper reading of the information, the fast clock must be activated before any read operation of a size greater than one word of four bytes.*

The driver must read the calibration information useful for the post processing function.

Below is an example of code to read calibration data.

```
WRITE SWITCH_TO_FAST_CLOCK (7) in COMMAND register
READ Offset Calibration data blocks READ Lens Centering
READ Rate Normalization Data
WRITE SWITCH_TO_EXT_CLOCK (8) in COMMAND register
```

2.5.4 Device specific configuration

After boot, the following settings need to be configured:

- MIPI CSI-2 IP
- CAB (custom analog block)
- DSS (dynamic SPAD selection) algorithm

2.5.4.1 MIPI CSI-2 configuration

2.5.4.1.1 Data buffers

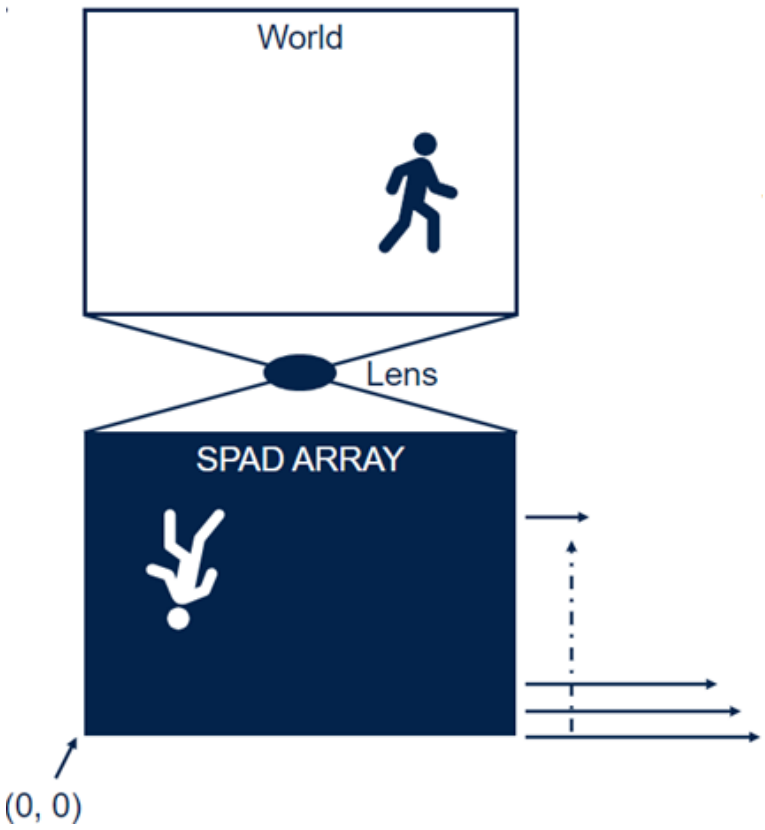
The distance, amplitude, and ambient buffers have a size in bytes corresponding to twice the number of pixels. For a resolution of 54x42, the buffers are each 4536 bytes. The two consecutive bytes per zone are encoded in little endian (least significant byte first).

The DSS buffer is added only when the DSS is active. For each pixel, the information from the DSS lookup table (LUT) used is encoded in 4 bits. Thus, the DSS buffer has a size in bytes corresponding to half the resolution, which is 1134 bytes for a resolution of 54x42.

The embedded data line (also called ISL) is always 100 bytes.

The first streamed byte corresponds to index (0,0), located in the bottom-left corner of the array when the device is viewed with Rx on the left and Tx on the right. The last byte corresponds to the top-right corner. Streaming is performed line by line, from bottom to top.

Figure 4. **Array streaming order**



2.5.4.1.2 CSI-2 formatting

The MIPI interface can adapt to the constraints of the receivers. It is possible to configure the data types as well as the frame size and data rate.

Below are several examples of data formatting.

ISL and datatype share the resolution (option 1)

In the first configuration, both the embedded data line (ISL) and the data buffers share the same width dimensions. The four data buffers (distance, amplitude, ambient, and DSS) are concatenated followed by padding byte to complete the row. The embedded data starts on the next line, also completed with padding. In this configuration, the register FORCE_ISL_WIDTH is set to 0.

The figure below illustrates the frame format.

Figure 5. **Configuration with a single width (ISL and data)**

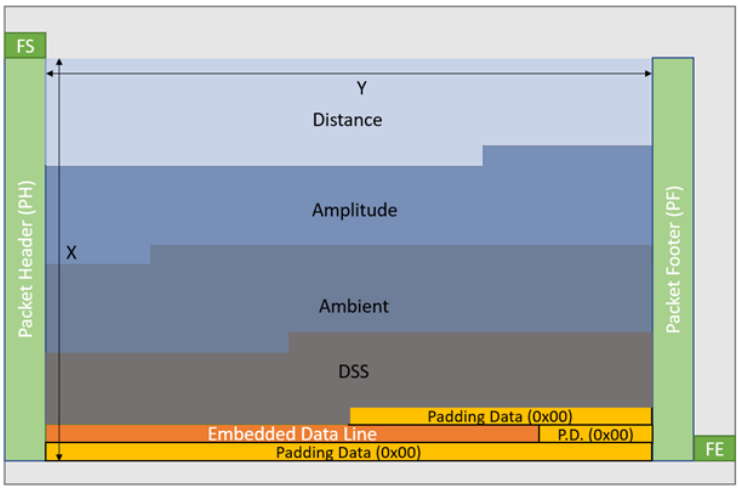
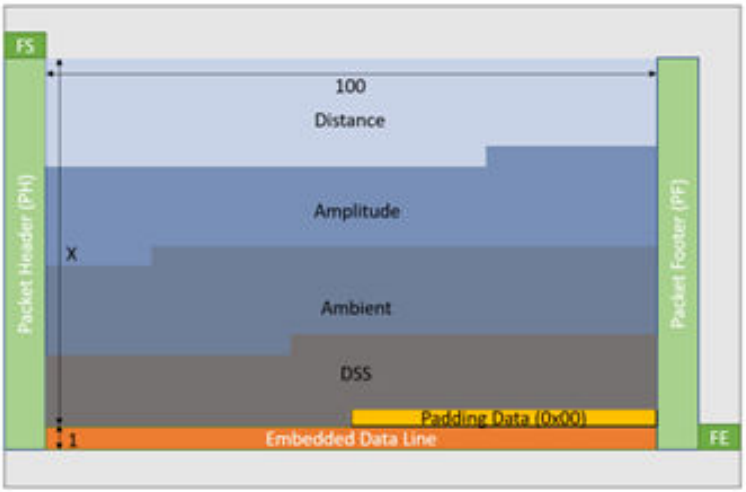


Table 19. **CSI format guideline (option 1)**

Configuration	54x42	24x24	18x14
FORCE_ISL_WIDTH	0	0	0
CSI2_ISL_DATA_TYPE	0x12	0x12	0x12
CSI2_FRAME_DATA_TYPE	0x2A	0x2A	0x2A
CSI2_VIRTUAL_CHANNEL	0	0	0
CSI2_FRAME_WIDTH	100	100	100
CSI2_FRAME_HEIGHT	148	38	17

With these configurations, each line is 100 bytes like the ISL, which is found at the end of the buffer, and the number of lines varies depending on the resolution, as illustrated below for a frame with a resolution of 54x42.

Figure 6. **Option 1: 54 x 42 frame Resolution illustration**



X depends on the frame resolution (for example 148 in 54x42)

ISL and datatype have two different dimensions (option 2)

The second option is to differentiate the size of the data. The size of the embedded data line can also be differentiated. In this case, the ISL has a size of 100 bytes on a single line. In this configuration the register, FORCE_ISL_WIDTH is set to 1.

It is therefore possible to match the CSI-2 frame size to the frame resolution, as shown in the example below. This allows the padding after the DSS buffer to be reduced.

Figure 7. Configuration with independent width (ISL and data)

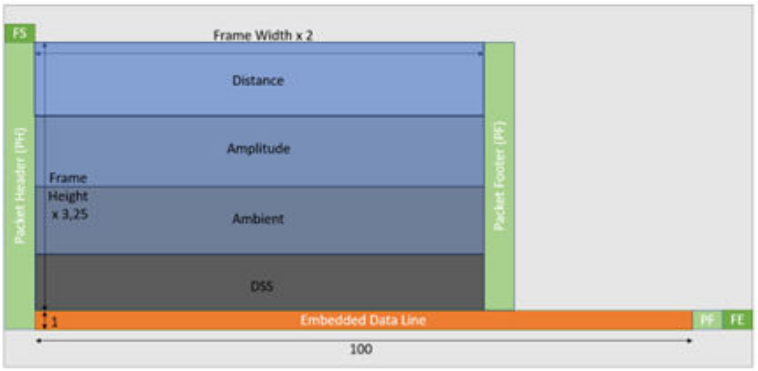


Table 20. CSI format guideline (option 2)

Configuration	54x42	24x24	18x14
FORCE_ISL_WIDTH	**1**	**1**	**1**
CSI2_ISL_DATA_TYPE	0x12	0x12	0x12
CSI2_FRAME_DATA_TYPE	0x2A	0x2A	0x2A
CSI2_VIRTUAL_CHANNEL	0	0	0
CSI2_FRAME_WIDTH	108	48	36
CSI2_FRAME_HEIGHT	137	78	46

Below is a guideline to configure the MIPI CSI-2 interface

```
WRITE CSI2_ISL_DATA_TYPE 0x12
WRITE CSI2_FRAME_DATA_TYPE 0x2A
WRITE CSI2_DATA_RATE 1000000000
WRITE CSI2_VIRTUAL_CHANNEL 0
WRITE FORCE_ISL_WIDTH 0
```

2.5.4.2 *CAB configuration*

The ambient attenuation byte needs to be overwritten as in the example below. The ambient data is stored over 24 bits but only 16 bits are streamed out. The ambient attenuation register shifts the data to the left. Configuring the byte to four divides the integrated value by 16.

Below is a guideline to configure the CAB.

```
WRITE SOC_CABDT_ALGO_SCALE.amb_att 0x04
```

2.5.4.3 *DSS configuration*

Below is a guideline to tune the DSS.

```
WRITE DSS_DEFAULT_INIT_LUT = 3
WRITE SHORT_DSS_OR_TREE_LIMIT = 656
WRITE LONG_DSS_OR_TREE_LIMIT = 656
WRITE SHORT_DSS_AMB_WEIGHT = 12
WRITE SHORT_DSS_AMB_WEIGHT = 12
```

2.5.5 Streaming profile configuration

2.5.5.1 *Switchover configuration*

The switchover function ensures better linearity of ranging data. The transition between short-range integration and long-range integration occurs linearly around the switchover distance.

Below is a guideline to tune the switchover

Configuration for a seven-step (precision) mode profile:

```
WRITE DISTANCE_SWITCHOVER 325
WRITE PULSE_WIDTH_SHORT 21
WRITE PULSE_WIDTH_LONG 21
WRITE DISTANCE_RTN_SHORT_OFFSET 0
WRITE SOC_CABDT_DIST_SCALE 0x01000800 (Scaler Short 256 long 2048)
WRITE CAL_PROG_OFFSET_1_TO_5 -1
WRITE CAL_PROG_OFFSET_6 5
```

Configuration for a six-step (ambient) mode profile:

```
WRITE DISTANCE_SWITCHOVER 650
WRITE PULSE_WIDTH_LONG 42
WRITE PULSE_WIDTH_LONG 42
WRITE DISTANCE_RTN_SHORT_OFFSET 2
WRITE SOC_CABDT_DIST_SCALE 0x02AB0800 (Scaler Short 683 long 2048)
WRITE CAL_PROG_OFFSET_1_TO_5 -8
WRITE CAL_PROG_OFFSET_6 -1
```

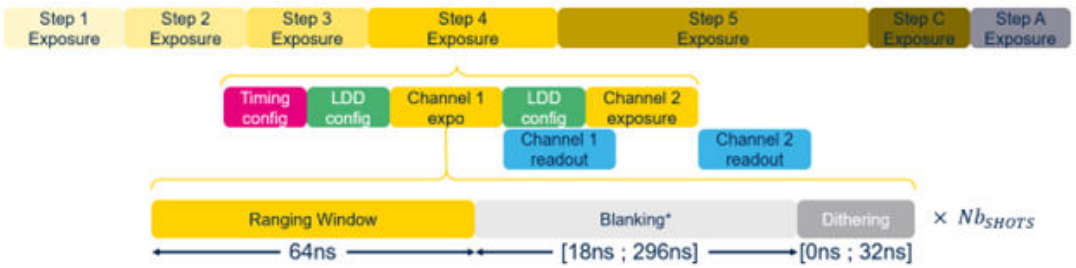
2.6 Profile guidelines

2.6.1 Exposure

The operation of the VL53L9CX is based on an iterative zoom in four or five steps, followed by a short-distance measurement and an ambient measurement. Each channel is exposed successively during each step. The exposure time of the SPADs is defined as the sum of the six or seven exposure steps.

$$FRAME_{EXPOSURE} = \sum_{i=1}^{7} STEPi_{EXPOSURE}$$

Figure 8. Frame exposure



For a given step and channel, the receiver is exposed for several cycles determined by the number of shots programmed in the dynamic context registers (see Table 13. Streaming settings UI).

The cycle consists of a fixed ranging period of 64 ns (which corresponds to a maximum ranging distance of 9.6 m) followed by a blanking period. This blanking period is defined based on the duration of the optical pulse as well as its power to comply with the power limits of laser Class 1.

An optional period of dynamic blanking (Dithering) may eventually be added to mitigate interference.

The formula below defines the total exposure time of a step.

$$STEP_{EXPOSURE} = (RANGING_{WINDOW} + BLANKING_{FIXED} + BLANKING_{DITHER}) \times STEP_{SHOTS} \times CHANNEL_{NUMBER}$$

$$STEP_{EXPOSURE} = (64ns + BLANKING_{FIXED} + BLANKING_{DITHER}) \times STEP_{SHOTS} \times 2$$

It is recommended to maintain an equivalent signal-to-noise ratio (SNR) between steps to ensure the best performance. The Table 21. Number of shot guidelines provides recommendations for configuring the number of shots per step.

Table 21. Number of shot guidelines

STEP index	Ambient mode (six steps)				Ratio	Precision mode (seven steps)		
	Ratio	Example (expo 3.5 ms)	Blanking (1)	VCSEL duty cycle		Example (expo 5.5 ms)	Blanking (1)	VCSEL duty cycle
STEP 1	1.00	1000	296	4.4%	1.00	1000	296	4.4%
STEP 2	2.00	2000	116	4.4%	2.00	2000	116	4.4%
STEP 3	3.08	3076	26	4.4%	4.00	4000	26	4.4%
STEP 4	6.15	6153	20	3.1%	6.15	6153	20	3.1%
STEP 5	0.00	0	0	0.0%	12.31	12307	18	1.6%
STEP C	6.15	6153	20	3.2%	12.31	12307	18	1.6%
STEP A	1.00	1000	0	0.0%	1.00	1000	0	0.0%

1. *Blanking values in the table are the minimum blanking duration but the customer can increase the value. The device is not operational below the minimum values.*

2.6.2 Frame rate limitations

There is no software limitation related to the frame rate in the driver or firmware. The user is responsible for the configuration, which may not be physically achievable. In standalone mode, the frame rate is controlled via the frame period. It is entirely possible to set a frame period much shorter than the frame integration time. However, in this case, the frame is fully integrated before another frame integration can be started.

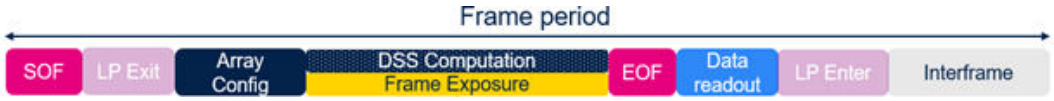
This also applies to external or manual synchronization modes. All frames start requests will be ignored regardless of their source during the integration of a frame. Therefore, it is highly likely to achieve a lower frame rate than expected if the integration time is too long.

For a given frame rate, if the user increases the frame integration time, at some point, the actual frame rate is halved compared to the expected frame rate. If the integration time increases further, it is possible that the division will be even greater.

The following section describes in detail the breakdown of the integration time of a frame and the various factors that can influence its evolution.

2.6.3 Frame period

Figure 9. Frame period overview



The frame period is divided into several phases:

- **Start of frame**: The profile configuration is applied during this phase. Some configurations, such as those related to exposure, can be changed dynamically. These configurations are applied to the different hardware blocks at the beginning of the frame.
- **Low-power exit (Optional)**: Exit low-power mode and reactivate PLLs and power supplies in case the device was in low power.
- **Array configuration**: The SPAD array is configured, SPADs are selected, and the SPAD array supply booster is set.
- **Frame exposure** and **DSS computation** in parallel: In parallel with the Rx exposure, the firmware will calculate the DSS configuration for the next frame, which takes approximately 5.5 ms of computation. The minimum duration of the frame exposure cannot be shorter, even in the case of short exposure. Between each step of the iterative zoom, the firmware configures the laser driver, and approximately 2.6 ms of the complete frame will be dedicated to synchronization actions.
- **End of frame**: The SPAD array supply booster is controlled, and the temperature is measured to potentially readjust the SPADs' supply voltage for the next cycle.
- **Data readout**: The data is being streamed
- **Enter Low power (Optional):** The PLLs and the power supplies are turned off if the devices are in low-power mode.
- **Interframe**: The device is waiting for a request to start a new frame.

The following table summarizes the execution times of the different actions.

Table 22. Phase durations

Power modes	Regular	Low power / ultralow power
Start of frame	100 µs	100 µs
LP exit	-	3.5 ms
Array configuration	1 ms	1 ms
Frame exposure*	Expo (1) + 2 ms	Expo (1) + 2 ms
DSS computation in full resolution precision(2)	13.5 ms	13.5 ms
End of frame	400 µs	400 µs
Readout	500 µs	2 ms
Entering Low power	-	100 µs

1. *Expo is defined as the sum of all steps exposure*
2. *DSS computation (in full resolution) and frame exposure are running in parallel. The longest activity determines the phase duration.*

2.6.4 Recommended profile settings

The Table 23. Recommended configuration provides two examples of profiles for either precision mode measurement or ranging mode measurement. The user can then adjust the resolution, frame rate, and exposure according to the desired application.

Table 23. Recommended configuration

Profile name		VR headset	Outdoor lidar
Description		Precision mode	Ambient mode
Resolution		54 x 42	54 x 42
Frame rate		30 FPS	30 FPS
Exposure		5 ms	16 ms
Power		150 mW	450 - 800 mW
Standby settings	Mode	Ranging	Ranging

Profile name			VR headset	Outdoor lidar
Standby settings	Context		Short	Long
	Format		Wide	Wide
	Frame period		33333	33333
	Power mode		Ultralow power	Regular
Switchover	Cal prog offset 1_5		1	-8
	Cal prog offset 6		5	-1
	REF long offset		-32	-32
	RTN long offset		0	0
	RTN short offset		0	2
	Switchover		325	650
Standby context	Binning		2	2
	DSS		Long	Long
	Repeat		1	1
	Step number		7	6
Stream context	VCSEL config ch0	Step 1	1	1
		Step 2	3	3
		Step 3	5	13
		Step 4	11	11
		Step 5	9	0
		Step 6	9	11
		Step 7	0	0
	VCSEL config ch1	Step 1	2	2
		Step 2	4	4
		Step 3	6	14
		Step 4	12	12
		Step 5	10	0
		Step 6	10	12
		Step 7	0	0
	Blanking	Step 1	296	296
		Step 2	116	116
		Step 3	26	54
		Step 4	20	20
		Step 5	18	0
		Step 6	18	20
		Step 7	0	0
	Max dithering	Step 1	31	31
		Step 2	31	31
		Step 3	31	31
		Step 4	31	31
		Step 5	31	31
		Step 6	31	31

Profile name			VR headset	Outdoor lidar
Stream context	Max dithering	Step 7	0	0
	Shot number	Step 1	900	4600
		Step 2	1800	9200
		Step 3	3600	14153
		Step 4	5538	28307
		Step 5	11076	0
		Step 6	11076	28307
		Step 7	900	4600
	Pulse width short		21	42
	Pulse width long		21	42

2.7 Application configuration

2.7.1 Frame signaling

The interrupt PIN is the output I/O that signals the new frame (falling edge). The driver can configure the device to drive the INTR pin to signal a new frame or use the I3C in-bound interrupt mechanism. By default, this is the INTR configuration that is set.

The configuration of the frame signaling is possible thanks to register FRAME_SIGNALING_MODE (see Table 12. Standby settings UI).

2.7.2 Frame synchronization

There are three streaming modes:

- Autonomous: the frame rate is controlled via the frame period register.
- Manual: The device starts a new frame when the driver calls the trigger next frame command.
- Follower: The device starts a new frame using the SYNC_IN pin (active Low)

The configuration of the synchronization mode is possible thanks to register SYNCHRO.

The SYNC_IN pin is very useful to synchronize two devices together, for example a camera with a ToF sensor, or several ToF sensors.

2.8 Device addressing

2.8.1 I²C device addressing

The default device I²C address is 0x29 (7 bits) but the user can change the default address. Firmware is reading the custom OTP memory during the Ready to boot State. If the I2C_SLAVE_ID is different from 0x00, then the firmware applies the new I²C address prior to enable the communication interface. There are two mechanisms allowing to change the I²C address.

Note: Two devices on the same I²C interface cannot share the same address without generating a conflict.

Temporary change

The driver can change the I²C address in live through the I²C IP registers.

Permanent change

The user can write the custom OTP memory (see Table 15. OTP mirror UI) to force the default I²C address.

2.8.2 I3C device addressing

The I3C leader allocates dynamic address to any device present on the I3C interface. The handshake is performed using the I²C address, after which the leader allocates a dynamic address.

Working with many I3C devices

If there are many devices on the same I3C bus, all devices should have a different instance ID. Follow the procedure below to program another instance ID in OTP (see Table 15. OTP mirror UI).

2.8.3 OTP programming procedure

ST recommends to program I^2C address and I3C instance ID at the same time in OTP to avoid the CRC computation issue. Follow the procedure described below.

```
WRITE I3C_Instance_ID (e.g. 0x1)
WRITE I2C_SLAVE_ID (e.g. 0x2A)
WRITE OTP_ADDRESS 0x0000
WRITE OTP_SIZE 8
WRITE OTP_CUSTOM_WRITE (0x9) in COMMAND register
RESET the device (to apply the new setting).
```

3 Acronyms and abbreviations

Table 24. **Acronyms and abbreviations**

Acronym	Definition
CAB	custom analog block
CRC	cyclic redundancy check
DSS	dynamic SPAD selection
FoV	field of view
FPS	frame per second
FW	firmware
GPIO	general-purpose I/O
HW	hardware
I^2C	inter-integrated circuit bus
IBI	inbound interrupt
ISL	embedded data line
LDO	low dropout
OTP	one-time programmable memory
PLL	phase-locked loop
SPAD	single photon avalanche diode
SPI	serial peripheral interface
SW	software
ToF	Time-of-Flight
UI	user interface
VCSEL	vertical-cavity surface-emitting laser

Revision history

Table 25. **Document revision history**

Date	Version	Changes
10-Jul-2026	1	Initial release.
23-Jul-2026	2	Section 2.4.1: Firmware errors: Changed the description from *register 0x0066* to *register 0x0064*.
27-Aug-2026	3	Updated Section 2.4: Device errors management.
02-Oct-2026	4	Table 21. Number of shot guidelines: Updated values for Step 5 and Step C.
20-Oct-2026	5	Section 1.3: Synchronization interfaces: Updated introduction sentence for clarity. Table 13. Streaming settings UI: Modifed the reset value for register DISTANCE_RTN_SHORT_OFFSET, address 0x057A. Table 23. Recommended configuration: Updated values for Standby context and Stream context. Section 2.7.1: Frame signaling: Updated introduction sentence for clarity.

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