



VIPower M0-9 SPI standard high side drivers

Introduction

This document complements "UM3352" (user manual for VIPower M0-9 standard high-side drivers).

The following arguments are relevant for integrated circuits (ICs) in the M0-9 family that implements the digital serial peripheral interface (SPI).

1 General items and application schematics

1.1 Overview about M0-9 SPI high-side drivers

The M09-SPI is a family of devices made using STMicroelectronics VIPower technology. They are intended for driving resistive or inductive loads directly connected to the ground. These devices are protected against voltage transients on the VCC pin. Programming, control, and diagnostics are implemented via the SPI bus. Digital current sense feedback for each channel is provided through an integrated 10-bit ADC with 0.1% of FSR. Dedicated trimming bits allow adjusting the ADC reference current. The devices are equipped with 4-6 outputs controllable via SPI or with the 2-OTP assignable direct inputs. The devices detect open-load in OFF-state conditions. Real-time diagnostics are available through the SPI bus (open load, output short to VCC, overtemperature, communication error, power limitation, or latch off). Output current limitation protects the devices in an overload condition. The devices can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or programmable time-limited auto restart. The devices enter a limp-home mode in case of loss of digital supply (VDD), reset of digital memory, or watchdog monitoring time-out event. In limp-home mode, each output is set according to the programmed register: to be always OFF, or according to the 2x direct input pins.

1.2 Typical application schematic and BOM

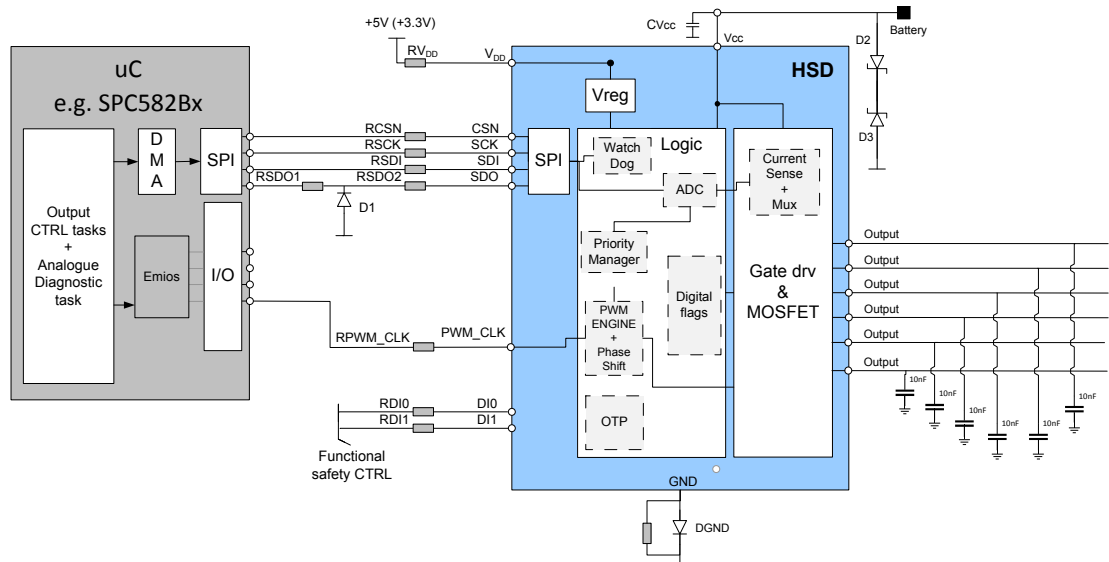
1.2.1 M0-9 SPI typical application schematics – 6ch device example

A DC supply voltage is applied to VDD to supply the digital control part and SPI interface.

The Vdd pin is compatible with +5 V or +3.3 V to supply an internal voltage regulator Vreg.

This supply voltage can be derived from an external source (for example, microcontroller section) to ensure SPI communication of the digital part.

Figure 1. Typical application schematic for M0-9 SPI device



1.2.2 M0-9 SPI typical BOM

The following table shows the BOM for a typical M0-9 application schematic.

Table 1. M0-9 SPI typical BOM

Symbol	Description	Value	Rating	Note
C _{VCC}	Ceramic filtering capacitor	100 nF	50 V	To be placed as close as possible to VCC pin.
D1	MCU protection diode	BAT54		Recommended
D2	TVS 20 V	SM6F18AY		Recommended
D3	TVS 36 V	SMA6T33AY		Recommended
R _{VDD}	Protection resistor	150 Ω		Needed for Pulse1/reverse polarity condition
C _{DD}	VDD bulk capacitor	1 nF		
RCSN	Protection resistor	2.2 kΩ		Needed for reverse polarity condition
RSCK	Protection resistor	2.2 kΩ		Needed for reverse polarity condition
RSDI	Protection resistor	2.2 kΩ		Needed for reverse polarity condition
RSDO1	Protection resistor	50 Ω		Needed for reverse polarity condition
RSDO2	Protection resistor	220 Ω		Needed for reverse polarity condition
RPWM_CLK	Protection resistor	2.2 kΩ		Needed for reverse polarity condition
RDI0	Protection resistor	2.2		Needed for reverse polarity condition
RDI1	Protection resistor	2.2 kΩ		Needed for reverse polarity condition
RGND	Reverse polarity turn-on bias	4.7 kΩkΩ		
DGND	Reverse polarity protection	BAS21 for VDD = 5 V BAT54-Y for VDD = 3.3 V		Usage of Schottky or standard diode dependent on VDD

BOM description:

C_{VCC} is a 100nF ceramic capacitor between pin and ground recommended (capacitor as close as possible to pin) to absorb all fast transients between the VCC pin and GND pin.

Transient suppressors **D2** and **D3** are necessary to protect the device from both positive and negative transients on the battery line.

RCSN, **RSCK**, **RSDI**, **RPWM_CLK**, **RDI0**, **RDI1** resistors on all MCU interface input lines (DI0, DI1, CSN, SCK, SDI, PWM_CLK) are necessary to provide protection for MCU and M0-9 device during positive or negative voltage transients and reverse polarity on battery supply line.

For a detailed description of this resistors network and its dimensioning refer to [Section 2.2](#).

The protection scheme for the SDO pin differs from other SPI lines. It consists of two resistors, RSDO1 and RSDO2, and a Schottky diode, D1, positioned between them.

RSDO2 must be significantly lower than other SPI protection resistors to ensure maximum SPI communication speed minimizing the propagation delay, and at the same time limit the current in case of reverse polarity.

Because the SDO reverse polarity current is higher due to the lower value of RSDO2, adequate protection for the MISO pin (Master Input Slave Output) requires a lower impedance path. This is achieved by using the Schottky diode D1 and the decoupling resistor RSDO1.

The purpose of the resistor RSDO1 is to create a higher impedance path inside the MCU pin for the reverse polarity current, and 50 Ω is a suitable value.

For a detailed description of this network and its dimensioning refer to chap. 2.2.

A serial protection resistor of 150 Ω on V_{DD} line (**RVDD**) is needed to limit the current in the input device structure to a safer value during transient (on the battery line) and reverse polarity condition.

As specified by the related AMR limit for reverse polarity condition, this current cannot exceed the value of 80 mA. To guarantee this maximum value (occurring during reverse polarity condition), the recommended **RVDD** resistor value shall be not less than 150 Ω.

For a detailed description of this network and its dimensioning refer to chap. 2.2

Reverse battery device protection circuit (**DGND** and **RGND**) is needed to prevent damage of the device in case of reverse battery polarity. The recommended diode is a Schottky type to ensure $V_F \approx 0.3 \text{ V}$ or below @25°C.

RGND recommended value is 4.7k.

If the device is used in a 5V MCU supply system, there is no need to use the BAT54-Y Schottky diode and it can be used for instance a standard signal diode as BAS21.

In this case, with the aim to reduce the reverse polarity current flowing into the RVDD resistor, and consequently reduce the associated power dissipation, a higher ohmic value for RVDD can be used.

The diode DGND is needed to limit the GND voltage shift, while the RGND helps to reduce voltage spikes during the demagnetization phase.

A 10 nF ceramic capacitor on each output OUTx is recommended, dissipating high frequency energy, high-voltage transients, particularly ESD transient pulses.

C_{VCC} capacitor helps to suppress voltage transients that originate from other actuators connected in parallel and sharing the same battery line. This capacitor is placed to suppress only low energetic short transient pulses. Moreover, the **C_{VCC}** capacitor helps to suppress HF noise at the VCC pin that is generated by the high side driver device itself. The noise can originate from the charge pump circuitry or from the switching slopes of the PWMed outputs.

Using 100 nF low ESR MLCC, mounted close to the device VCC pin and GND PCB, is recommended to help meet CISPR25 class 5 requirements, measured with conducted emission voltage method during DC-as well as PWM-operation.

2 Reverse battery protection requirements

A universal problem in the automotive environment is the threat of damage when an end user inverts the battery polarity. Users of battery-powered equipment expect safeguards to prevent damage to the internal electronics in the event of reverse battery installation. These safeguards can be either mechanical (use of special connectors) or electronic. In that case, battery-powered equipment designers and manufacturers must ensure that any reverse current flow and a reverse bias voltage are low enough to prevent damage to the equipment's internal electronics. Different concepts applying passive or active reverse polarity protection are possible and described in this chapter to provide these electronic safeguards.

The reverse battery protection needs to be inserted according to the instructions suggested in this chapter.

Given the general low ohmic nature of the M0-9 devices, we consider that the reverse polarity protection is installed on the device GND connection; in that case the device conducts through the power MOSFETs itself, when featured with the "Reverse turn-on" capability, with the current limited by the external load.

Regarding those M0-9 devices (for example, VN9D5D20FN) that does not feature the "reverse turn-on" capability, it is recommended to protect the module on the battery line side to avoid that the reverse polarity current flows through device body diode, producing very high internal power dissipation.

It is important to highlight that all the standard features of the devices (i.e., Short circuit, current sense, etc.) are not available when operating under reverse polarity condition for the whole product family.

2.1 Reverse battery GND Protection Network

We describe hereafter three possible recommended reverse polarity protection schemes, listed in the following Table 2.

The criteria to choose the reverse polarity network doesn't change if the device is featured with reverse polarity turn-on or not.

Table 2. Reverse polarity networks

Reverse battery protection concept	Reference	Active/ passive
Schottky Diode resistor	Section 2.1.1	Passive
N-Ch MOS resistor	2.1.2	Active

We will describe following cases:

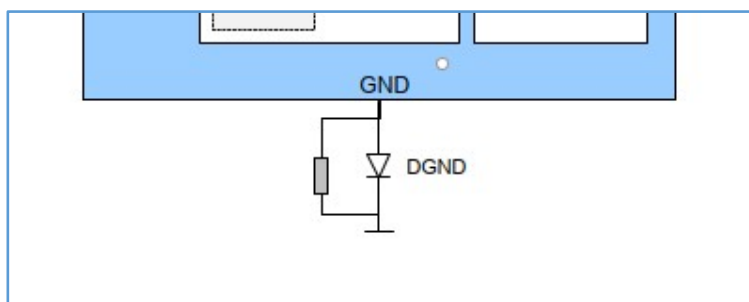
- Usage of Schottky diode in parallel with resistor
- Usage of N-Ch MOSFET in parallel with resistor

2.1.1 Schottky diode in parallel with resistor

The reverse battery protection network is applied between the GND pin of the driver and the GND of the module, see Figure 2. This kind of protection doesn't block the current flow through the power MOSFET in reverse polarity condition but is protecting the internal logic structure.

In reverse polarity condition, the current flow in the Power MOSFET will be limited only by the external load.

Figure 2. Detail of reverse polarity network with diode // resistor



In reverse polarity condition no active protection is available, so special attention must be paid to the total power dissipation in the device. During the reverse battery event, the peak junction temperature shall remain safely below the maximum allowed junction temperature (T_{TSD_max}).

If the device does not feature the “Reverse turn-on capability”, special care must be considered since the Power MOSFET will be in off condition, and all the load current will flow across its body diode whose voltage drop will be $V_{F_max} = 0.7$ V. The resulting power dissipation in the high side driver per output channel is $P_D = 0.7$ V * I_{LOAD} . The diagrams of Zthj-a, reported in HSD M0-9 SPI datasheets, support the user to calculate the maximum affordable load current for a given PCB layout.

If the device features the “Reverse turn-on capability” the afore mentioned consideration is not valid anymore since the Power MOSFET will be in full ON condition as it was in normal polarization bias.

For what concern the GND path of the device, the integrated VCC-GND clamping protection, which circuit behaves like a Zener diode, will be forward biased in reverse battery condition. The power dissipation in the GND resistor of this “as zener diode” is therefore determined by:

$P_D = (|V_{bat_rev}| - V_F)^2 / R_{GND}$ which is anyhow negligible.

The Table 3 provides an overview of pins' resulting voltage levels in a typical application schematic during reverse battery condition when:

Loads:

- OUT 0, 1: H9-65W
- OUT 2, 3: P27W+R5W

Table 3. Reverse battery-voltage to GND on pins (VN9D5D20F)

Pin Voltage [V] & Current [A] VN9D5D20FN			Pin voltage [V] (uC side) (no serial resistors on output/input pin of the uController)	
VCC	-13.5 V	~ 14 A	VDD_uC	-0.5 V
VDD	-12.4 V	80 mA	VCSN_uC	-0.78 V
CSN	-7.5 V	3 mA	VSCK_uC	-0.78 V
SCK	-7.5 V	3 mA	VSDO_uC	-0.5 V
SDI	-7.5 V	3 mA	VSDI_uC	-0.78 V
SDO	-12 V	51 mA	VPWM_CLK_uC	-0.75 V
PWM_CLK	-5.7 V	2.5 mA	VDI0_uC	-0.7 V
DI0	-6.5 V	2.6 mA	VDI1_uC	-0.7 V
DI1	-6.5 V	2.6 mA		
VGND	-12.9 V	2.7 mA		
VOUtx	-13.4 V	~ 14 A		

2.1.2 N-ch MOSFET in parallel with diode and resistor

Compared to the solution described in the previous chapters, reverse polarity protection with MOSFETs offers two main advantages:

- Lower power losses
- Minimal voltage drop

The N-channel MOSFET body diode is aligned with the normal current path, as shown in Figure 3, with the drain connected to the module GND and the source connected to GND_dev. If the battery is inserted with reversed polarity, the N-channel MOSFET gate-source voltage remains low, preventing the device from turning on. When the battery is inserted correctly, the N-channel MOSFET gate-source voltage is driven high, and the channel conducts to bypass the diode.

A voltage drop equal to $R_{DS(on)} \times I_{GND_Dev}$ is observed in the ground return path when using the N-channel MOSFET.

The N-channel MOSFET has its gate driven directly by the battery voltage, and its drain connected to the ground. Under normal conditions, it is ON, while a reverse-battery event switches it OFF because $V_{GS} \leq 0$, thereby protecting the HSD.

The N-channel MOSFET breakdown voltage, $BVDSS$, should be higher than the maximum negative TVS voltage rating of diode D2 in Figure 1. The 4.7 nF capacitor helps ensure fast MOSFET turn on and turn off during negative transient conditions, such as ISO 7637-2:2011 Pulse 1 (Figure 4).

In the case of ISO 7637-2 Pulse 2a, a large current may flow through the GND_dev pin.

The BAT54 diode protects the N-channel MOSFET by clamping its V_{DS} voltage to the diode forward voltage V_F .

Figure 3. Detail of reverse polarity network with N-channel MOSFET diode and resistor

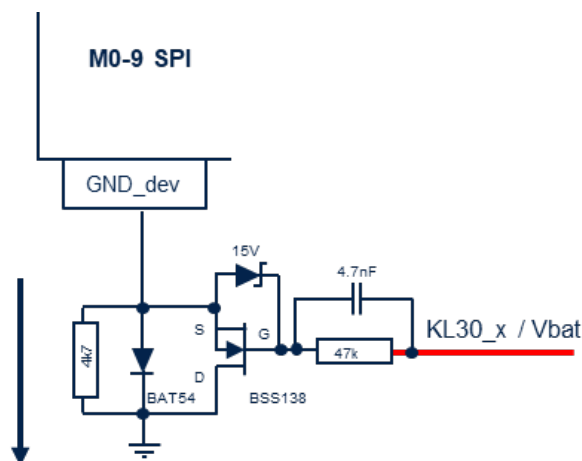
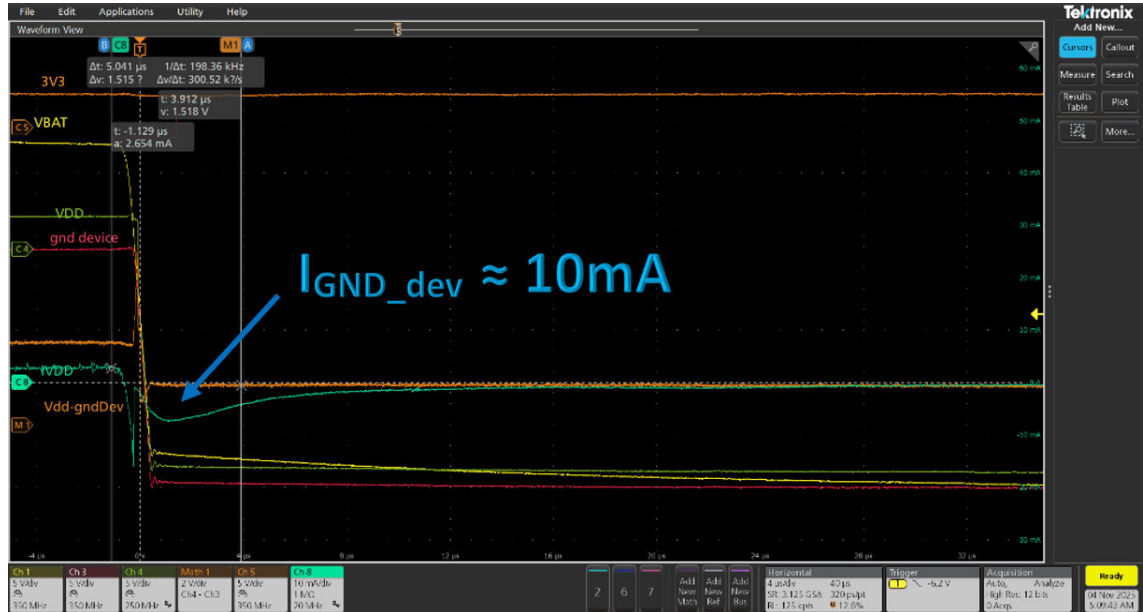


Figure 4. I_{GND_dev} current during ISO 7637-2 Pulse 1


2.2

Reverse battery protection resistors dimensioning

We describe hereafter how to determine protection resistors on SPI pins, RSCK, RCSN, RSDI, RPWM_CLK, RDI0, RDI1 (R_{PROT}) with the following calculations, assuming that during reverse polarity conditions we have the following **worst-case** configuration:

$$R_{PROT} \geq \frac{(V_{CCREVERSE} - V_{DEVICE_clamping_diode}) - (V_{MCU_clamping_diode})}{(I_{INJ_max})}$$

Where:

- $V_{CCREVERSE} = 16V$
- $V_{DEVICE_clamping_diode} = 7V$
- $V_{MCU_clamping_diode} = -0.3V$
- $I_{INJ_max} = 4mA$

$$R_{PROT} \geq \frac{16V - 7V - 0.3V}{4mA} \approx 2.2k\Omega$$

This calculation is performed considering a reverse polarity condition which, according to ISO 16750-2/2023 and LV124, is foreseen to last normally not more than 1 minute.

Considering that the system shall sustain also ISO Pulse 1 condition, as per ISO 7637-2/2011, the TVS clamps the negative supply voltage to -20 V roughly. In this case, with the already dimensioned R_{PROT} , the peak current injected into MCU pin reaches a maximum value of 5.77 mA lasting 2 ms worst case, which is still acceptable using the following formula:

$$I_{INJ} = \frac{20V - 7V - 0.3V}{2.2k\Omega} = 5.77mA$$

How to determine R_{VDD} :

Assuming that the minimum supply voltage for the V_{DD} pin, referred to its GND, is calculated as follows:

$$V_{DD} = 3.3V \cdot (1 - 2\%) - V_F - I_{VDD} \cdot R_{VDD} \approx 2.7V$$

Where:

- -2% is the typical automotive grade LDO worst case tolerance
- V_F is the BAT54-Y forward voltage
- I_{VDD} is the maximum current drawn by the V_{DD} supply input
- R_{VDD} is the protection resistor of V_{DD} pin

The BAT54-Y diode is subjected to the current flowing from the GND device pin, which is roughly 6.56 obtained from characterization data at room temperature of -40°C.

At this temperature, as shown in Figure 5 we have:

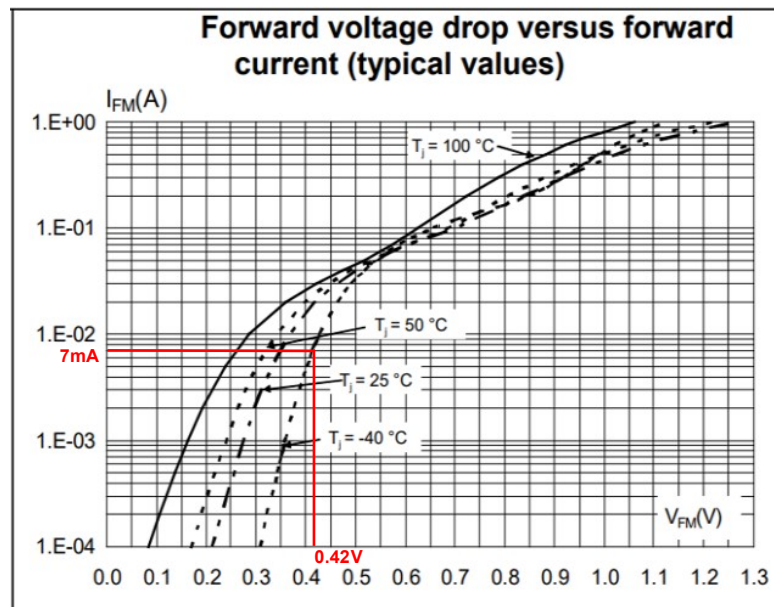
- $V_F = 0,42 \text{ V}$ (@6.56mA, worst case I_{SON})
- $I_{VDD} = 0,82 \text{ mA}$ (maximum worst case)
- $R_{VDD} = 150 \Omega$ (2% tolerance is introducing negligible effect)

So:

$$V_{DD} = 3.234V - 0.42V - 0.123V \approx 2.7V$$

This voltage value can guarantee the SPI electrical characteristic as per any M0-9 SPI device datasheet.

Figure 5. BAT54 VF characteristics



How to determine R_{SDO2} :

Considering that the AMR value for SDO pin, in reverse polarity condition is 54 mA, we need to dimension R_{SDO2} so that:

$$I_{SDO} \leq \frac{(V_{SDO} - V_{FD1})}{R_{SDO2}} = 54mA$$

Given that, according to Table 3

- $V_{SDO} = 12 \text{ V}$
- $V_{FD1} = 0.75 \text{ V}$

$$R_{SDO2} \geq \frac{11.25V}{54mA} \approx 208\Omega$$

We can choose as standard value $R_{SDO2} = 220 \Omega$

3 Protection against battery transients

3.1 Introduction to automotive electrical hazards

The automotive environment is the source of many electrical hazards. These hazards, such as electromagnetic interference, electrostatic discharges and other electrical disturbances are generated by various accessories like ignition, relay contacts, alternators, injectors, SMPS (that is, HID front lights) and other accessories. Because electronic modules are sensitive to electromagnetic disturbances (EMI), electrostatic discharges (ESD) and other electrical disturbances, caution must be taken wherever electronic modules are used in the automotive environment.

These hazards can occur directly in the wiring harness in case of conduct hazards or be applied indirectly to the electronic modules by radiation. These generated hazards can impact the electronics in two ways-either on the data lines or on the supply rail wires, depending on the environment.

Several standards have been produced to model the electrical hazards that are currently found in automobiles. As a result, manufacturers and suppliers have to consider these standards and have to add protection devices to their modules to fulfill the major obligations imposed by these standards.

The chapter deals with the robustness of M0-9 SPI devices submitted to ISO7637-2:2011 disturbances on the battery line and mounted in the typical application scheme.

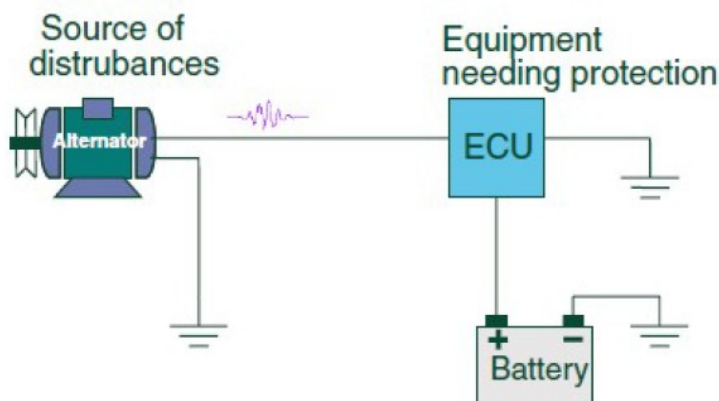
3.2 Source of hazard in automotive

3.2.1 Conducted and radiated hazards

Conducted hazards occur directly in the cable harness. Inductive loads, such as electrovalves, solenoids, alternators, etc., generate these hazards.

The schematic in Figure 6 shows a typical condition in which conducted hazards can occur

Figure 6. Conducted hazard

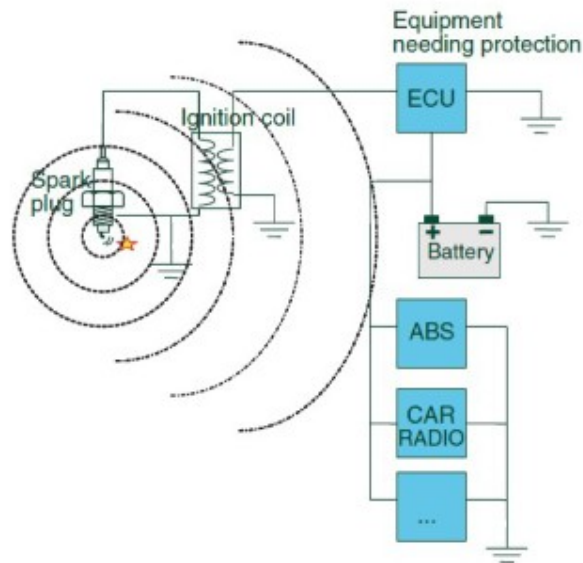


These hazards are generated by high-current switching, such as relay contacts, high-current MOSFET or insulated gate bipolar transistor (IGBT) switches, and ignition systems.

The electromagnetic field generated by these circuits directly affects lines or modules near the source of the electromagnetic radiation.

The schematic diagram in the following figure indicates how electromagnetic radiation creates hazards, such as electromagnetic interference, in electronic modules.

Figure 7. Radiated hazards



3.2.2 Propagation of electrical hazards on supply rail

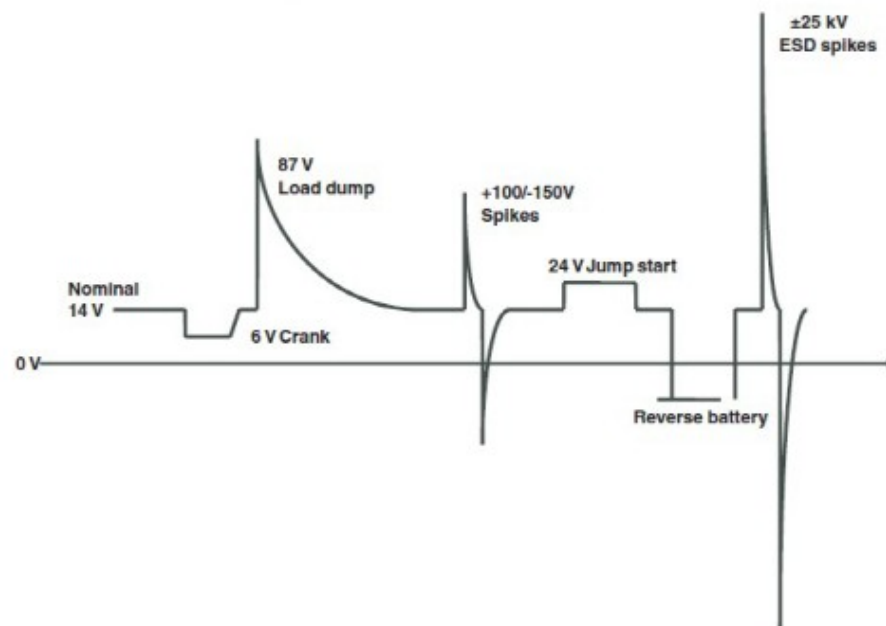
Transients that are generated on supply rail range mainly concern ISO7637-2 and ISO10605 standards.

The most energetic transients are those resulting from "load-dump" and "jump-start". But all other hazards may affect the normal operation of electronic modules.

The load-dump is caused by the battery being disconnected from the alternator while the alternator is generating charging current. This transient can last 400 ms and the equivalent generator internal resistance is specified as 0.5 Ω minimum to 4 Ω maximum.

According to the ISO 7637-2 standard, the "positive spikes" are due to supply sudden interruption of currents in a device connected in parallel with the DUT due to the inductance of the wiring harness, while the "negative spikes" are due to a supply disconnection from inductive loads. This chapter deals with voltage transient pulses, detailed on the ISO 7637-2 standard.

Figure 8. Various surges occurring in the supply rail



3.2.3 Electrical transients requirements for automotive electronics

All the hazards indicated above are described by several standards bodies such as the society of automobile engineers (SAE), the automotive electronic council (AEC) and the international standard organization (ISO). Since the ISO7637 is the most important automotive standards regarding electrical transient hazards, this document mainly concerns the cases considering such standard: Below the electrical characteristics of ISO 7637-2 2011 edition.

The following table reports typical performance of M0-9 SPI device (in this case VN9D5D20F) according to ISO 7637-2.

Table 4. ISO 7637-2 - Electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_S^{(1)}$		min	max	
1 ⁽²⁾	III	-112 V	500 pulses	0.5 s	-	2 ms, 10 Ω
2a ⁽³⁾	III	+55 V	500 pulses	0.2 s	5 s	50 μ s, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 μ s, 50 Ω
4 ⁽⁴⁾	IV	-7 V	1 pulse	-	-	100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		87 V	5 pulses	1 min	-	400 ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. With -18 V external suppressor (**SM6F18AY**) referred to ground (from -40°C to 150 °C).
3. With 35 V external suppressor (**SMA6T33AY**) referred to ground (-40°C < Tj < 150°C).
4. Test pulse from ISO 7637-2:2004(E).

3.3 ISO pulse test on VN9D5D20F according to ISO 7637-2

With reference to the typical application schematic depicted in [Section 1.2.1](#), here after the capture waveforms for following pulses according to ISO 7637-2/2011 in **OFF State**.

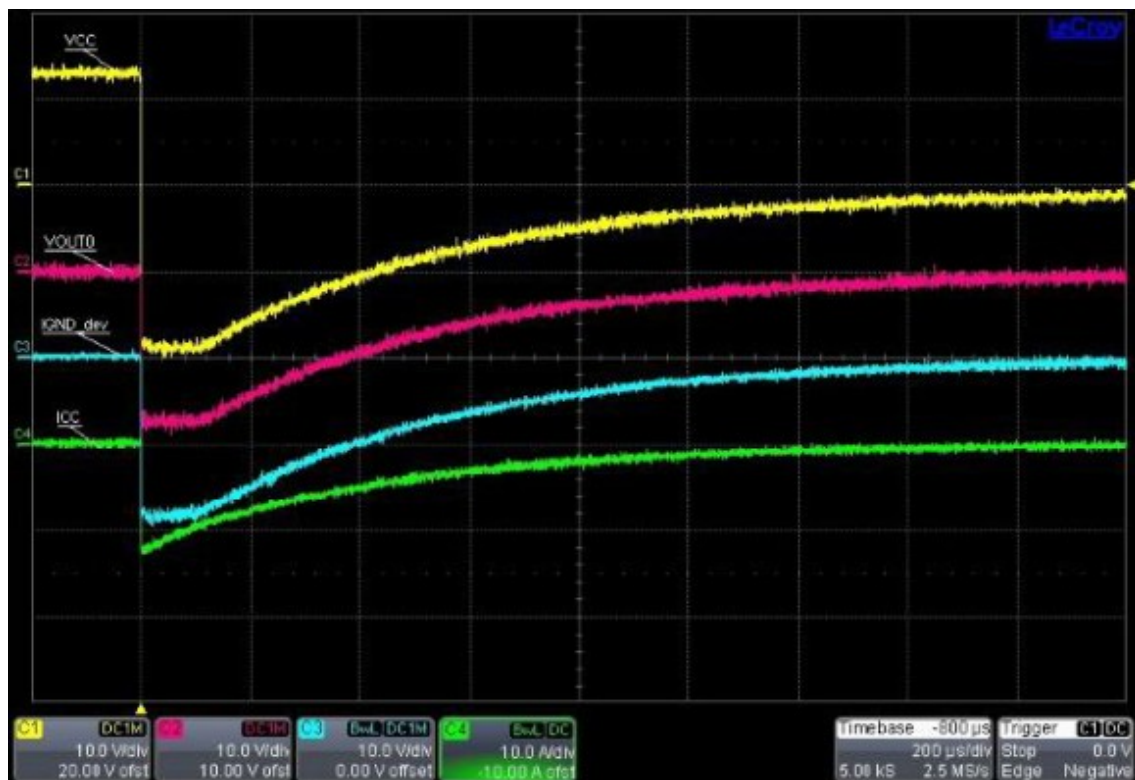
3.3.1 Test pulse 1

DUT configuration: Applicative **OFF STATE**, pulse on VCC pin

Generator configuration: Tr = 1 μ s / Td = 200 ms 0 μ s / Ri = 10 Ω / T1=0.5 s/ T2 = 200 / 500 pulses

Test results: **PASS level IV (-150 V / 500 pulses)**

Figure 9. Test pulse 1



3.3.2

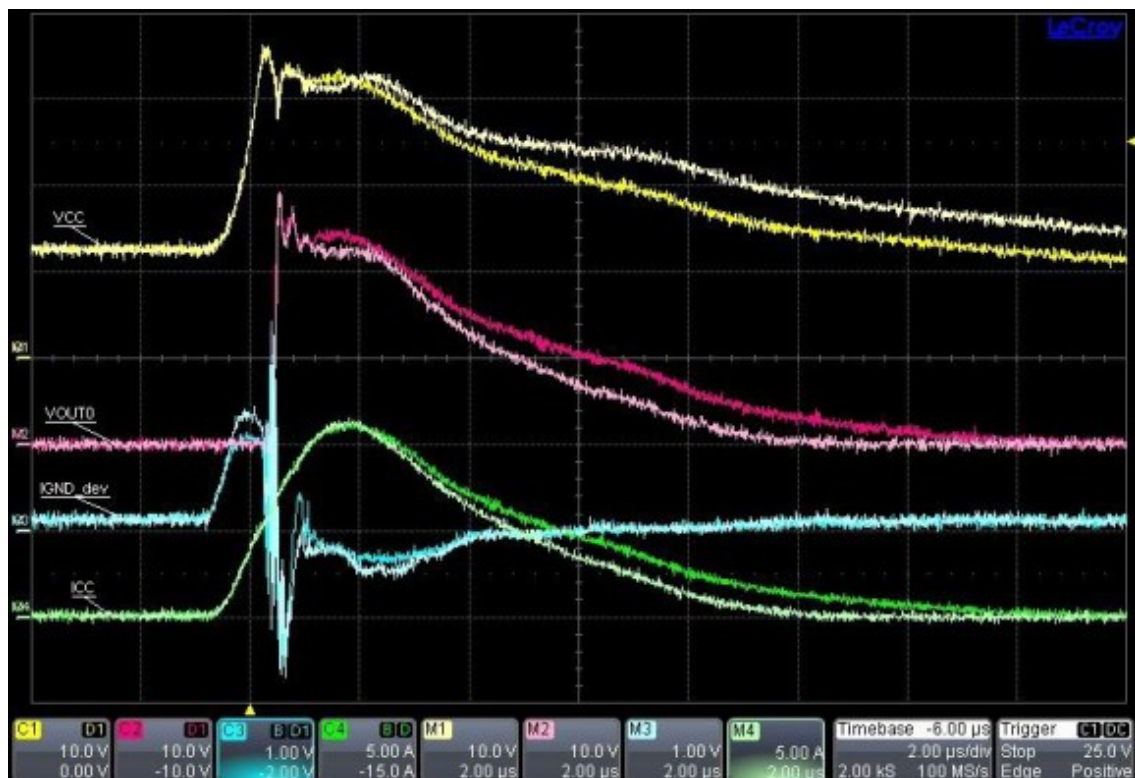
Test pulse 2a

DUT configuration: Applicative **OFF STATE**, pulse on VCC pin

Generator configuration: $T_r = 1 \mu s$ / $T_d = 50 \mu s$ / $T_1 = 0.5 \text{ sec}$ / $T_2 = 0 \text{ ms}$ / $R_i = 2 \Omega$ / 500 pulses

Test results: **PASS level III: +55 V / 500 pulses**

Figure 10. Test pulse 2a



3.3.3

Test pulse 3a

DUT configuration: Applicative **OFF STATE**, pulse on VCC pin

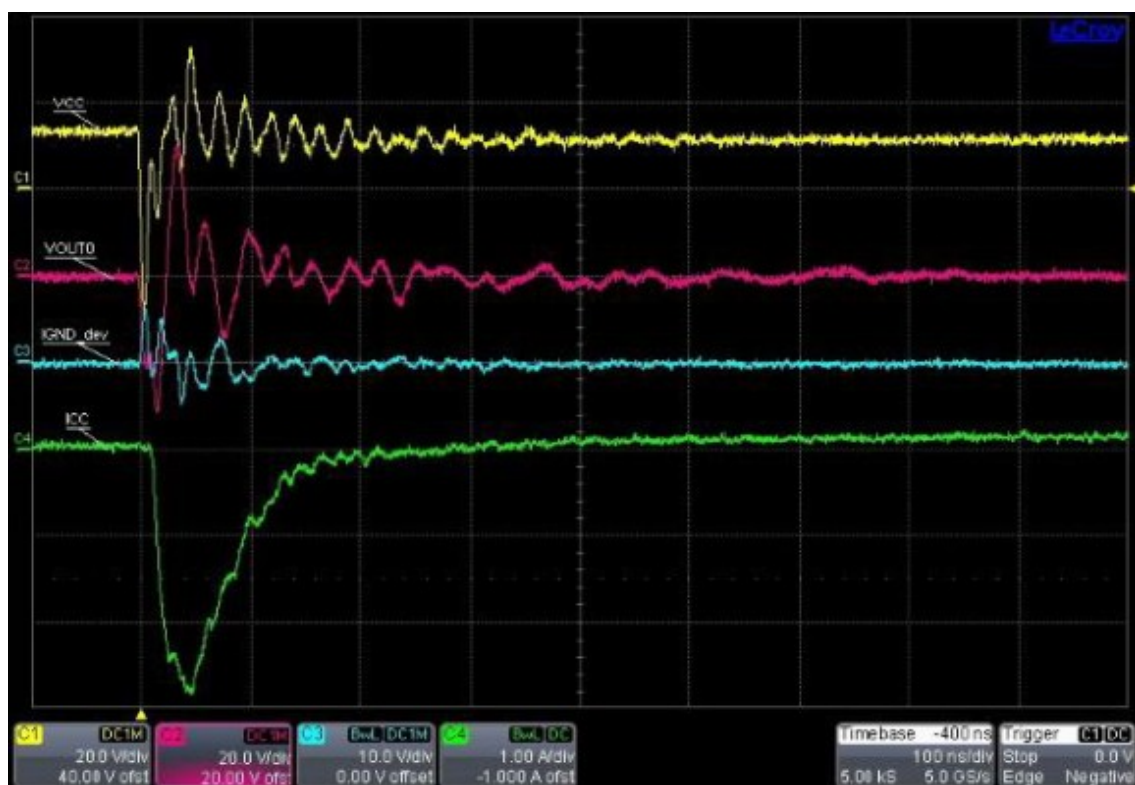
Generator configuration: $F = 1 \text{ kHz}$ ($t_1 = 100 \mu\text{s}$)/ $T_4 = 10 \text{ ms}$ / $T_5 = 90 \text{ ms}$ / $V_{\text{PULSE}} = -220 \text{ V}$ / 1

Test results: **PASS level IV (-220V/1h)**

Figure 11. Test pulse 3a (burst)



Figure 12. Test pulse 3a (zoom)



3.3.4

Test pulse 3b

DUT configuration: Applicative **OFF STATE**, pulse on VCC pin

Generator configuration: $F = 10 \text{ kHz}$ ($t_1 = 100 \mu\text{s}$)/ $T_4 = 10 \text{ ms}$ / $T_5 = 90 \text{ ms}$ /VPULSE = +150 V / 1 h
Test results: **PASS level IV (+150V/1h)**

Figure 13. Test pulse 3b (burst)

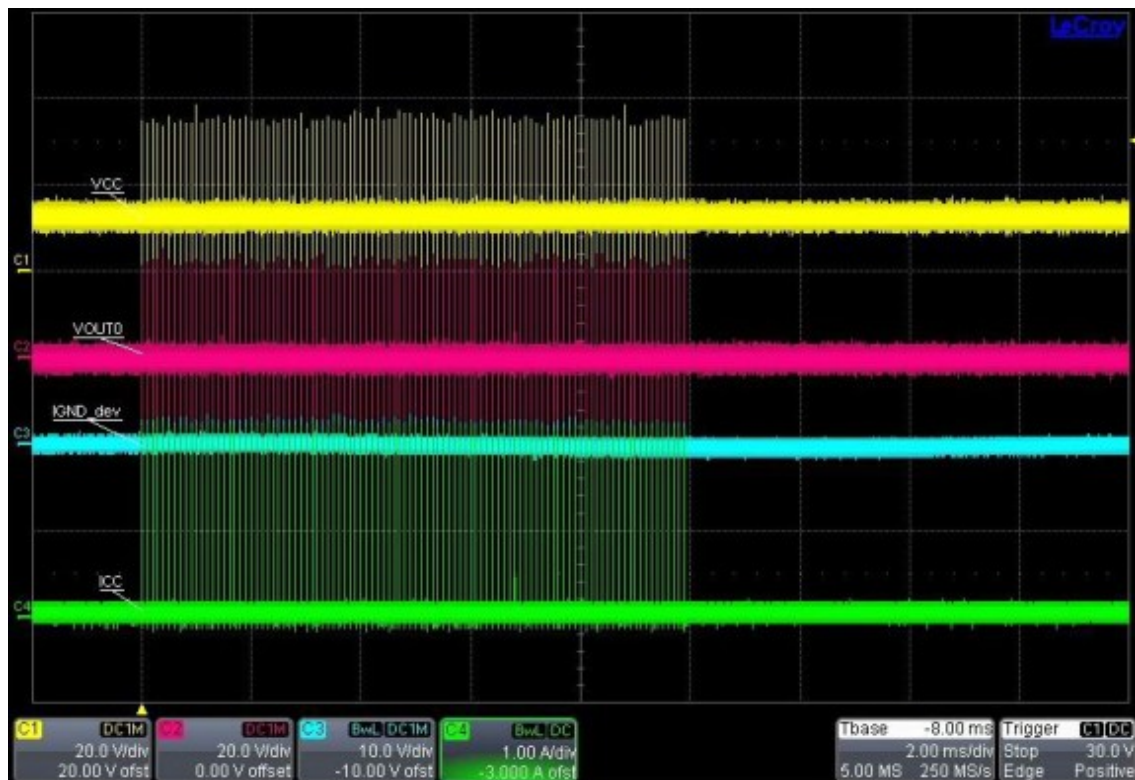
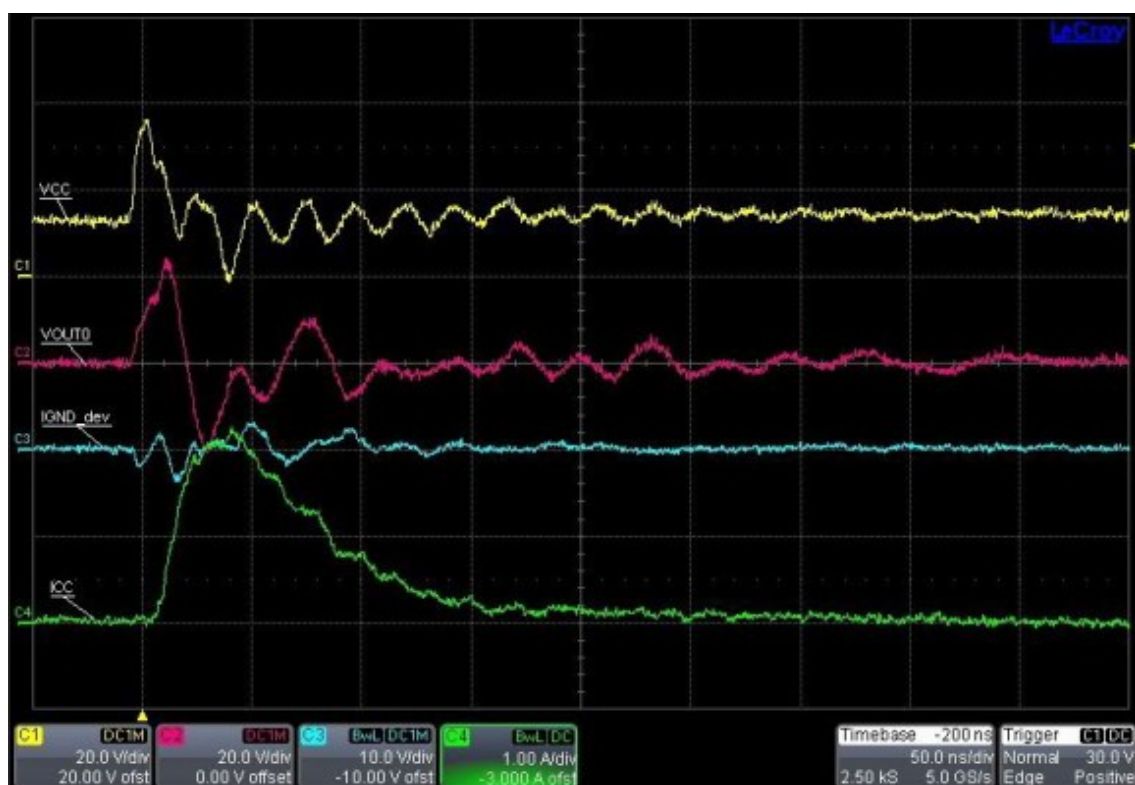


Figure 14. Test pulse 3b (zoom)



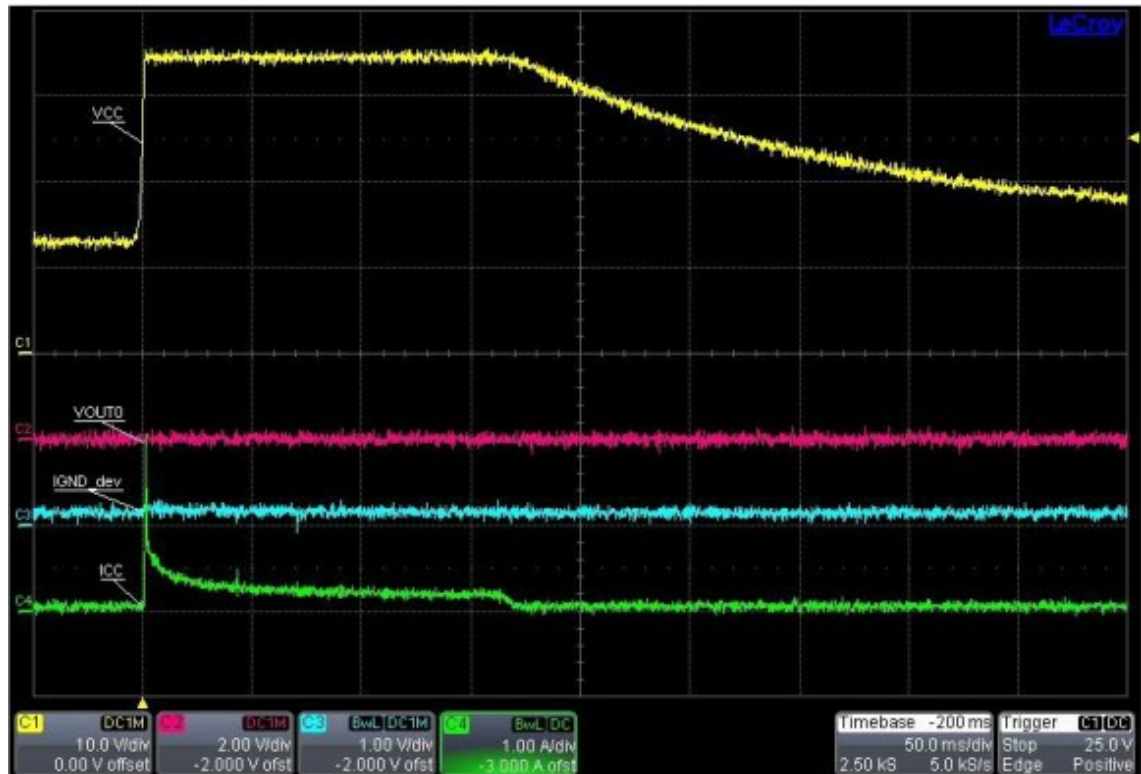
3.3.5 Test B (load dump) as per ISO 16750-2:2010

DUT configuration: Applicative **OFF STATE**, pulse on VCC pin

Generator configuration: $R_i = 2 \Omega$, $t_r = 5 \text{ ms}$, $t_d = 400 \text{ ms}$, $T_1 = 60 \text{ s}$ (interval).

Test result: **PASS** $V_{PULSE} = +87 \text{ V}$, $V_{CLAMP} = +35 \text{ V V}$, 5 pulses

Figure 15. Test B (load dump)

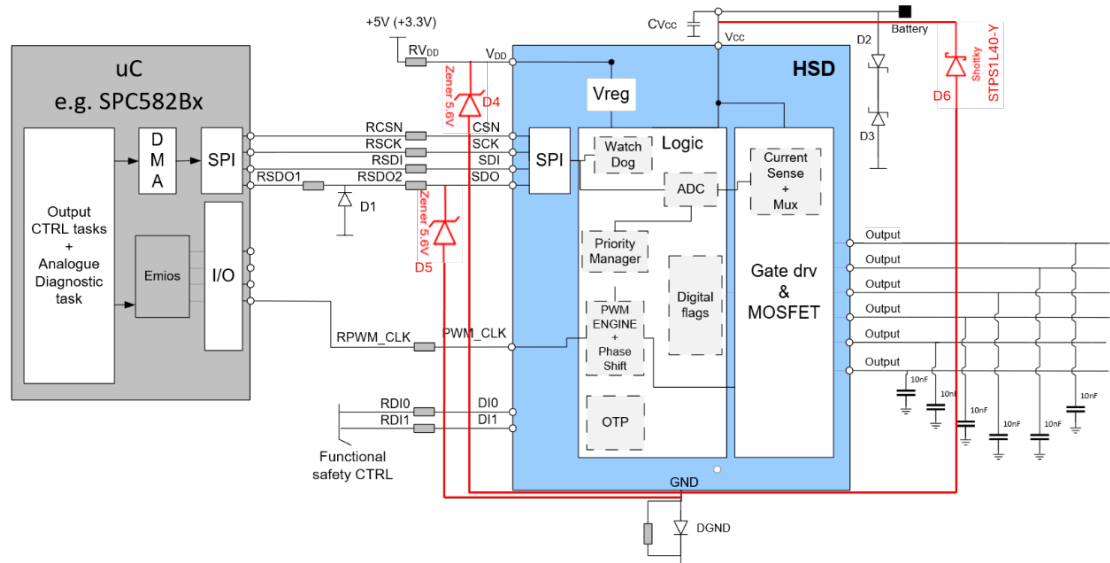


3.3.6 RAM register preservation during negative battery voltage transient

- D4, zener 5.6 V between VDD and GND_DEV;
- D5, zener 5.6 V between SDO and GND_DEV;
- D6, Schottky STPS1L40-Y between VCC and GND_DEV pin to avoid the internal vertical NPN structure of the power MOSFET being triggered during ISO pulse1. In fact the typical V_F of STPS1L40-Y is 0.37 V. This diode V_F must be sufficiently lower than the value of parasitic activation, guaranteeing robust protection to the negative ISO, avoiding latch-up.

The rest of the BOM is the same as in Table 1.

Figure 16. Recommended schematic for SPI registers data preservation



As written before, the purpose of inserting the mentioned diodes is to avoid triggering some intrinsic parasitic structures that would cause excessive current flow across RVDD, bringing to an undesired device logic reset. The following oscilloscope captures show a Pulse 1 test setup according to ISO 7637-2:2011 applied on VND5D20F as DUT.

In the applied setup we assumed that only the VCC device supply is subjected to Pulse 1, while the MCU and VDD device pin will remain supplied by a permanent 3.3 V or 5 V LDO.

We can observe that the oscilloscope M3 trace, representing the difference between VDD and GND_{DEVICE} , is kept always above the POR voltage level ($POR < 2.7 V$).

In this condition, being $VDD - GND_{DEV}$ always $> VPOR$, the RAM content is preserved.

Figure 17. ISO 7637-2 pulse 1 (zoomed view)

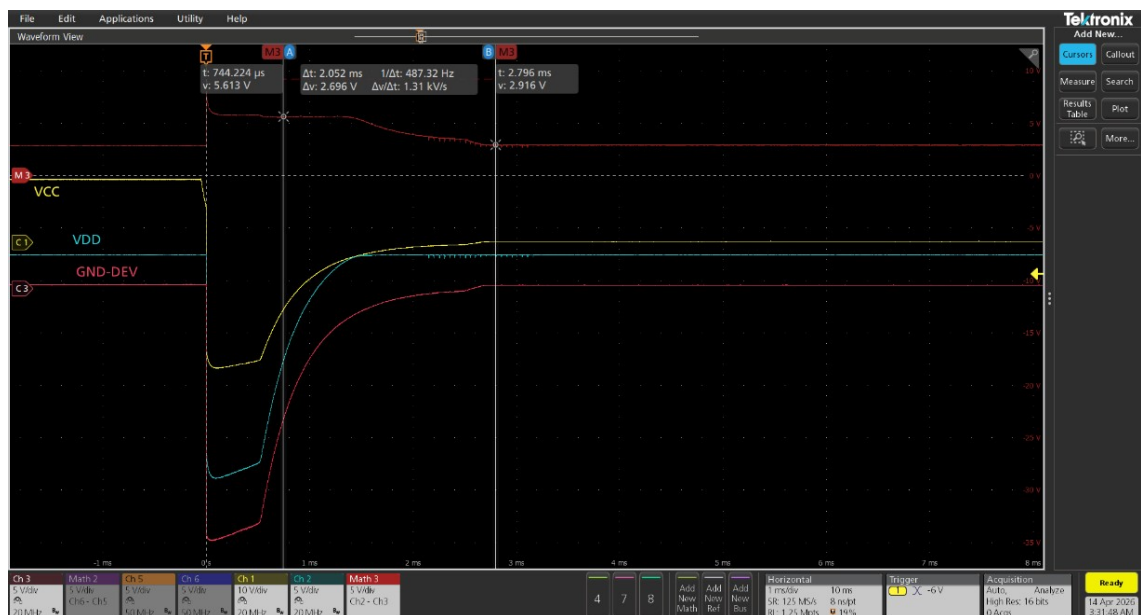
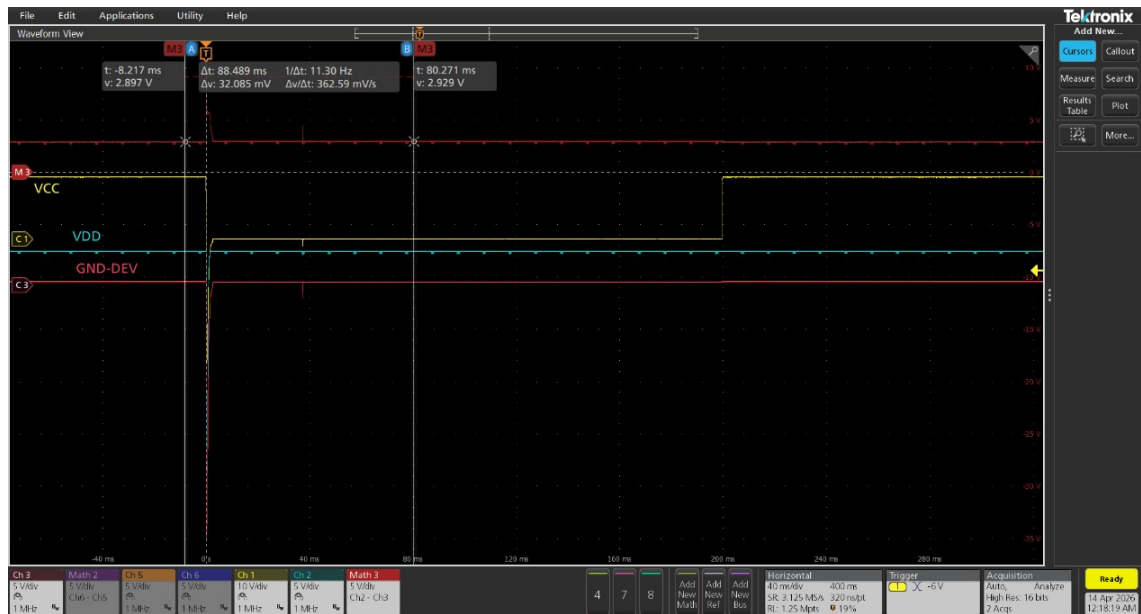


Figure 18. ISO 7637-2 pulse 1 (complete pulse)



4 OTP programming circuit for M0-9 SPI

OTP (one-time programmable) is a type of nonvolatile memory that can be programmed only once and cannot be modified later. This means that once a '1' has been written into the OTP memory, it cannot be erased.

In an integrated circuit, data is usually processed by a series of functional blocks. Each of them has one or more inputs and one or more outputs. With DIAO (Direct input assignment to output) technology, through OTP, it is possible to program the OTP memory to directly associate an input with a specific output without the need of an intermediate functional block. This approach offers several advantages to end customers such as:

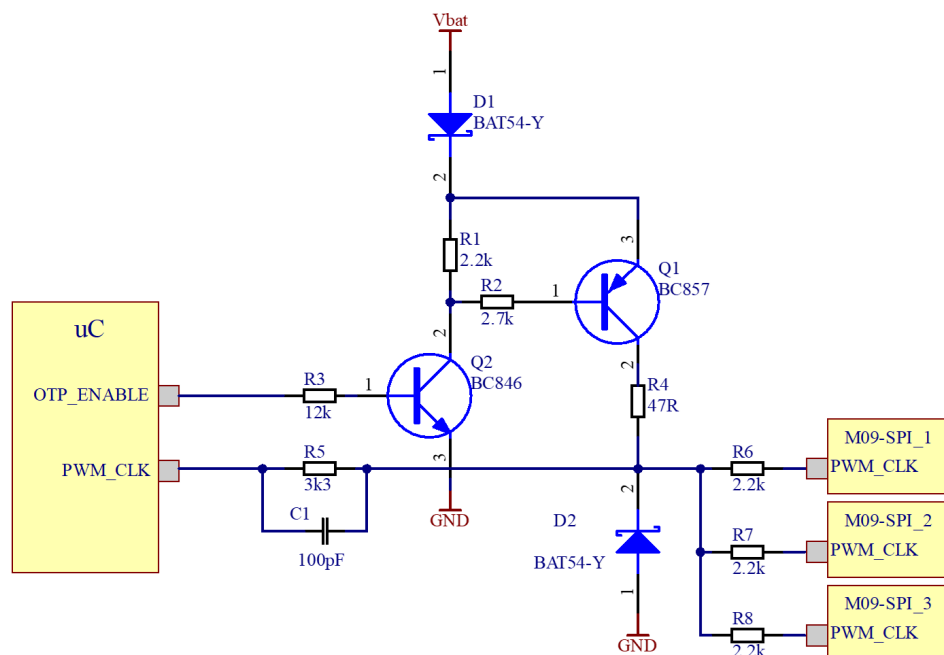
- The possibility to use the same device in different configurations.
- To reduce the number of MCU I/Os dedicated to parallel commands.
- To define the appropriate strategy for fail-safe operation.

Furthermore, it reduces the number of functional blocks required to process data, simplifying the design of the integrated circuit, and reducing power consumption. The direct input assignment to output through OTP is achievable by setting two dedicated bits per channel in the OTP memory map documented in the product datasheets, in the OTP programming chapter. For more details, refer to UM3268 (OTP programming for M0-9 SPI devices).

Note:

The schematic in Figure 19, unlike the schematic in UM3268, considers the reverse polarity requirement.

Figure 19. Proposed OTP programming circuit schematic



Circuit description:

During the programming phase the PWM_CLK pin of the device shall be set to 10 V. To achieve this, set the OTP_ENABLE signal of the microcontroller high. Due to the 2.2 k Ω resistor, the PWM_CLK pin voltage of each device is clamped to its typical value of approximately 10.9 V. The 2.2 k Ω resistors before the PWM_CLK pin limit the current to remain below the maximum value for the AMR pin.

- D1 allows to block the reverse current path that would be created during the reverse battery.
- D2 diode and 2.2 k Ω (R6, R7, R8) R_{PROT} resistor, allow to ensure the necessary bias current path for each device to activate the reverse turn-on function during the reverse battery, when the device is provided with the function.
- R5=3.3 k Ω limits the current on MCU pin during the programming phase below AMR.
- C1=100 pF speed-up capacitor ensures the necessary signal amplitude PWM_CLK (up to 600 kHz).

Table 5. OTP programming circuit bill of materials

Quantity	Comment	Designator	Footprint
1	BAT54-Y	D1, D2	SOT-23
1	BC857	Q1	SOT-23
1	BC846	Q2	SOT-23
4	2.2 k	R1, R6, R7, R8	0805_R
1	2.7 k	R2	0805_R
1	12 k	R3	0805_R
1	47 R	R4	0805_R
1	3.3 k	R5	0805_R
1	100 pF	C1	0805_C

Circuit characteristic:

- Static total consumption 32 mA at Vbat=18 V with enabled high with 3 devices (as in the schematic)
- PWM_CLK pin current= 0.85 mA
- AMR of PWM_CLK pin guaranteed up to Vcc=18.4 V (2.9 mA)
- Pin clamp voltage 10.9 V
- Max frequency = 600 kHz
- Negligible standby consumption (with OTP_Enable Low)

5 Multiple M0-9 SPI sharing the same SPI bus

This argument is specifically treated in the application note AN6476.

Revision history

Table 6. Document revision history

Date	Version	Changes
08-Oct-2026	1	Initial release.

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