Low-voltage high-current inverter motor board

Introduction

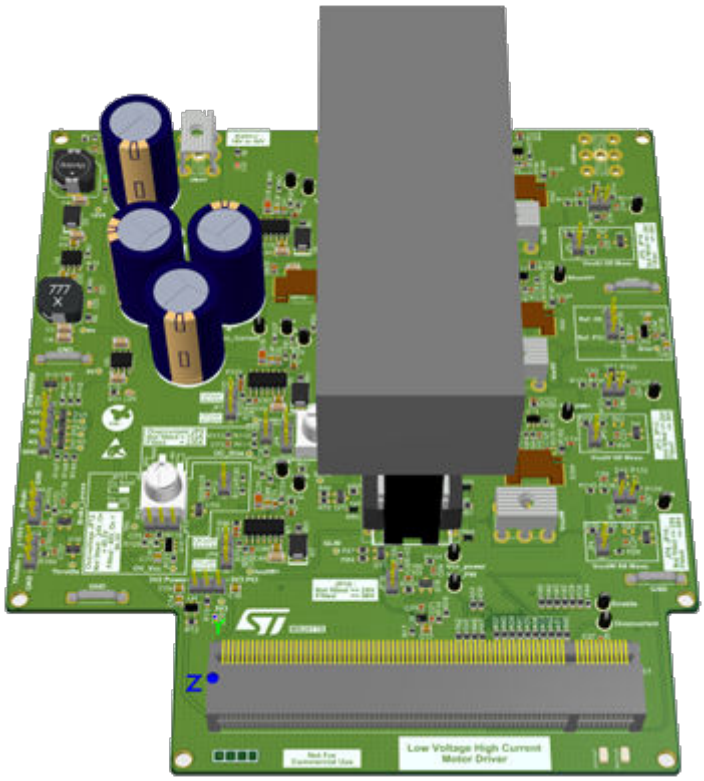
This STDES-LVHP01 reference design is a power board dedicated to driving a three-phase motor with different possible sensorless strategies:

- FOC (ZeST) with three shunts
- FOC single shunt
- Six steps

The main characteristics of this board are:

- Input voltage (battery) from 18 V up to 48 V
- Output current per phase up to 50 A rms continuous (refer to temperature limitations section)
- PWM frequency from 10 kHz up to 70 kHz (refer to temperature limitations section)
- Hardware dead time set at 250 ns
- Hardware overcurrent protection and built-in overvoltage detection
- This board must be coupled with a dedicated ZeST Discovery board controller (B-G473E-ZEST1S) through the PCI port.

Figure 1. 3D view of low-voltage high-current inverter motor board



STM32 ZeST

1 Features

- Input voltage (battery) from 18 V up to 48 V
- Output current per phase up to 50 A rms continuous (refer to temperature limitations section)
- PWM frequency from 10 kHz up to 70 kHz (refer to temperature limitations section)
- Hardware dead time set at 250 ns
- Hardware overcurrent protection fixed at 152 A or 236 A. A lower overcurrent value is possible through an onboard variable resistance.
- Overvoltage detection fixed at 48 V or 96 V. A lower overvoltage value is possible through an onboard variable resistance.
- This board must be coupled to a dedicated ZeST Discovery board controller through the PCI port. Refer to B-G473E-ZEST1S.

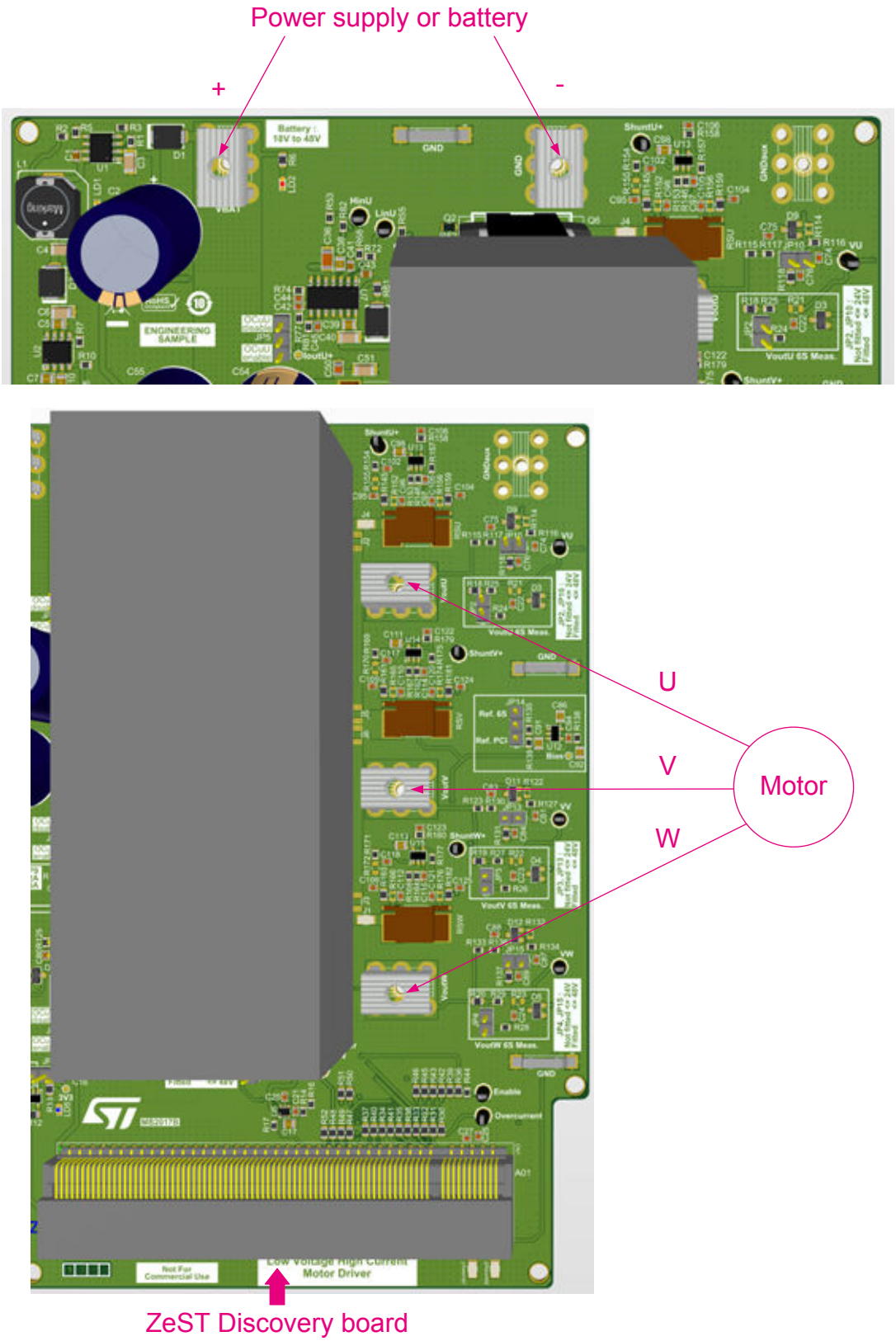
Figure 2. ZeST Discovery board controller

- Possible sensor-less strategies:
  - FOC 3 x shunts with integrated OPAMP in MCU for current sensing
  - FOC 3 x shunts with external OPAMP for current sensing
  - FOC single shunt with integrated OPAMP in MCU for current sensing
  - FOC single shunt with external OPAMP for current sensing
  - Six steps with single shunt and integrated amplifier in MCU for current sensing
  - Six steps with single shunt and external amplifier (pregain) for current sensing

2 Quick setup

2.1 Connections

Figure 3. **Power supply (battery) and motor wiring connection**



DT77224V1

2.2 Jumper configuration

Power supplies

The power board provides a +5 V power supply to the ZeST Discovery board through the PCI connector.
The 3.3 V power supply for analog features can be provided in two ways:

- 3.3 V is derived from 5 V present on the power board.
- 3.3 V is provided by the Discovery board through the PCI connector.

A jumper must be placed in position JP1 depending on the option selected (refer to Figure 4):

- For 3.3 V on-board, place the jumper on the left side (red rectangle).
- For 3.3 V coming from the Discovery board, place the jumper on the right side (blue rectangle).

Note: By default, use the 3.3 V provided on-board.

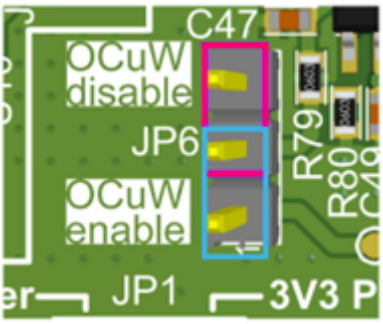
Figure 4. 3.3 V jumper setting

Overcurrent

To set the hardware overcurrent ON or OFF for OCux (x = U, W, V), use respectively JP5, JP6, and JP7.
The example shown in Figure 5 illustrates the JP6 settings for OCuW:

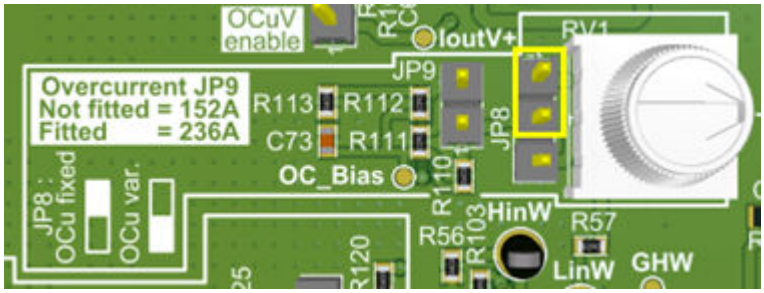
- To enable overcurrent protection for OCuW, place the jumper in the position of the blue rectangle.
- To disable overcurrent protection for OCuW, place the jumper in the position of the red rectangle.

Figure 5. Onboard overcurrent jumper setting



The default configuration with JP9 is left OFF and a jumper on JP8 in the position illustrated by the yellow rectangle gives an overcurrent threshold value of 152 A.

Figure 6. Overcurrent threshold jumper setting



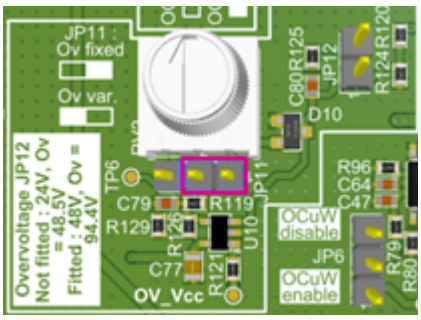
Overvoltage

Placing a jumper on JP11 in the position illustrated by the red rectangle (refer to Figure 7) gives a fixed overvoltage value.

For JP12:

- If the power supply (battery) is lower or equal to 24 V, let JP12 OFF and the overvoltage threshold value to 48.5 V.
- If the power supply (battery) is higher or equal to 24 V and lower or equal to 48 V, set JP12 ON and the overvoltage threshold value to 94.4 V.

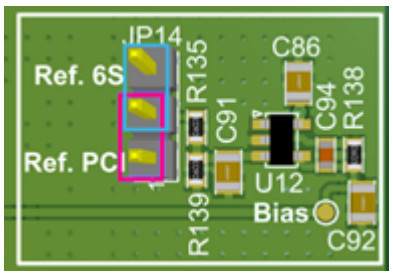
Figure 7. Overvoltage threshold jumper setting



If the power stage is configured (refer to Figure 8):

- FOC mode → Place a jumper on JP14 between Ref. PCI and the center pin (red rectangle).
- 6-step mode → Place a jumper on JP14 between Ref. 6S and the center pin (blue rectangle).

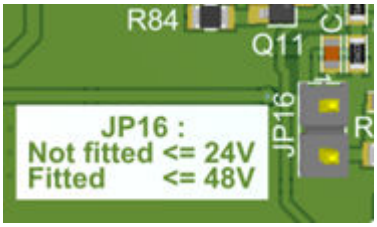
Figure 8. Onboard bias voltage jumper setting



For power supply voltage (battery) sensing, JP16 must be configured as follows (refer to Figure 9):

- If the power supply (battery) is ≤ 24 V, let JP16 OFF.
- If the power supply (battery) is ≥ 24 V and ≤ 48 V, set JP16 ON.

Figure 9. Power supply (battery) sensing jumper setting



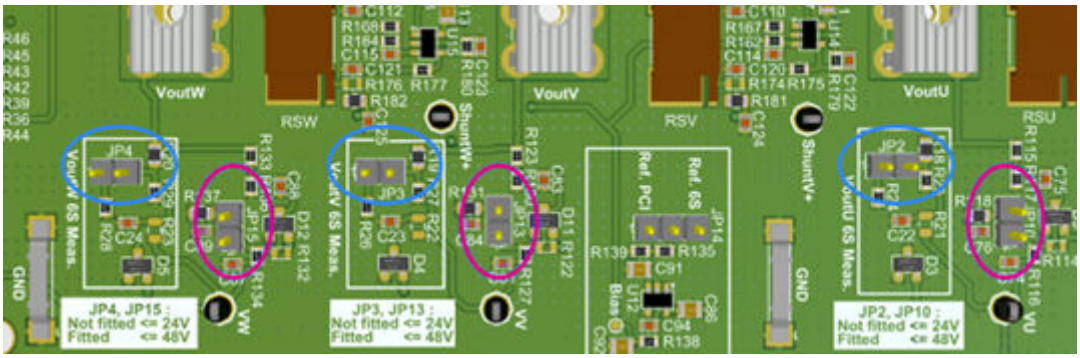
If the power stage is configured (refer to Figure 10):

- FOC mode
  - If the power supply (battery) is ≤ 24 V, let JP10, JP13, and JP15 OFF.
  - If the power supply (battery) is ≥ 24 V and ≤ 48 V, set JP10, JP13, and JP15 ON.

Warning: *Even if they are relevant to the 6-step mode, to avoid any potential failure on 3.3 V LDO when the power supply is above 28 V, close JP2, JP3, and JP4. However, if 6-step mode is not used, R18, R19, and R20 can be removed safely.*

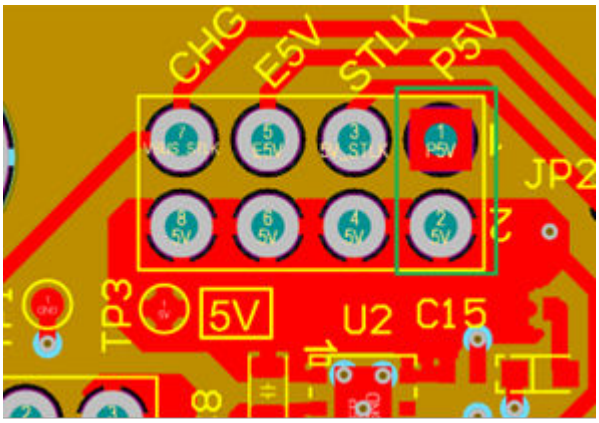
- 6-step mode (JP10, JP13, and JP15 are not relevant)
  - If the power supply (battery) is ≤ 24 V, let JP2, JP3, and JP4 OFF.
  - If the power supply (battery) is ≥ 24 V and ≤ 48 V, set JP2, JP3, and JP4 ON.

Figure 10. Phase motor voltage sensing jumper setting



Verify on JP2 (ZeST Discovery board) that only P5V is populated (refer to the green rectangle in Figure 11)

Figure 11. ZeST Discovery board JP2 configuration



2.3 FOC with three shunts and internal MCU OPAMPs for current sensing

The following table shows how to set the power board for this configuration.

Table 1. Components configuration for FOC with three shunts and internal MCU OPAMPs

Components	ON	OFF
J1, J4 C74, C81, C87, C95, C104, C108, C109, C124, C125 R116, R127, R134, R145, R159, R161, R163, R181, R182	X	-
J2, J3, J5, J6 R21, R22, R23, R114, R122, R132, R152, R155, R156, R165, R166, R170, R172, R174, R176	-	X

On the ZeST Discovery board:

- By default, the board is configured for this mode.
- Make sure that:
  - SB75, SB76, and SB81 are ON while SB73, SB77, and SB80 are OFF for phase voltage measurement (refer to Figure 12).
  - SB11, SB22, SB32, SB35, SB38, and SB39 are ON, while SB21, SB31, and SB37 are OFF for shunt current measurement (refer to Figure 13).

Figure 12. Bottom layer ZeST Discovery board solder ball setting

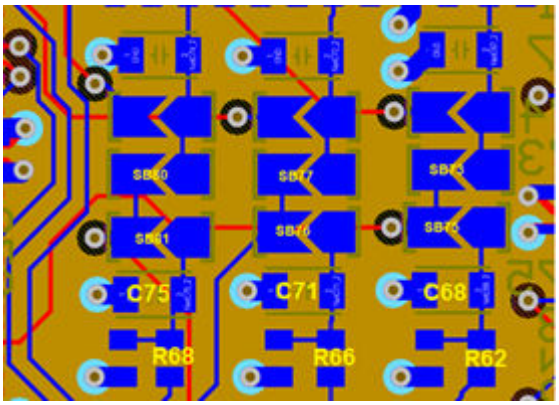
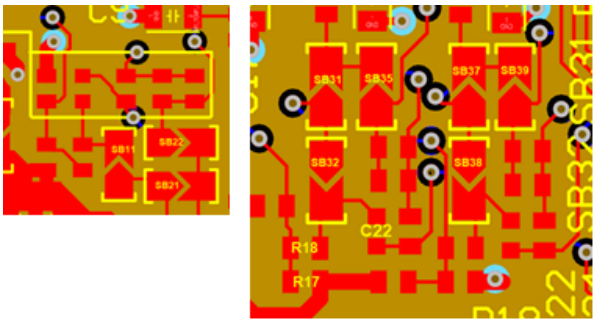


Figure 13. Top layer ZeST Discovery board ball setting



2.4 FOC with three shunts and external OPAMPs for current sensing

The following table shows how to set the power board for this configuration.

Table 2. Components configuration for FOC with three shunts and external OPAMPs

Components	ON	OFF
J1, J4 C74, C81, C87 R116, R127, R134, R145, R159, R161, R163, R181, R182, R152, R155, R156, R165, R166, R170, R172, R174, R176	X	-
J2, J3, J5, J6 C95, C104, C108, C109, C124, C125 R21, R22, R23, R114, R122, R132, R145, R159, R161, R163, R181, R182	-	X

On the ZeST Discovery board:

- Modify the default configuration as:
  - No change: SB75, SB76, and SB81 are ON while SB73, SB77, and SB80 are OFF for phase voltage measurement (refer to Figure 14).
  - SB11, SB22, SB32, SB35, SB38, and SB39 are OFF and SB21, SB31, and SB37 are ON for shunt current measurement (refer to Figure 15).

Figure 14. **Bottom layer ZeST Discovery board solder ball setting**

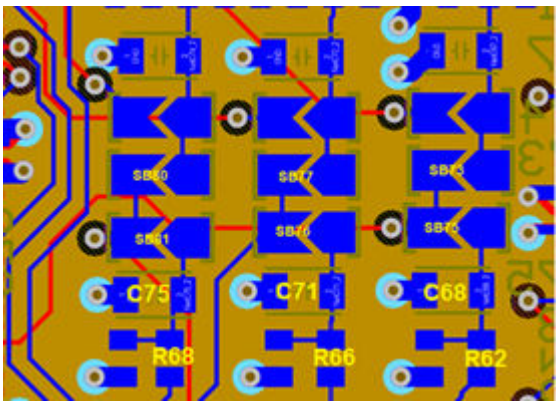
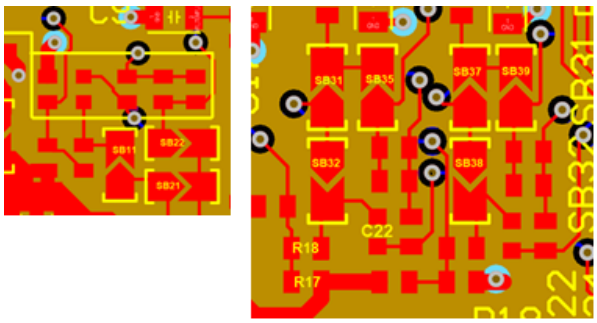


Figure 15. **Top layer ZeST Discovery board solder ball setting**



2.5 Six steps and internal PGA for current regulation

The following table shows how to set the power board for this configuration.

Table 3. **Components configuration for six steps and internal MCU PGA**

Components	ON	OFF
J2, J3, J5, J6 C95, C104, C108, C125 R21, R22, R23, R152, R156, R161, R165, R166, R174, R176	X	-
J1, J4 C74, C81, C87, C109, C124 R114, R116, R122, R127, R132, R134, R145, R155, R159, R163, R170, R172, R181, R182	-	X

On the ZeST Discovery board:

- Modify the default configuration as:
  - SB75, SB76, and SB81 are ON while SB73, SB77, and SB80 are OFF for phase voltage measurement. In case of need, C68, C71, C75, R62, R66, and R68 are on the bottom layer (refer to Figure 16).
  - SB11, SB21, SB22, SB31, SB35, SB37, SB38, and SB39 are OFF and SB32 is ON for shunt current measurement. Remove R17 (refer to Figure 17).

Figure 16. **Bottom layer ZeST Discovery board solder ball setting**

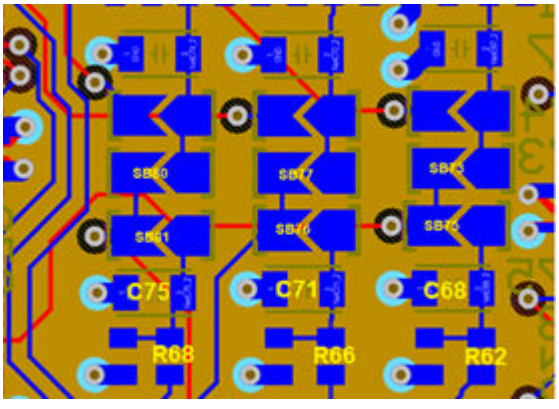
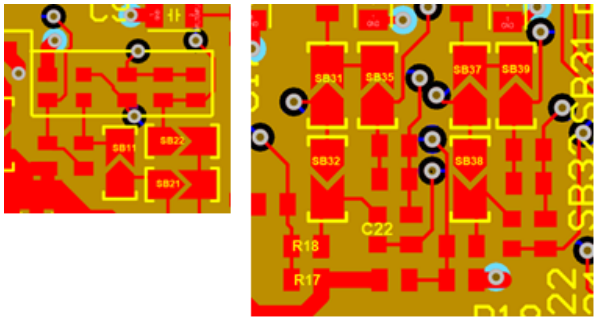


Figure 17. **Top layer ZeST Discovery board solder ball setting**



2.6 Six steps and an external amplifier for current regulation

The following table shows how to set the power board for this configuration.

Table 4. Components configuration for six steps and an external amplifier

Components	ON	OFF
J2, J3, J5, J6 C95, C104, C108, C125 R21, R22, R23, R152, R156, R165, R166, R170, R174, R176	X	-
J1, J4 C74, C81, C87, C109, C124 R114, R116, R122, R127, R132, R134, R145, R155, R159, R161, R163, R172, R181, R182	-	X

On the ZeST Discovery board:

- Modify the default configuration as:
  - SB75, SB76, and SB81 are ON while SB73, SB77, and SB80 are OFF for phase voltage measurement. In case of need, C68, C71, C75, R62, R66, and R68 are on the bottom layer (refer to Figure 18).
  - SB11, SB21, SB22, SB31, SB35, SB37, SB38, and SB39 are OFF and SB32 is ON for shunt current measurement. Remove R17 (refer to Figure 19).

Figure 18. Bottom layer ZeST Discovery board solder ball setting

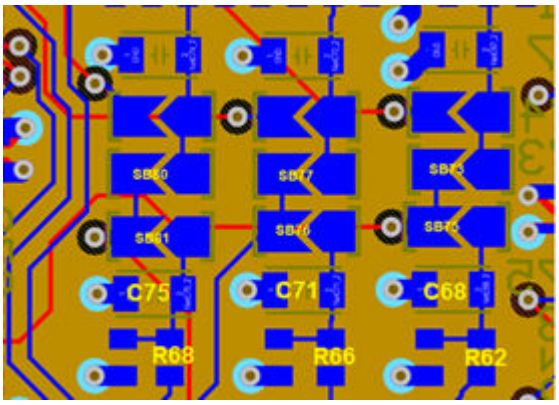
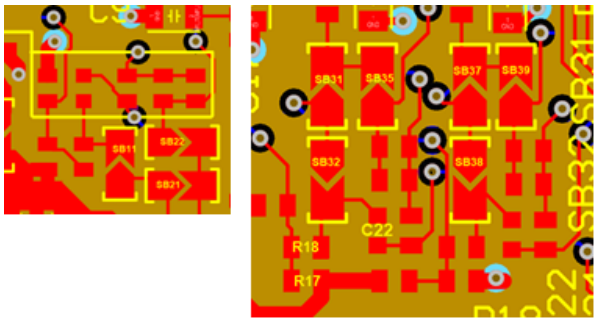


Figure 19. Top layer ZeST Discovery board solder ball setting



2.7 FOC with one shunt and internal MCU OPAMPs for current sensing

The following table shows how to set the power board for this configuration.

Table 5. Components configuration for FOC with one shunt and internal MCU OPAMPs

Components	ON	OFF
J2, J3, J5, J6 C74, C81, C87, C95, C104, C108, C109, C124, C125 R116, R127, R134, R152, R156, R161, R166, R176, R181	X	-
J1, J4 R21, R22, R23, R114, R122 R132, R145, R155, R159, R163, R165, R170, R172, R174, R182	-	X

On the ZeST Discovery board:

- By default, the board out of the box can be used for this mode.
- Make sure that:
  - SB75, SB76, and SB81 are ON while SB73, SB77, and SB80 are OFF for phase voltage measurement (refer to Figure 20).
  - SB11, SB22, SB32, SB35, SB38, and SB39 are ON while SB21, SB31, and SB37 are OFF for shunt current measurement (refer to Figure 21).

Figure 20. Bottom layer ZeST Discovery board solder ball setting

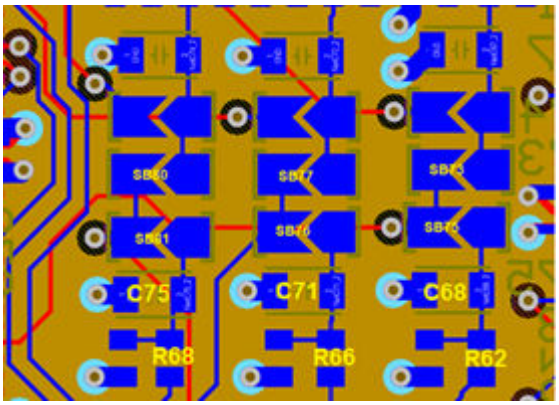
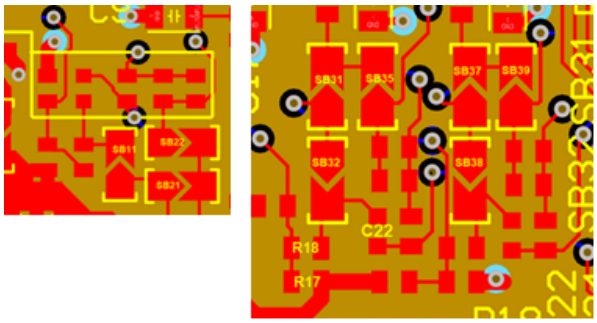


Figure 21. Top layer ZeST Discovery board solder ball setting



2.8 FOC with one shunt and external OPAMPs for current sensing

The following table shows how to set the power board for this configuration.

Table 6. Components configuration for FOC with one shunt and external OPAMPs

Components	ON	OFF
J2, J3, J5, J6 C74, C81, C87 R116, R127, R134, R152, R156, R165, R166, R170, R174, R176	X	-
J1, J4 C95, C104, C108, C109, C124, C125 R21, R22, R23, R114, R122, R132, R145, R155, R159, R161, R163, R172, R181, R182	-	X

On the ZeST Discovery board:

- Modify the default configuration as:
  - No change: SB75, SB76, and SB81 are ON while SB73, SB77, and SB80 are OFF for phase voltage measurement (refer to Figure 22).
  - SB11, SB22, SB32, SB35, SB38, and SB39 are OFF and SB21, SB31, and SB37 are ON for shunt current measurement (refer to Figure 23).

Figure 22. Bottom layer ZeST Discovery board solder ball setting

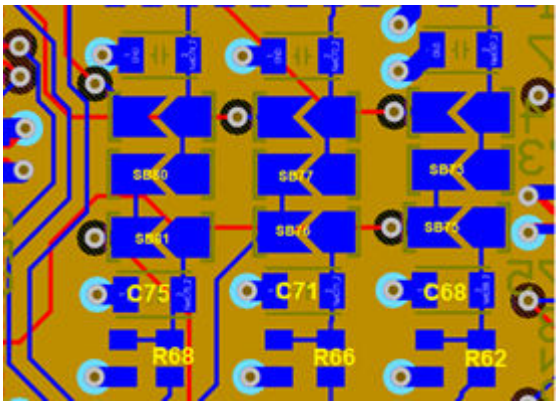
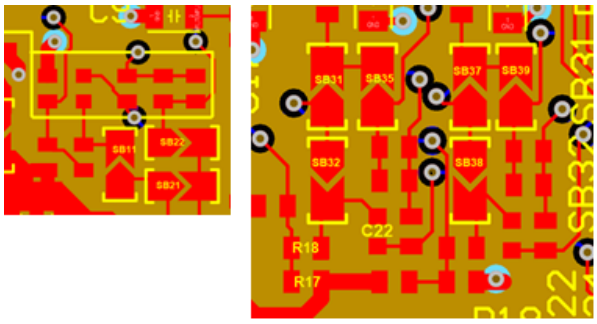


Figure 23. Top layer ZeST Discovery board solder ball setting



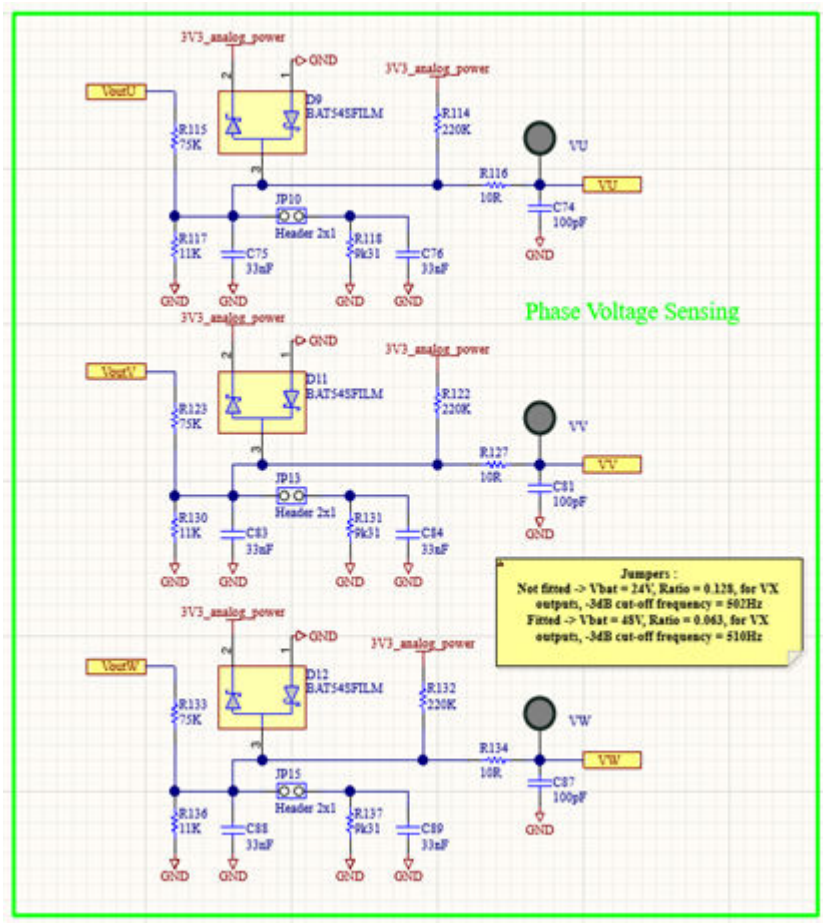
3 Feature explanations

3.1 Voltage sense

3.1.1 Phase voltage sense schematic (FOC mode)

The three phases have the same schematic. R114, R122, and R132 are OFF. These resistors add a slight offset if necessary (refer to Section 3.7: Utility of R114, R122, and R132).

Figure 24. Phase voltage sensing schematic in FOC mode



Take U phase output for example:

When JP10 is OFF (24 V mode)

$VU = VoutU\frac{R117}{R115 + R117} = 0.1279 \times VoutU$, when VoutU = 24 V, VU = 3.07 V

C75 acts as a first-order low-pass filter with -3 dB cutoff frequency.

$F_{-3dB} = \frac{1}{2\pi \times Rint \times C75}$ with $Rint = \frac{R115 \times R117}{R115 + R117}$ gives 502 Hz

When JP10 is ON (48 V mode)

$VU = VoutU\frac{\frac{R117 \times R118}{R117 + R118}}{R115 + \frac{R117 \times R118}{R117 + R118}} = 0.06299 \times VoutU$, when VoutU = 48 V, VU = 3.023 V

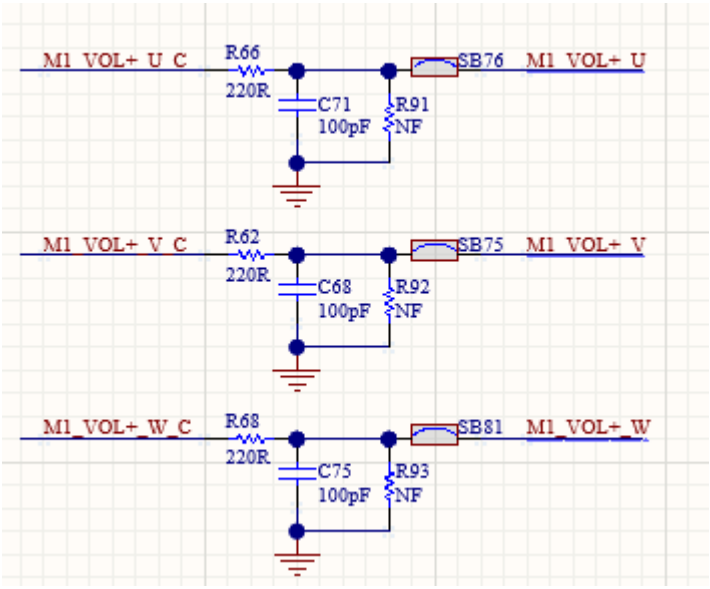
C75+C76 acts as a first-order low-pass filter with -3 dB cutoff frequency:

$$F_{-3dB} = \frac{1}{2\pi \times Rint2 \times (C75 + C76)} \text{ with } Rint2 = \frac{R115 \times \frac{R117 \times R118}{R117 + R118}}{R115 + \frac{R117 \times R118}{R117 + R118}} \text{ gives 510 Hz.}$$

Of course, one can use the 48 V mode with 24 V, but the opposite is impossible.

3.1.2 Schematic on the ZeST Discovery board (FOC mode)

Figure 25. Phase voltage sensing schematic on the ZeST Discovery board



With VU = M1_VOL+_U_C, VV = M1_VOL+_V_C, VW = M1_VOL+_W_C. M1_VOL+_U/V/W are connected to MCU ADC inputs.

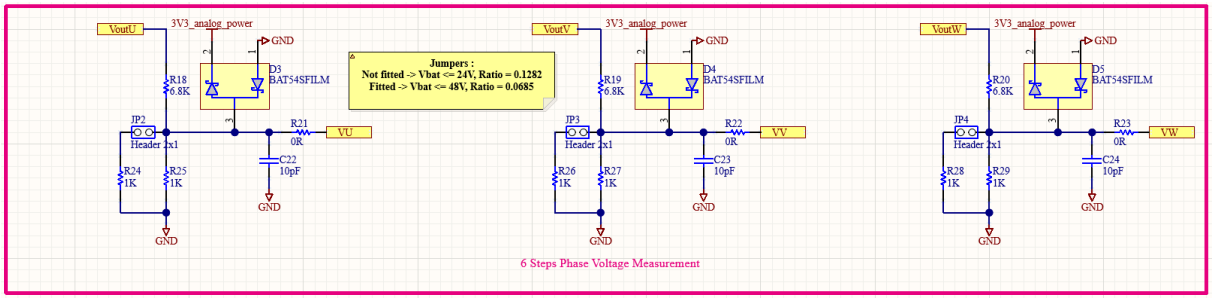
The first-order low-pass filter formed by R66(R62, R68) and C71(C68, C75) has a -3 dB cutoff frequency

$$fc = \frac{1}{2\pi \times R66 \times C71}$$

With R66 = 220 Ω and C71 = 100 pF, fc = 7.23 MHz. 7.23 MHz is very high for a motor control application, but C71 (C68, C75) acts as a kickback capacitor to counteract the effects of the ADC sampling capacitor.

3.1.3 Phase voltage sense schematic (six-step mode)

Figure 26. **Phase voltage sense schematic in six-step mode**



The three phases have the same schematic.

For example, for U phase output:

When JP2 is OFF (24 V mode)

$$VU = VoutU\frac{R25}{R18 + R25} = 0.1282 \times VoutU$$

When JP2 is ON (48 V mode)

$$VU = VoutU\frac{\frac{R24 \times R25}{R24 + R25}}{R18 + \frac{R24 \times R25}{R24 + R25}} = 0.0685 \times VoutU$$

Of course, one can use the 48 V mode with 24 V, but the opposite is impossible.

On the ZeST Discovery board, it is the same schematic as FOC mode with VU = M1_VOL+_U_C, VV = M1_VOL+_V_C, VW = M1_VOL+_W_C.

M1_VOL+_U/V/W are connected to MCU ADC inputs.

Looking at U phase, the worst constant time is with 24 V mode and is approximately:

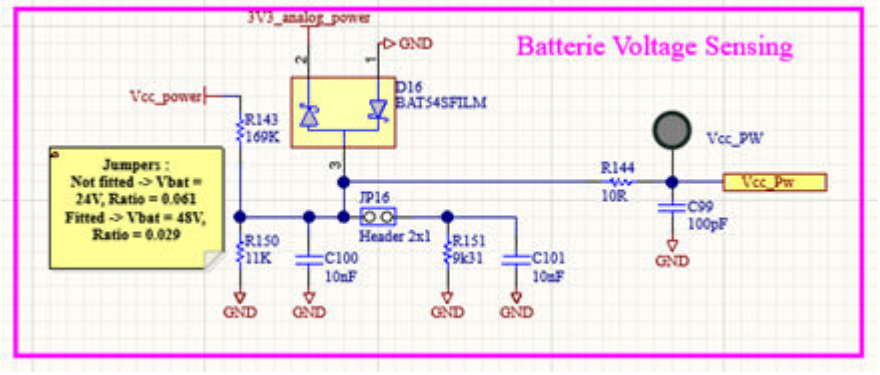
$$\tau = \left(\frac{R18 \times R25}{R18 + R25} + R66\right) \times C71 = 0.11\ \mu s$$

To get an idea of the rising/falling time, a first approximation consists of multiplying τ by 3. With the previous values, the rising/falling time is about 0.33 µs.

For many motors, a PWM frequency of about 20 kHz (so a period of 50 µs) is good enough. So, 3τ = 0.33 µs is less than 1% of 50 µs and this gives a good operating margin. If a higher PWM frequency is required, consider reducing the value of C71(C68, C75), but not below 22 pF.

3.1.4 Battery voltage sense schematic

Figure 27. **Power supply (battery) voltage sense schematic**



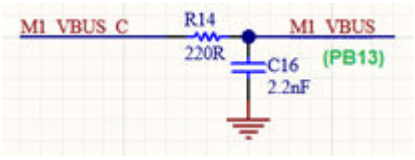
Vcc_power is the image of battery voltage. This voltage is first scaled to the ADC input range by:

- R143+R150 if JP16 is OFF.
- R143+R150//R151 if JP16 is ON.

Note: This signal is first-order low-pass filtered by C100 if JP16 is OFF and by C100+C101 if JP16 is ON.

Vcc_Pw is connected to the Discovery board through PCI connector M1_VBUS_C and then first-order low-pass filtered by R14 and C16 before entering ADC port PB13.

Figure 28. Power supply (battery) sensing schematic on the ZeST Discovery board



When JP16 is OFF (24 V mode)

$$Vcc\_Pw = Vcc\_power\frac{R143}{R143 + R150} = 0.061 \times Vcc\_power$$

- When Vcc_Power = 24 V, Vcc_Pw = 1.464 V
- When Vcc_Power = 48 V, Vcc_Pw = 2.928 V

$\mathrm{Re}\,q1 = \frac{R143 \times R150}{R143 + R150}$ and $\mathrm{d} = \frac{\mathrm{Re}\,q1 \times C100 + \mathrm{Re}\,q1 \times C16 + R14 \times C16}{2\sqrt{\mathrm{Re}\,q1 \times C100 \times R14 \times C16}}$ then

$\mathrm{fn} = \frac{1}{2\pi\sqrt{\mathrm{Re}\,q1 \times C100 \times R14 \times C16}}$

So:

$f_{-3dB} = fn \times \sqrt{1 - 2d^2 + \sqrt{4d^4 - 4d^2 + 2}}$, f_{-3dB} at PB13 = 1.36 kHz

When JP16 is ON (48 V mode)

$$Vcc\_Pw = Vcc\_power\frac{\frac{R150 \times R151}{R150 + R151}}{R143 + \frac{R150 \times R151}{R150 + R151}} = 0.029 \times Vcc\_Power$$

- When Vcc_Power = 48 V, Vcc_Pw = 1.392 V
- When Vcc_Power = 96 V, Vcc_Pw = 2.784 V

$\mathrm{Re}\,q2 = \frac{R143 \times \frac{R150 \times R151}{R150 + R151}}{R143 + \frac{R150 \times R151}{R150 + R151}}$ and $\mathrm{d} = \frac{\mathrm{Re}\,q2 \times (C100 + C101) + \mathrm{Re}\,q2 \times C16 + R14 \times C16}{2\sqrt{\mathrm{Re}\,q2 \times (C100 + C101) \times R14 \times C16}}$ then

$\mathrm{fn} = \frac{1}{2\pi\sqrt{\mathrm{Re}\,q2 \times (C100 + C101) \times R14 \times C16}}$

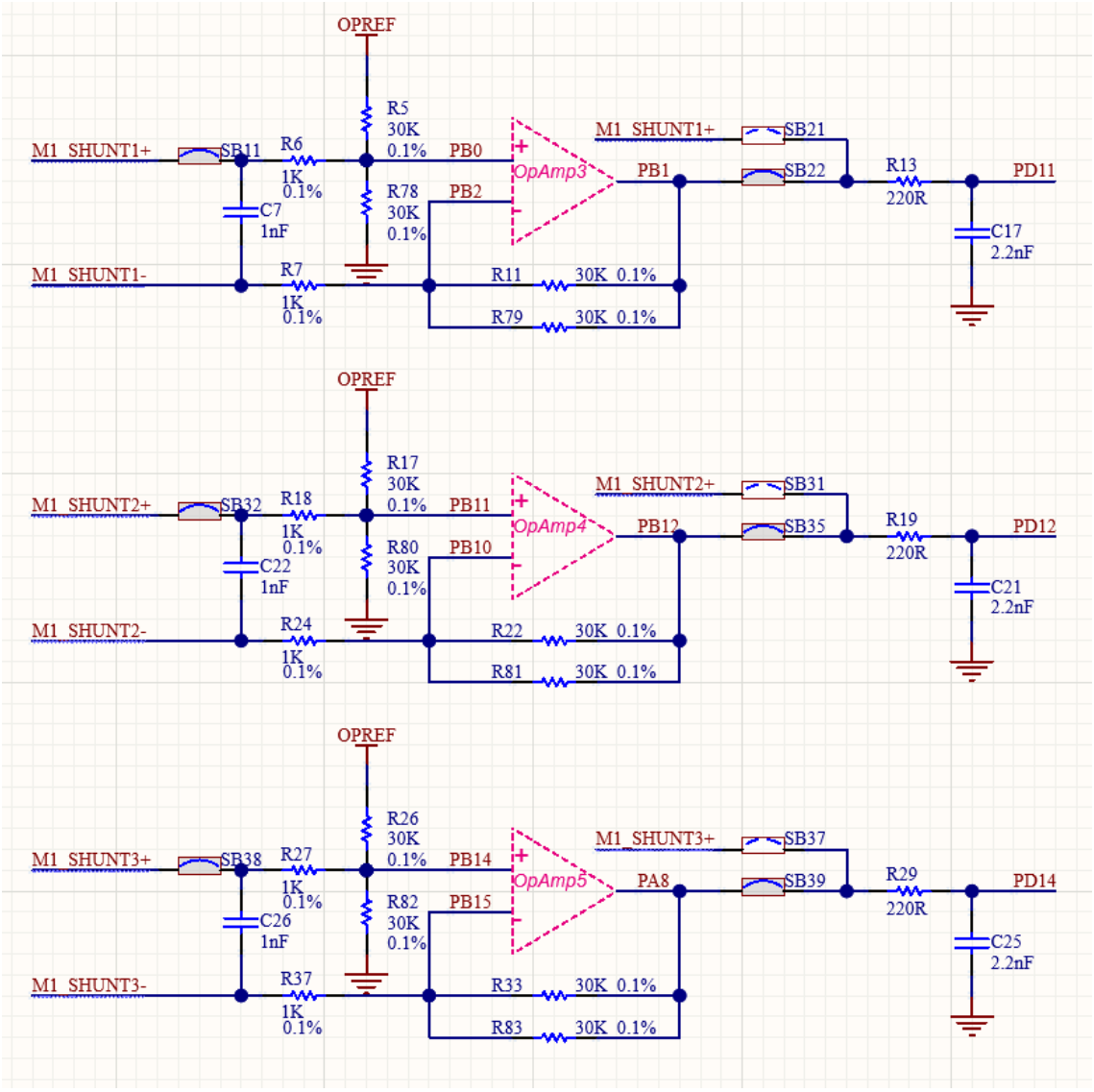
So $f_{-3dB} = fn \times \sqrt{1 - 2d^2 + \sqrt{4d^4 - 4d^2 + 2}}$, f_{-3dB} at PB13 = 1.51 kHz

3.2 Current sense

3.2.1 In FOC mode and internal MCU op amp, current sense amplifier circuitry is located on the ZeST Discovery board:

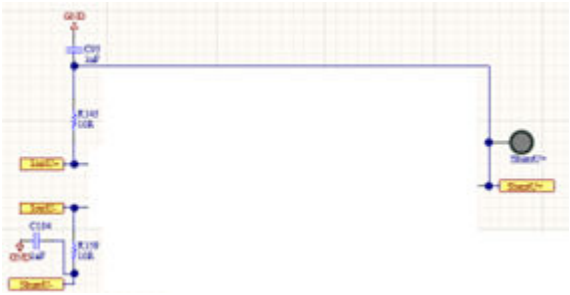
The three phases have the same schematic.

Figure 29. Three shunts ZeST Discovery board internal MCU OPAMPs current sensing schematic



For example, M1_Shunt1 (ADC input PD11). The RSU shunt from the power board is connected to the M1_Shunt1x pins through 10 Ω resistors R145 and R159. ShuntU+ = M1_SHUNT1+ and ShuntU- = M1_SHUNT1-

Figure 30. **Shunt path to ZeST Discovery board in internal MCU OPAMPs**



With:

- R6 + R145 = R7 + R159 = Ra
- R5 = R78 = R11 = R79 = Rb

$PB1 = \frac{OPREF}{2} + \frac{Rb}{2 \times Ra} \times (M1_{Shunt1+} - M1_{Shunt1-})$ with ($M1_{Shunt1+}$ - $M1_{Shunt1-}$) = RShunt × Imotorphase = RSU × Imotorphase

PD11 (ADC input) is PB1 output filtered by a first-order low-pass filter with a -3 dB cutoff frequency $\frac{1}{2\pi \times R13 \times C17}$.

Numerical application:

Ra = 1.01 kΩ, Rb = 30 kΩ, R13 = 220 Ω, C17 = 2.2 nF, Rshunt on power board RSU = 1 mΩ, OPREF = 3.3 V

PB1 = 1.65 V + 14.85 mΩ×Imotorphase and f_{-3dB} = 328 kHz

If a 12-bit ADC is used with a reference voltage of 3.3 V, the LSB is 805 µV in single-ended mode.

The “AC” component of PB1 is 14.85 mΩ×Imotorphase.

Imotorphase = 1A gives 14.85 mV.

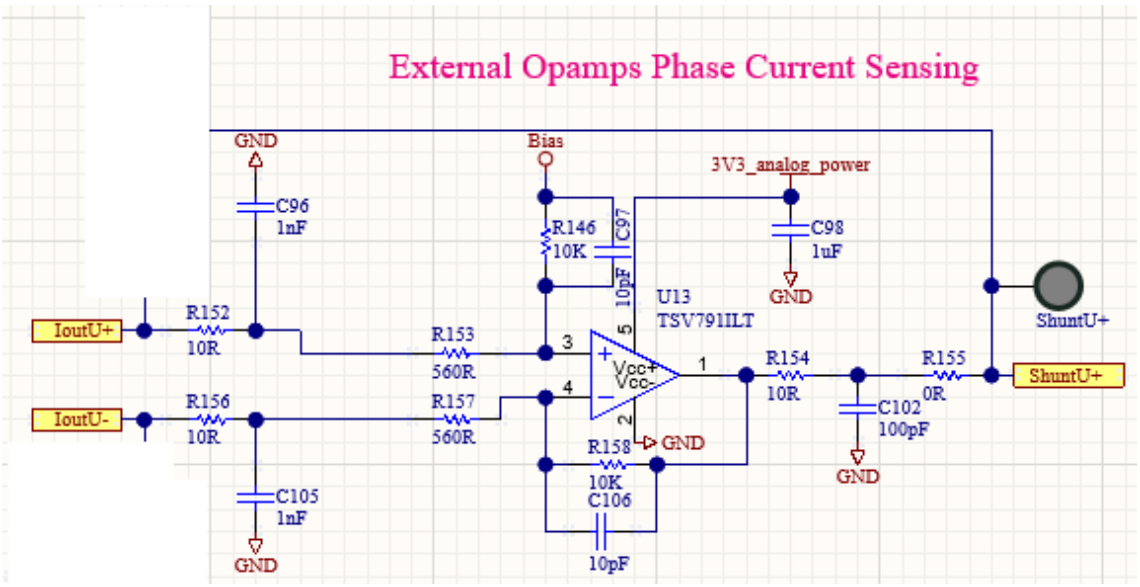
14.85 mV is 18LSB, and then 18LSB per Amp, therefore 1LSB represents 55 mA.

For 50 Arms (70 A peak), PB1 = 1.65 V +/-1.05 V ≈ 2048LSB +/-1304LSB

3.2.2 External OPAMP current sense schematic (FOC mode)

The three phases have the same schematic.

Figure 31. **External OPAMP current sense schematic**



For example, for phase U:

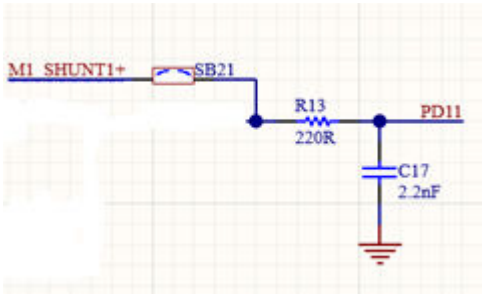
- R152 + R153 = R156 + R157 = Ra
- R146 = R158 = Rb

$$Shunt_{U+} = Bias + \frac{Rb}{Ra} \times (I_{OutU+} - I_{OutU-})$$

with $Bias = \frac{Vref\_pci}{2}$ and

ShuntU+ is connected to M1_Shunt1+.PD11 (ADC input) is ShuntU+ filtered by a first-order low-pass filter with a -3 dB cutoff frequency $\frac{1}{2\pi \times (R13 + R154) \times C17}$.

Figure 32. External OPAMP current sensing schematic on the ZeST Discovery board



Note: Low pass filter R154 + C102 can be neglected because the cutoff frequency is 159 MHz.

Numerical application:

Ra = 570 Ω, Rb = 10 kΩ, R13 + R154 = 230 Ω, C17 = 2.2 nF, Rshunt on power board = 1 mΩ, Vref_pci = 3.3 V

PD11 = 1.65 V + 17.54 mΩ × Imotorphase and F_{-3dB} = 314 kHz

If a 12-bit ADC is used with a reference voltage of 3.3 V, the LSB is 805 µV in single-ended. The “AC” component of ShuntU+ is 17.54 mΩ × Imotorphase.

Imotorphase = 1 A gives 17.54 mV.

17.54 mV is 21 LSB and then 21 LSB per Amp, or 1 LSB represents 47 mA.

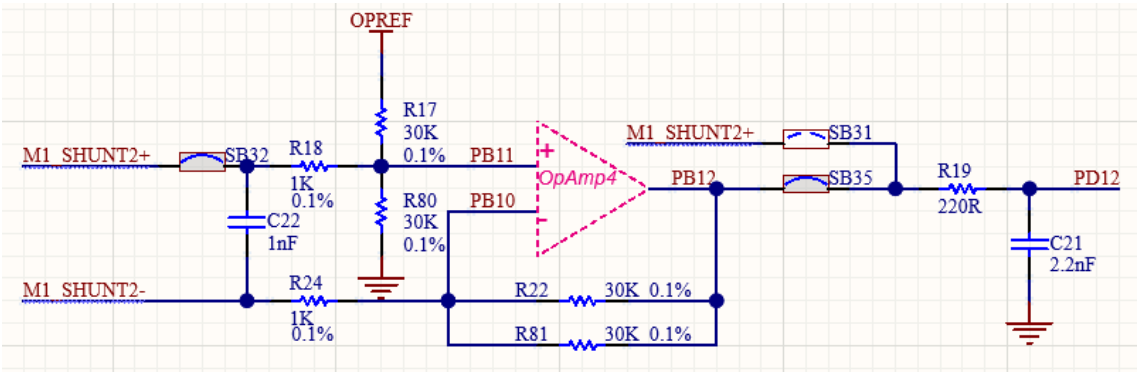
For 50 Arms (70 A peak), ShuntU+ = 1.65 V +/-1.2278 V ≈ 2048 LSB +/-1525 LSB

3.2.3 Internal OPAMP current sense amplifier circuitry on the ZeST Discovery board (six-step mode)

The six-step mode is a single-shunt mode. On the power board, **RSV** is used as a single shunt.

RSV positive sense is connected to M1_Shunt2+ on the Discovery board through a 10 Ω (R161). The negative sense of RSV is left open.

Figure 33. ZeST Discovery board internal MCU op OPAMPs current sensing schematic for the six-step configuration



R17 is removed and the shunt voltage is applied to pin PB11 via a bridge divider R18 + R80.
The calculated value of PB11:

$$PB11 = RSV \times Imotorphases \frac{R80}{R18 + R161 + R80}$$

PB11 is the positive input of the internal MCU PGA.
Then, the voltage output of the internal PGA is: PGAout = PGAgainset × PB11 with Imotorphases = (IU+IV+IW)

Numerical application:

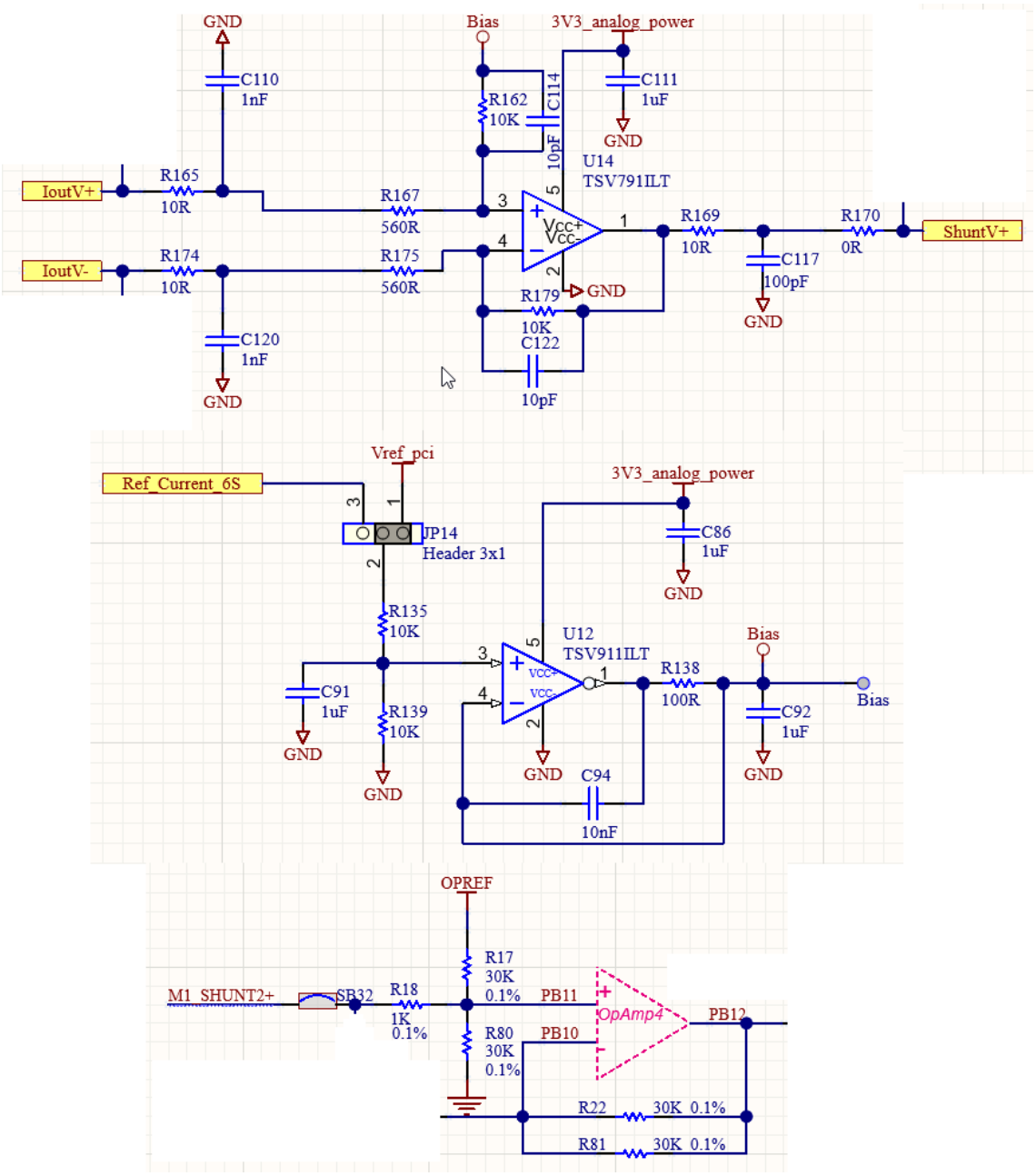
R18 = 1 kΩ, R80 = 30 kΩ, R161 = 10 Ω, RSV = 1 mΩ

PB11 = 0.967 mΩ × Imotorphases and PGAout = PGAgainset × 0.967 mΩ × Imotorphases

3.2.4 External OPAMP (six-step mode)

The six-step mode is a single shunt mode and, on the power board, it is the RSV shunt that is used.
RSV shunt is connected to IoutV+ and IoutV-

Figure 34. Six-step external OPAMP current sensing schematic



ShuntV+ is connected to M1_Shunt2+ and then to PB11 through R18 = 1kΩ and R80 = 30kΩ. JP14 is ON between pins 2 and 3.

R165 + R167 = R174 + R175 = Ra, R162 = R179 = Rb

$$PB11 = \frac{R80}{R18 + R169 + R80} \times \left(Bias + \frac{Rb}{Ra} \times (IoutV_+ - IoutV_-)\right)$$

The voltage output of the internal PGA is then: $PGout = PGAgainset \times PB11$ with $Bias = \frac{Ref\_Current\_6s}{2}$

and $(IoutV_+ - IoutV_-) = RSV \times Imotorphases$ with $Imotorphases = Imotorphaseq = (IU + IV + IW)$

Numerical application

R169 = 10 Ω, RSV = 1 mΩ, Ra = 570 Ω, Rb = 10 kΩ, R18 = 1 kΩ, R80 = 30 kΩ

PB11 = Ref_Current_6S÷2 + 16.96 mΩ × Imotorphases

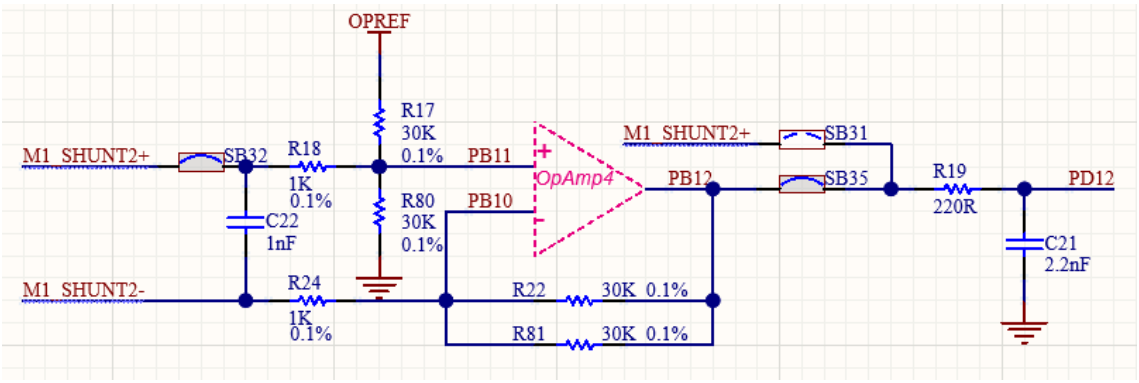
Note: Ref_Current_6S is a DAC output. The DAC must be set in buffer mode ON and, referring to the datasheet of STM32G4 products, Ref_Current_6S varies from 0.2 V to Vref - 0.2 V. To reach a bias of about 0 V, the DAC output must be set in buffer mode OFF.

3.2.5 Internal OPAMP current sense amplifier on the ZeST Discovery board (single-shunt FOC mode)

The single-shunt FOC mode uses a single shunt and, on the power board, an RSV shunt is used.

RSV positive sense is connected to M1_Shunt2+ on the Discovery board through a 10 Ω (R161). RSV negative sense is connected to M1_Shunt2- on the Discovery board through a 10 Ω (R181).

Figure 35. Single shunt ZeST Discovery board internal MCU OPAMPs current sensing schematic



R18 + R161 = R24 + R181 = Ra, R17 = R22 = R80 = R81 = Rb

$$PB12 = \frac{OPREF}{2} + \frac{Rb}{2 \times Ra} \times (M1_{Shunt2+} - M1_{Shunt2-})$$

with $(M1_{Shunt2+} - M1_{Shunt2-}) = RSV \times Imotorphases$ with $Imotorphases = (IU + IV + IW)$

PD12 (ADC input) is PB12 output filtered by a first-order low-pass filter with a -3 dB cutoff frequency $\frac{1}{2\pi \times R19 \times C21}$

Numerical application

Ra = 1.01 kΩ, Rb = 30 kΩ, R19 = 220 Ω, C21 = 2.2 nF

Rshunt on power board RSV = 1 mΩ, OPREF = 3.3 V

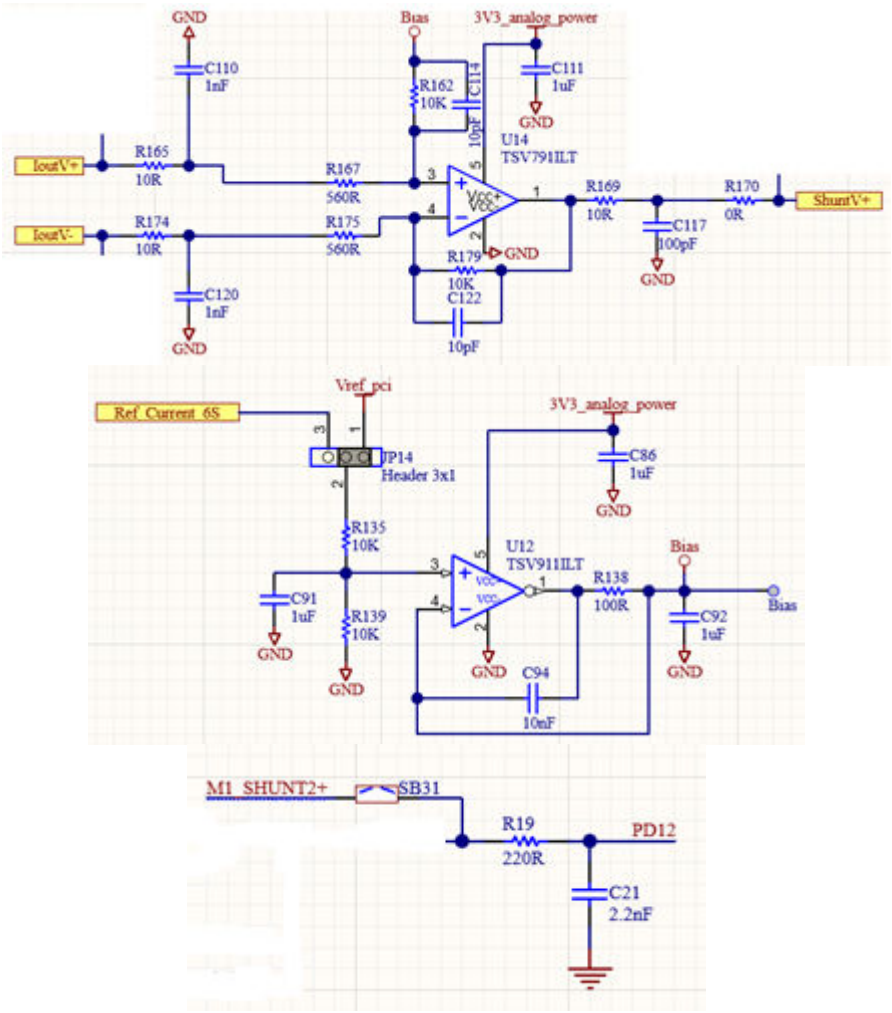
PB12 = 1.65 V + 14.85 mΩ × Imotorphases and F-3dB = 328 kHz

If a 12-bit ADC is used with a reference voltage of 3.3 V, the LSB is 805 µV in single-ended. The “AC” component of PB12 is 14.85 mΩ × Imotorphases. With Imotorphases = 1 A, it gives 14.85 mV. 14.85 mV is 18 LSB so 18 LSB per ampere or one LSB represents 55 mA. For 50 Arms (70 A peak), PB12 = 1.65 V +/-1.05 V ≈ 2048 LSB +/-1304 LSB.

3.2.6 External OPAMP (single-shunt FOC mode)

The single-shunt FOC mode uses a single shunt and, on the power board, it is RSV that is used. The RSV shunt is connected to IoutV+ and IoutV-. RSV positive sense is connected to IoutV+ through a 10 Ω (R165) and RSV negative sense is connected to IoutV through a 10 Ω (R174). JP14 is fitted between pins 1 and 2.

Figure 36. Single shunt external OPAMPs current sensing schematic



ShuntV+ is connected to M1_SHUNT2+ on the Discovery board with R165 + R167 = R174 + R175 = Ra, R162 = R179 = Rb

Bias $= \frac{Vref\_pci}{2}$ with Bias $= \frac{Vref\_pci}{2}$ and $(IoutV_+ - IoutV_-) = RSV \times Imotorphases$ with $Imotorphases = (IU + IV + IW)$

PD12 (ADC input) is ShuntV+ output filtered by a first-order low-pass filter with a -3 dB cutoff frequency $f_{-3dB} = \frac{1}{2\pi \times (R19 + R169) \times C21}$

Numerical application

Vref_pci = 3.3 V, R161 and R181 = 10 Ω, RSV = 1 m Ω, Ra = 570 Ω, Rb = 10kΩ

PD12 = 1.65 V + 17.54 mΩ × Imotorphases and F-3dB = 314 kHz

If a 12-bit ADC is used with a reference voltage of 3.3 V, the LSB is 805 µV in single-ended. The “AC” component of ShuntV+ is 17.54 mΩ × Imotorphase.

With Imotorphases = 1 A, it gives 17.54 mV. 17.54 mV is 21 LSB so 21 LSB per ampere or one LSB represents 47 mA.

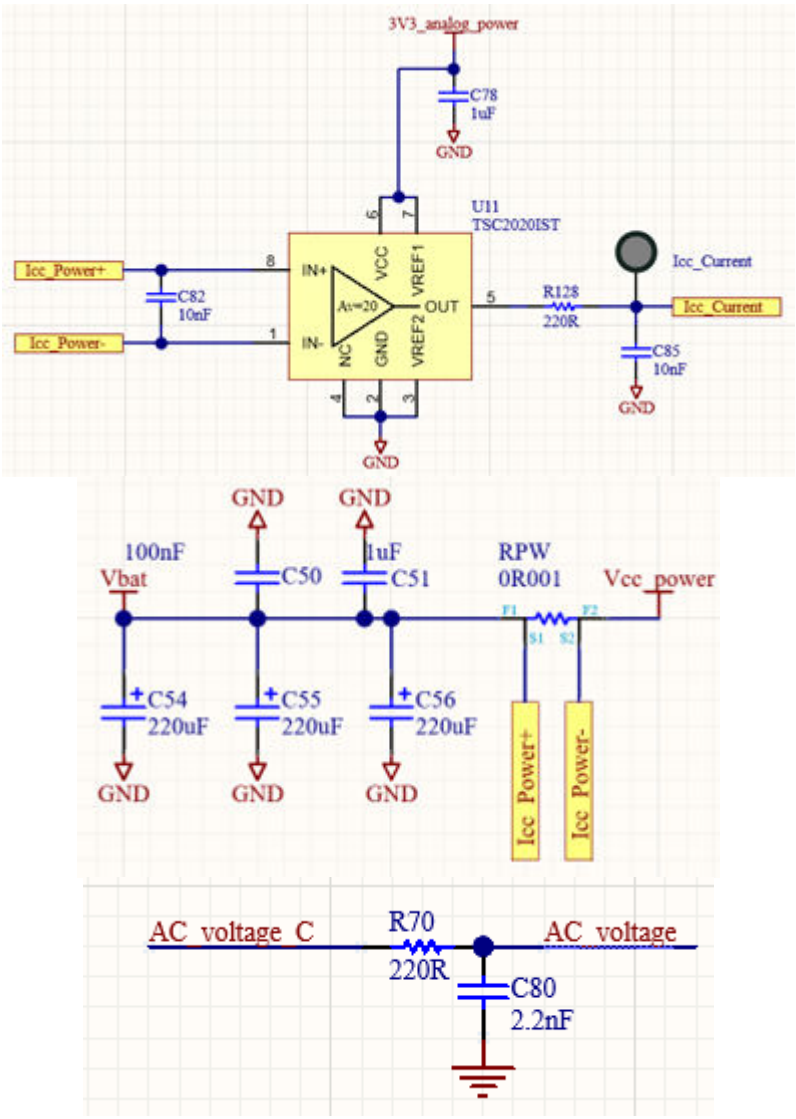
For 50 Arms (70 A peak), ShuntV+ = 1.65 V +/-1.2278 V ≈ 2048 LSB +/-1525 LSB

3.2.7 Battery current sense

On the power board, there is an option to measure the current drained or provided to the battery. This measurement is done by a shunt resistor RPW and a high-side current sensing TSC2020.

R128 with C85 acts as a first-order low-pass filter before entering the Discovery board. The TSC2020 has an internal gain set at 20 V/V, and V_{ref1} and V_{ref2} connections allow a DC bias of the output (OUT) to be set to 3.3V_analog_power/2.

Figure 37. Power supply (battery) current sensing schematic



Icc_Current is connected on the Discovery board to AC_voltage_C and then again first-order low-pass filtered (R70 + C80) before entering in ADC input named AC_voltage.

$$Icc_{Current} = \frac{3V3\_analog\_power}{2} + 20 \times (Icc\_Power_{+} - Icc\_Power_{-})$$

with $\text{Icc\_Power}_{+} - \text{Icc\_Power}_{-} = RPW \times IBattery$ and $\mathrm{d} = \frac{R128 \times C85 + R128 \times C80 + R70 \times C80}{2\sqrt{R128 \times C85 \times R70 \times C80}}$ then

$\mathrm{fn} = \frac{1}{2\pi\sqrt{R128 \times C85 \times R70 \times C80}}$ so $f_{-3dB} = fn \times \sqrt{1 - 2d^2 + \sqrt{4d^4 - 4d^2 + 2}}$

Numerical application

3V3_analog_power = 3.3 V, RPW = 1 m Ω, R128 = R70 = 220 Ω, C85 = 10 nF, C85 = 10 nF

Icc_Current = 1.65 V + 20 mΩ × IBattery and f_{-3dB} = 56.3 kHz

If a 12-bit ADC is used with a reference voltage of 3.3 V, the LSB is 805 µV in single-ended. The “AC” component of Icc_Current is 20 mΩ × IBattery.

IBattery = 1 A gives 20 mV. 20 mV is 24 LSB. Thus, 24 LSB per ampere or one LSB represents 41.6 mA.

For 50 Arms (70 A peak), Icc_Current = 1.65 V +/-1.4 V ≈ 2048 LSB +/-1739 LSB.

Note: As the gain of the TSC2010 is fixed internally, the best way to change the current range measurement is to change the RPW value.

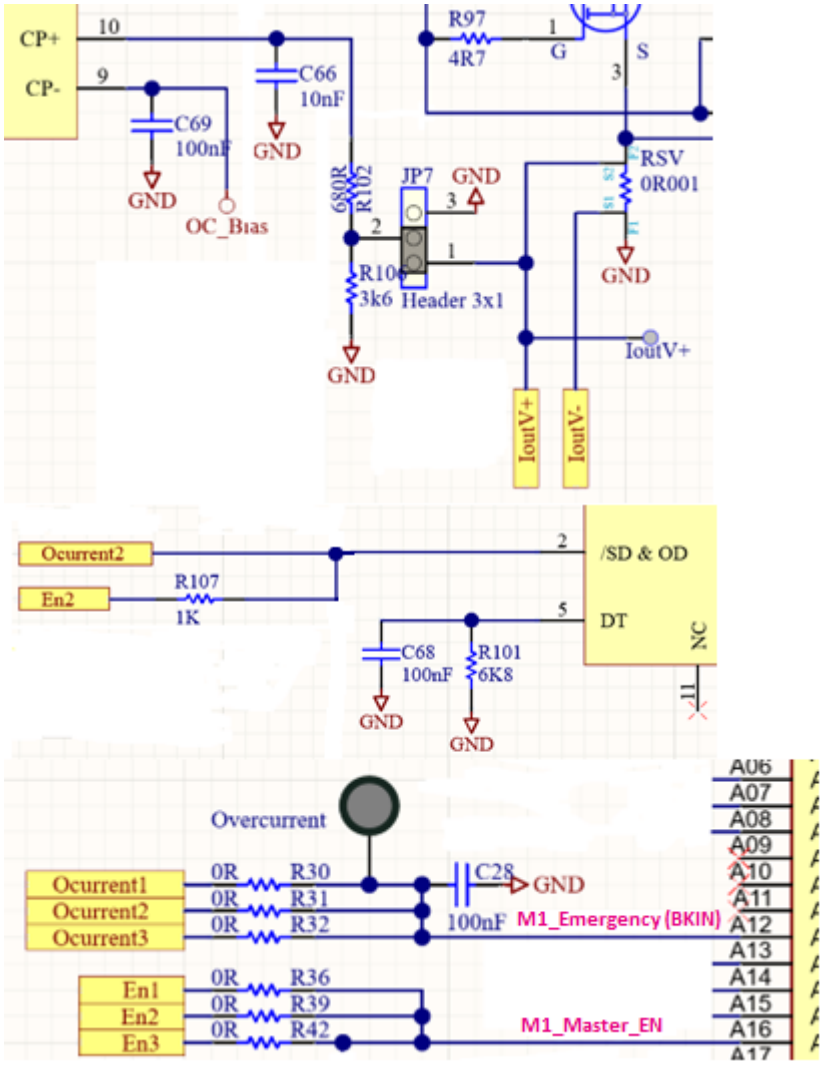
3.3 Overcurrent protection

On the power board, there are three L6491 transistor drivers. Each L6491 driver has an integrated comparator with its two inputs externally accessible (CP+ and CP-).

While Cp+ voltage is lower than CP- voltage, the comparator is not triggered, and /SD and OD pins are not tied to GND.

When Cp+ voltage is higher than CP- voltage, the comparator is triggered, and /SD and OD pins tied to GND set the L6491 driver to standby mode. As a consequence, the output power stage is in a high-Z state.

Figure 38. Overcurrent protection schematic



Overcurrent pins are connected to M1_Energency (BKIN) on the Discovery board. When one of the L6491 drivers detects an overcurrent, as all /SD and OD pins are connected, the three L6491 are set to standby at the same time. As the L6491 drivers are set to standby, overcurrent "virtually disappears" (because the output power stage is in high-Z) and thanks to the C28 capacitor, all L6491 drivers are forced to remain in standby until the C28 voltage reaches the enable voltage threshold, which is 2 V at minimum.

Note: C28 is charged through the three 1 kΩ resistors connected to Enx pins. The time to reach the threshold of the enable pin after an overcurrent detection is expressed by:

$t = -\mathrm{Re}\,q \times C28 \times \ln\left(1 - \frac{2V}{3.3V}\right)$ with Req = R82 // R103 // R107

Numerical application

C28 = 100 nF and Req = 1k // 1k // 1k = 333 Ω so t = 31 µs.

Note: The RC filter made by R102 (R77, R79) and C66 (C42, C47) is there to "attenuate" the inevitable oscillations in the shunt measurement due to their parasitic inductance.

The cutoff frequency of this filter must be low enough to reject parasitic oscillations but high enough not to penalize the overcurrent detection speed.

It is also necessary to consider the safe operating area (SOA) of the transistor to prevent the current amplitude from extending outside this area.

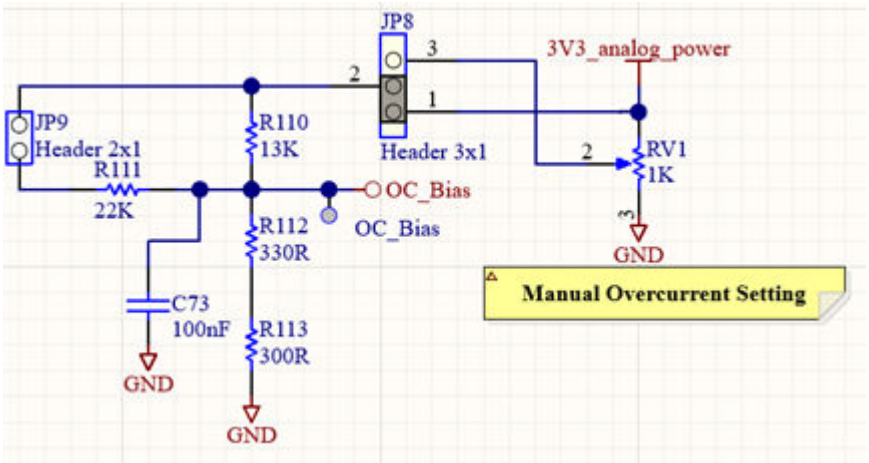
For the STP110N10F7 MOSFET, the datasheet gives 100 µs in a single pulse. Being conservative and knowing that it is very likely that there is more than one pulse before reaching the trigger threshold, a 5 or 20 µs margin is taken.

If C66 = 10 nF and knowing that 3 × RC is 95% of the final value, then the resistance is: 20 µs/(3 × C66) = 666 Ω or 680 Ω.

Then the cutoff frequency is $\frac{1}{2\pi \times R102 \times C66} = 23\ \mathrm{kHz}$.

The level of the overcurrent setting is defined by the voltage applied to the CP- pin. This voltage is named OC_Bias on the schematic.

Figure 39. Overcurrent threshold setting schematic



Depending on the JP8 position, this voltage can be fixed or variable.

- 1-2: fixed by resistor divider R110, R111, R112+R113
- 2-3: variable by RV1 and the resistor divider R110, R111, R112+R113

The following formula is used at the threshold to calculate the needed OC_Bias value:

$Cp_+ = RSx \times Imotorphase_{\max} = Cp_- = OC_{Bias}$

For example, with RSx = 1 mΩ and a max current requested Imotorphases_max = 80 A, OC_Bias = 1 mΩ ×0.80 A = 80 mV.

On a power board with JP8 ON between 1-2 pins:

- $OC\_Bias = 3.3 \times \frac{(R112 + R113)}{R112 + R113 + R110}$ if JP9 is OFF.

- $OC\_Bias = 3.3 \times \frac{(R112 + R113)}{R112 + R113 + \frac{R110 \times R111}{R110 + R111}}$ if JP9 is ON.

Then with a 1 mΩ shunt:

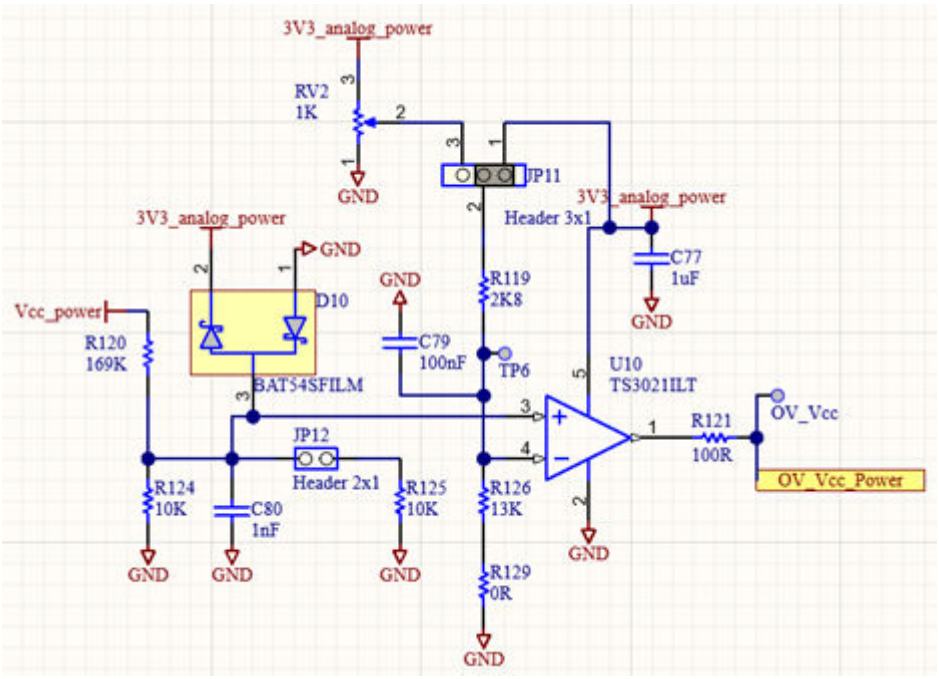
- JP9 OFF gives OC_Bias = 152 mV so Imotorphases_max = 152 A
- JP9 ON gives OC_Bias = 236 mV so Imotorphases_max = 236 A

On the power board, if JP8 is ON between 2-3 pins, then with a 1 mΩ shunt, adjust RV1 to have the desired overcurrent value. For example, set OC_Bias at 80 mV (pad layout OC_Bias) to have an overcurrent set at 80 A.

3.4 Overvoltage protection

The power board has a comparator for the overvoltage detection feature. The comparator is U10.

Figure 40. Overvoltage protection schematic

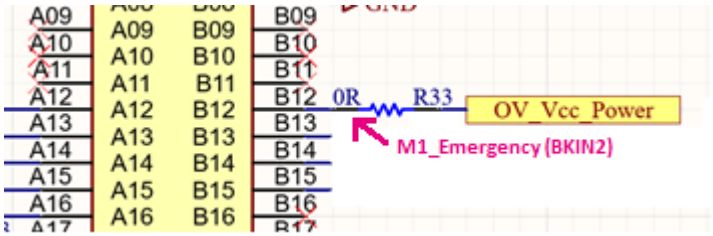


While U10 In+ voltage is lower than In- voltage, the comparator is not triggered and the OV_Vcc_Power pin is tied to GND.

When U10 In+ voltage is higher than In- voltage, the comparator is triggered, OV_Vcc_Power pin is tied to 3V3_analog_power.

When an overvoltage is detected, the rising edge of OV_Vcc_Power is sent to the Discovery board to M1_Emergency (BKIN2).

Figure 41. Overvoltage PCI connector highlight



The level of overvoltage setting is defined by the voltage applied on the U10 In- pin. This voltage is named TP6 on the schematic. Depending on the JP11 position, this voltage can be fixed or variable.

- 1-2: fixed by resistor divider R119, R126+R129

- 2-3: variable by RV2 and the resistor divider R119, R126+R129

The voltage applied to U10 In+ is proportional to battery voltage (Vcc_power) and is named k.Vcc_power.

The value of TP6 is chosen in the range of 1/5 to 4/5 of 3V3_analog_power.

When JP11:

- When JP11 is ON between 1-2 pins, $TP6 = 3V3\_analog\_power \times \frac{R126 + R129}{R119 + R126 + R129}$
- When JP11 is ON between 2-3 pins, TP6 variable thanks to RV2.

The k factor for Vcc_power is calculated depending on the JP12 state:

- When JP12 is OFF: $k = \frac{R124}{R120 + R124}$
- When JP12 is ON: $k = \frac{\frac{R124 \times R125}{R124 + R125}}{R120 + \frac{R124 \times R125}{R124 + R125}}$

Numerical application

3V3_analog_power = 3.3 V, R119 = 2.8 kΩ, R120 = 169 kΩ, R124 = 10 kΩ, R125 = 10 kΩ, R126 = 13 kΩ, R129 = 0Ω

- TP6 = 2.71 V with JP11 ON between 1 and 2.
- k (JP12 OFF) = 0.0558, k (JP12 ON) = 0.0287.

At threshold k.Vcc_power = TP6, then

- When JP12 is OFF: Vcc_power overvoltage threshold = 2.71/0.0558 = 48.56 V.
- When JP12 is ON: Vcc_power overvoltage threshold = 2.71/0.0283 = 94.42 V.

When JP11 is set between 2-3, JP12 must be ON. In this case, 0.0287.Vcc_power = TP6.

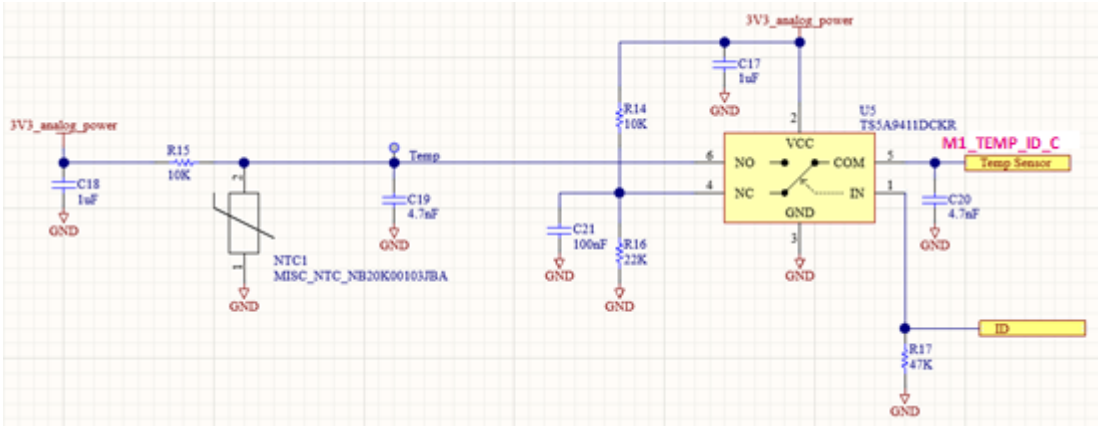
If an overvoltage of 35 V is requested, adjust TP6 with RV2 to have TP6 = 0.0287.35V = 1 V.

3.5 Temperature sensor

On the power board, there is a temperature sensor located under the heatsink. This temperature sensor is multiplexed with the board identification (board identification is a simple bridge resistor divider generating a predetermined voltage).

The ID label is connected to ID_Enable on the Discovery board and the Temp_Sensor label is connected to M1_TEMP_ID_C on the Discovery board.

Figure 42. Temperature sensor schematic



- When ID is a logical 0, Temp_Sensor = Board ID.
- When ID is a logical 1, Temp_Sensor = heatsink temperature.

Board ID is a DC voltage, and its value is

$$\text{Board ID} = 3V3\_analog\_power \times \frac{R16}{R14 + R16} = 3.3\ \text{V} \times 0.6875 = 2.268\ \text{V}$$

The heatsink temperature is a DC voltage that is temperature-dependent:

$$\text{NTC1 resistance(T)} = \text{NTC1(25°C)} \times \exp\left(\beta \times \left(\frac{1}{273+T} - \frac{1}{273+25}\right)\right)$$

With for NTC1 = NB20K00103JBA from AVX/KYOCERA, NTC1(25°C) ≈ 10kΩ, b = 3630°K and T in °C

$$\text{So, heatsink temperature(T)} = 3V3\_analog\_power \times \frac{\text{NTC1 resistance(T)}}{\text{NTC1 resistance(T)}+10k} = 3.3V \times \frac{\text{NTC1 resistance(T)}}{\text{NTC1 resistance(T)}+10k}$$

Note: At T = 25°C, heatsink temperature(25°C) ≈ 1.65 V

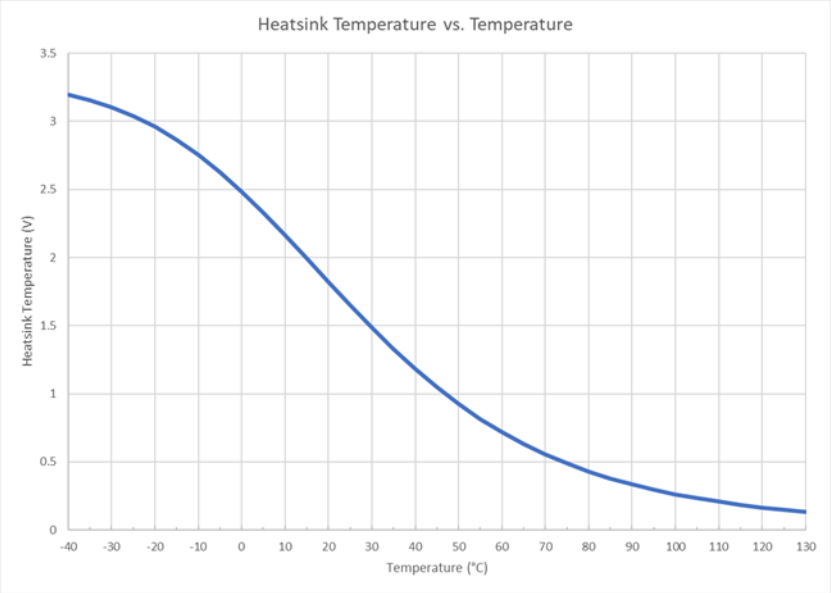
With the value of the heatsink temperature measured (voltage), the NTC resistance value can be calculated

$$\text{NTC1 resistance(T)} = \frac{10k \times heatsink\ \ temperature(T)}{3V3\_analog\_power - \text{heatsink temperature(T)}}$$

And then calculate the temperature:

$$T\ (°C) = \frac{\beta}{\ln\left(\text{NTC1 resistance(T)}\right) - \ln(NTC1(25°C)) + \frac{\beta}{298}} - 273$$

Figure 43. Image of heatsink temperature versus temperature

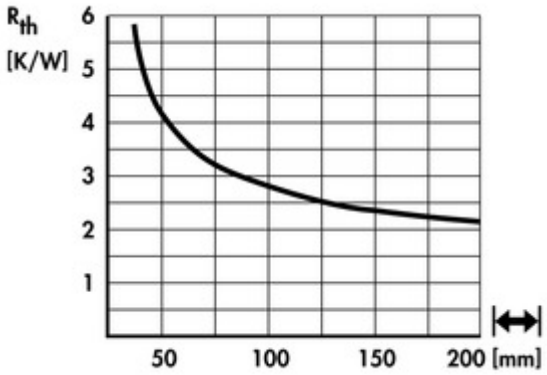


3.6 Temperature limitation

Due to the heatsink size used, there are combinations (VBAT, PWM frequency, output current) that can only be handled with a fan cooling the heatsink.

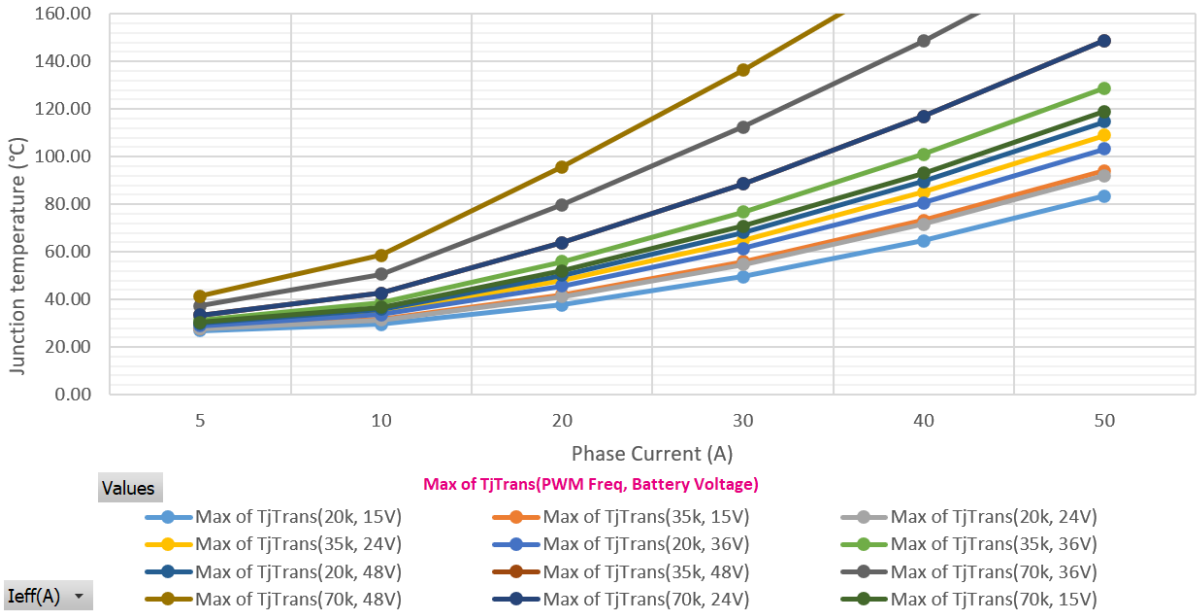
The chosen heatsink is a heatsink from Fischer Elektronik with reference SK664100SA. It has a 100 mm length with a thermal resistance of 2.7°C/W without fan cooling.

Figure 44. Thermal resistance versus length



To compute power transistor junction temperature, the isolation pad for TO-220 of STP110N10F7 has a thermal resistance of about 1°C/W.

Figure 45. Transistor junction temperature versus PWM frequency versus power supply voltage

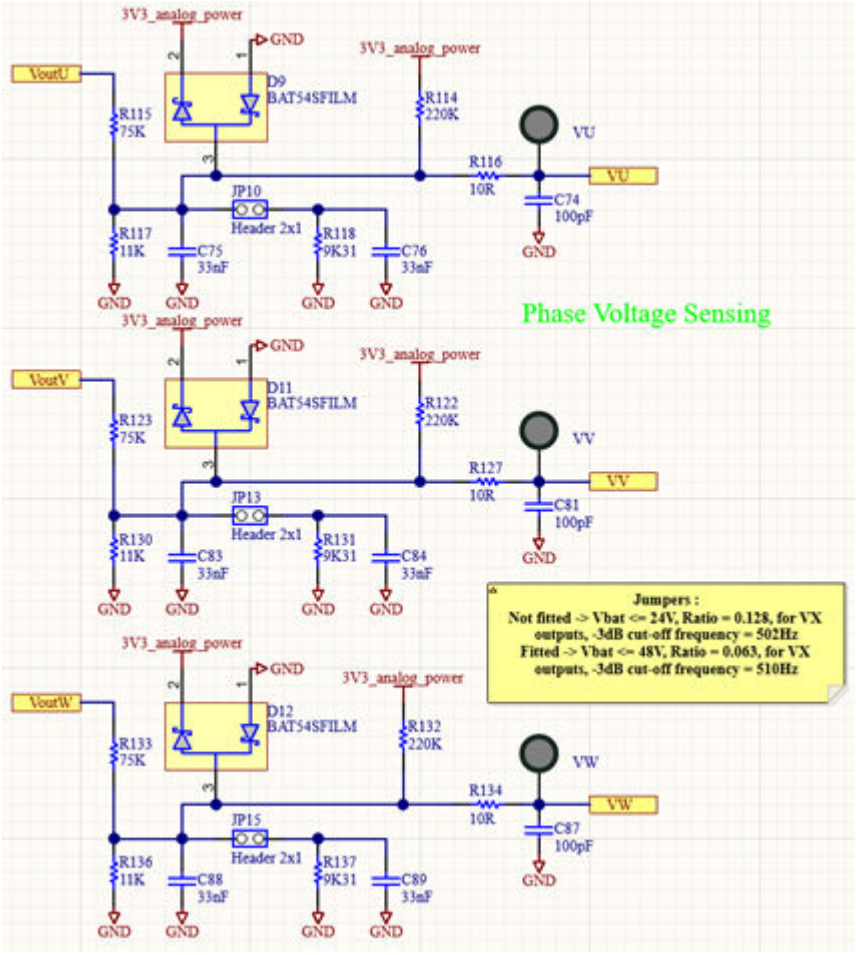


The previous curves represent the maximum combination of VBAT and PWM frequency possible without using a FAN versus RMS current on each phase. To be in a safe area, the junction temperature must be kept lower than 125°C. For higher combinations, adding a fan to cool the heatsink or changing the heatsink is necessary.

3.7 Utility of R114, R122, and R132

These three resistors (R114, R122, R132), OFF by default, can be used to add an offset that avoids having a negative voltage on the ADC input.

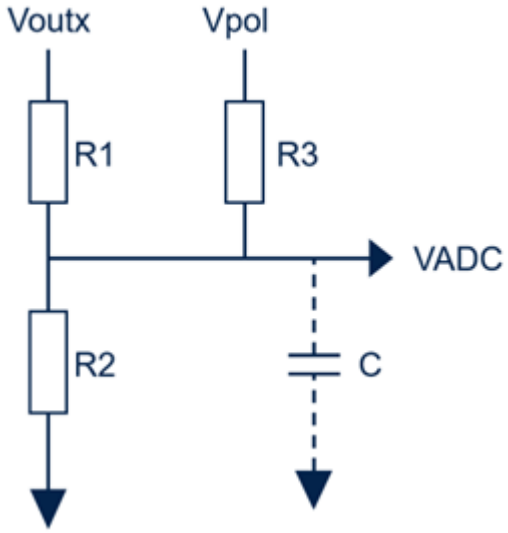
Figure 46. Phase voltage sensing schematic



To calculate the value of these resistors, the variation of the inverter output voltage (Voutx), of the ADC input voltage (VADC), and the bias voltage (VPOL) are considered.

Figure 47 shows a simplified version of the schematic.

Figure 47. **Resistor bridge divider with DC level shifting schematic**



$VADC = \frac{R2 \times (R3 \times Voutx + R1 \times vpol)}{R1 \times R2 + R2 \times R3 + R1 \times R3}$, $RADC = \frac{R1 \times R2 \times R3}{R1 \times R2 + R2 \times R3 + R1 \times R3}$, and $F_{-3dB} = \frac{1}{2\pi \times RADC \times C}$

What is requested:

- When Voutx = Voutmax so VADC must be lower or equal to VADCmax.
- When Voutx = -VD (in dead time mode, Vout = -Vdiode if the output current is positive), so VADC ≈ 0.

Finally: $VADC = 0$ gives $R1 = \frac{-R3 \times VD}{Vpol}$

$VADC = VADC\max$ gives $R3 = \frac{R2 \times [VADC\max \times (Vpol - VD) - Vpol \times (Vout\max - VD)]}{VADC\max \times VD}$

Numerical application

Referring to the power board schematic for phase U, R115 = R1, R114 = R3, and R117 = R2 or R117//R118, C = C75 or C75 + C76, VoutU = Voutx and 3V3_analog_power = Vpol

Example: JP10 OFF and Voutmax = 20 V, Vpol = 3.3 V, VD = -1 V, VADCmax = 3 V

R2 = 11 kΩ is chosen for a practical reason (no need to unsolder R117).

So, R3 = 206.8 kΩ which is 205 kΩ in the E48 series, and then R1 = 62.1 kΩ which is 61.9 kΩ in the E48 series.

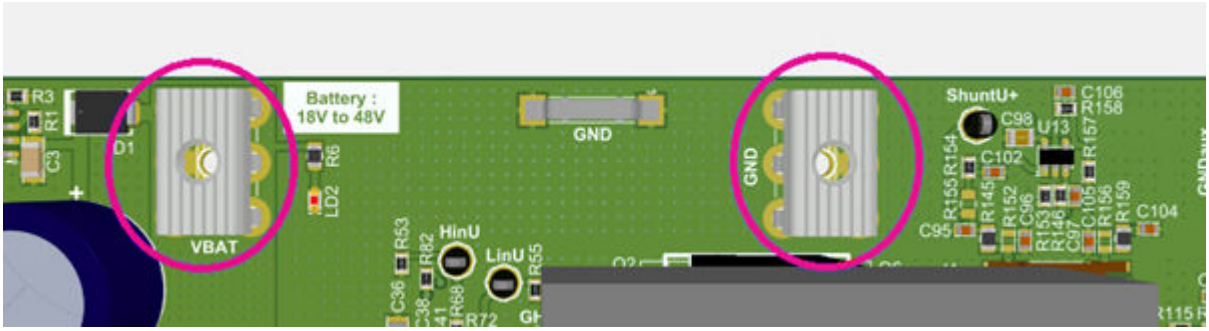
To finish, RADC = 8.9kΩ and to reach f_{-3dB} = 500 Hz and C = 35.6 nF is needed with its normalized value, C = 33 nF gives f_{-3dB} = 542 Hz.

4 Power board initial tests

4.1 Step 1

Provide a DC voltage = 20 V with a current limitation set at 150 mA between the VBAT connector (positive node) and GND (negative node).

Figure 48. Location of power supply (battery) connector

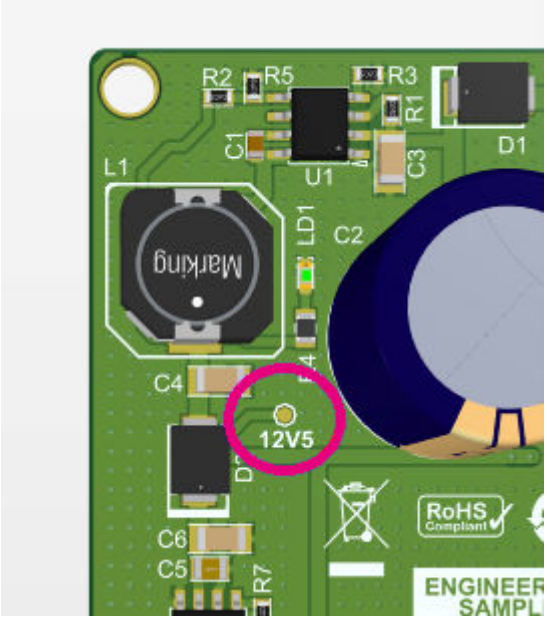


4.2 Step 2

Set the power supply ON and measure with a DC voltmeter the voltage between test points and GND.

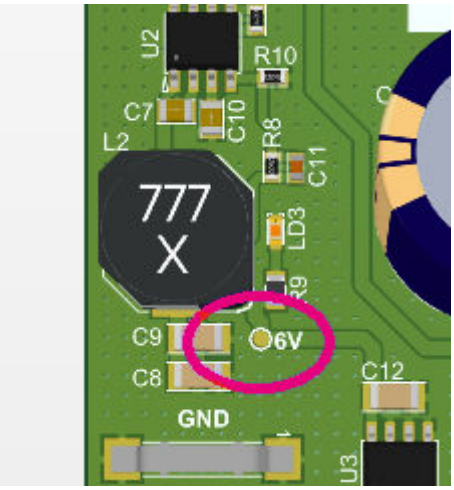
- 12.5 V +/-10% at 12V5 test point:

Figure 49. Location of 12.5 V test point



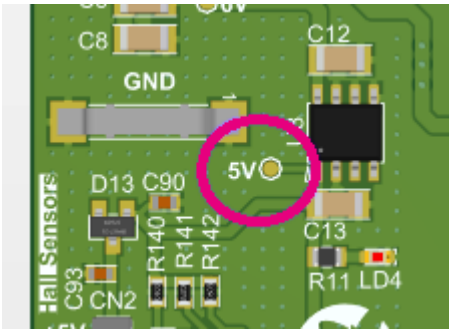
- 6 V +/-10% at 6V test point:

Figure 50. Location of 6 V test point



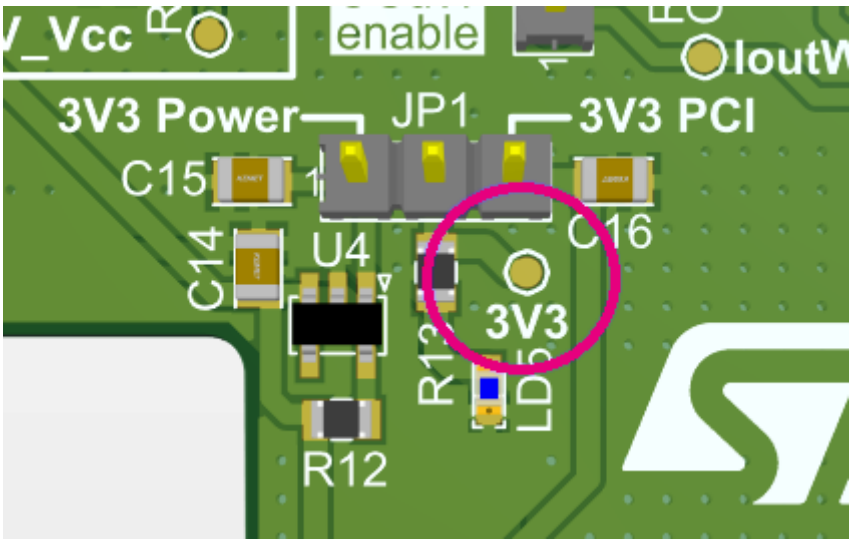
- 5 V +/-5% at 5V test point:

Figure 51. Location of 5 V test point



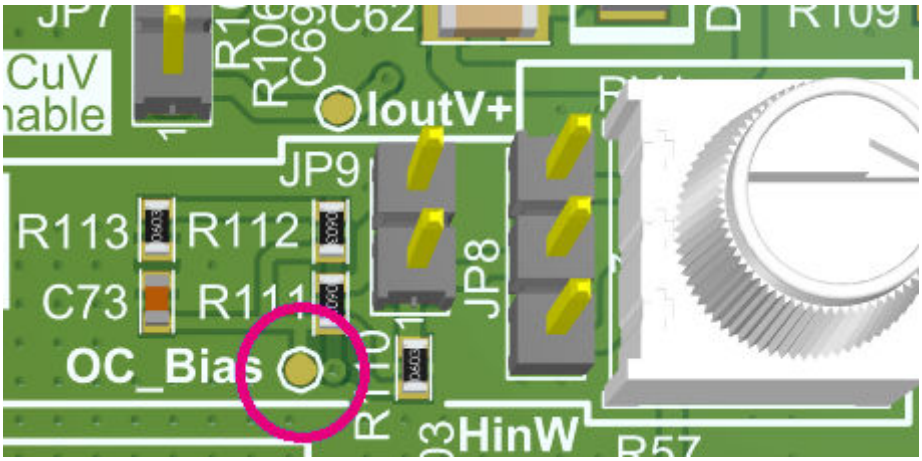
- 3.3 V +/-5% at 3V3 test point:

Figure 52. Location of 3.3 V test point



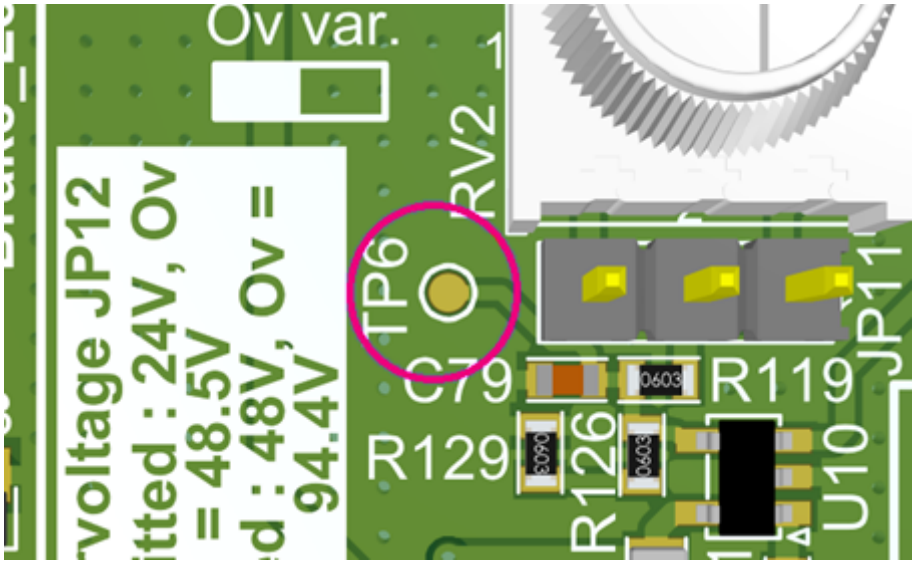
- 0.152 V +/-5% at OC_Bias test point:

Figure 53. Location of bias test point



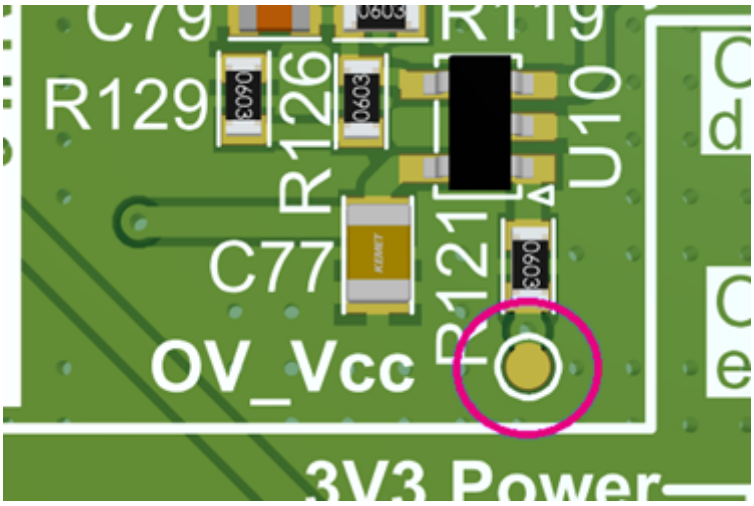
- 2.715 V +/-5% at TP6 test point:

Figure 54. Location of TP6 test point



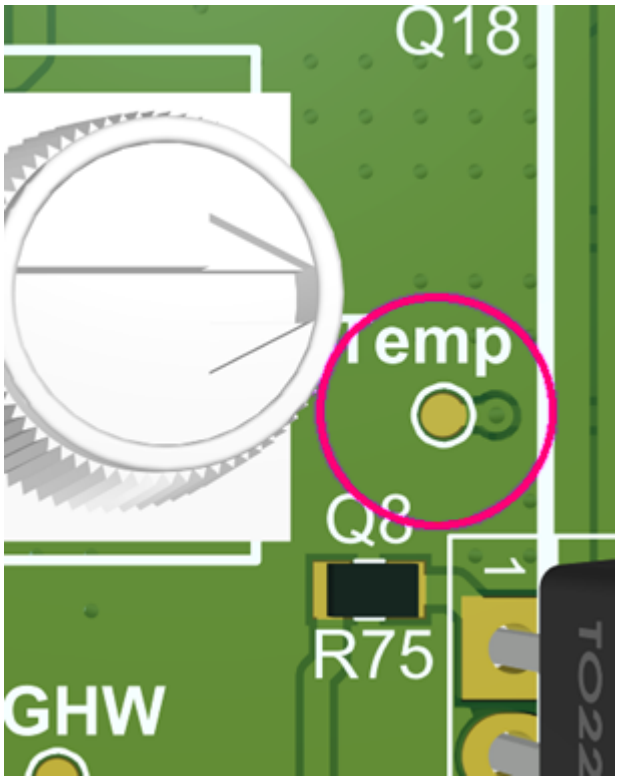
- 0 V to few mV at OV_Vcc test point (logic level low):

Figure 55. Location of OV_Vcc test point



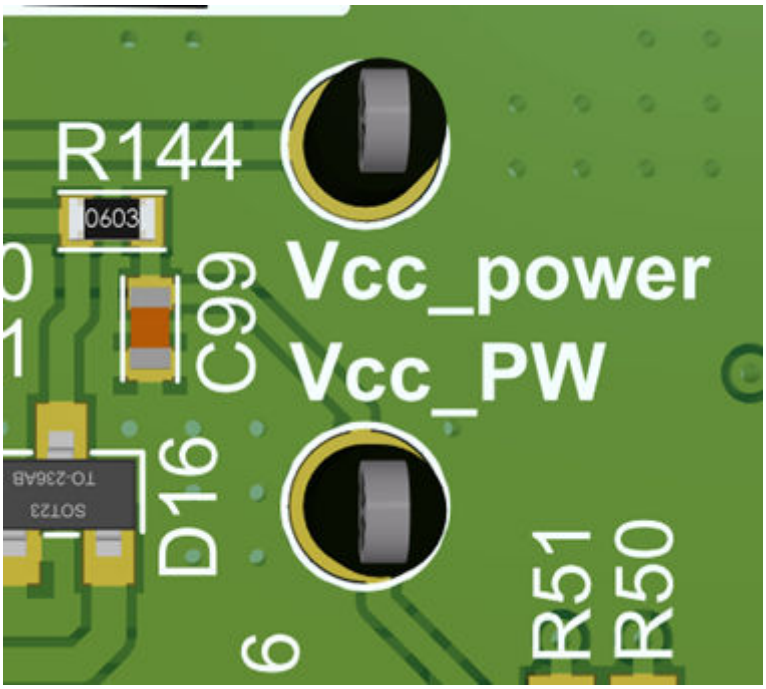
- 1.65 V +/-100 mV at Temp test point:

Figure 56. Location of Temp test point



- About 20 V at test point Vcc_power and about 1.222 V at test point Vcc_PW:

Figure 57. Location of test point Vcc_power and test point Vcc_PW

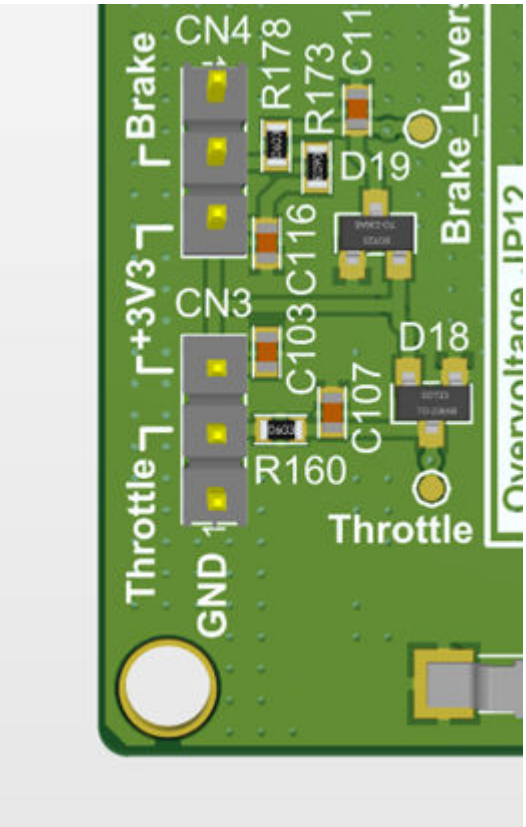


Note: A DC consumption of about 30 mA must be read from the 20 V DC power source.

4.3 Step 3

Connect a wire between the 3.3 V present on CN3 or CN4 (pin 3V3) to the Enable pin:

Figure 58. Location of CN3 and CN4



Verify that the Overcurrent test pin is about 3.3 V.

Use a function generator and configure it as follows:

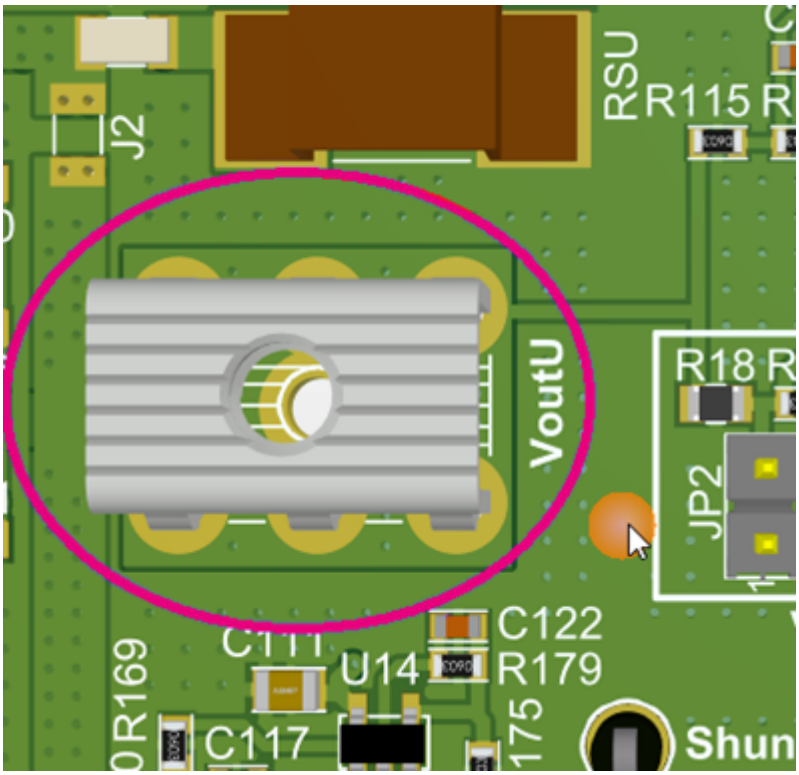
- Square wave output 50% duty-cycle
- Low level = 0 V
- High level = 3.3 V
- Frequency = 10 kHz

Connect the generator output to HinU and LinU **together** and the GND of the generator to the GND of the board:

Figure 59. Location of HinU and LinU

Connect an oscilloscope probe to VoutU and the ground lead (alligator clip) to the GND of the board:

Figure 60. Location of VoutU connector



Set to ON the output of the generator and read on the oscilloscope a square wave of 50% duty cycle with an amplitude of about 0 to 20 V like the following screenshots (ch1 = generator output = HinU = LinU, ch2 = VoutU):

Figure 61. Screenshot of VoutU versus HinU/LinU

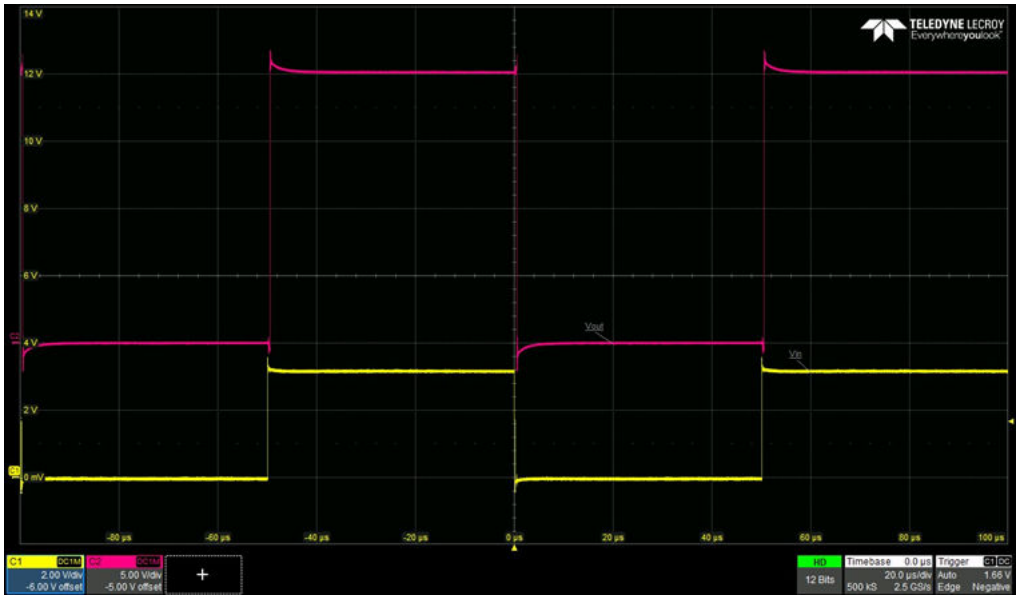
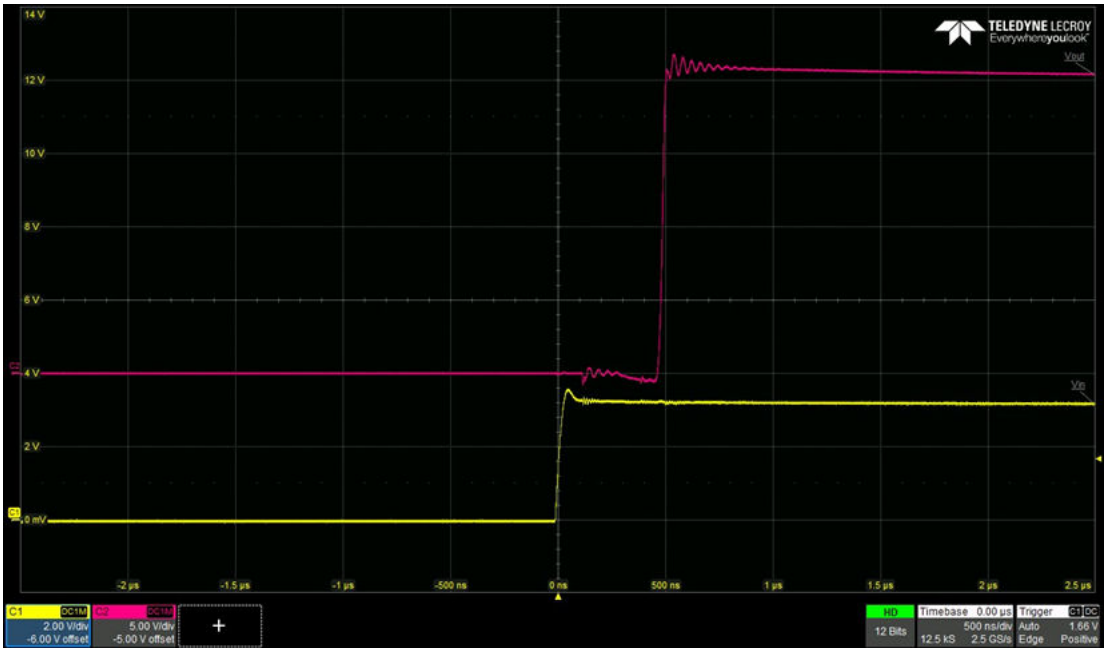
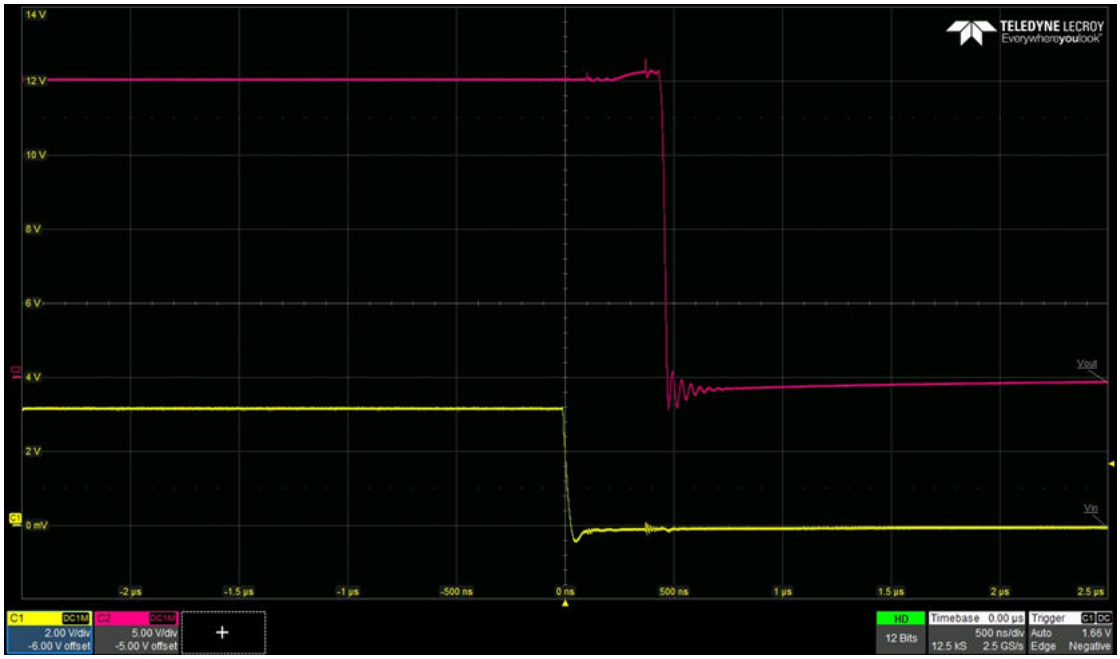


Figure 62. **Screenshot of VoutU rise time**



The delay of about 500 ns is due to the hardware dead time of L6491 with the delay input (HinU/LinU) to VoutU.

Figure 63. **Screenshot of VoutU fall time**



The delay of about 500 ns is due to the hardware dead time of L6491 with the delay input (HinU/LinU) to VoutU. Repeating this operation for HinV/LinV/VoutV and HinW/LinW/VoutW must show the same behavior.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
25-Apr-2025	1	Initial release.
03-Jul-2025	2	Updated the cover page with a reference to the STDES-LVHP01 reference design.

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