Getting started with the battery management system (BMS) evaluation board based on the L99BM114

Introduction

The STEVAL-BMS114 battery management system (BMS) evaluation board can handle from 1 to 31 Li-ion battery nodes. Each battery node manages from 4 to 14 battery cells, for a voltage range between 48 and 800 V.

The board is based on the L99BM114. The main activity of the L99BM114 is monitoring cells and battery node status through stack voltage, cell voltage, and temperature measurements and coulomb counting. Measurement and diagnostic tasks can be executed either on demand or periodically at a programmable cycle interval. Measurement data are available for an external microcontroller to perform charge balancing and to compute the state of charge (SOC) and the state of health (SOH).

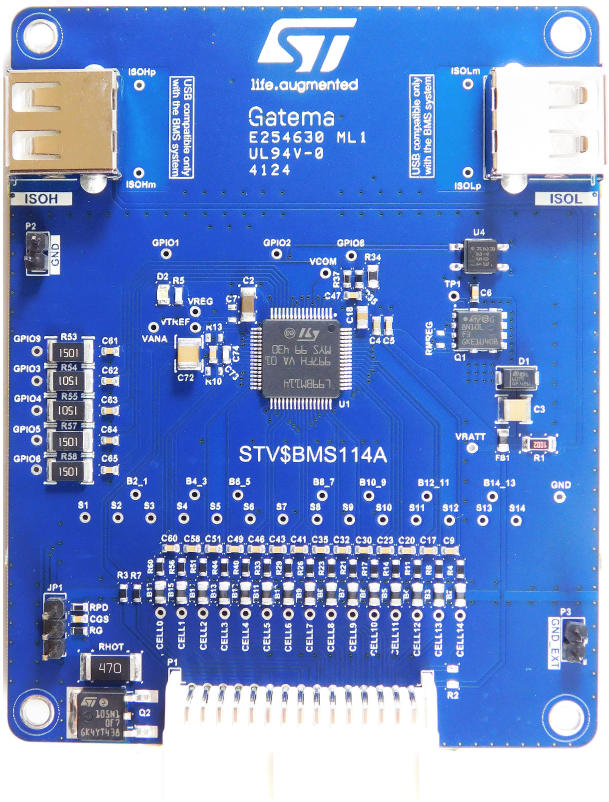
The STEVAL-BMS114 can measure 5 values of temperature through 5 GPIOs (which can be configured as analog inputs to connect NTCs).

The STEVAL-BMS114 provides an elaborate monitoring network to sense the voltage, current, and temperature of each cell.

ST offers BMS evaluation boards (STEVAL-BMS114, STEVAL-BMS114TX) to meet customers' needs and help designers build different types of BMS chain topologies fit for any end-user application.

The STEVAL-BMS114 provides an elaborate monitoring network to sense the voltage, current, and temperature of each cell.

Figure 1. STEVAL-BMS114 evaluation board



Notice: *For dedicated assistance, submit a request through our online support portal at **www.st.com/support**.*

1 BMS evaluation board overview

1.1 STEVAL-BMS114 overview

1.1.1 Features

- Hosts the L99BM114 multicell battery monitoring and balancing IC
- Voltage monitoring of every individual cell and of the entire battery node
- Voltage, current, and temperature sensing of each cell
- 5 GPIOs to connect temperature sensors as NTCs
- An NTC hosted on the L99BM114 to sense the chip temperature
- Passive balancing
- Compact size: 100 x 76 mm

1.1.2 Main components

1. ISOL port to connect the board to another STEVAL-BMS114 in a daisy chain
2. ISOH port to connect the board to the STEVAL-BMS1T
3. L99BM114 multicell battery monitoring and balancing IC
4. GPIOs for external NTC connection
5. Hot plug protection
6. Balancing resistors
7. Connector for the battery pack

Figure 2. STEVAL-BMS114 main components

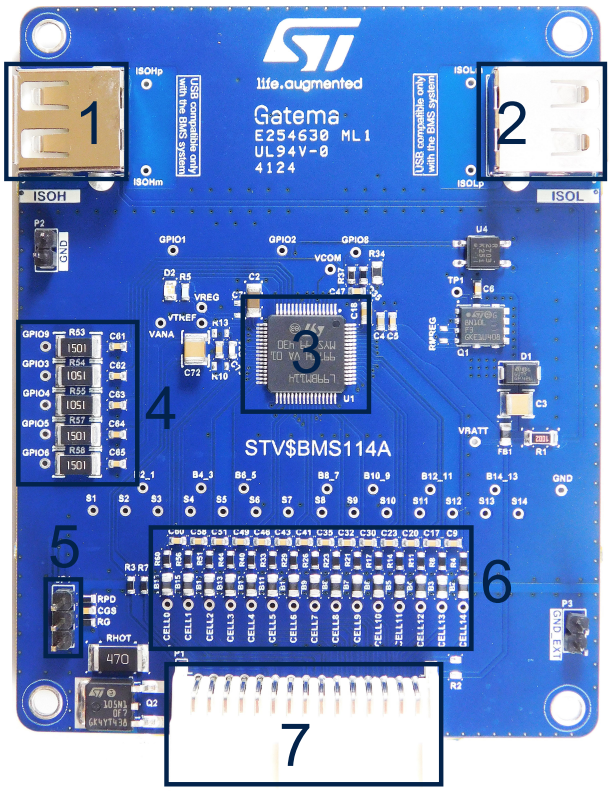


Table 1. STEVAL-BMS114 connector details

Name	Description	Type
ISOH	Isolated serial communication port: 1. VBUS 2. ISOHm 3. ISOHp 4. FaultH	USB Type A connector
ISOL	Isolated serial communication port: 1. VBUS 2. ISOLm 3. ISOLp 4. FaultH	USB Type A connector
P1	Battery connector: 1. VBAT_CELL 2. Cell 14 3. Cell 13 4. Cell 12 5. Cell 11 6. Cell 10 7. Cell 9 8. Cell 8 9. Cell 7 10. Cell 6 11. Cell 5 12. Cell 4 13. Cell 3 14. Cell 2 15. Cell 1 16. Cell 0 17. External Ground 18. External Ground 19. ISENSEP (external shunt resistor) 20. ISENSEN (external shunt resistor) 21. NTC 1+ 22. NTC 1- 23. NTC 2+ 24. NTC 2- 25. NTC 3+ 26. NTC 3- 27. NTC 4+ 28. NTC 4- 29. NTC 5+ 30. NTC 5-	Multi pin connector
P2	GND test point	1-2 shorted to GND
P3	GND_EXT test point	1-2 shorted to GND_EXT
JP1	Hot plug protection reference voltage	1-2 VREG (default) 2-3 VTREG

1.2 Embedded devices

1.2.1 L99BM114

The L99BM114 is intended for operation in systems using lithium battery packs. The IC embeds all the features needed to perform battery management. A single device can monitor from 4 up to 14 cells.

The device can be supplied with the same battery it monitors, and its main activity consists of monitoring cells and battery pack status through stack voltage measurement, cell voltage measurement, temperature measurement, and coulomb counting. Measurement and diagnostic tasks can be executed either on demand or periodically, with a programmable cycle interval.

Measurement data is available for an external microcontroller to perform charge balancing and to compute the state of health (SOH) and state of charge (SOC).

The IC works in normal mode performing measurement conversions, diagnostics, and communication. The device can also be put into a cyclic wakeup state in order to reduce the current consumption from the battery.

Passive cell balancing can be performed either via internal discharge path or via external MOSFETs. The controller can either manually control the balancing drivers or start a balancing task with a fixed duration. In the second case, the balancing may be programmed to continue also when the IC enters a low power mode called silent balancing, to avoid unnecessary current absorption from the battery pack.

Thanks to the GPIOs, the device also offers the possibility to operate a distributed cell temperature sensing via external NTCs resistances.

The external microcontroller can communicate with L99BM114 via SPI protocol. The physical layer can either be a traditional 4-wire based SPI or 2-wire transformer/capacitive based isolated interface through a dedicated isolated transceiver device.

The L99BM114 performs automatic validation of any failure involving the cells or the whole battery pack. The device can detect the loss of the connection to a cell or GPIO terminal. Moreover, it features a hardware self-check (HWSC) that verifies the correct functionality of the internal analog comparators and the ADCs. All these checks are automatically performed in case a failure involving both cells or when the battery pack is detected. The current sensing interface used for coulomb counting is also capable of detecting failures such as open wires and overcurrent in sleep mode. The cell balancing terminals can detect any short/open fault and the internal power MOS are protected against overcurrent.

1.3 Voltage operating range

The STEVAL-BMS114 maximum voltage range for each cell is 4.2 V.

The power supply range is from 9.6 V to a maximum of 64 V.

1.3.1 Linear regulators

The STEVAL-BMS114 features several linear voltage regulators, which are switched on according to a specific sequence at power-up (see L99BM114 datasheet).

VREG

This linear regulator exploits an external MOS to decrease the power dissipation inside the L99BM114.

It acts as a pre-regulator, supplying all other internal regulators (VANA, VCOM, VTREF, and VDIG). It is switched off in low power modes (sleep, silent balancing, off phase of the cyclic wakeup).

VANA

This low drop regulator supplies all the INTERNAL ADC, comparators, monitors, main bandgap, current generator, and other analogic blocks.

VCOM

The isolated communication receiver/transmitter and the GPIO output buffers are supplied by this low drop regulator.

VTREF

This low drop regulator is used to supply external components such as NTCs for temperature sensing.

The recommended application circuit in NTC analog front end guarantees that each NTC channel sinks no more than 500 µA.

VTREF regulator is disabled by default. Its operation can be controlled via SPI.

In absolute measurements, there is no reference value, while the ratiometric measurement is based on reference value defined by the VTREF regulator. If the VTREF goes low in case of an error, the VTREF varies to compensate this error.

All of the above regulators have dedicated UV/OV diagnostics.

2 BMS topologies

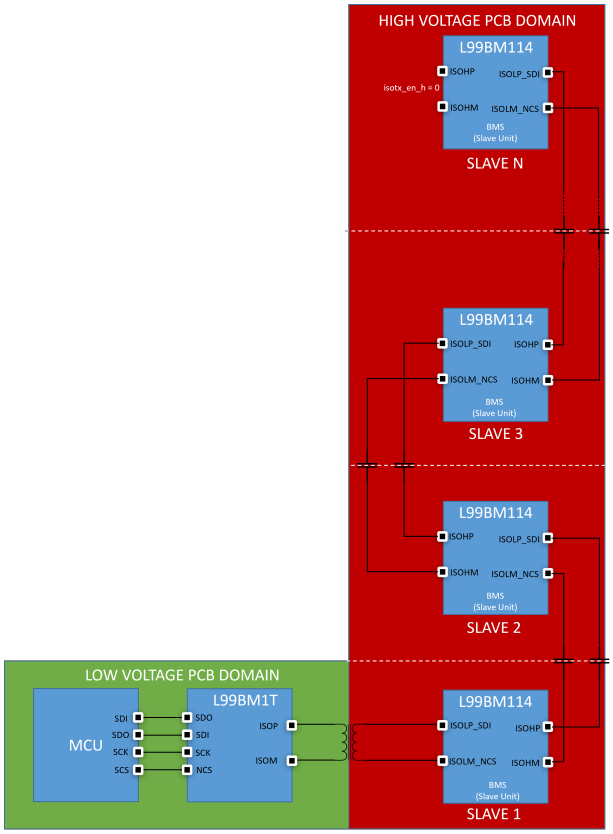
The STEVAL-BMS114 can work in two different daisy chain topologies: single access and dual access ring.

2.1 Single access configuration

In a single access daisy chain configuration, a series of BMS is connected to an MCU board through a single transceiver connected to the STEVAL-BMS114 isolated ISOL port. The BMS are connected to each other through the isolated ISOH port.

The MCU communicates with the STEVAL-BMS1T hosted L99BM1T transceiver through the SPI protocol. The transceiver converts these signals into ISO SPI signals to communicate with the BMS.

Figure 3. Single access BMS diagram



2.2 Dual access ring configuration

A dual access ring configuration is implemented by adding another transceiver that makes the communication bidirectional. The secondary transceiver is used as a backup in case the primary transceiver fails. Data moves in opposite directions around the rings, and each ring remains independent of the other unless the primary ring fails. The two rings are connected to continue the flow of data traffic.

Figure 4. Dual access ring BMS diagram

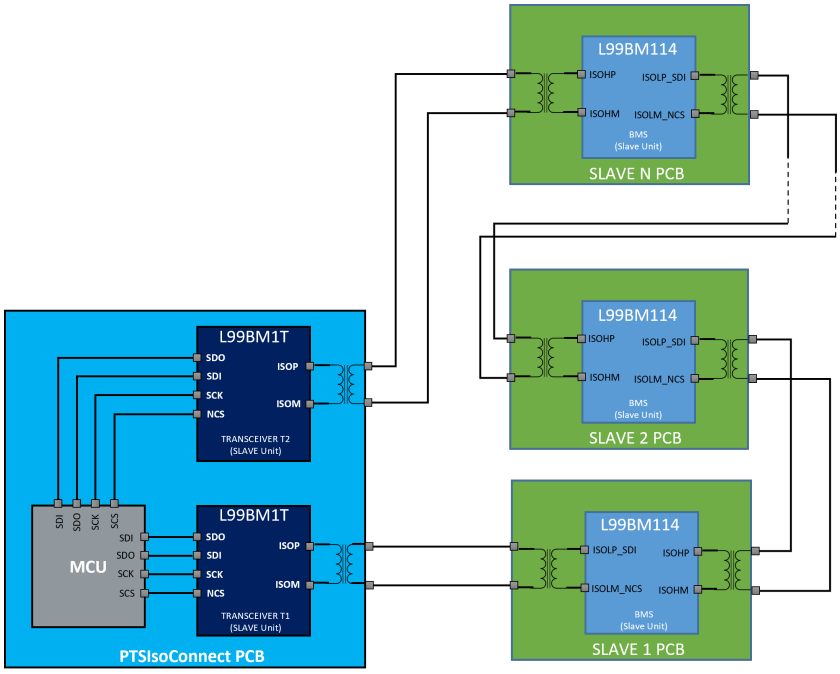
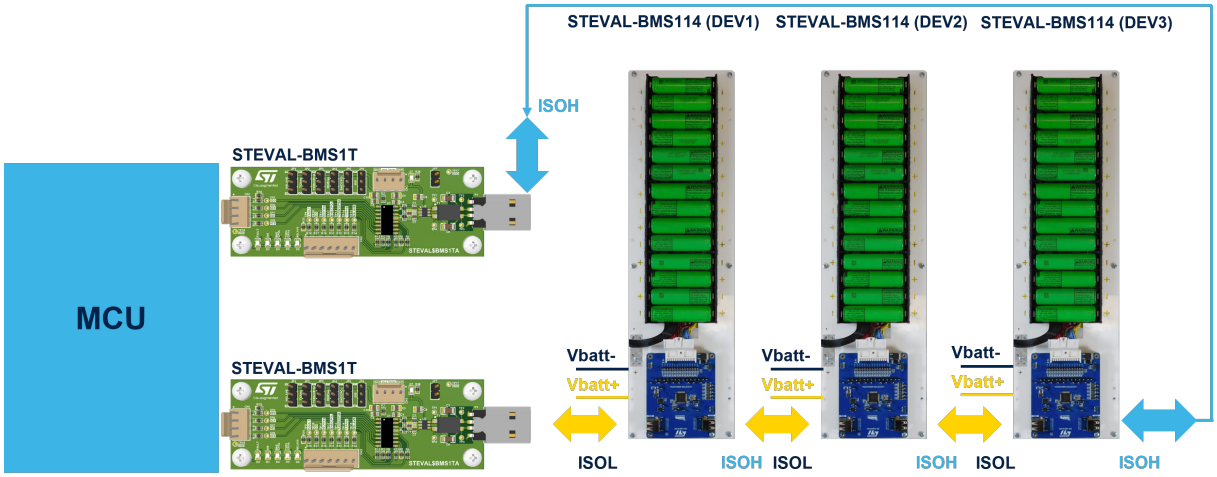


Figure 5. Dual ring configuration example



3 Cell current measurement

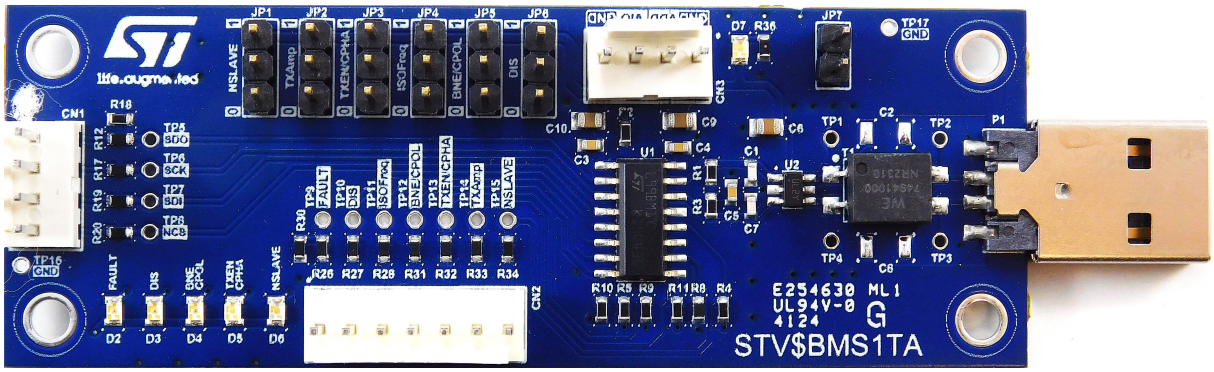
The current flowing into the external shunt resistance RSENSE is measured through a differential amplifier stage (connected between ISENSEP/ISENSEM pins) feeding a 18-bit ADC.

The current conversion chain can be enabled through the **CoulombCounter_en bit** and runs in background to perform the **Coulomb Counting Routine**.

Moreover, L99BM114 also allows you to synchronize the **Voltage Conversion Routine** and the **Coulomb Counting Routine** for a precise State Of Charge estimation. Every time an on-demand voltage conversion is requested by setting **SOC = 1**, the actual conversion start is delayed until the first useful current conversion takes place. This might result in a maximum delay of TCYCLEADC_CUR, which must be taken into account by user software only in the case that current ADC is enabled.

4 Fault condition in daisy chains

Figure 6. **Fault LED on the STEVAL-BMS1T**



The fault LED on the STEVAL-BMS1T is related to the state of all the BMS nodes in the daisy chain. If an undervoltage, overvoltage, overcurrent, or overtemperature occurs on any cell of a BMS, a fault condition is detected. To solve this condition, diagnosis via software code must be activated.

The overcurrent detection is linked to a threshold defined in the application, not in the software driver. The threshold must be modified according to the load. For further details, refer to the L99BM114 datasheet.

5 Cell balancing

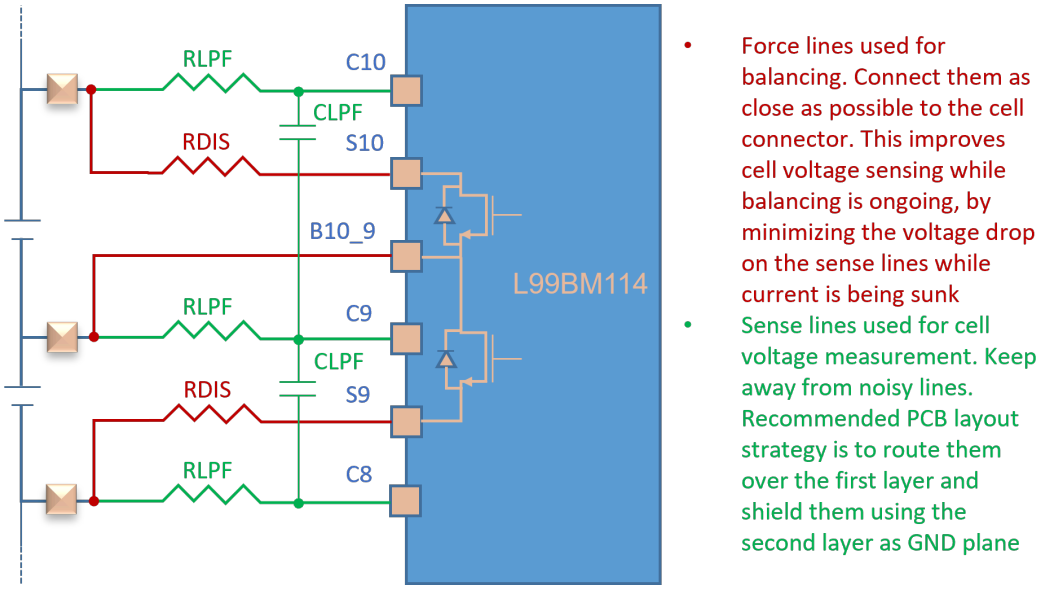
In the L99BM114, the Sx and Bx_x-1 pins are used to balance the charge of the cells by discharging the ones with a higher SOC. Balancing can be performed either with external resistors or internal MOSFETs.

Cell balance drivers are powered by VBAT stack voltage. Hence, balancing is theoretically possible even at low cell voltages, except for cell 14. In case $V_{CELL14} < V_{CELL14\_BAL\_MIN}$, the corresponding balancing circuitry does not operate properly, and false overcurrent detection may occur.

5.1 Passive cell balancing with internal MOSFETs

The board is designed using internal MOSFETs.

Figure 7. Cell monitoring with internal balancing

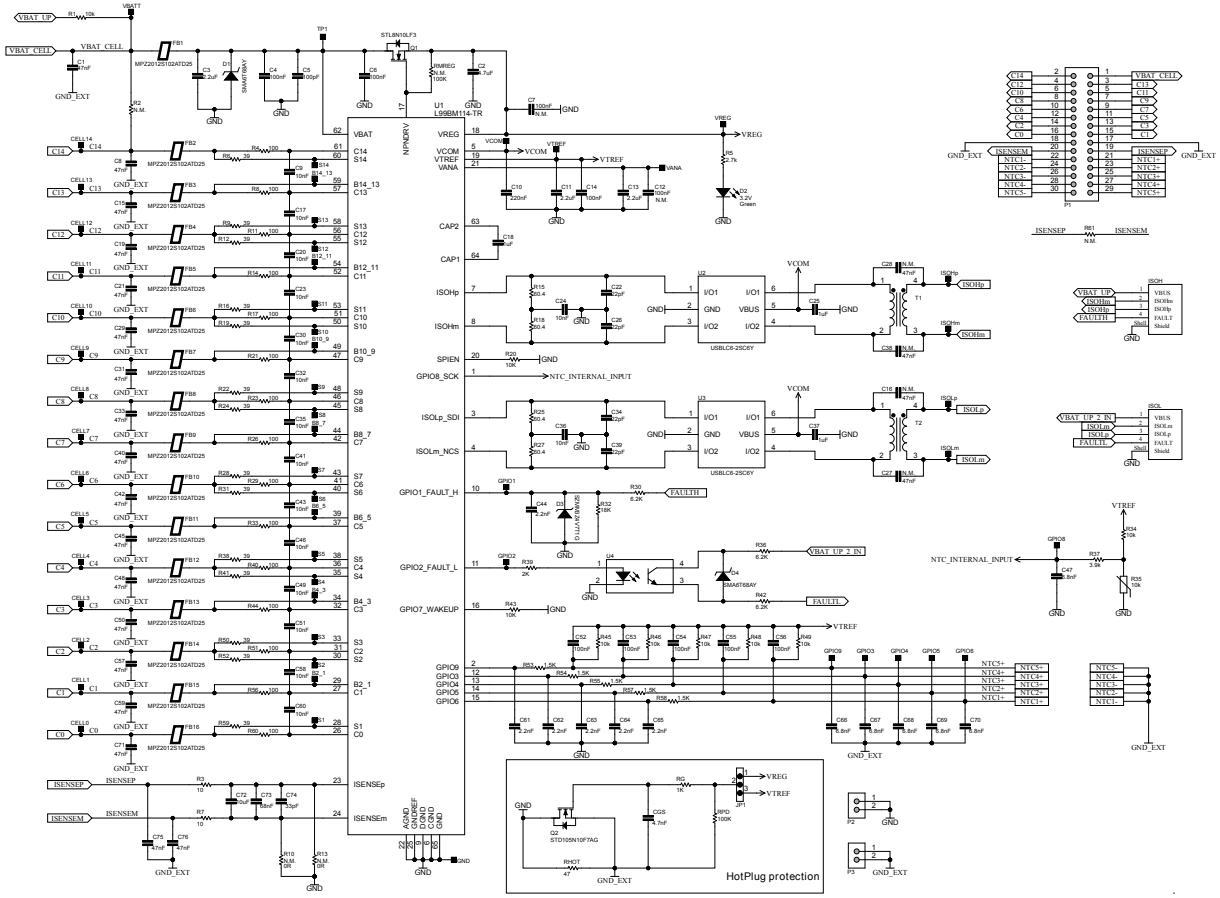


The on-chip MOSFETs are switched on to sink a current from the cell, thus dissipating charge on RDIS. The affordable balancing current is restricted by the thermal relief on the current source circuits.

The maximum balance current on each cell is 200 mA. All cells can be balanced simultaneously, if the junction temperature does not exceed the maximum operating defined in the datasheet. To prevent thermal overstress, the die temperature diagnostic and overtemperature protections are implemented.

6 Schematic diagram

Figure 8. **STEVAL-BMS114 circuit schematic**



7 Bill of materials

Table 2. **STEVAL-BMS114 bill of materials**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	18	C1, C8, C15, C19, C21, C29, C31, C33, C40, C42, C45, C48, C50, C57, C59, C71, C75, C76	47nF	0603 - 50V - X7R Class II	WE	885012206093
2	1	C2	4.7uF	1206 - 50V - X7R Class II	WE	885012208094
3	1	C3	2.2uF	1210 - 100V - X7R Class II	WE	885012209071
4	3	C4, C6, C14	100nF	0603 - 100V - X7R Class II	WE	885012206120
5	1	C5	100pF	0603 - 100V - X7R Class II	WE	885012206102
6	2	C7, C12	N.M.	0603	N.M.	N.M.
7	16	C9, C17, C20, C23, C24, C30, C32, C35, C36, C41, C43, C46, C49, C51, C58, C60	10nF	0603 - 50V - X7R Class II	WE	885012206089
8	1	C10	220nF	0603 - 50V - X7R Class II	WE	885012206125
9	2	C11, C13	2.2uF	0805 - 25V - X7R Class II	WE	885012207079
10	4	C16, C27, C28, C38	N.M.	1206	N.M.	N.M.
11	3	C18, C25, C37	1uF	0805 - 50V - X7R Class II	WE	885012207103
12	4	C22, C26, C34, C39	22pF	0603 - 50V - NP0 Class I	WE	885012006053
13	6	C44, C61, C62, C63, C64, C65	2.2nF	0603 - 50V - X7R Class II	WE	885012206085
14	6	C47, C66, C67, C68, C69, C70	6.8nF	0603 - 50V - X7R Class II	WE	885012206088
15	5	C52, C53, C54, C55, C56	100nF	0603 - 50V - X7R Class II	WE	885012206095
16	1	C72	10uF	1210 - 50V - X7R Class II	WE	885012209073
17	1	C73	68nF	0603 - 50V - X7R Class II	WE	885012206094
18	1	C74	33pF	0603 - 50V - NP0 Class I	WE	885012006054
19	1	CGS	4.7nF	0603 - 50V - X7R Class II	WE	885012206087
20	2	D1, D4	SMA6T68AY, SMA	Automotive 600 W, 68V TVS in SMA	ST	SMA6T68AY
21	1	D2	Green	0805 - Led Green - 3.2V	WE	150080GS75000
22	1	D3	SZMM3Z4V7T1G	4.7V Zener Voltage Regulators, 300mW	Onsemi	SZMM3Z4V7T1G

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
23	16	FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11, FB12, FB13, FB14, FB15, FB16	1K@100MHz	Ferrite Beads Multi-Layer Power 1KOhm 25% 100MHz 1.5A 0.15Ohm DCR 0805	TDK	MPZ2012S102ATD25
24	2	ISOH, ISOL	61400416021	USB 2.0 Type A, Receptacle, Horizontal, THT	WE	61400416021
25	1	JP1		THT Vertical 3 pins Header, Pitch 2.54 mm, Single Row	WE	61300311121
26	1	P1		2.00mm - WR-WTB - Male Dual Row Horizontal Shrouded Header w. positive locking	WE	62403021722
27	2	P2, P3	61300211121	2.54mm - WR-PHD Pin Header, THT, pitch 2.54mm, Single Row, Vertical, 2p	WE	61300211121
28	1	Q1	STL8N10LF3, PowerFLAT 5x6_WF type C	Automotive-grade N-channel 100 V, 25 mΩ typ., 7.8 A STripFET™ F3 Power MOSFET in a PowerFLAT™ 5x6 package	ST	STL8N10LF3
29	1	Q2	STD105N10F7AG, DPAK_TO-252	Automotive-grade N-channel 100 V, 6.8 mΩ typ., 80 A, STripFET™ F7 Power MOSFET in a DPAK package	ST	STD105N10F7AG
30	1	R1	10k	1206 - ±1% - 0.66W	Panasonic	ERJUP8F1002V
31	1	R2	N.M.	0805	N.M.	N.M.
32	2	R3, R7	10	0603 - ±1% - 0.25W	Panasonic	ERJPA3F10R0V
33	15	R4, R8, R11, R14, R17, R21, R23, R26, R29, R33, R40, R44, R51, R56, R60	100	0603 - ±1% - 0.25W	Panasonic	ERJPA3F1000V
34	1	R5	2.7k	0603 - ±1% - 0.125W	Vishay	MCT06030C2701FP500
35	14	R6, R9, R12, R16, R19, R22, R24, R28, R31, R38, R41, R50, R52, R59	39	2010 - ±1% - 1.25W	TE Connectivity	CRGP2010F39R
36	3	R10, R13, RMREG	N.M.	0603	N.M.	N.M.
37	4	R15, R18, R25, R27	60.4	0603 - ±1% - 0.1W	Panasonic	ERJ3EKF60R4V
38	2	R20, R43	10K	0603 - ±1% - 0.2W	Panasonic	ERJP03F1002V
39	3	R30, R36, R42	6.2K	0805 - ±1% - 0.5W	Panasonic	ERJP06F6201V
40	1	R32	18K	0603 - ±1% - 0.2W	Panasonic	ERJP03F1802V
41	6	R34, R45, R46, R47, R48, R49	10k	0805 - ±1% - 0.5W	Panasonic	ERJP6WF1002V

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
42	1	R35	10k	0603 - ±1% - 0.1W	TDK	NTCG163JH103HTDS
43	1	R37	3.9k	0603 - ±1% - 0.1W	Panasonic	ERJ3EKF3901V
44	1	R39	2K	0603 - ±1% - 0.2W	Panasonic	ERJP03F2001V
45	5	R53, R54, R55, R57, R58	1.5K	2010 - ±1% - 2W	TE Connectivity	35021K5FT
46	1	R61	N.M.	N.M.	N.M.	N.M.
47	1	RG	1K	0603 - ±1% - 0.25W	Panasonic	ERJPA3F1001V
48	1	RHOT	47	2512 - ±5% - 1W	TE Connectivity	352047RJT
49	1	RPD	100K	0603 - ±1% - 0.25W	Panasonic	ERJP03F1003V
50	2	T1, T2	125uH	Transformer for BMS	WE	74941000
51	1	U1	L99BM114-TR, TQFP64	Chip for battery management applications with daisy chain up to 31 devices	ST	L99BM114-TR
52	2	U2, U3	USBLC6-2SC6Y, OT23-6L	Automotive ESD protection for high speed interfaces.	ST	USBLC6-2SC6Y
53	1	U4	PS2703-1-A	4-Pin Phototransistor Optocoupler	Renesas	PS2703-1-A
54	1	for blister	60900213421	WR-PHD 2.54 mm Multi-Jumper Jumper with Test Point	WE	60900213421
55	4	for blister	970080365	WA-SPAII Plastic Spacer Stud, metric, internal/ internal	WE	970080365
56	4	for blister	97790403111	WA-SCRW Pan Head Screw w. cross slot M3	WE	97790403111
57	1	for blister	624030213322	WR-WTB 2.00 mm Female Dual Row Terminal Housing w. positive locking	WE	624030213322
58	30	for blister	62400113722	WR-WTB 2.00 mm Female Dual Row Crimp Contact	WE	62400113722

8 Board versions

Table 3. **STEVAL-BMS114 versions**

Finished good	Schematic diagrams	Bill of materials
STV$BMS114A[1]	STV$BMS114A schematic diagrams	STV$BMS114A bill of materials

1. *This code identifies the STEVAL-BMS114 evaluation board first version.*

9 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

Revision history

Table 4. **Document revision history**

Date	Version	Changes
10-Jan-2025	1	Initial release.

Contents

List of figures

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