

Evaluation board with STM32MP257F MPU

Introduction

The **STM32MP257F-EV1** Evaluation board is designed as a complete demonstration and development platform for the STMicroelectronics **STM32MP257F** microprocessor based on Arm® dual-core Cortex®-A35 1.5 GHz and Cortex®-M33 400 MHz, and the **STPMIC25APQR** companion chip.

It leverages the capabilities of the STM32MP257F microprocessor to allow users to develop easily applications using STM32 MPU OpenSTLinux Distribution software (such as **STM32MP2Starter**).

The STM32MP257F-EV1 Evaluation board, shown in [Figure 1](#) and [Figure 2](#), is used as a reference design for the user application development. It cannot be considered as the hardware design of a final application. The hardware features of the Evaluation board are available for users to develop their applications: USB, 3×Ethernet, microSD™ card, user buttons, PCIe, LVDS/DSI and CSI for a camera module. Extension headers allow the easy connection of a third-party board for a specific application.

STLINK-V3EC is integrated on the board as an embedded in-circuit debugger and programmer for the STM32 MPU and the USB Virtual COM port bridge.

Figure 1. STM32MP257F-EV1 top view

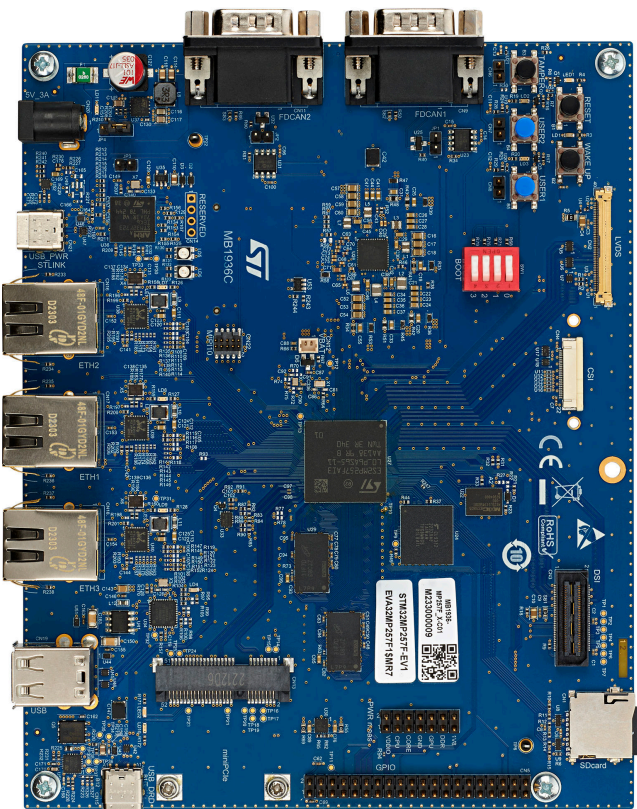
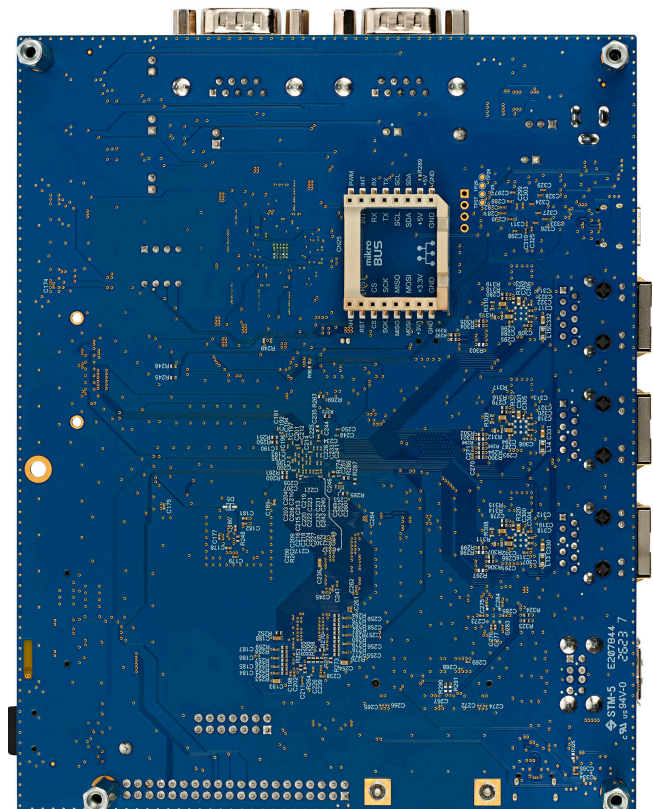


Figure 2. STM32MP257F-EV1 bottom view



Pictures are not contractual.

1 Features

- STM32MP257FAI3 microprocessor based on the Arm® dual-core Cortex®-A35 1.5 GHz and Cortex®-M33 400 MHz in a TFBGA436 package
- ST power management [STPMIC25APQR](#)
- Two 16-Gbit DDR4 DRAMs
- 512-Mbit (64 Mbytes) S-NOR flash memory
- 32-Gbit (4 Gbytes) eMMC v5.0
- Three 1-Gbit/s Ethernet (RGMII) with TSN switch compliant with IEEE-802.3ab
- High-speed USB Host 2-port hub
- High-speed USB Type-C® DRP
- Four user LEDs
- Two user, one tamper, and one reset push-buttons
- Wake-up button
- Four boot pin switches
- Board connectors:
 - Three Ethernet RJ45
 - Two USB Host Type-A
 - USB Type-C®
 - microSD™ card holder
 - Mini PCIe
 - Dual-lane MIPI CSI-2® camera module expansion connector
 - Two CAN FD
 - LVDS
 - MIPI10
 - GPIO expansion connector
 - mikroBUS™ expansion connector
 - VBAT for power backup
- On-board STLINK-V3EC debugger/programmer with USB re-enumeration capability: Two Virtual COM ports (VCPs), and debug port
- Mainlined open-source Linux® STM32 MPU OpenSTLinux Distribution and STM32CubeMP2 software with examples
- Linux® Yocto project, Buildroot, and STM32CubeIDE as development environments

STM32 Arm Cortex MPUs are based on the Arm® Cortex®-A and Cortex®-M processors.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

arm

2 Ordering information

To order the STM32MP257F-EV1 Evaluation board, refer to [Table 1](#). Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board reference	Target STM32
STM32MP257F-EV1	MB1936	STM32MP257FAI3

2.1 Codification

The meaning of the codification is explained in [Table 2](#).

Table 2. Codification explanation

STM32MP2XXY-EV1	Description	Example: STM32MP257F-EV1
STM32MP2	MPU series in STM32 Arm Cortex MPUs	STM32MP2 series
XX	MPU product line in the series	STM32MP257 product line
Y	Option: <ul style="list-style-type: none"> F: Secure boot, cryptography hardware, maximal frequency 	Secure boot, cryptography hardware, 1.5 GHz
EV1	Toolkit type: <ul style="list-style-type: none"> EV1: Evaluation board 	Evaluation board

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10 and 11, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to USB Type-C® cable

Note: macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.
Linux® is a registered trademark of Linus Torvalds.
Windows is a trademark of the Microsoft group of companies.

3.2 Development tools

- Linux® Yocto Project®
- Buildroot
- STMicroelectronics - STM32CubeIDE

3.3 Demonstration software

The STM32 MPU OpenSTLinux Distribution and STM32CubeMP2 base demonstration software is preloaded in the microSD™ to demonstrate the device peripherals in standalone mode easily. The latest versions of the demonstration source code and associated documentation can be downloaded from www.st.com.

3.4 EDA resources

All board design resources, including schematics, EDA databases, manufacturing files, and the bill of materials, are available from the [STM32MP257F-EV1](#) product page at www.st.com.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between pin 1 and pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

5 Safety recommendations

5.1 Targeted audience

This product targets users with at least basic electronics or embedded software development knowledge like engineers, technicians, or students.

This board is not a toy and is not suited for use by children.

5.2 Handling the board

This product contains a bare printed circuit board and like all products of this type, the user must be careful about the following points:

- The connection pins on the board might be sharp. Be careful when handling the board to avoid hurting yourself.
- This board contains static sensitive devices. To avoid damaging it, handle the board in an ESD-proof environment.
- While powered, do not touch the electric connections on the board with your fingers or anything conductive. The board operates at a voltage level that is not dangerous, but components might be damaged when shorted.
- Do not put any liquid on the board and avoid operating it close to water or at a high humidity level.
- Do not operate the board if it is dirty or dusty.
- The pins of the board are exposed and must not come into contact with a metal surface, as this can produce a short circuit and damage the board.

5.3 Delivery recommendations

Before the first use, inspect the board for any damage that may have occurred during shipment. Ensure that all socketed components are securely fixed in their sockets and that nothing is loose in the plastic bag.

6 Quick start

Before installing and using the product, accept the evaluation product license agreement from the www.st.com/epl webpage.

Follow the sequence below to configure the STM32MP257F-EV1 Evaluation board and launch the demonstration application (refer to [Figure 4](#) and [Figure 5](#) for component location).

To start using this board, follow the steps below:

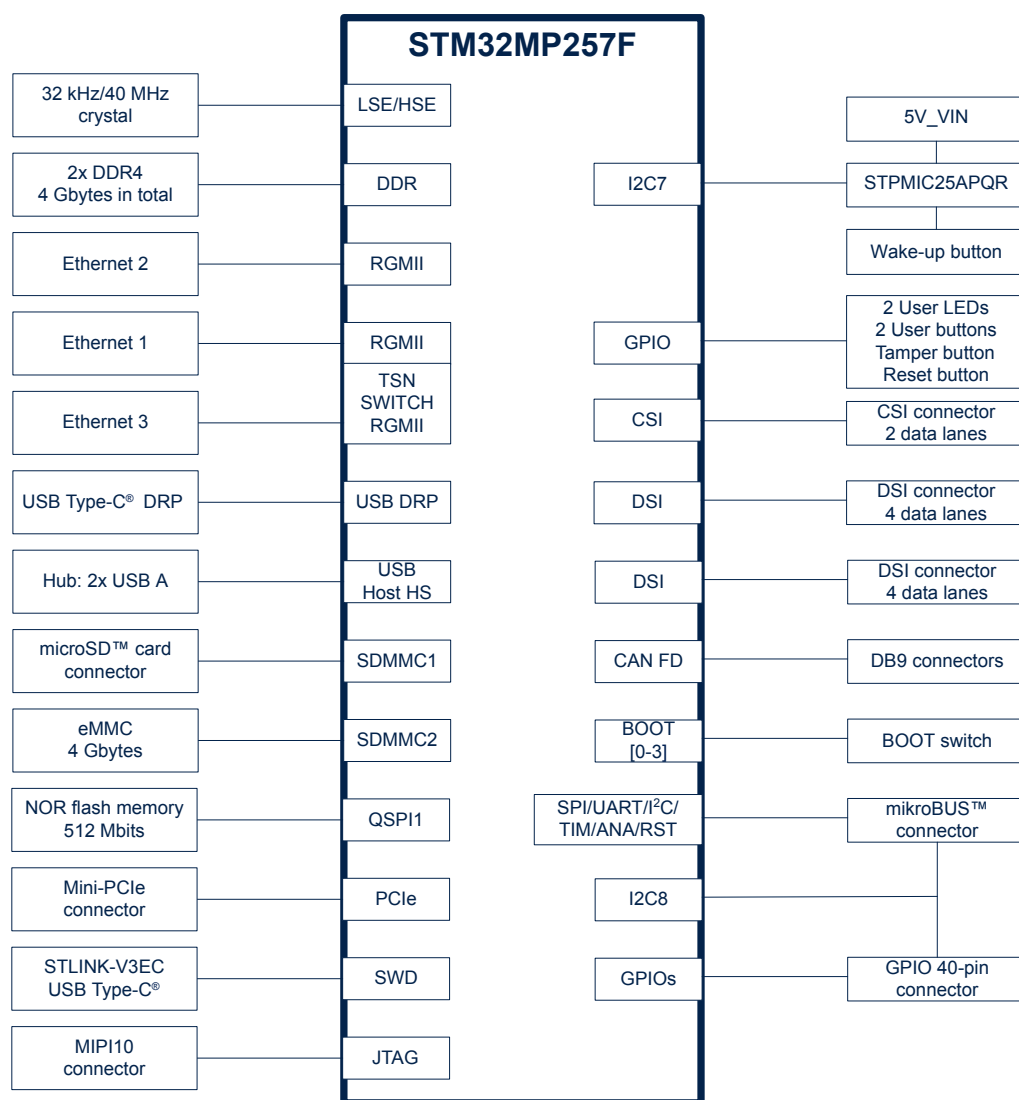
- To identify correctly all device interfaces from the host PC, install the Evaluation USB driver available on the www.st.com website, before connecting the board.
- Check that jumper JP4 is in the right position ([2-3]: power from 5V/3A jack wall charger on CN20, [1-2]: 5 V/3 A USB Type-C® charger on CN21) and JP3 is OFF on the board.
- To power the board, connect the Evaluation board to a 5 V/3 A USB Type-C® charger with its cable through the USB connector (CN21) or to the computer with USB Type-C®. As a result, the 5V_PWR (LD11) and POWER (LD6) green LEDs light up, and the COM LED (LD5) blinks.
- The software demonstration and several software examples, which allow the user to use the Evaluation features, are available at the www.st.com/stm32mp2 webpage.
- Develop an application using the available examples.

7 Hardware layout and configuration

7.1 Hardware block diagram

STM32MP257F-EV1 is designed around the STM32MP257FAI3 microprocessor in the TFBGA436 package. The hardware block diagram (refer to Figure 3) illustrates the connection between the microprocessor and its peripherals, such as Ethernet, CSI camera connector, USB Type-C® DRP and USB Type-A connectors, GPIO expansion, and embedded ST-LINK.

Figure 3. STM32MP257F-EV1 hardware block diagram



DT59425V1

7.2 Hardware board layout

Figure 4 and Figure 5 help users locate these features on the STM32MP257F-EV1 board.

Figure 4. STM32MP257F-EV1 PCB layout (top side)

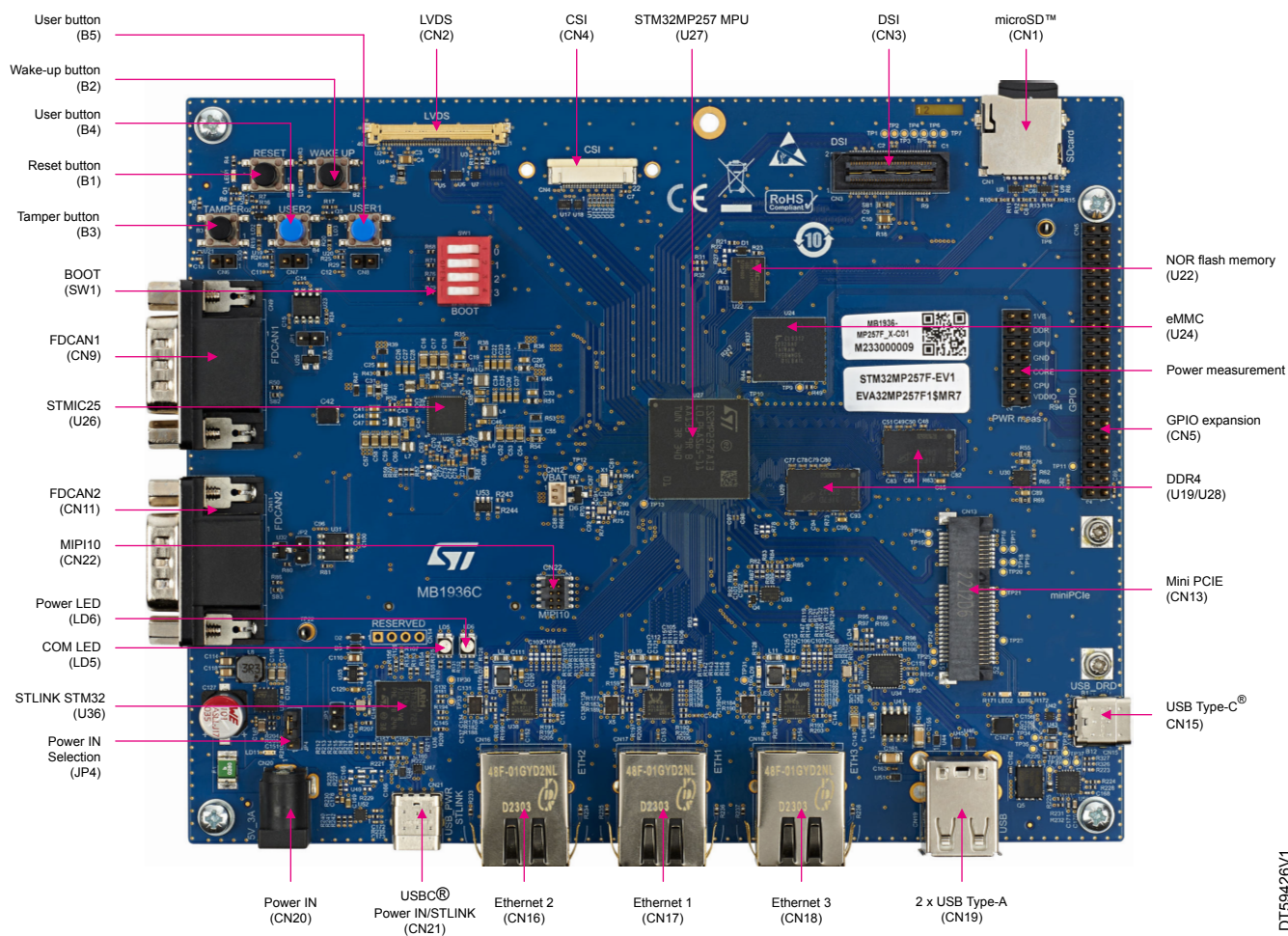
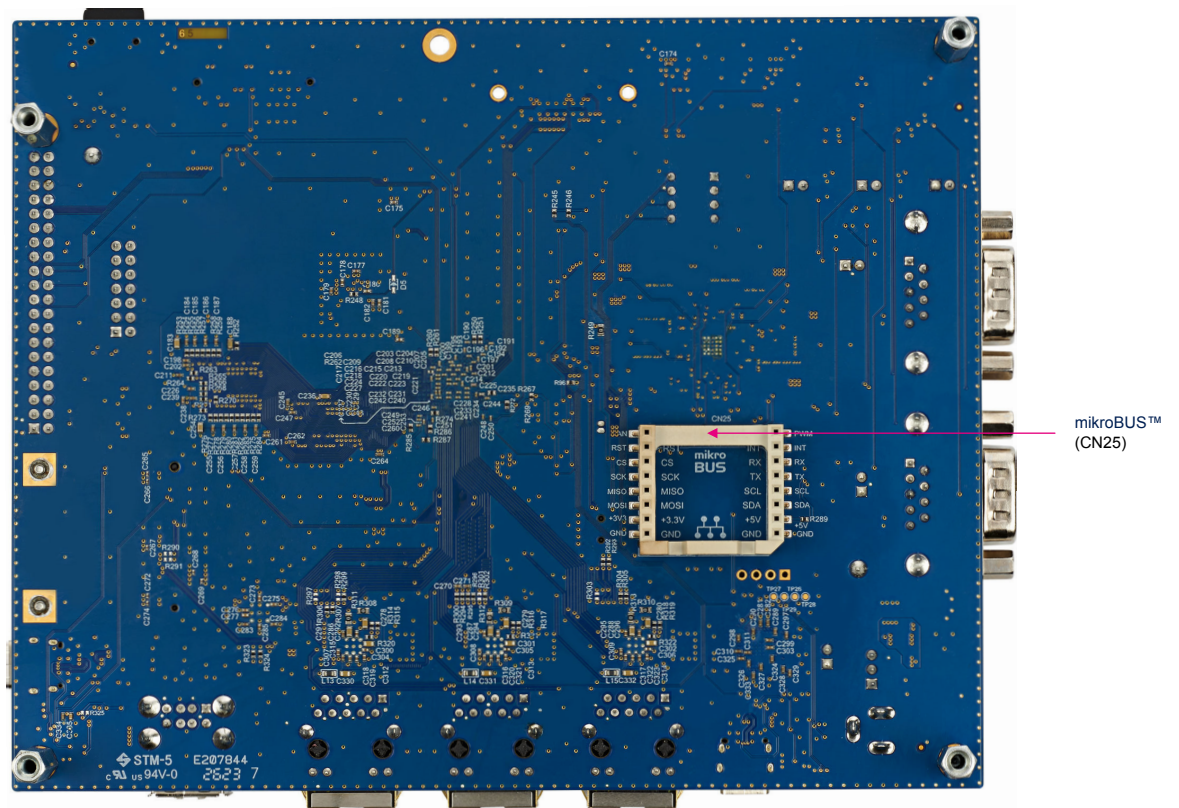


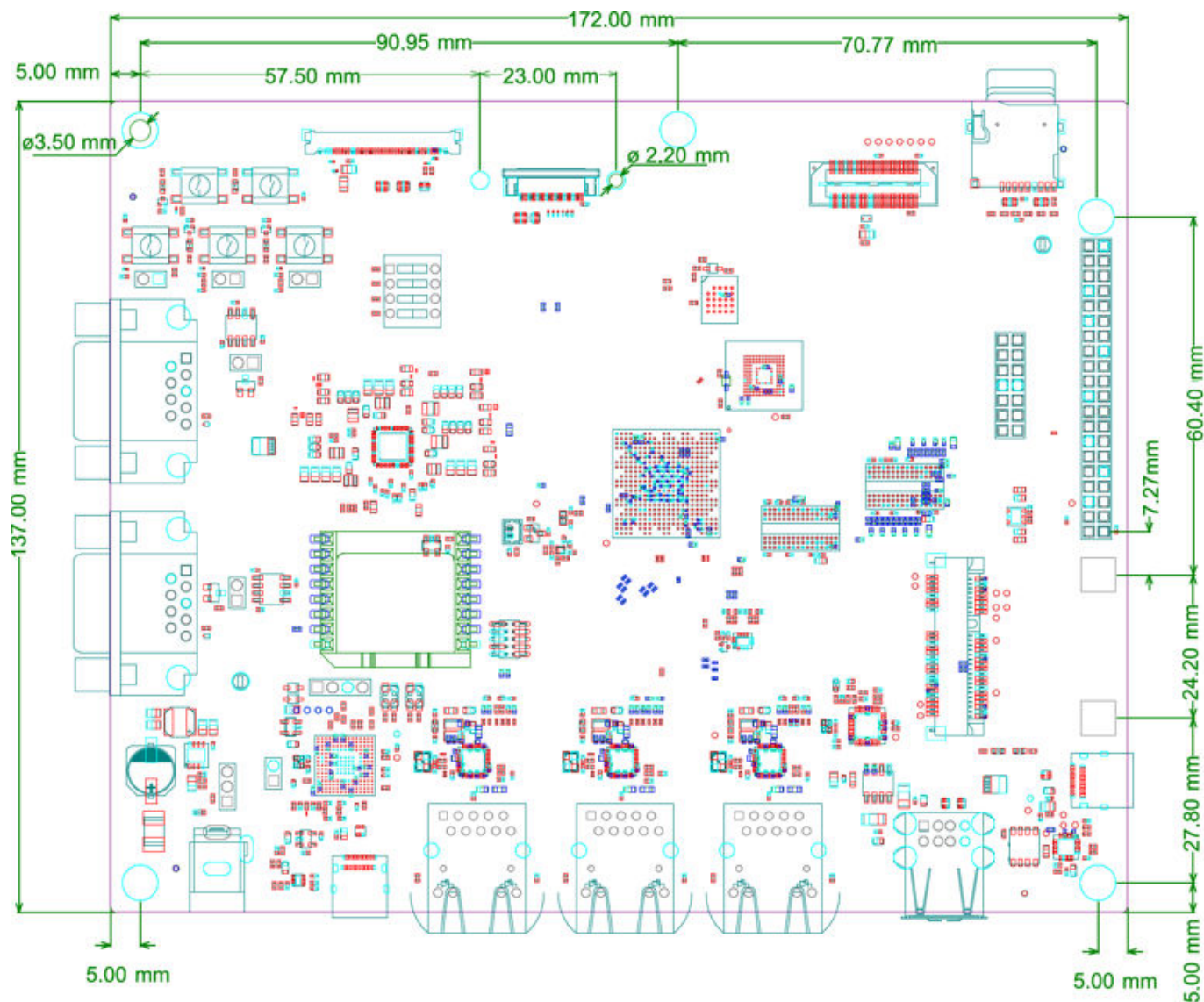
Figure 5. STM32MP257F-EV1 PCB layout (bottom side)



DT59427V1

7.3

Figure 6. STM32MP257F-EV1 Evaluation board mechanical dimensions (in millimeters)



7.4 Embedded STLINK-V3EC

This section gives some information about the implementation of STLINK-V3EC on this board.

Attention: *Before using STLINK-V3EC, ensure that the complete system is well-configured and up-to-date with the STLINK-V3EC function. For detailed information about the STLINK-V3EC features such as drivers, firmware upgrades, USB interface selection, and LED management, refer to the technical note Overview of ST-LINK derivatives (TN1235).*

7.4.1 Description

To debug the onboard STM32MP257 device, the STLINK-V3EC programming and debugging tool is integrated in STM32MP257F-EV1. The embedded STLINK-V3EC supports only SWD and VCP for STM32 devices. For information about the debugging and programming features of STLINK-V3EC, refer to the user manual *ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32 (UM1075)* and to the corresponding technical note Overview of ST-LINK derivatives (TN1235).

7.4.2 STLINK-V3EC deactivation (Reset mode)

It is simple to deactivate the STLINK-V3EC function by putting a jumper on the JP3 header, to connect STLK_Nrst to GND. Programming, debugging, and monitoring through ST-LINK are impossible in this Reset state, where all STLINK-V3EC PIOs are in high impedance.

Attention: *The Reset mode is useful for connecting an external probe to the MIPI10 debug (CN22) connector for the embedded STM32MP2 debug.*

7.4.3 Drivers

Before connecting STM32MP257F-EV1 to a Windows® PC via the USB, a driver for STLINK-V3EC must be installed (it is not required for Windows 10® and above). It is available from the www.st.com webpage.

If STM32MP257F-EV1 is connected to the PC before the driver is installed, some STM32MP257F-EV1 interfaces might be declared *Unknown* in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager.

7.4.4 STLINK-V3EC firmware upgrade

STLINK-V3EC embeds a firmware upgrade mechanism for in-place upgrades through the USB port. Firmware might evolve during the lifetime of the STLINK-V3EC product (addition of new functionalities, bug fixes, or support of new microprocessor families). Therefore, it is recommended to visit the www.st.com website periodically before starting to use STM32MP257F-EV1 to stay up-to-date with the latest firmware version.

7.4.5 Use of STLINK-V3EC to program and debug the on-board STM32

To debug the on-board STM32, no specific hardware configuration is required. Programming through STLINK-V3EC is not supported with microprocessor products.

7.4.6 LED signification

Refer to the technical note *Overview of ST-LINK derivatives (TN1235)*.

7.5 Power supply

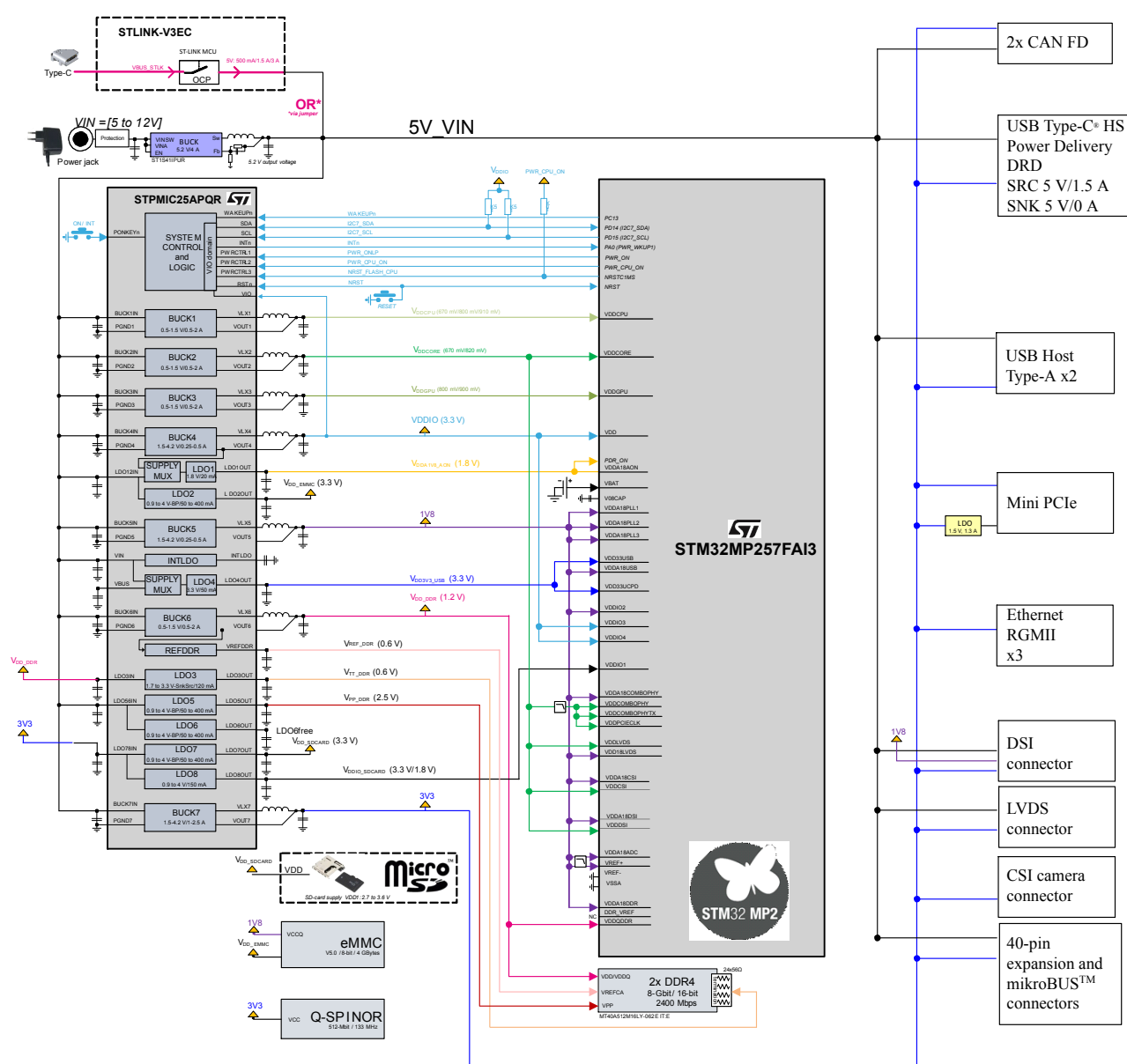
This product is not delivered with a power supply.

A power supply unit or auxiliary equipment complying with the EN 62368-1 (2014+A11/2017) standard and safety extralow voltage (SELV/ES1) with limited power capability (LPS/PS2) must power this equipment.

7.5.1 Power diagram

Figure 7 describes the power architecture and the maximum voltage and current limits, under which functions can be safely used on the STM32MP257F-EV1 product. In any case, ensure the total power budget of the application always conforms to the selected 5 V power source mode, if not, malfunction can occur. For detailed configuration, refer to the relevant function description and technical application notes.

Figure 7. Power diagram



7.5.2 Power source selection

It is possible to configure the STM32MP257F-EV1 Evaluation board with the JP4 header to use any of the two sources described in Table 4 for the 5V DC power supply.

Table 4. 5 V selection configuration jumper (JP4)

Reference	Jumper ⁽¹⁾	Function
JP4	[2-3]	5 to 12 V/3 A is supplied by a power jack (CN20).
	[1-2]	5 V is supplied by the USB Type-C [®] connector of the ST-LINK (CN21).

1. The default setting is in bold

In all the above power source configurations, the 5V LED (LD11) must be lit when the Evaluation board is correctly powered by the 5V supply.

7.5.3 5 V power supply

The STM32MP257F-EV1 Evaluation board is designed to be powered by a 5V power source. It is recommended to use a power supply able to source 15 W such as:

- VBUS 5 V connected to the CN21 connector through a USB Type-C[®] to USB Type-C[®] cable . The USB_PWR_CC1 and USB_PWR_CC2 lines are connected to PC3 and PC4 of the ST-LINK MCU respectively to check what is connected to CN21 and control features enabling:
 - Legacy cable
 - Personal computer
 - 5 V DC power source at 3 A

Depending on the current needed on the devices connected to the USB port, and the board itself, power limitations can prevent the system from working as expected. The user must ensure that the STM32MP257F-EV1 Evaluation board is supplied with the correct power source depending on the current needed. It is recommended to use a USB Type-C[®] to USB Type-C[®] cable.

- Power supply source from Wall charger connected to CN20:
 - It is recommended to supply the boards with a 5 to 12 V/15 W min source.

7.5.4 STPMIC25APQR power supply

For general information concerning STPMIC25APQR, refer to the datasheet on the www.st.com website.

For the boot on the SD card (EV1 application), the STPMIC25APQR NVM is programmed to enable LDO7 and LDO8.

For information about STPMIC25APQR NVM, refer to the application note *How to use STPMIC25 for a wall adapter powered application on STM32MP25x lines MPUs* (AN5727).

Note: *STPMIC25DPQR part number is also available. There is no need to program the nonvolatile memory: LDO7 and LDO8 are enabled by default. Fully compatible with STPMIC25APQR.*

STPMIC25APQR supply

- VDDCPU (BUCK1) used to supply the CPU1 of the STM32MP257
 - Value: 670 mV LPLV-STOP1
 - Value: 800 mV RUN at 1.2 GHz
 - Value: 910 mV RUN at 1.5 GHz
- VDDCORE (BUCK2) used to supply the digital logic of the STM32MP257
 - Value: 670 mV LPLV-STOP
 - Value: 820 mV RUN
- VDDGPU (BUCK3) used to supply the GPU of the STM32MP257
 - Value: 800 mV RUN at 800 MHz
 - Value: 900 mV RUN at 900 MHz
- VDDIO (BUCK4) used to supply the VDD domains of the STM32MP257
 - Value: 3.3 V
- 1V8 (BUCK5) used to supply the 1.8V analog domain of the STM32MP257
 - Value: 1.8 V
- VDD_DDR (BUCK6) used to supply the DDR4
 - Value: 1.2 V
- 3V3 (BUCK7) used to supply some of the 3.3V domains of the STM32MP257F-EV1 peripherals
 - Value: 3.3 V
- VREF_DDR provides the DDR reference voltage
 - Value: 0.6 V
- VDDA1V8_ON (LDO1) used to supply the 1.8 V always ON domain of the STM32MP257
 - Value: 1.8 V
- VDD_EMMC (LDO2) used to supply the eMMC memory
 - Value: 3.3 V
- VTT_DDR (LD03) used to supply the DDR4 termination
 - Value: 0.6 V
- VDD3V3_USB (LD04) used to supply the USB PHY of the STM32MP257
 - Value: 3.3 V
- VPP_DDR (LDO5) used to supply the DDR4 VPP
 - Value: 2.5 V
- FREE (LDO6) not used
 - Value: None
- VDD_SDCARD (LDO7) used to supply the microSD™ card
 - Value: 3.3 V
- VDDIO_SDCARD (LDO8) used to supply the I/O of the microSD™ card
 - Value: 3.3 V or 1.8 V

7.5.5 Other power supply

A dedicated LDO provides the 1V5_PCIE for the 1.5 V of the mini-PCIE connector.

7.6 Clock sources

7.6.1 LSE clock reference

The LSE clock reference on the STM32MP257FAI3 microprocessor is provided by the external crystal X2:

- 32.768 kHz crystal

7.6.2 HSE clock reference

The HSE clock reference on the STM32MP257FAI3 microprocessor is provided by the external crystal X4:

- 40 MHz crystal

7.7 Reset sources

The reset signal of STM32MP257F-EV1 is active LOW. The internal pull-up of the STM32MP2 forces the NRST signal to a high level.

The sources of reset are:

- The reset button B1 (black button)
- STPMIC25APQR
- The embedded STLINK-V3EC
- STM32MP257FAI3

7.8 Boot options

At startup, the boot pins select the boot source used by the internal bootROM. [Table 5](#) describes the configurations of the boot pins.





Table 5. Boot mode pin simplified table

Boot 3	Boot 2	Boot 1	Boot 0	Boot mode A35	Boot mode M33
0	0	0	0	Forced USB boot for flash programming	Forced USB boot for flash programming
0	0	0	1	SD card on SDMMC1	-
0	0	1	0	eMMC on SDMMC2	-
0	0	1	1	Development boot	
0	1	0	0	QSPI	-
0	1	1	1	-	SD card on SDMMC1
1	0	0	0	-	eMMC on SDMMC2
1	0	1	1	-	QSPI

Note: For the complete table, refer to the STM32MP257 datasheet.

Table 6 shows the configurations of the boot-related switch SW1.

Table 6. Boot mode switch SW1 example of A35

BOOT0 BOOT1 BOOT2 BOOT3	Boot pin selection	Boot mode
	BOOT0: 0 BOOT1: 0 BOOT2: 0 BOOT3: 0	Forced USB boot for flash programming
	BOOT0: 0 BOOT1: 0 BOOT2: 0 BOOT3: 1	SD card on SDMMC1
	BOOT0: 0 BOOT1: 0 BOOT2: 1 BOOT3: 0	eMMC on SDMMC2
	BOOT0: 0 BOOT1: 1 BOOT2: 0 BOOT3: 0	QSPI

8 Board functions

This section explains all the functions, peripherals, and interfaces of the board. Refer to [Features](#), [Hardware layout and configuration](#), [Figure 4](#), and [Figure 5](#) of STM32MP257F-EV1 top and bottom layout views.

8.1 LEDs

8.1.1 Description

The LD11 LED turns green when the power cable is inserted into the CN2 or CN21 connector.

Two general-purpose color LEDs (LD4 and LD3) are available as light indicators:

- The blue LED (LD4) is used as the Linux® Heartbeat LED, which is blinking as long as Linux® is alive on the Cortex®-A.
- The orange LED (LD3) is used as a STM32Cube example verdict LED.

The two indicator LEDs, the red (LD4) and green (LD7) LEDs are either connected to the STM32MP257 MPU.

The LEDs (LD5 and LD6) are used as ST-LINK indicator status. Refer to [Section 7.4.6](#).

8.1.2 Operating voltage

The I/O level drives all the LEDs. They operate in the 3.3 V voltage range.

8.1.3 LED interface

[Table 7](#) describes the I/O configuration of the LED interfaces.

Table 7. I/O configuration of the LED interfaces

I/O	Configuration
PJ7	PJ7 is connected to the blue LED (LD4). Active high.
PH4	PH4 is connected to the red LED (LD1). Active low.
PD8	PD8 is connected to the green LED (LD2). Active high.
PJ6	PJ6 is connected to the orange LED (LD3). Active high.

8.2 Buttons

8.2.1 Description

The STM32MP257F-EV1 Evaluation board provides five buttons:

1. USER1 button (B1):
 - Used at boot time by U-Boot to enter the USB programming mode with STM32CubeProgrammer
 - Can be used at runtime for Linux® on STM32MP25
 - Can be used at runtime for Linux® examples or STM32Cube examples
2. USER2 button (B2):
 - Used at boot time by U-Boot to enter the Android™ Fastboot mode
 - Can be used at runtime for STM32Cube examples on STM32MP25
3. Wake-up button (B3):
 - Allows the platform to be woken up from any low-power mode
 - Connected to STPMIC25APQR PONKEYn, which generates a wake-up signal on STM32MP257FAI3 pin PA0
4. Tamper button (B4):
 - Allows the detection of case opening as a security event
5. Reset button (B5):
 - Used to reset the Evaluation board

8.2.2 I/O interface

Table 8 describes the I/O configuration for the physical user interface.

Table 8. I/O configuration of the buttons

I/O	Configuration
PD2	USER1 user button (B5)
PG8	USER2 user button (B4)
-	Wake-up button (B2). Connected to the PONKEYn pin of the STPMIC25APQR
PI8	TAMPER button (B3)
NRST	Reset button (B1). Active Low.

8.3 USB Host

8.3.1 Description

The STM32MP257F-EV1 Evaluation board provides two USB 2.0 HS host ports (dual-USB sockets CN19) through the use of a USB hub. The USB hub has full power management for each USB port. No I/O is needed from STM32MP257.

8.3.2 USB Host interface

Table 9 describes the I/O configuration for the USB Host user interface.

Table 9. I/O configuration of the USB Host interfaces

I/O	Configuration
USB_HS_DP	USBIN_P
USB_HS_DM	USBIN_N

Figure 8 shows the USB Type-A connector (CN19) pinout.

Figure 8. USB Type-A connector (CN19) pinout

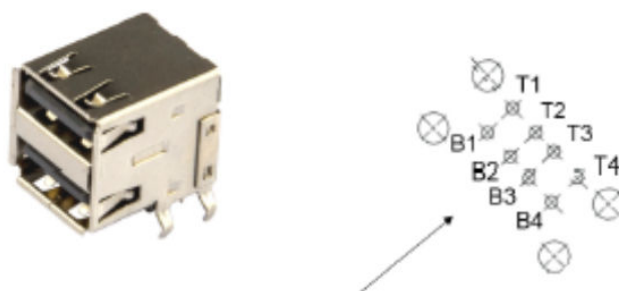


Table 10 describes the USB Host connector (CN19) pinout.

Table 10. USB Host connector (CN19) pinout

Pin	Pin name	Signal name	Function
T1	T1	VBUS	VBUS
T2	T2	USB1CN_N	DM
T3	T3	USB1CN_P	DP
T4	T4	GND	GND
B1	B1	VBUS	VBUS
B2	B2	USB2CN_N	DM
B3	B3	USB2CN_P	DP
B4	B4	GND	GND

8.4 USB Type-C® HS

8.4.1 Description

The STM32MP257F-EV1 Evaluation board supports USB high-speed (HS) communication. The USB connector is a USB Type-C® connector (CN15).

The STM32MP257F-EV1 Evaluation board supports USB Type-C® Source mode.

8.4.2 Operating voltage

The STM32MP257F-EV1 Evaluation board supports a 5 V USB voltage from 4.75 to 5.25 V.

8.4.3 USB HS Source

When a USB Device connection to the USB Type-C® connector (CN15) of STM32MP257F-EV1 is detected, the Evaluation board starts behaving as a USB Host.

8.4.4 USB Type-C® connector

Figure 9 shows the pinout of the USB Type-C® connector (CN15).

Figure 9. USB Type-C® connector (CN15) pinout

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Table 11 describes the pinout of the USB Type-C® connector (CN15).

Table 11. USB Type-C® connector (CN15) pinout

Function	I/O	Signal name	Pin name	Pin	Pin	Pin name	Signal name	I/O	Function
GND	-	GND	GND	A1	B12	GND	GND	-	GND
TX1+	-	-	TX1+	A2	B11	RX1+	-	-	RX1+
TX1-	-	-	TX1-	A3	B10	RX1-	-	-	RX1-
VBUS	-	-	VBUS	A4	B9	VBUS	-	-	VBUS
CC1	-	(1)	CC1	A5	B8	SBU2	-	-	SBU2
D+	USB3DR_DP	USBDR_P	D+	A6	B7	D-	USBDR_N	USB3DR_DM	D-
D-	USB3DR_DM	USBDR_N	D-	A7	B6	D+	USBDR_P	USB3DR_DP	D+
SBU1	-	-	SBU1	A8	B5	CC2	(1)	-	CC2
VBUS	-	VBUSc	VBUS	A9	B4	VBUS	VBUSc	-	VBUS
RX2-	-	-	RX2-	A10	B3	TX2-	-	-	TX2-
RX2+	-	-	RX2+	A11	B2	TX2+	-	-	TX2+
GND	-	GND	GND	A12	B1	GND	GND	-	GND

1. The CCx pins from CN15 are connected to the CCxc pins of TCPP03-M20.

8.5 Debug connector (CN22)

8.5.1 Description

The Evaluation board embeds a MIPI10 debug connector to connect a debug probe.

Attention: Before using CN22, check the specific constraints in [Section 7.4.2: STLINK-V3EC deactivation \(Reset mode\)](#).

8.5.2 MIPI10 debug connector

Figure 10. MIPI10 debug connector (CN22)

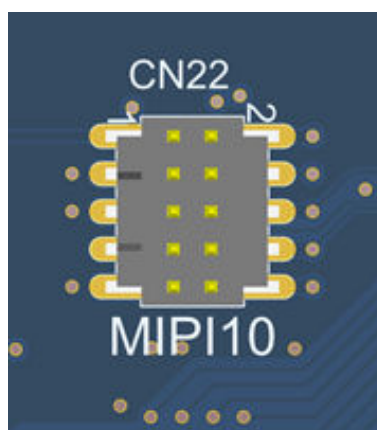


Table 12. MIPI10

Pin number	Description	Signal assignment	Pin number	Description	Signal assignment
1	VREF	VDDIO	2	SWDIO/JTMS	JTMS_SWDIO

Pin number	Description	Signal assignment	Pin number	Description	Signal assignment
3	GND	GND	4	SWCLK/JTCK	JTCK_SWCLK
5	GND	GND	6	SWDO/JTDO	JTCK_SWCLK
7	SWCLK/JTCK	JTCK_SWCLK	8	JTDI	JTDI
9	GND	GND	10	RESET	NRST

8.6 microSD™ card

8.6.1 Description

The CN1 slot for the microSD™ card is routed to the STM32MP257FAI3 SDIO port (SDMMC). This interface is fully compliant with version 6.0 of the SD memory card specifications.

8.6.2 Operating voltage

The microSD™ card interface is compatible with 1.8 and 3.3 V. All microSD™ card types are supported on STM32MP257F-EV1. The UHS-I modes (1.8 V) are supported on this Evaluation board.

8.6.3 microSD™ card interface

The microSD™ card interface is used in the four data lines D[0:3] with one clock (CLK), one command line (CMD), and one card detection signal (uSD_DETECT). The SDMMC1 is a bootable interface. [Table 13](#) describes the I/O configuration for the SDIO interface.

Table 13. I/O configuration for the SDIO interface

I/O	Configuration
PD9	PD9 is connected to SD.uSD_DETECT
PE4	PE4 is connected to SD.SDMMC1_D0
PE5	PE5 is connected to SD.SDMMC1_D1
PE0	PE0 is connected to SD.SDMMC1_D2
PE1	PE1 is connected to SD.SDMMC1_D3
PE3	PE3 is connected to SD.SDMMC1_CLK
PE2	PE2 is connected to SD.SDMMC1_CMD

Figure 11 shows the pinout of the microSD™ connector CN1.

Figure 11. microSD™ card connector (CN1)



Table 14 describes the pinout of the microSD™ connector (CN1).

Table 14. microSD™ connector (CN1) pinout

Pin	Pin name	Signal name	I/O	Function
1	DAT2	SD.SDMMC1_D2	PE0	SDIO.D2
2	DAT3_CD	SD.SDMMC1_D3	PE1	SDIO.D3
3	CMD	SD.SDMMC1_CMD	PE2	SDIO.CMD
4	VDD	VDD_SD	-	VDD_SDCARD
5	CLK	SD.SDMMC1_CLK	PE3	SDIO.CLK
6	VSS	GND	-	GND
7	DAT0	SD.SDMMC1_D0	PE4	SDIO.D0
8	DAT1	SD.SDMMC1_D1	PE5	SDIO.D1
9	CARD_DETECT	uSD_DETECT	PD9	uSD_DETECT active low

8.7 Quad-SPI NOR flash memory

The 512-Mbit NOR flash memory is managed through the Octo-SPI interface used in Quad-SPI mode. The NRST reset pin from the microcontroller manages the Quad-SPI flash memory RESET function. Octo-SPI is a bootable interface.

Table 15. Octo-SPI flash memory I/O interface

I/O	Configuration
PD3	CSn (QSPI1.NCS1)
PD0	SCLK (QSPI1.CLK)
PD4	IO0 (QSPI1.IO0)
PD5	IO1 (QSPI1.IO1)
PD6	IO2 (QSPI1.IO2)
PD7	IO3 (QSPI1.IO3)
NRST	RESETn (NRST)

8.8 eMMC flash memory

The 4-Gbyte eMMC flash memory is compatible with eMMC v5.0.

The eMMC RSTn (NRSTC1MS, active LOW) is the reset for eMMC. The embedded footprint is also compatible with other eMMC references in the 153-ball package. Check the compatibility of the memory datasheet with the MB1936 schematics. The SDMMC2 is a bootable interface.

Table 16. eMMCflash memory I/O interface

I/O	Configuration
PE15	CMD (eMMC.SDMMC2_CMD)
PE14	CLK (eMMC.SDMMC2_CLK)
PE13	D0(eMMC.SDMMC2_D0)
PE11	D1(eMMC.SDMMC2_D1)
PE8	D2(eMMC.SDMMC2_D2)
PE12	D3(eMMC.SDMMC2_D3)
PE10	D4(eMMC.SDMMC2_D4)
PE9	D5(eMMC.SDMMC2_D5)
PE6	D6(eMMC.SDMMC2_D6)
PE7	D7(eMMC.SDMMC2_D7)
NRSTC1MS	RSTn

8.9 Mini PCIe

8.9.1 Description

The STM32MP257F-EV1 Evaluation board supports a mini-PCIE connector. The 100 MHz CLK (REF CLK) can be generated by the STM32MP2:

- R87, R88, R89, R90, R288, and R328 OFF,
- R77 and R78 ON.

Or by an external 100 MHz clock generator (U33):

- R87, R88, R89, and R90 ON,
 - R77, R78, R288, and R328 OFF.
- This is the default configuration on the MB1936 board

Or by a device plugged into the mini-PCIE connector:

- R77, R78, R87, R88, R89, and R90 OFF,
- R288 and R328 ON.

8.9.2 Mini-PCIe interface

Figure 12. Mini-PCIe connector (CN13)



Table 17. Mini-PCIe connector pinout

Function	I/O	Pin	Pin	I/O	Function
WAKEn/PCIE.NWAKE	PH5	1	2	-	3V3
-	-	3	4	-	GND
-	-	5	6	-	1V5
CLKnotREQ/PCIE.CLKREQ	PJ0	7	8	-	-
GND	-	9	10	-	-
REFCLKN/PCIE.CLKOUT_N	(1)	11	12	-	-
REFCLKP/PCIE.CLKOUT_P	(1)	13	14	-	GND
GND	-	15	16	-	-
-	-	17	18	-	GND
-	-	19	20	-	-
GND	-	21	22	PJ8	PERSTnot/PCIE.RSTN
PERN0/PCIE.RX_N	RX1N	23	24	-	3v3
PERP0/PCIE.RX_P	RX1P	25	26	-	GND
GND	-	27	28	-	1V5
GND	-	29	30	PZ4	SMB_CLK/I2C8.SCL
PETN0/PCIE.TX_N	TX1N	31	32	PZ3	SMB_DATA/I2C8.SDA
PETP0/PCIE.TX_P	TX1P	33	34	-	GND
GND	-	35	36	(2)	USB_DN/PCIE.USB_N
GND	-	37	38	(2)	USB_DP/PCIE.USB_P
3V3	-	39	40	-	GND
3V3	-	41	42	-	-
GND	-	43	44	-	LED_notWLAN/Green Wi-Fi® LED

Function	I/O	Pin	Pin	I/O	Function
-	-	45	46	-	LED_notWPAN/Blue BT LED
-	-	47	48	-	1V5
-	-	49	50	-	GND
-	-	51	52	-	3V3
GND	-	53	54	-	GND

1. Refer to the description for the default configuration.
2. PCIE.USBx signals from the USB hub

8.10 CAN FD

8.10.1 Description

The STM32MP257F-EV1 Evaluation board supports two CAN FDs compliant with ISO-11898-1 version 2.0 part A, B. The two DB9 male connectors (CN9 and CN11) are available as CAN FD interfaces.

8.10.2 Operating voltage

A 5 V/3.3 V I/O-compliant high-speed CAN-FD transceiver is fitted between the CN9-CN11 connectors and the CAN controller port of the STM32MP257.

8.10.3 CAN-FD interface

Table 18. I/O interface for the FDCAN1 configuration

I/O	Configuration
PJ13	CAN_STBY
PG11	CAN_TX
G12	CAN_RX

Table 19. I/O interface for the FDCAN2 configuration

I/O	Configuration
PJ15	CAN_STBY
PJ14	CAN_TX
PI12	CAN_RX

Figure 13. CAN-FD connector pinout (CN9 and CN11)

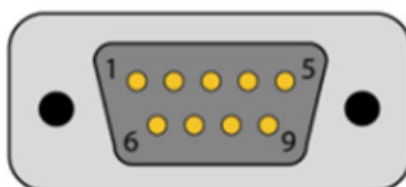


Table 20. CAN-FDconnectors (CN9 and CN11) pinout

CAN transceiver	Board function	Pin	Pin	Board function	CAN transceiver
-	NC	1	6	GND	-
CANL	CANL	2	7	CANH	CANH
GND	GND	3	8	NC	-
-	NC	4	9	NC	-
-	GND	5	-	-	-

8.11 DSI

8.11.1 Description

The 64-pin DSI connector (CN3) supports a DSI display and HDMI add-on boards.

Add-on boards example:

- HDMI, MB1232 adapter board provides a DSI input port and HDMI output port (order code B-LCDAD-HDMI1: for HDMI full HD 30-fps display)
- DSI LCD 720p from STM32MP157x-EV1

8.11.2 DSI interface

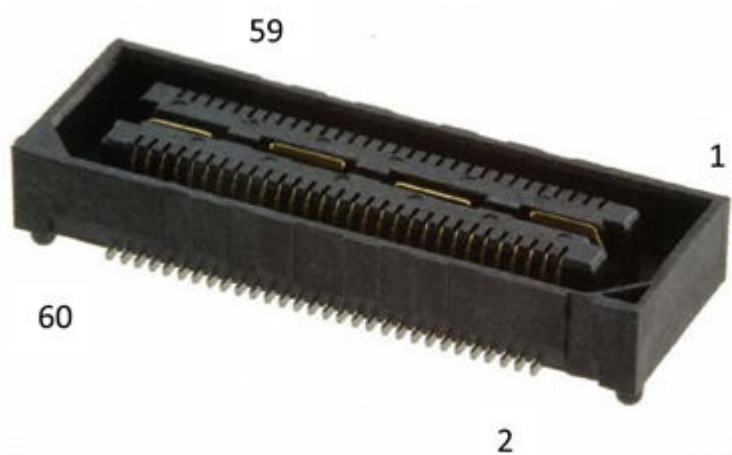
Figure 14. DSI display interface (CN3)


Table 21 describes the DSI interface and the pinout of the DSI connector (CN3).

Table 21. DSI connector pin assignment (CN3)

Function	GPIO	Signal name	Pin number (CN2)		Signal name	GPIO	Function
GND	-	GND	1	2	NC	-	-
Differential DSI clock	-	DSI.CK_P	3	4	DISP.DSI_INT	PD10	Touch interrupt
	-	DSI.CK_N	5	6	GND	-	GND
GND	-	GND	7	8	DSI.D2_P	-	Differential DSI data 2
Differential DSI data 0	-	DSI.D0_P	9	10	DSI.D2_N	-	
	-	DSI.D0_N	11	12	GND	-	GND
GND	-	GND	13	14	DSI.D3_P	-	Differential DSI data 3

Function	GPIO	Signal name	Pin number (CN2)		Signal name	GPIO	Function
Differential DSI data 1	-	DSI.D1_P	15	16	DSI.D3_N	-	Differential DSI data 3
	-	DSI.D1_N	17	18	GND		GND
GND	-	GND	19	20	NC	-	-
Power	-	5V_VIN	21	22	NC	-	-
Power	-	5V_VIN	23	24	NC	-	-
-	-	NC	25	26	NC	-	-
GND	-	GND	27	28	NC	-	-
GND	-	GND	29	30	NC	-	-
-	-	NC	31	32	RESERVED	-	-
-	-	NC	33	34	NC	-	-
I2S clock	PB0	HDMI_I2S2.CK	35	36	3V3	-	3.3 V
I2S word	PI14	HDMI_I2S2.WS	37	38	NC	-	-
I2S data	PK1	HDMI_I2S2_SDO	39	40	I2C2.SDA	PB4	Touch panel I ² C data
-	-	NC	41	42	NC	-	-
-	-	NC	43	44	I2C2.SCL	PB5	Touch panel ² clock
-	-	NC	45	46	-	-	Test point
HDMI consumer electronic control	PK0	HDMI_CEC	47	48	-	-	Test point
Tearing effect	PI9	DISP.TE	49	50	-	-	Test point
	-	NC	51	52	-	-	Test point
DSI backlight control	PI5	DISP.BLCTRL	53	54	-	-	Test point
-	-	NC	55	56	-	-	Test point
DSI and touch-panel reset	PG14	DISP.RESET	57	58	-	-	Test point
-	-	NC	59	60	1V8	-	1.8 V

8.12 LVDS

8.12.1 Description

The STM32MP257F-EV1 Evaluation board supports one LVDS with four data lanes. The FFC/FPC connector (CN2) is available as an LVDS interface. The B-LVDS7-WSVGA LVDS display, which is not included in the package, can be plugged into CN2.

This display can be purchased at www.st.com with the B-LVDS7-WSVGA order code.

8.12.2 LVDS interface

Figure 15. LVDS display connector (CN2)

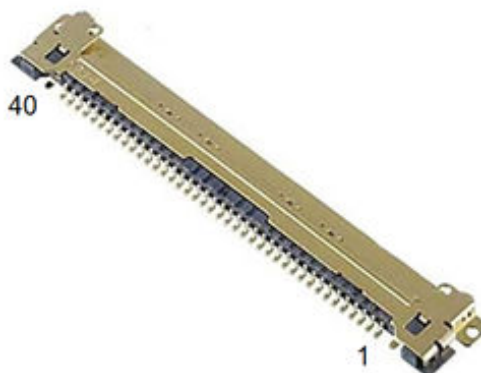


Table 22 describes the LVDS interface and pinout of LVDS connector CN2.

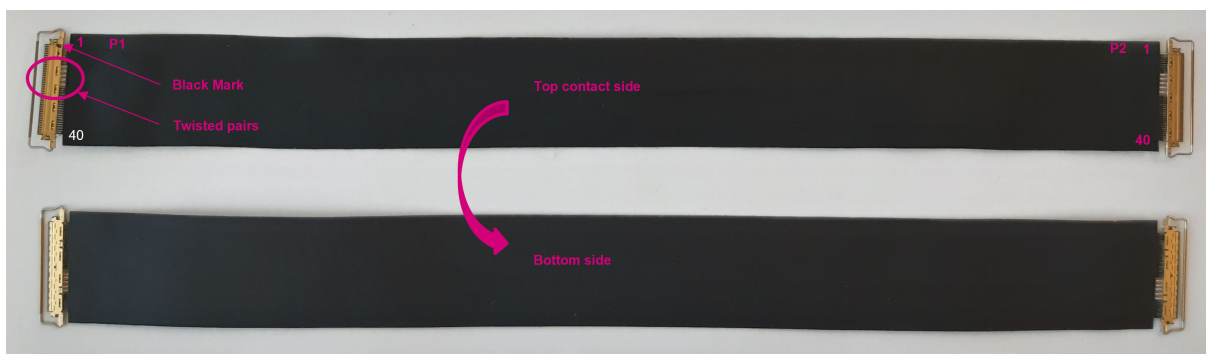
Table 22. LVDS interface and CN2 connector pinout

Pin	I/O	Signal name	Function
1	-	GND	GND
2	PI3	DISP.LVDS_INT	INT
3	-	VDD	3V3
4	-	VDD	3V3
5	-	VSS	GND
6	PG14	LVDS.RESET	RESET
7	PB5	I2C2.SCL	I2C2.SCL shared with CSI
8	PB4	I2C2.SDA	I2C2.SDA shared with CSI
9	-	GND	GND
10	LVDS1.D0_N	LVDS1.D0con_N	Differential LVDS1 data 0
11	LVDS1.D0_P	LVDS1.D0con_P	
12	LVDS1.D1_N	LVDS1.D1con_N	Differential LVDS1 data 1
13	LVDS1.D1_P	LVDS1.D1con_P	
14	LVDS1.2_N	LVDS1.D2con_N	Differential LVDS1 data 2
15	LVDS1.D2_P	LVDS1.D2con_P	
16	LVDS1.CLK_N	LVDS1.CLKcon_N	Differential LVDS1 CLK
17	LVDS1.CLK_P	LVDS1.CLKcon_P	
18	LVDS1.D3_N	LVDS1.D3con_N	Differential LVDS1 data 3
19	LVDS1.D3_P	LVDS1.D3con_P	
20	-	-	Not connected
21	-	-	Not connected
22	-	-	Not connected
23	-	-	Not connected
24	-	-	Not connected

Pin	I/O	Signal name	Function
25	-	-	Not connected
26	-	-	Not connected
27	-	-	Not connected
28	-	-	Not connected
29	-	-	Not connected
30	-	GND	GND
31	-	GND	GND
32	-	VLED	5 V
33	-	VLED	5 V
34	-	VLED	5 V
35	-	VLED	5 V
36	PG15	DISP.LED_EN	Display LED enable
37	PI5	DISP.BLCTRL	Display backlight control
38	-	VSS	GND
39	-	VSS	GND
40	-	VSS	GND

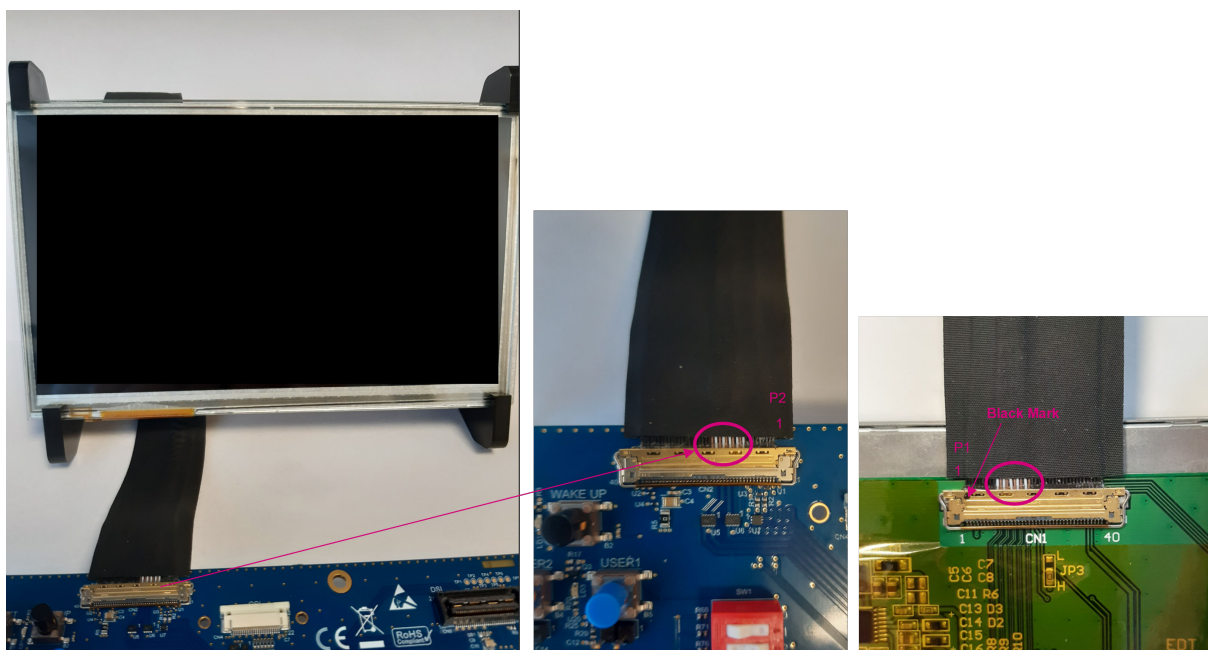
8.12.3 How to connect the LVDS display?

Figure 16. Step 1



- Check the above cable orientation thanks to the black mark and the white twisted pairs.
- Find the LVDS port on the Evaluation board (CN2) and the one on the display (CN1). One FPC is provided in the EV box.
- On each port, insert the cable as described:

Figure 17. Step 2



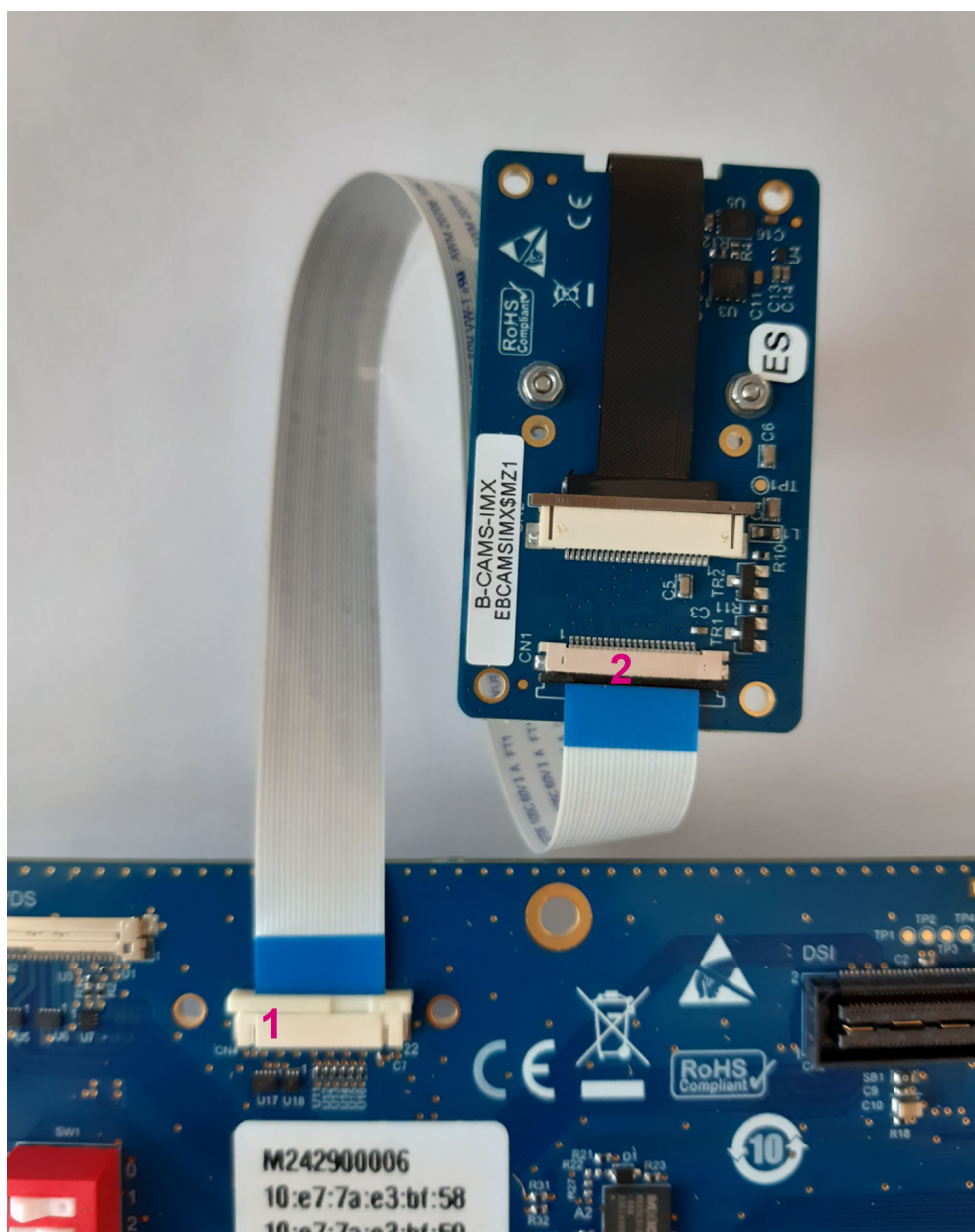
8.13 CSI

8.13.1 Description

The STM32MP257F-EV1 Evaluation board provides a CSI connector (CN4) to plug an external camera module. The B-CAMS-IMX camera module, not included in the package, can be plugged into CN4.

- The B-CAMS-IMX camera module provides a 5-Mpx image sensor, an inertial motion unit, and a Time-of-Flight sensor
- This camera module can be purchased at www.st.com with the B-CAMS-IMX order code.
- Complete documentation can be found at www.st.com.

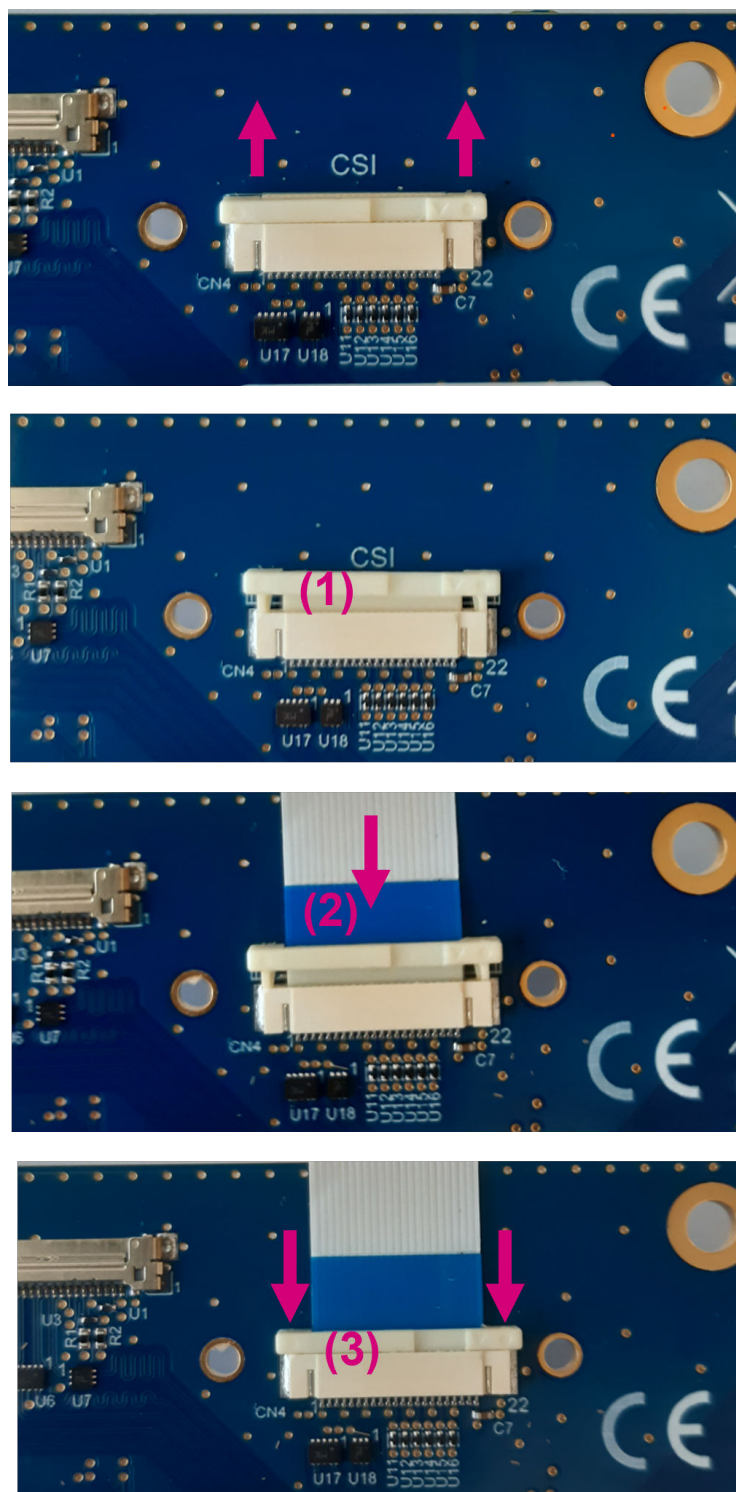
Figure 18. B-CAMS-IMX connected to a target STM32 board



- Make sure that the target STM32 board is not powered.
- Find the camera connector on the target STM32 board (example Figure 18.1) and the one on MB1854 (CN1 Figure 18.2).

- On each connector, carefully:

Figure 19. Connecting B-CAMS-IMX to the target STM32 board



- Lightly pull the white plastic (1) to insert the contact side of the FFC towards the board (2).
- Push the white plastic to hold the FFC(3).

Table 23 describes the CSI interface and pinout of the CSI connector (CN4).

Table 23. CSI interface and CN4 connector pinout

Pin	I/O	Signal name	Function
1	-	GND	GND
2	CSI_D0N	CSI.D0_N	MIPI-CSI receiver 1 data Lane 1 negative
3	CSI_D0P	CSI.D0_P	MIPI-CSI receiver 1 data Lane 1 positive
4	-	GND	GND
5	CSI_D1N	CSI.D1_N	MIPI-CSI receiver 1 data Lane 2 negative
6	CSI_D1P	CSI.D1_P	MIPI-CSI receiver 1 data Lane 2 positive
7	-	GND	GND
8	CSI_CKN	CSI.CK_N	clock Lane negative
9	CSI_CKP	CSI.CK_P	clock Lane positive
10	-	GND	GND
11	PG7	TOF_LPn	Time-of-Flight
12	PI2	TOF_INT	Time-of-Flight interruption
13	-	GND	-
14	PI3	IMU_INT1	Inertial motion unit interruption
15	PI4	IMU_INT2	Inertial motion unit interruption
16	-	GND	GND
17	PI7	CAM_RESET	Camera reset
18	PIO	CAM_ENABLE	Camera enable
19	-	GND	GND
20	PB5	I2C2.SCL	I2C2.SCL shared with LVDS touch panel
21	PB4	I2C2.SDA	I2C2.SDA shared with LVDS touch panel
22	-	3V3	3V3

8.14 Gigabit Ethernet

8.14.1 Description

The STM32MP257F-EV1 Evaluation board offers a 3-gigabit Ethernet feature using three external physical interface devices (PHYs):

- Two independent PHYs, Ethernet 1 and Ethernet 2
- An additional PHY, Ethernet 3, if the TSN switch is activated.

Those three PHYs are connected to the STM32MP257 reduced gigabit medium-independent interface (RGMII), and can be clocked using the 25 MHz from STM32MP257 or a crystal (for example X4 for ETH2). The default configuration is 25 MHz from the crystal.

The Ethernet PHY is supplied by 3V3. It generates its supply 1V05 and digital/analog 3V3.

The green LD7, LD8, and LD9 LEDs on the board blink to indicate data transmission.

8.14.2 RGMII interface

Table 24 describes the I/O configuration for the Ethernet 1 interface.

Table 24. I/O configuration Ethernet 1 interface

I/O	Configuration
PJ9	PJ9 is used as ETH1.NRST active Low.
PF2	PF2 is used as ETH1.MDIO.
PA12	PA12 is used as ETH1.MDINT.
PG2	PG2 is used as ETH1.MDC.
PA11	PA11 is used as ETH1.RX_CTL.
PF1	PF1 is used as ETH1.RXD0.
PC2	PC2 is used as ETH1.RXD1.
PH12	PH12 is used as ETH1.RXD2.
PH13	PH13 is used as ETH1.RXD3.
PA13	PA13 is used as ETH1.TX_CTL.
PA15	PA15 is used as ETH1.TXD0.
PC1	PC1 is used as ETH1.TXD1.
PH10	PH10 is used as ETH1.TXD2.
PH11	PH11 is used as ETH1.TXD3.
PA14	PA14 is used as ETH1.RXCLK.
PC0	PC0 is used as ETH1.GTX_CLK.
PH9	PH9 is used as ETH1.CLK125.
PF3	PF3 is used as ETH1.CLK is not used by default

Table 25 describes the I/O configuration for the Ethernet 2 interface.

Table 25. I/O configuration Ethernet 2 interface

I/O	Configuration
PG6	PG6 is used as ETH2.NRST active Low.
PC5	PC5 is used as ETH2.MDIO.
PF5	PF5 is used as ETH2.MDINT.
PC6	PC6 is used as ETH2.MDC.
PC3	PC3 is used as ETH2.RX_CTL.
PG0	PG0 is used as ETH2.RXD0.
PC12	PC12 is used as ETH2.RXD1.
PF9	PF9 is used as ETH2.RXD2.
PC11	PC11 is used as ETH2.RXD3.
PC4	PC4 is used as ETH2.TX_CTL.
PC7	PC7 is used as ETH2.TXD0.
PC8	PC8 is used as ETH2.TXD1.
PC9	PC9 is used as ETH2.TXD2.
PC10	PC10 is used as ETH2.TXD3.
PF6	PF6 is used as ETH2.RXCLK.
PF7	PF7 is used as ETH2.GTX_CLK.
PF8	PF8 is used as ETH2.CLK125.
PF4	PF4 is used as ETH2.CLK is not used by default

Table 26 describes the I/O configuration for the Ethernet 3 interface.

Table 26. I/O configuration Ethernet 3 interface

I/O	Configuration
PJ9	PJ9 is used as ETH1.NRST active LOW (shared with ETH1).
PF2	PF2 is used as ETH1.MDIO (shared with ETH1).
PF0	PF0 is used as ETH1.MDC (shared with ETH1).
PA1	PA1 is used as ETH3.MDINT.
PA2	PA2 is used as ETH3.RX_CTL.
PA9	PA9 is used as ETH3.RXD0.
PA10	PA10 is used as ETH3.RXD1.
PH7	PH7 is used as ETH3.RXD2.
PH8	PH8 is used as ETH3.RXD3.
PA3	PA3 is used as ETH3.TX_CTL.
PA6	PA6 is used as ETH3.TXD0.
PA7	PA7 is used as ETH3.TXD1.
PH6	PH6 is used as ETH3.TXD2.
PH3	PH3 is used as ETH3.TXD3.
PA5	PA5 is used as ETH3.RX_CLK.
PH2	PH2 is used as ETH3.GTX_CLK.
PH9	PH9 is used as ETH3.CLK125.
PF3	PF3 is used as ETH1.CLK is not used by default

Figure 20 shows the pinout of the Ethernet connectors (CN16, CN17, and CN18).

Figure 20. Ethernet connectors (CN16, CN17, and CN18) pinout



Table 27 describes the Ethernet interface and pinout of the CN16, CN17, and CN18 connectors.

Table 27. Ethernet connectors (CN16, CN17, and CN18) pinout

Pin number	Pin name	Function
CN16, CN17, and CN18		
1	TX1+	First bidirectional pair to transmit and receive data
2	TX1-	
3	TX2+	Second bidirectional pair to transmit and receive data
4	TX2-	
5	CT1	Common connected to GND
6	CT2	Common connected to GND
7	TX3+	Third bidirectional pair to transmit and receive data
8	TX3-	
9	TX4+	Fourth bidirectional pair to transmit and receive data
10	TX4-	
11	GA	Green LED anode
12	GC	Green LED cathode
13	YA	Yellow LED anode
14	YC	Yellow LED cathode
15	GND	GND
16	GND	GND

8.15

mikroBUS™

The STM32MP257F-EV1 Evaluation board provides a mikroBUS™ socket to utilize a large range of Click boards™.

Table 28 describes the pinout of the mikroBUS™ socket.

Table 28. mikroBUS™ socket pinout

Function	I/O	Pin ⁽¹⁾	Pin ⁽¹⁾	I/O	Function
AN	ANA0	1	16	PB15	PWM
RST	PZ5	2	15	PZ9	INT
CS	PZ6	3	14	PZ8	Rx
SCK	PZ2	4	13	PZ7	Tx
MISO	PZ1	5	12	PZ4	SCL
MOSI	PZ0	6	11	PZ3	SDA
3.3 V	-	7	10	-	5 V
GND	-	8	9	-	GND

1. mikroBUS™ pins are compatible with 3.3 V (analog and digital signals) Click boards™.

8.16 GPIO expansion connector

8.16.1 Description

The GPIO pins can be used as GPIOs or alternate functions. The available alternate functions are listed in [Table 29. GPIO connector pinout](#).

Other functions can be mapped on the GPIO connectors, for instance using the STM32CubeMX tool. The GPIO expansion connector (CN5) offers shield capability.

8.16.2 GPIO expansion connector interface

Figure 21 shows the pinout of the GPIO connectors.

Figure 21. GPIO connectors

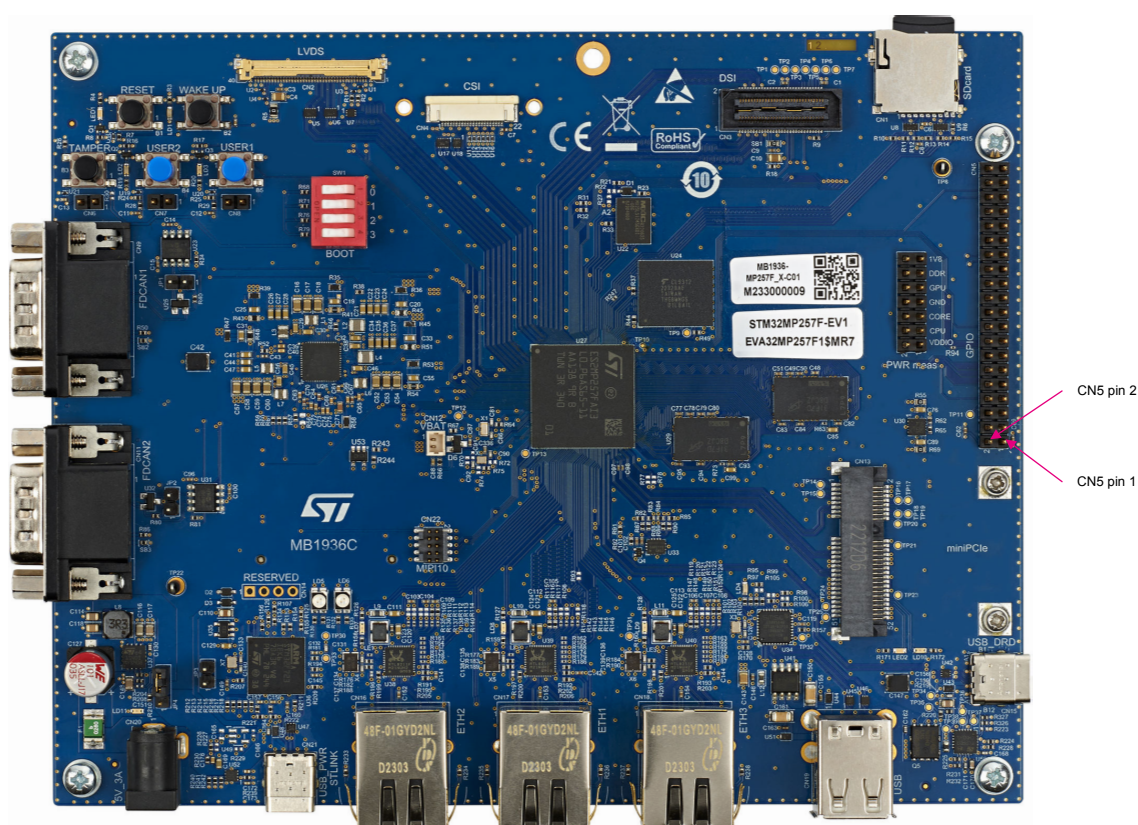


Table 29 describes the pinout of the GPIO connector.

Table 29. GPIO connector pinout

Function	I/O	Pin	Pin	I/O	Function
3V3	-	1	2	-	5 V
GPIO2/I2C8_SDA	PZ3	3	4	-	5 V
GPIO3/I2C8_SCL	PZ4	5	6	-	GND
GPIO4/MC01	PF11	7	8	PF13	GPIO14/USART6_TX
GND	-	9	10	PF14	GPIO15/USART6_RX
GPIO17/USART6_RTS	PG5	11	12	PJ11	GPIO18/SAI2_SCKA
GPIO27/SDMMC3.D3	PI11	13	14	-	GND
GPIO22/SDMMC3.CK	PB13	15	16	PD12	GPIO23/SDMMC3.CMD
3V3	-	17	18	PB14	GPIO24/SDMMC3.D0
GPIO10/SPI3_MOSI	PB8	19	20	-	GND
GPIO9/SPI3_MISO	PB10	21	22	PD13	GPIO25/SDMMC3.D1
GPIO11/SPI3_SCK	PB7	23	24	PB1	GPIO8/SPI3_NSS
GND	-	25	26	PJ1	GPIO7
I2C2_SDA	PB4	27	28	PB5	I2C2_SCL
GPIO5/TIM8_CH4	PJ4	29	30	-	GND
GPIO6/TIM12_CH2	PB11	31	32	PB9	GPIO12/TIM10_CH1
GPIO13/TIM8_CH1	PJ5	33	34	-	GND
GPIO19/SAI2_FSA	PJ3	35	36	PF15	GPIO16/USART6_CTS
GPIO26/SDMMC3.D2	PB12	37	38	PJ12	GPIO20/SAI2_SDA
GND	-	39	40	PJ2	GPIO21/SAI2_SDB

8.17 VBAT connector

8.17.1 Description

The VBAT connector allows a power mode that maintains critical operations when a power loss occurs on VDDIO. The VBAT power domain contains the RTC, the backup registers, the retention RAM, and the backup SRAM. To enable VBAT mode, a backup power source must be connected to the VBAT connector.

8.17.2 Operating voltage

The VBAT connector enables external power supply from 2.3 to 3.6 V.

8.17.3 VBAT interface

Table 30 describes the I/O configuration of the VBAT interface.

Table 30. I/O configuration of the VBAT interface (CN11)

I/O	Configuration
1	VBAT
2	GND

Figure 22 shows the pinout of the VBAT connector (CN11).

Figure 22. VBAT connector (CN11) pinout



DT59446V1

Table 31 describes the VBAT interface and pinout of the CN11 connector.

Table 31. VBAT connector (CN11) pinout

I/O	Pin name	Function
1	VBAT	VBAT supply
2	GND	Ground

9 STM32MP257F-EV1 I/O assignment

Table 32. STM32MP257 Evaluation board I/O assignment

Ball	Pin	Assignment
Y2	PA0	PA0_WKUP
V15	PA1	ETH3.MDINT
W13	PA2	ETH3.RX_CTL
T14	PA3	ETH3.TX_CTL
Y15	PA4	USART2_TX
Y13	PA5	ETH3.RX_CLK
V14	PA6	ETH3.TXD0
Y14	PA7	ETH3.TXD1
W15	PA8	USART2_RX
T12	PA9	ETH3.RXD0
U13	PA10	ETH3.RXD1
W12	PA11	ETH1.RX_CTL
U12	PA12	ETH1.MDINT
Y12	PA13	ETH1.TX_CTL
U10	PA14	ETH1.RX_CLK
T10	PA15	ETH1.TXD0
C11	PB0	HDMI_I2S2.CK
D11	PB1	GPIO.SPI3_NSS
C10	PB2	-
E10	PB3	-
D10	PB4	I2C2.SDA
B11	PB5	I2C2.SCL
C12	PB6	-
D12	PB7	GPIO.SPI3_SCK
G11	PB8	GPIO.SPI3_MOSI
A12	PB9	GPIO.TIM10_CH1
A11	PB10	GPIO.SPI3_MISO
B12	PB11	GPIO.TIM12_CH2
B20	PB12	GPIO.SDMMC3_D2
D19	PB13	GPIO.SDMMC3_CK
C20	PB14	GPIO.SDMMC3_D0
AB4	PB15	mkB.PWM
AA12	PC0	ETH1.GTX_CLK
V11	PC1	ETH1.TXD1
Y11	PC2	ETH1.RXD1
W9	PC3	ETH2.RX_CTL
V9	PC4	ETH2.TX_CTL
U9	PC5	ETH2.MDIO

Ball	Pin	Assignment
AA10	PC6	ETH2.MDC
Y8	PC7	ETH2.TXD0
V8	PC8	ETH2.TXD1
U8	PC9	ETH2.TXD2
T8	PC10	ETH2.TXD3
AB7	PC11	ETH2.RXD3
Y7	PC12	ETH2.RXD1
P6	PC13	WAKEUPn
R1	OSC32_IN	OSC32_IN
R2	OSC32_OUT	OSC32_OUT
D14	PD0	QSPI1.CLK
E15	PD1	-
E14	PD2	BUTTON.User1
C15	PD3	QSPI1.NCS1
C14	PD4	QSPI1.IO0
B15	PD5	QSPI1.IO1
A15	PD6	QSPI1.IO2
D15	PD7	QSPI1.IO3
C13	PD8	LED2
B13	PD9	SD.uSD_DETECT
D13	PD10	DISP.DSI_INT
E13	PD11	-
A21	PD12	GPIO.SDMMC3_CMD
B21	PD13	GPIO.SDMMC3_D1
G15	PD14	I2C7.SDA
F16	PD15	I2C7.SCL
A16	PE0	SD.SDMMC1_D2
B16	PE1	SD.SDMMC1_D3
C16	PE2	SD.SDMMC1_CMD
D16	PE3	SD.SDMMC1_CK
B17	PE4	SD.SDMMC1_D0
C17	PE5	SD.SDMMC1_D1
E16	PE6	eMMC.SDMMC2_D6
D17	PE7	eMMC.SDMMC2_D7
C18	PE8	eMMC.SDMMC2_D2
D18	PE9	eMMC.SDMMC2_D5
A19	PE10	eMMC.SDMMC2_D4
E17	PE11	eMMC.SDMMC2_D1
C19	PE12	eMMC.SDMMC2_D3
B19	PE13	eMMC.SDMMC2_D0
A20	PE14	eMMC.SDMMC2_CK

Ball	Pin	Assignment
F17	PE15	eMMC.SDMMC2_CMD
V12	PF0	ETH1.MDC
W11	PF1	ETH1.RXD0
V10	PF2	ETH1.MDIO
W10	PF3	ETH1.CLK
Y10	PF4	ETH2.CLK
Y9	PF5	ETH2.MDINT
AB8	PF6	ETH2.RX_CLK
T9	PF7	ETH2.GTX_CLK
AA8	PF8	ETH2.CLK125
AA7	PF9	ETH2.RXD2
AA6	PF10	VBUS_DIV
Y6	PF11	MCO1
K3	PF12	-
L4	PF13	GPIO.USART6_TX
H1	PF14	GPIO.USART6_RX
L7	PF15	GPIO.USART6_CTS
W7	PG0	ETH2.RXD0
W6	PG1	TCP_P_INTN
Y4	PG2	TCP_P_EN
W4	PG3	-
AA4	PG4	-
L1	PG5	GPIO.USART6_RTS
H2	PG6	ETH2.NRST
K4	PG7	TOF_LPn
L5	PG8	BUTTON.User2
G3	PG9	UART5_TX
H3	PG10	UART5_RX
J4	PG11	FDCAN1.TX
J3	PG12	FDCAN1.RX
K5	PG13	I2C1.SCL
G4	PG14	DISP.RESET
H4	PG15	DISP.LED_EN
V3	OSC_IN	HSE_IN
V2	OSC_OUT	HSE_OUT
V13	PH2	ETH3.GTX_CLK
W14	PH3	ETH3.TXD3
AB15	PH4	LED1
AA15	PH5	PCIE.NWAKE
AA14	PH6	ETH3.TXD2
T13	PH7	ETH3.RXD2

Ball	Pin	Assignment
U14	PH8	ETH3.RXD3
AB12	PH9	ETH1.CLK125
U11	PH10	ETH1.TXD2
T11	PH11	ETH1.TXD3
AA11	PH12	ETH1.RXD3
G5	PI0	CAM_ENABLE
H6	PI1	I2C1.SDA
J5	PI2	TOF_INT
J6	PI3	IMU_INT1
K6	PI4	IMU_INT2
H5	PI5	DISP.BLCTRL
J7	PI6	-
L6	PI7	CAM_RESET
M6	PI8	BUTTON.TAMP
K7	PI9	DISP.TE
G16	PI10	-
E18	PI11	GPIO.SDMMC3_D3
G1	PI12	FDCAN3.RX
G2	PI13	DISP.LVDS_INT
G13	PI14	HDMI_I2S2.WS
E11	PI15	-
U15	PJ0	PCIE.CLKREQN
Y3	PJ1	GPIO.GPIO7
AB3	PJ2	GPIO.SAI2_SDB
AA3	PJ3	GPIO.SAI2_FSA
W3	PJ4	GPIO.TIM8_CH4
V4	PJ5	GPIO.TIM8_CH1
U5	PJ6	LED3
W2	PJ7	LED4
M2	PJ8	PCIE.RSTN
M1	PJ9	ETH1.NRST
M3	PJ10	-
M5	PJ11	GPIO.SAI2_SCKA
L2	PJ12	GPIO.SAI2_SDA
M4	PJ13	FDCAN1.STBY
L3	PJ14	FDCAN3.TX
K2	PJ15	FDCAN3.STBY
F12	PK0	HDMI_CEC
E12	PK1	HDMI_I2S2_SDO
F13	PK2	-
F15	PK3	-

Ball	Pin	Assignment
F11	PK4	-
F14	PK5	-
G12	PK6	-
G14	PK7	-
N5	PZ0	mkB.MOSI
N6	PZ1	mkB.MISO
P4	PZ2	mkB.SCK
N4	PZ3	I2C8.SDA
R5	PZ4	I2C8.SCL
P5	PZ5	mkB.RST
R6	PZ6	mkB.CS
P2	PZ7	mkB.TX
P3	PZ8	mkB.RX
N3	PZ9	mkB.INT

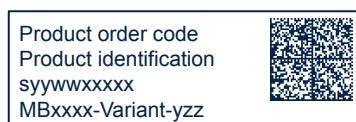
10 STM32MP257F-EV1 product information

10.1 Product marking

The product and each board composing the product are identified with one or several stickers. The stickers, located on the top or bottom side of each PCB, provide product information:

- Main board featuring the target device: product order code, product identification, serial number, and board reference with revision.

Single-sticker example:



Dual-sticker example:



- Other boards if any: board reference with revision and serial number.

Examples:



On the main board sticker, the first line provides the product order code, and the second line the product identification.

On all board stickers, the line formatted as “MBxxxx-Variant-yyz” shows the board reference “MBxxxx”, the mounting variant “Variant” when several exist (optional), the PCB revision “y”, and the assembly revision “zz”, for example B01. The other line shows the board serial number used for traceability.

Products and parts labeled as “ES” or “E” are not yet qualified or feature devices that are not yet qualified. STMicroelectronics disclaims any responsibility for consequences arising from their use. Under no circumstances will STMicroelectronics be liable for the customer's use of these engineering samples. Before deciding to use these engineering samples for qualification activities, contact STMicroelectronics' quality department.

“ES” or “E” marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the www.st.com website).
- Next to the ordering part number of the evaluation tool that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a “U” marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

10.2 STM32MP257F-EV1 product history

Table 33. Product history

Order code	Product identification	Product details	Product change description	Product limitations
STM32MP257F-EV1	VA32MP257F1\$MR1	MPU: STM32MP257FAI3 silicon revision "Y"	Initial revision	Limitation on some boards. Affected serial numbers are explained in ⁽¹⁾ .
		MPU errata sheet: STM32MP251x/3x/5x/7x device errata (ES0598)		
		Board: • MB1936-MP257F_X-D01 (main board)		
	VA32MP257F1\$CR1	MPU: STM32MP257FAI3 silicon revision "Y"	Product revision	No limitation.
		MPU errata sheet: STM32MP251x/3x/5x/7x device errata (ES0598)		
		Board: • MB1936-MP257F_X-D02 (main board)		

10.3 Board revision history

Table 34. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB1936 (main board)	MP257F_X-D01	Initial revision	Limitation ⁽¹⁾
	MP257F_X-D02	Minor passive-component update.	No limitation.

1. A minor issue on the PCB version D01 with LD2 and LD3 silk-screen designator inversion is present on the following product:
VA32MP257F1\$MR1

The impacted board serial numbers are:

- M242400001 to M242400140
- M242900001 to M242900200
- M243700001 to M243700340

11 Compliance statements and conformity declarations

11.1 Federal Communications Commission (FCC) compliance statement

Part 15.19

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

Note: Use only shielded cables.

Responsible Party - U.S. Contact Information:

Francesco Doddo
STMicroelectronics, Inc.
200 Summit Drive | Suite 405 | Burlington, MA 01803
USA
Telephone: +1 781-472-9634

11.2 Innovation, Science and Economic Development Canada (ISED) compliance statement

This product complies with the ICES-003 standard class A of the ISED regulation.

ISED Canada ICES-003 Compliance Label: CAN ICES (A)/NMB (A).

Note: Use only shielded cables.

Ce produit est conforme à la norme NMB-003 classe A de la ISDE.

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES (A) / NMB (A).

Note: Utiliser uniquement des câbles blindés.

11.3 UKCA conformity

Simplified UK declaration of conformity

Hereby, the manufacturer STMicroelectronics, declares that the equipment type STM32MP257F-EV1 is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK SI 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK SI 2012 No. 3032).

Note: Use only shielded cables.

11.4 CE conformity

11.4.1 Simplified EU declaration of conformity

Hereby, STMicroelectronics declares that the equipment type STM32MP257F-EV1 is in compliance with directives 2011/53/EU and 2015/863/EU (RoHS), and 2014/30/EU (EMC).

- Note:*
- *RoHS: Restriction of hazardous substances*
 - *EMC: Electromagnetic compatibility*

Warning

This device is compliant with Class A of EN55032/CISPR32. In a residential environment, this equipment may cause radio interference.

- Note:* *Use only shielded cables.*

11.4.2 Déclaration de conformité UE simplifiée

STMicroelectronics déclare que l'équipement électrique du type STM32MP257F-EV1 est conforme aux directives 2011/53/UE et 2015/863/UE (LdSD), et à la directive 2014/30/UE (CEM).

- Note:*
- *LdSD : directive sur la limitation de l'utilisation des substances dangereuses*
 - *CEM : compatibilité électromagnétique*

Avertissement

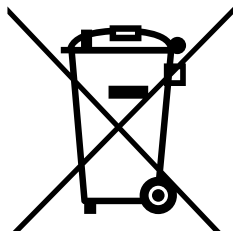
Cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

- Note:* *Utiliser uniquement des câbles blindés.*

12 Product disposal

Disposal of this product: WEEE (Waste Electrical and Electronic Equipment)

(Applicable in Europe)



This symbol on the product, accessories, or accompanying documents indicates that the product and its electronic accessories must not be disposed of with household waste at the end of their working life.

To prevent possible harm to the environment and human health from uncontrolled waste disposal, separate these items from other types of waste and recycle them responsibly at a designated collection point to promote the sustainable reuse of material resources.

Household users:

Contact the retailer that you purchased the product from or your local authority for details of your nearest designated collection point.

Business users:

Contact your dealer or supplier for further information.

Revision history

Table 35. Document revision history

Date	Revision	Changes
10-Jul-2024	1	Initial release.
21-Oct-2024	2	Updated: <ul style="list-style-type: none"> Quick start and Power source selection with JP4 default setting Figure 16 to Figure 19 Table 29 with PJ2 replaced by PB13 Added: <ul style="list-style-type: none"> Mechanical drawing
22-Apr-2025	3	Updated Section 7.5.4: STPMIC25APQR power supply. Added Section 5: Safety recommendations and Section 12: Product disposal.
08-Oct-2025	4	Updated: <ul style="list-style-type: none"> Section 5: Safety recommendations Table 8. I/O configuration of the buttons Table 33. Product history Table 34. Board revision history Section 11: Compliance statements and conformity declarations Section 11.4: CE conformity

Contents

1	Features	2
2	Ordering information	3
2.1	Codification	3
3	Development environment	4
3.1	System requirements	4
3.2	Development tools	4
3.3	Demonstration software	4
3.4	EDA resources	4
4	Conventions	5
5	Safety recommendations	6
5.1	Targeted audience	6
5.2	Handling the board	6
5.3	Delivery recommendations	6
6	Quick start	7
7	Hardware layout and configuration	8
7.1	Hardware block diagram	8
7.2	Hardware board layout	9
7.3	Mechanical drawing	11
7.4	Embedded STLINK-V3EC	12
7.4.1	Description	12
7.4.2	STLINK-V3EC deactivation (Reset mode)	12
7.4.3	Drivers	12
7.4.4	STLINK-V3EC firmware upgrade	12
7.4.5	Use of STLINK-V3EC to program and debug the on-board STM32	12
7.4.6	LED signification	12
7.5	Power supply	13
7.5.1	Power diagram	13
7.5.2	Power source selection	14
7.5.3	5 V power supply	14
7.5.4	STPMIC25APQR power supply	15
7.5.5	Other power supply	15
7.6	Clock sources	16
7.6.1	LSE clock reference	16
7.6.2	HSE clock reference	16
7.7	Reset sources	16

7.8	Boot options	16
8	Board functions	18
8.1	LEDs	18
8.1.1	Description	18
8.1.2	Operating voltage	18
8.1.3	LED interface	18
8.2	Buttons	18
8.2.1	Description	18
8.2.2	I/O interface	19
8.3	USB Host	19
8.3.1	Description	19
8.3.2	USB Host interface	19
8.4	USB Type-C® HS	20
8.4.1	Description	20
8.4.2	Operating voltage	20
8.4.3	USB HS Source	20
8.4.4	USB Type-C® connector	20
8.5	Debug connector (CN22)	21
8.5.1	Description	21
8.5.2	MIPI10 debug connector	21
8.6	microSD™ card	22
8.6.1	Description	22
8.6.2	Operating voltage	22
8.6.3	microSD™ card interface	22
8.7	Quad-SPI NOR flash memory	23
8.8	eMMC flash memory	24
8.9	Mini PCIe	24
8.9.1	Description	24
8.9.2	Mini-Pcie interface	25
8.10	CAN FD	26
8.10.1	Description	26
8.10.2	Operating voltage	26
8.10.3	CAN-FD interface	26
8.11	DSI	27
8.11.1	Description	27
8.11.2	DSI interface	27
8.12	LVDS	28

8.12.1	Description	28
8.12.2	LVDS interface	29
8.12.3	How to connect the LVDS display?	31
8.13	CSI	32
8.13.1	Description	32
8.14	Gigabit Ethernet	35
8.14.1	Description	35
8.14.2	RGMII interface	35
8.15	mikroBUS™	38
8.16	GPIO expansion connector	39
8.16.1	Description	39
8.16.2	GPIO expansion connector interface	39
8.17	VBAT connector	41
8.17.1	Description	41
8.17.2	Operating voltage	41
8.17.3	VBAT interface	41
9	STM32MP257F-EV1 I/O assignment	42
10	STM32MP257F-EV1 product information	47
10.1	Product marking	47
10.2	STM32MP257F-EV1 product history	48
10.3	Board revision history	48
11	Compliance statements and conformity declarations	49
11.1	Federal Communications Commission (FCC) compliance statement	49
11.2	Innovation, Science and Economic Development Canada (ISED) compliance statement ..	49
11.3	UKCA conformity	49
11.4	CE conformity	50
11.4.1	Simplified EU declaration of conformity	50
11.4.2	Déclaration de conformité UE simplifiée	50
12	Product disposal	51
	Revision history	52
	List of tables	56
	List of figures	57

List of tables

Table 1.	Ordering information	3
Table 2.	Codification explanation	3
Table 3.	ON/OFF convention	5
Table 4.	5 V selection configuration jumper (JP4)	14
Table 5.	Boot mode pin simplified table	16
Table 6.	Boot mode switch SW1 example of A35	17
Table 7.	I/O configuration of the LED interfaces	18
Table 8.	I/O configuration of the buttons	19
Table 9.	I/O configuration of the USB Host interfaces	19
Table 10.	USB Host connector (CN19) pinout	20
Table 11.	USB Type-C® connector (CN15) pinout.	21
Table 12.	MIPI10	21
Table 13.	I/O configuration for the SDIO interface.	22
Table 14.	microSD™ connector (CN1) pinout	23
Table 15.	Octo-SPI flash memory I/O interface.	23
Table 16.	eMMCflash memory I/O interface	24
Table 17.	Mini-PCIe connector pinout	25
Table 18.	I/O interface for the FDCAN1 configuration	26
Table 19.	I/O interface for the FDCAN2 configuration	26
Table 20.	CAN-FDconnectors (CN9 and CN11) pinout	27
Table 21.	DSI connector pin assignment (CN3)	27
Table 22.	LVDS interface and CN2 connector pinout.	29
Table 23.	CSI interface and CN4 connector pinout	34
Table 24.	I/O configuration Ethernet 1 interface	35
Table 25.	I/O configuration Ethernet 2 interface	36
Table 26.	I/O configuration Ethernet 3 interface	37
Table 27.	Ethernet connectors (CN16, CN17, and CN18) pinout	38
Table 28.	mikroBUS™ socket pinout	38
Table 29.	GPIO connector pinout	40
Table 30.	I/O configuration of the VBAT interface (CN11).	41
Table 31.	VBAT connector (CN11) pinout	41
Table 32.	STM32MP257 Evaluation board I/O assignment	42
Table 33.	Product history	48
Table 34.	Board revision history	48
Table 35.	Document revision history	52

List of figures

Figure 1.	STM32MP257F-EV1 top view	1
Figure 2.	STM32MP257F-EV1 bottom view	1
Figure 3.	STM32MP257F-EV1 hardware block diagram	8
Figure 4.	STM32MP257F-EV1 PCB layout (top side)	9
Figure 5.	STM32MP257F-EV1 PCB layout (bottom side)	10
Figure 6.	STM32MP257F-EV1 Evaluation board mechanical dimensions (in millimeters)	11
Figure 7.	Power diagram	13
Figure 8.	USB Type-A connector (CN19) pinout	19
Figure 9.	USB Type-C® connector (CN15) pinout	20
Figure 10.	MIPI10 debug connector (CN22)	21
Figure 11.	microSD™ card connector (CN1)	22
Figure 12.	Mini-PCIe connector (CN13)	25
Figure 13.	CAN-FD connector pinout (CN9 and CN11)	26
Figure 14.	DSI display interface (CN3)	27
Figure 15.	LVDS display connector (CN2)	29
Figure 16.	Step 1	31
Figure 17.	Step 2	31
Figure 18.	B-CAMS-IMX connected to a target STM32 board.	32
Figure 19.	Connecting B-CAMS-IMX to the target STM32 board.	33
Figure 20.	Ethernet connectors (CN16, CN17, and CN18) pinout	37
Figure 21.	GPIO connectors	39
Figure 22.	VBAT connector (CN11) pinout	41

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved