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UM3268

User manual

OTP programming for M0-9 SPI devices

Introduction

OTP (one-time programmable) is a type of non-volatile memory that can be programmed only once and cannot be modified later. This means that once a ‘1’ has been written into the OTP memory, it cannot be erased.

In an integrated circuit, data is usually processed by a series of functional blocks. Each of them has one or more inputs and one or more outputs. With DIAO technology through OTP, it is possible to program the OTP memory to directly associate an input to a specific output without the need of an intermediate functional block. This approach offers several advantages to end customer: the possibility to use the same device in different configurations, reduce the number of microcontroller I/Os dedicated to parallel commands, define the appropriate strategy for fail safe operation. Furthermore, it reduces the number of functional blocks required to process data, simplifying the design of the integrated circuit, and reducing power consumption.

1 How to program

The direct input assignment to output through OTP is achievable by setting two dedicated bits per channel in the OTP memory map documented in the product datasheets, in the OTP programming chapter (here below an example for six channels VN9D30Q100F):

Table 1. OTP memory map for VN9D30Q100F

OTP memory map (register 3Eh)	Bit 1, bit 0	Bit 1, bit 0	Bit 1, bit 0	Bit 1, bit 0
	00(1)	01	10	11
CH5	**DI0**	DI0	DI1	OFF
CH4	**DI1**	DI0	DI1	OFF
CH3	**DI1**	DI0	DI1	OFF
CH2	**DI1**	DI0	DI1	OFF
CH1	**DI1**	DI0	DI1	OFF
CH0	**DI0**	DI0	DI1	OFF

1. *Represents the default configuration.*

The device is provided with the default configuration corresponding to the first column in the previous table (00). A customized configuration for each channel is possible by changing the two dedicated bits.

Each output status Register (OUTSRx) per channel contains the bits DIOTP1, DIOTP0 which report the assigned direct input signal to the channel. In addition, DIENSR bit reflects the logic state of the assigned direct input.

Here below an example of output status registers for six channels VN9D30Q100F:

Table 2. Address 20 h to 25 h – output status registers channels 0 to 5

Bit	Name	Access	Reset	Content
15	DIENSR	R	0	Direct input status, image of associated DI logic level (according to OTP allocation)
14	DIOTP1	R	x	Associated Dix input description bit 1
13	DIOTP0	R	x	Associated Dix input description bit 0
12	CHFBSRx	R	0	Channel feedback status. Combination of OTDIFF, OT, OVERLOAD detection (VDS at turn-off)
11	VDSFSRx	R/C	0	VDS feedback status. This bit is ‘1’ if VDS is high at turn-off, indicative of a potential overload condition
10	STKFLTRx	R/C	0	Output stuck to Vcc/openload off state status
9	OLPUSRx	R	0	Output pull up generator status
8	CHLOFFSRx	R/C	0	Channel Latch-off status. This bit is set when overload blanking time has elapsed and channel is latched off. This bit must be cleared to re-enable the output channel
7	RST	R/C	1	Chip Reset
6	SPIE	R/C	0	SPI Error
5	PWMCLOCKLOW	R/C	x	PWM Clock Frequency too low
4	VCCUV	R	x	VCC Undervoltage
3	Not Used	R	0	
2	Not Used	R	0	
1	Not Used	R	0	
0	PARITY	R	1	

2 OTP programming procedure description

OTP programming mode can be entered by using the following dedicated procedure.

OTP programming procedure to move from the DIx default assignment to a new configuration, consists of the following four steps:

1. Enter the DIx assignment mode.
2. Perform the OTP Write operation of the new DIx assignment.
3. Perform the Read back operation of the DIx registers to check the correct writing operation.
4. Exit from the DIx assignment mode

Description of each OTP programming step:

1. **Enter the DIx assignment mode:**
   - The battery voltage (Vcc) must be set to 13 V.
   - Apply a voltage of 10 V on PWM_CLK pin.
   - Perform the following two dedicated SPI communications at the specified address 3Ah.

Table 3. SPI frame

1st SPI frame		2nd SPI frame	
Address	**Content**	**Address**	**Content**
3Ah	F5AEh	3Ah	0A51h

   - Release the PWM_CLK pin to 0 V ;
2. **Perform the OTP write operation of the new DIx assignment:**
   - Increase the battery voltage (V_{cc}) to programming voltage (needed to perform the writing operation).
   - Enable OTP write operation with the following dedicated SPI frame in the 3Dh register:
     - Write (3Dh, 5000h).
   - Send data to be written through the SPI interface to the “test data register 3Eh” (only one bit set to ‘1’ at a time) for each channel.

Table 4. Test data register 3Eh for VN9D30Q100F:

DIx assignment												
Ch5		Ch4		Ch3		Ch2		Ch1		Ch0		
bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	bit 1	bit 0	parity bit
n	n	n	n	n	n	n	n	n	n	n	n	P

   - Apply a pulse on the SDI pin to trigger the write operation in OTP:
     - Min pulse duration is dependent on the applied V_{cc} voltage (see Figure 1. Flow chart). (Only one “b” may be high on each write command. To write the configuration 00 00 00 11, for instance, this procedure must be repeated twice with successive write commands: first write 00 00 00 01, second write 00 00 00 10).
3. **Perform a read back from registers of a new DIx assignment to check the correct writing operation:**
   - This operation will check the correct writing operation for all channels.
     - Send a WRITE command to Address 3Dh:
       Write (3Dh, 4801h).
   - Apply a 2 µs pulse on the SDI pin to trigger the read back operation in OTP.
   - While the device is set in « Dix assignment mode», the read operation of the OUTSRx register (for example for VN9D30Q100: address 20h to 25h - bit 13,14) corresponds to a margin read mode.
4. **Exit from DIx assignment mode:**
   - Set the PWM_CLK pin low.
   - Perform the dedicated SPI communication at the specified address 3Bh:

Table 5. SPI frame

SPI frame	
Address	Content
3Bh	F550h

Note: It is not possible to exit from DIx assignment mode if the PWM_CLK pin remains above 8 V.

3 OTP write flow chart

Figure 1. Flow chart

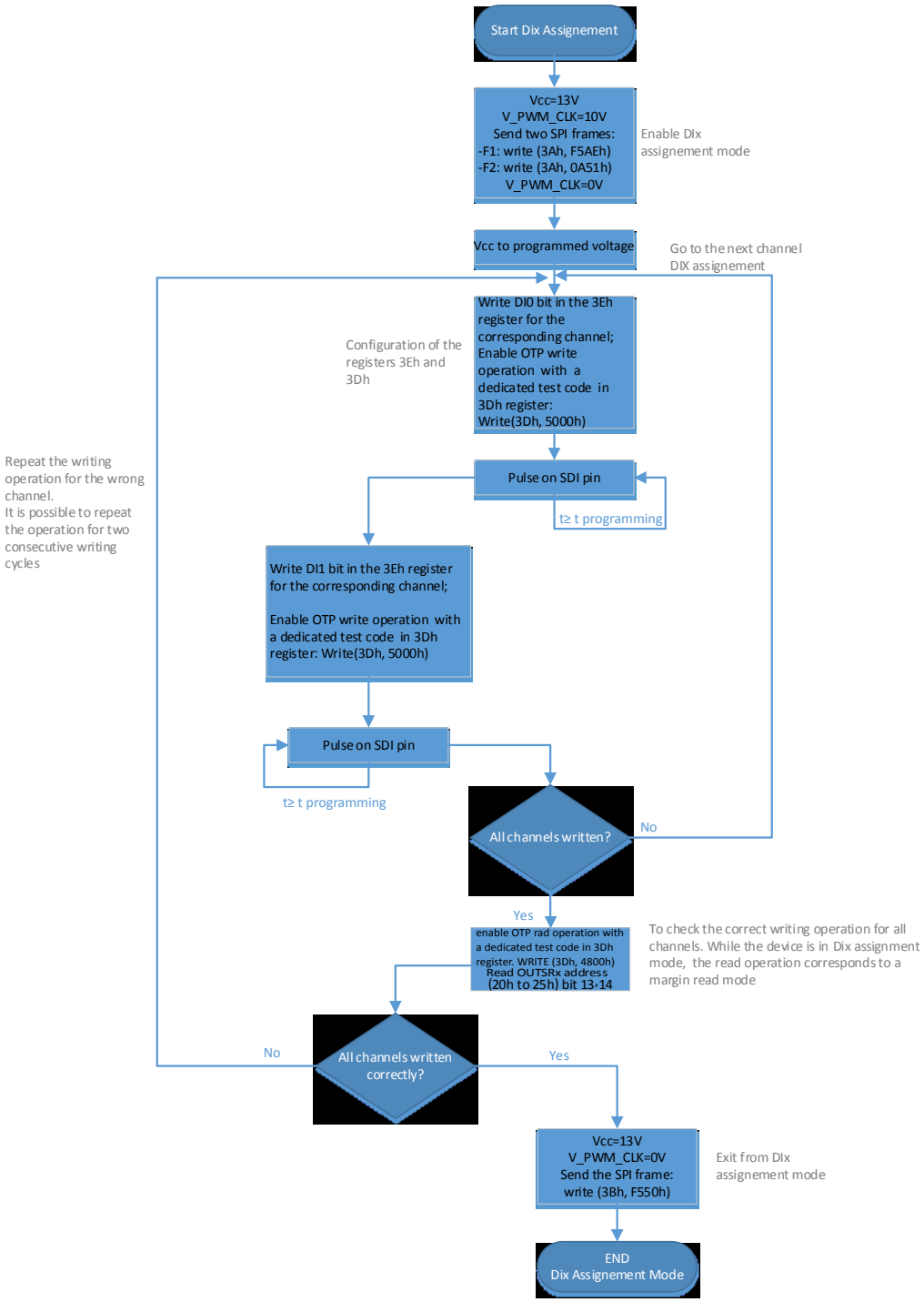
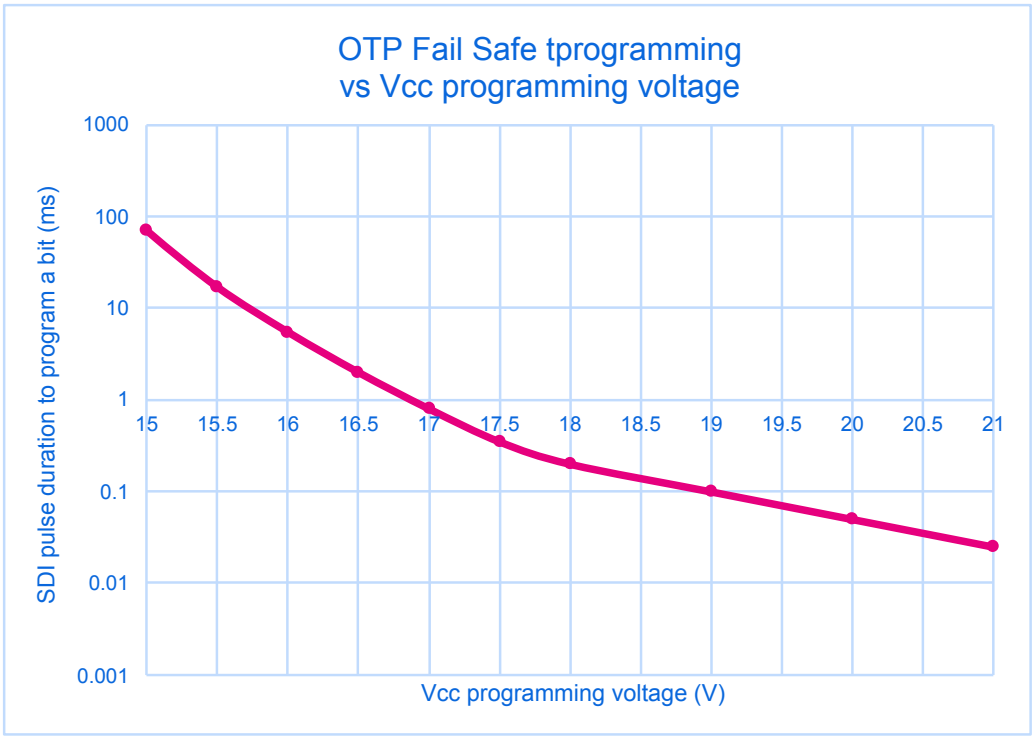


Figure 2. tprogramming vs V_{CC} programming voltage



4 OTP programming circuit for M0-9 SPI possible solution

Figure 3. OTP Programming Circuit for M0-9 SPI

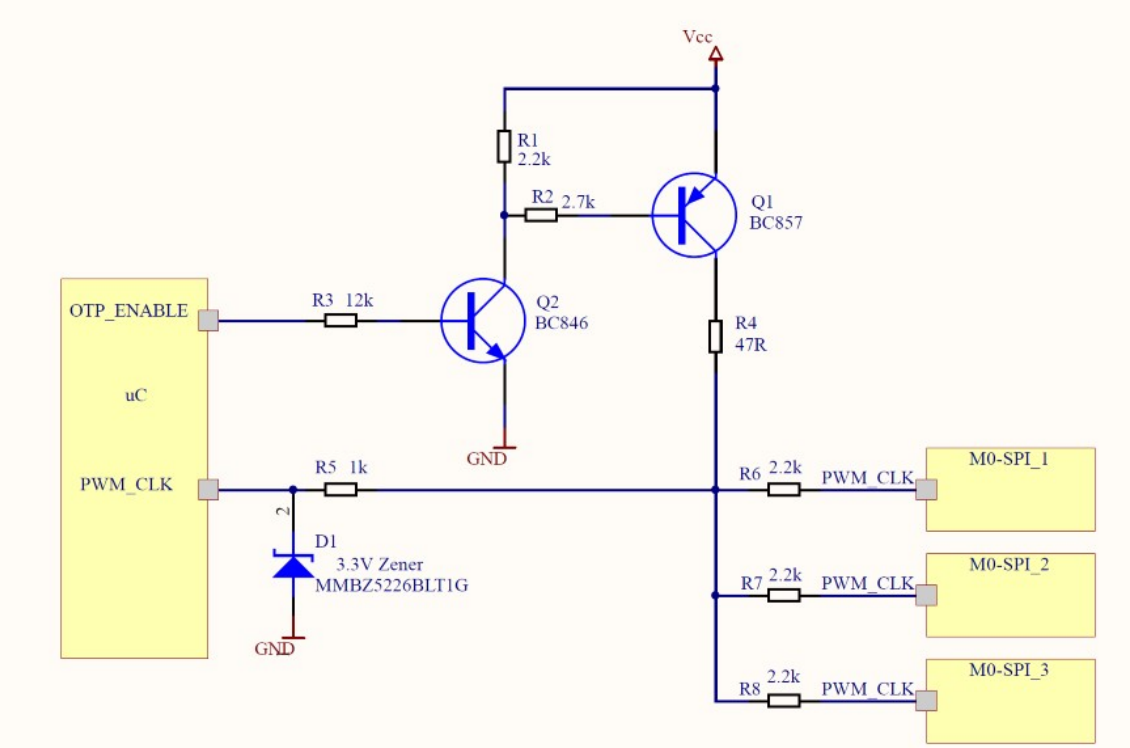


Table 6. Bill of materials

Quantity	Comment	Designator	Footprint
1	MMBZ5226BLT1G	D1	SOT23
1	BC857	Q1	SOT23
1	BC846	Q2	SOT23
4	2.2k	R1, R6, R7, R8	0805_R
1	2.7k	R2	0805_R
1	12k	R3	0805_R
1	47R	R4	0805_R
1	1k	R5	0805_R

Circuit Characteristic:

- V_{cc}=12.6 V, Total consumption 19mA, PWM_CLK pin current= 0.85 mA
- AMR of PWM_CLK pin guaranteed up to V_{cc}=18.4 V (2.9 mA)
- Pin clamp voltage 10.9 V
- Max frequency = 600 kHz

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
12-Feb-2024	1	First release.

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