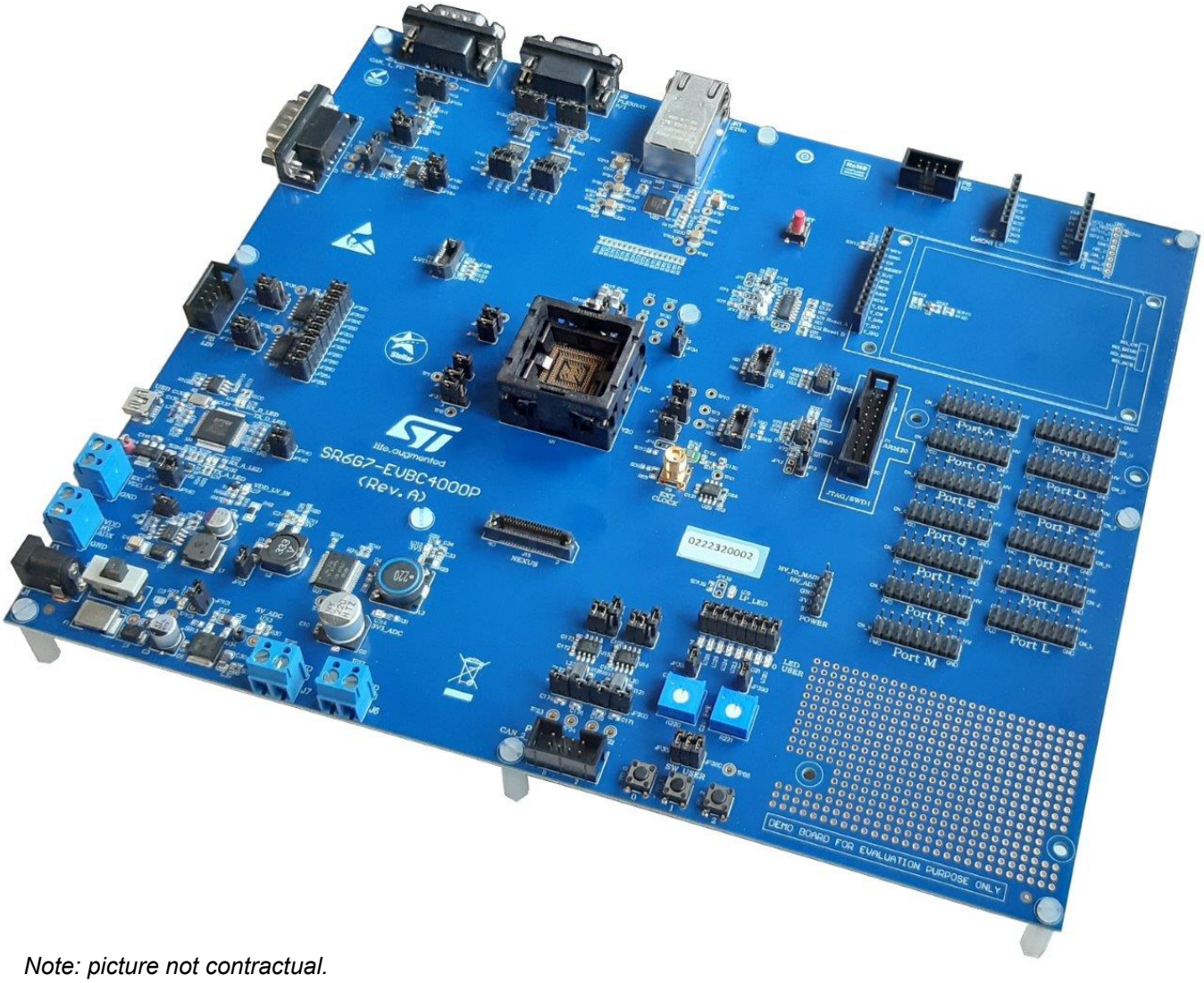
SR6G7-EVBC4000P rev. A evaluation board

Introduction

The SR6G7-EVBC4000P rev. A standalone evaluation board supports the STMicroelectronics SR6G7C4 microcontroller in FPBGA 292.

Figure 1. SR6G7-EVBC4000P rev. A



Note: picture not contractual.

1 Overview

The SR6G7-EVBC4000P rev. A standalone evaluation board supports the STMicroelectronics SR6G7C4 microcontroller with the package FPBGA 17X17X1.8 292 2R20+2R14+52 B0.55 P0.8.

The evaluation board is a standalone unit allowing access to the CPU plus full access to the I/O pins of each on-board peripheral.

The evaluation board is intended for bench/laboratory use and has been designed using normal temperature specified components.

Figure 2. Overview of SR6G7-EVBC4000P rev. A - top

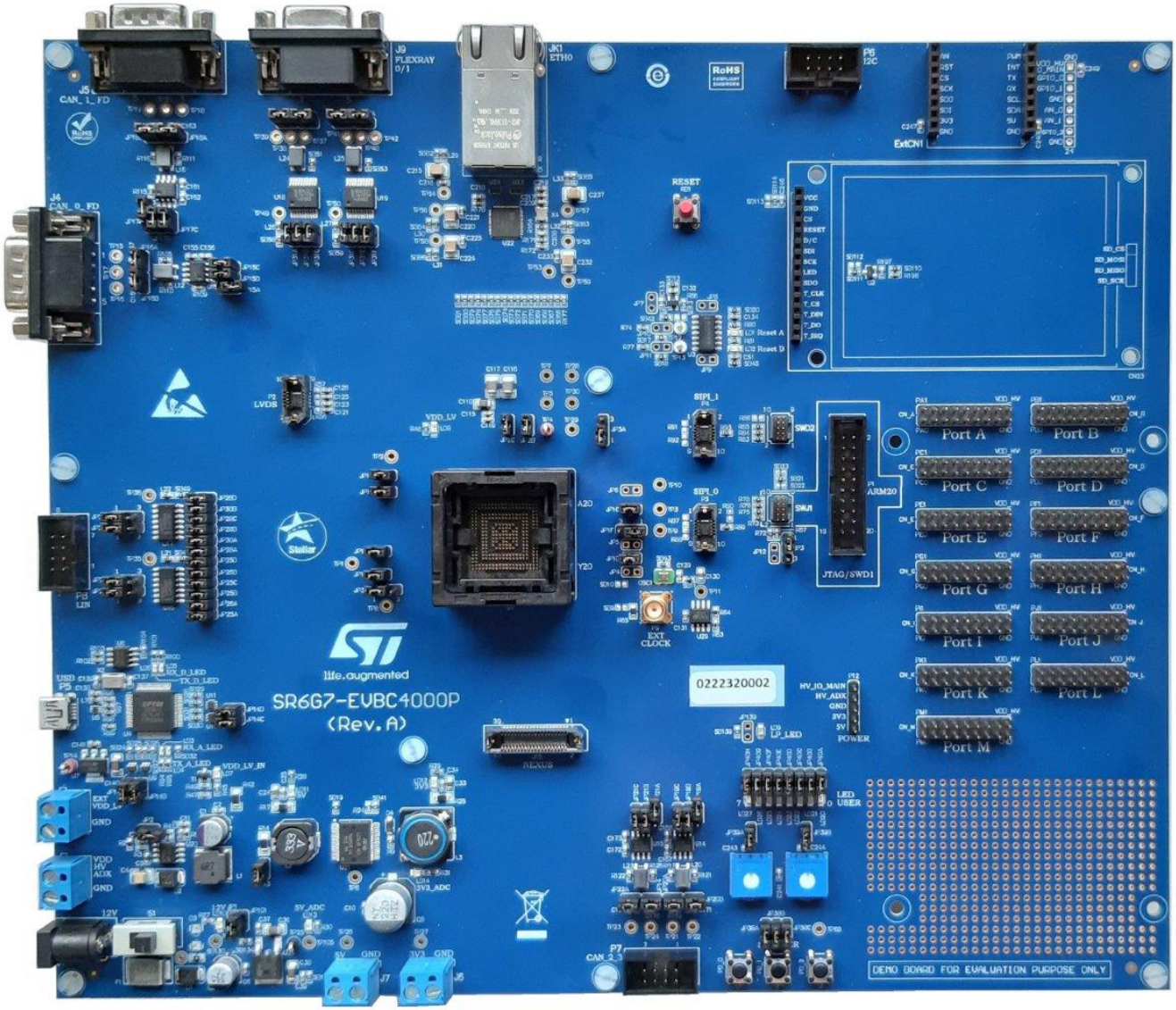
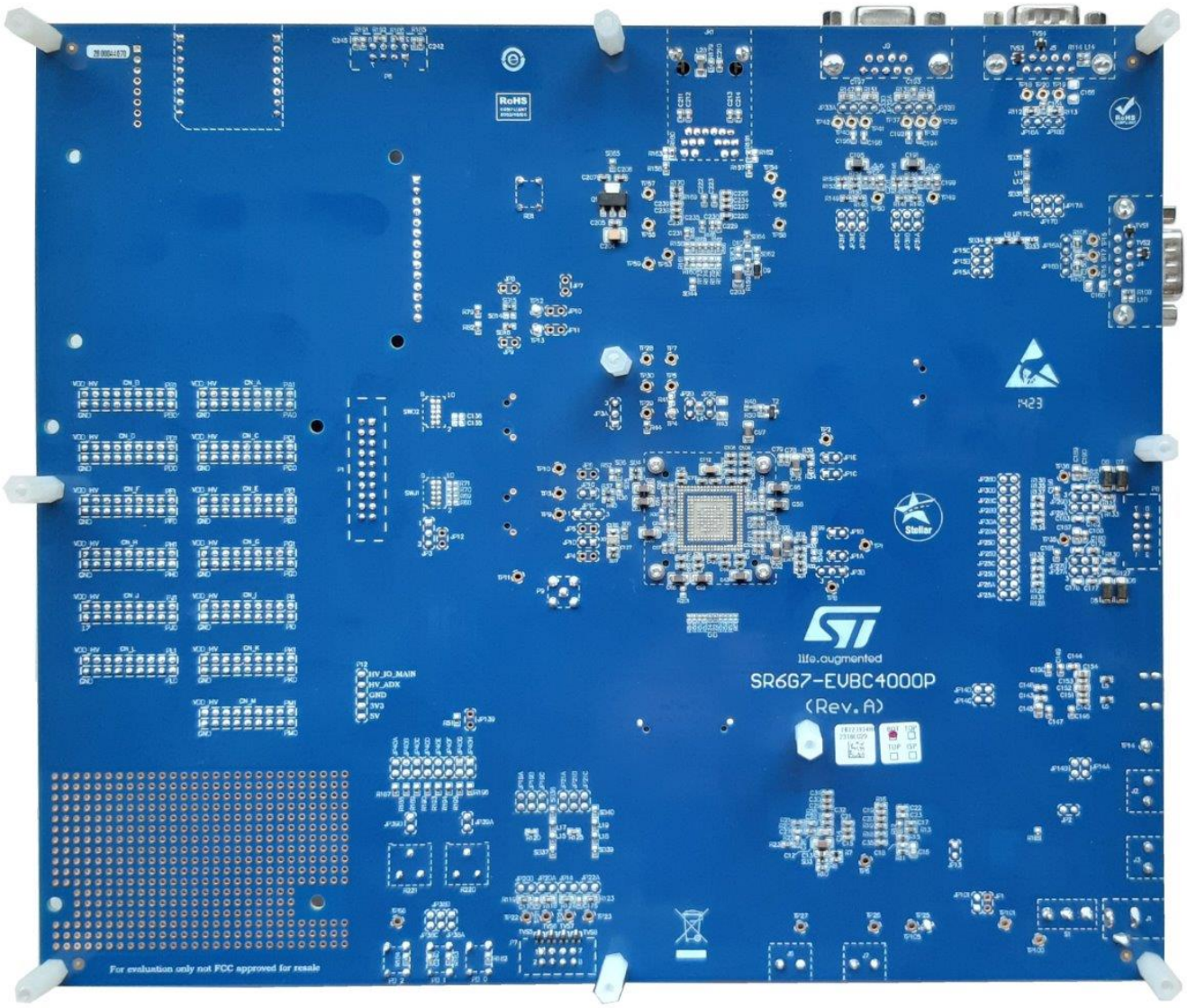


Figure 3. **Overview of SR6G7-EVBC4000P rev. A - bottom**



1.1 Package contents

An SR6G7-EVBC4000P rev. A adapter package includes the following items:

- SR6G7-EVBC4000P rev. A evaluation board
- Power supply
- EULA

1.2 Supported devices

The SR6G7-EVBC4000P rev. A evaluation board supports the following STMicroelectronics family of microcontrollers in FPBGA 292:

- SR6G7C4

2 License agreement

The packaging of this evaluation board was sealed with a seal stating, by breaking this seal, you agree to the terms and conditions of the evaluation board license agreement, the terms and conditions of which are available at https://www.st.com/resource/en/evaluation_board_terms_of_use/evaluationproductlicenseagreement.pdf.

Upon breaking the seal, you and STMicroelectronics entered into the evaluation board license agreement, a copy of which is also enclosed with the evaluation board for convenience.

Attention: *This evaluation board only offers limited features for evaluating ST products. It has not been tested for use with other products and is not suitable for any safety or other commercial or consumer application. This evaluation board is otherwise provided "AS IS" and STMicroelectronics disclaims all warranties, express or implied, including the implied warranties of merchantability and fitness for a particular purpose.*

3 Handling precautions

Caution: *Handle the package content carefully to prevent electrostatic discharge.*

Before using the EVB or applying power, read the following sections to correctly configure the board. Incorrect configuration may cause irreparable damage to components, the MCU, or the EVB.

4 Hardware description overview

4.1 Hardware features

The SR6G7-EVBC4000P rev. A evaluation board has the following features:

- Socket for device in FPBGA 292 package
- Selectable clock source:
  - 40 MHz crystal main oscillator
  - 8 MHz oscillator
  - Clock input through SMA connector
- Debug interfaces:
  - MIPI10 connector for JTAG main DAP interface
  - ARM® JTAG 20 connector for main DAP interface
  - MIPI10 header connector for secondary DAP interface
  - Mictor40 connector for AURORA Trace interface
- Two 2x6 pins header connectors for SIPI interface
- All MCU signals readily accessible at a port-ordered group of 0.1” pitch headers
- USB to UART
- 4x CAN-FD interfaces : 2 channels with DB9 + 2 channels with a 2x4 header connector
- 4x LINFlexD interfaces
- 2x FlexRay interfaces : 1 DB9 connector
- 1x Ethernet port:
  - Ethernet 0: 1xRGMII 1Gb/s with RJ45 connector
- I²C interface: 2 channels
- User section: 3 push buttons; 8 LEDs; 2 potentiometers
- Extension module port (option)
  - 1x external module connector (DSPI, I²C, UART, GPIO, ANx)
  - 1x LCD display port
- 12 V external power supply

4.2 Hardware dimensions

The evaluation board has the following dimensions:

- PCB area: 270 mm x 230 mm
- Top components height: 20 mm
- Bottom components height: 3.0 mm
- PCB thickness 2.0 mm

5 Power and system configuration

5.1 Power supplies

The SR6G7-EVBC4000P rev. A evaluation board requires an external power supply voltage of 12 V DC and 2 A minimum. The single input voltage is regulated on-board using an L5963 switching regulator providing the supply voltages of 5.0 V and 3.3 V, and an A7986A switching regulator providing the supply voltage of 0.97 V.

5.2 Power supply connector

2.1 mm barrel connector:

Figure 4. 2.1 mm power connector

5.3 Power switch, status LEDs and fuse

The main power switch (slide switch S1) can be used to isolate the power supply input from the EVB voltage regulators if required.

When power is applied to the evaluation board, the power LEDs adjacent to the voltage regulators show the presence of the supply voltages as follows:

- LED LD1 – reset A
- LED LD2 – reset B
- LED LD7 – VDD_LV_IN
- LED LD8 – VDD_LV
- LED LD9 – VDD_HV_LP
- LED LD10 – 12 V
- LED LD11 – 5 V
- LED LD12 - 3V3
- LED LD13 – 5V_ADC
- LED LD14 – 3V3_ADC

If no LED is illuminated when power is applied to the evaluation board and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch S1 is in the “OFF” position or that the fuse F1 has blown. The fuse blows also if the power is applied to the evaluation board in reverse-bias.

The following jumpers are used to configure the power supply (common for all supported devices):

Table 1. Power configuration jumpers

Jumper	Description	Default	Position
JP1A	VDD_HV_ADx voltage configuration: • Open: VDD_HV_ADx not connected • Closed: VDD_HV_ADx connected to 3V3_ADC	Closed	B3(1)
JP1B	VDD_HV_ADR_D0 voltage configuration: • Open: VDD_HV_ADR_D0 not connected • Closed: VDD_HV_ADR_D0 connected to VDD_HV_IO_MAIN	Closed	B3(1)
JP1C	VDD_HV_IO_EXT0 voltage configuration: • Open: VDD_HV_IO_EXT0 not connected • Closed: VDD_HV_IO_EXT0 connected to 3V3	Closed	B2(1)
JP1D	VDD_HV_IO_EXT1 voltage configuration: • Open: VDD_HV_IO_EXT1 not connected • Closed: VDD_HV_IO_EXT1 connected to 3V3	Closed	C3(1)
JP1E	VDD_HV_IO_MAIN voltage configuration: • Open: VDD_HV_IO_MAIN not connected • Closed: VDD_HV_IO_MAIN connected to 3V3	Closed	C3(1)
JP1F	VDD_HV_NVM_PRG voltage configuration: • 1-2: Connected to 3V3 • 2-3: Connected to 5V	1-2	C2(1)
JP1G	VDD_HV_LP voltage configuration: • 1-2: VDD_HV_LP connected to 3V3 • 2-3: VDD_HV_LP connected to 5V	Closed	C3(1)
JP2B	VDD_LV_TRACE voltage configuration • Closed: VDD_LV_TRACE connected to VDD_LV • Open: VDD_LV_TRACE not connected	Closed	B2(1)
JP2C	VDD_LV voltage configuration • Closed: VDD_LV connected to VDD_LV_IN • Open: VDD_LV not connected	Closed	B2(1)
SB1	VDD_HV_ADR voltage connection • Open: VDD_HV_ADR not connected • Closed: VDD_HV_ADR connected to JP1A	Closed	C3(2)
SB2	VDD_HV_ADV voltage connection • Open: VDD_HV_ADV not connected • Closed: VDD_HV_ADV connected to JP1A	Closed	C3(2)
SB47	VDD_HV_IO_ADC voltage connection • Open: VDD_HV_IO_ADC connected to JP1B • Closed: VDD_HV_IO_ADC not connected	Open	C3(2)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*
2. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*

5.4 System clock configuration

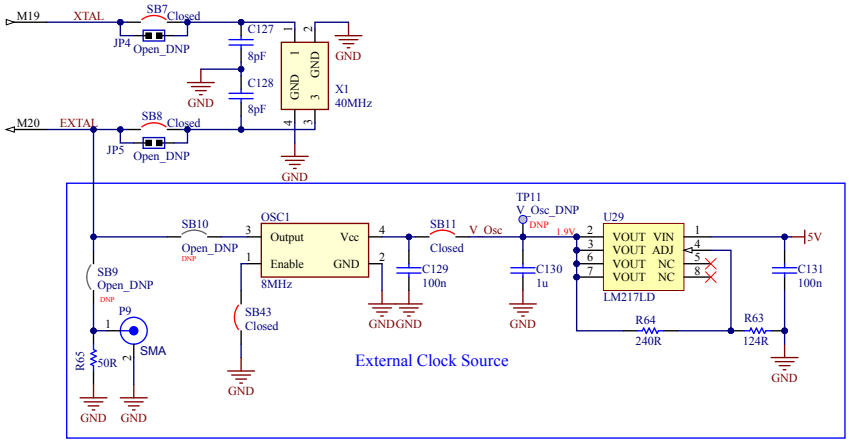
The evaluation board supports the usage of crystal clock sources as well as external clock source.

The following clock sources are supported:

- 40 MHz local crystal oscillator for PLL.
- 8 MHz
- A SMA connector is provided for the external clock input

The following figure shows the system oscillator schema.

Figure 5. System clock sources schema



The following table shows the system clock sources configuration setting:

Table 2. System clock configuration

Jumper	Description	Default	Position
SB7	XTAL configuration • Closed: connect pin 1 of the 40 MHz crystal (X1) to XTAL • Open: disconnect the 40 MHz crystal (X1).	Closed	C3(1)
SB8	EXTAL configuration • Closed: connect pin 3 of the 40 MHz crystal (X1) to EXTAL • Open: disconnect the 40 MHz crystal (X1).	Closed	C3(1)
SB9	System clock external source • Open: disconnect SMA connector (P2) from EXTAL • Closed: connect SMA connector (P2) to EXTAL	Open	C3(2)
SB10	EXTAL configuration • Open: disconnect the 8 MHz crystal (OSC1) from EXTAL. • Closed: connect pin 3 of the 8 MHz crystal (OSC1) to EXTAL	Closed	C3(2)
SB43	Enable 8 MHz oscillator • Open: Disabled • Closed: Enabled	Closed	C3(2)

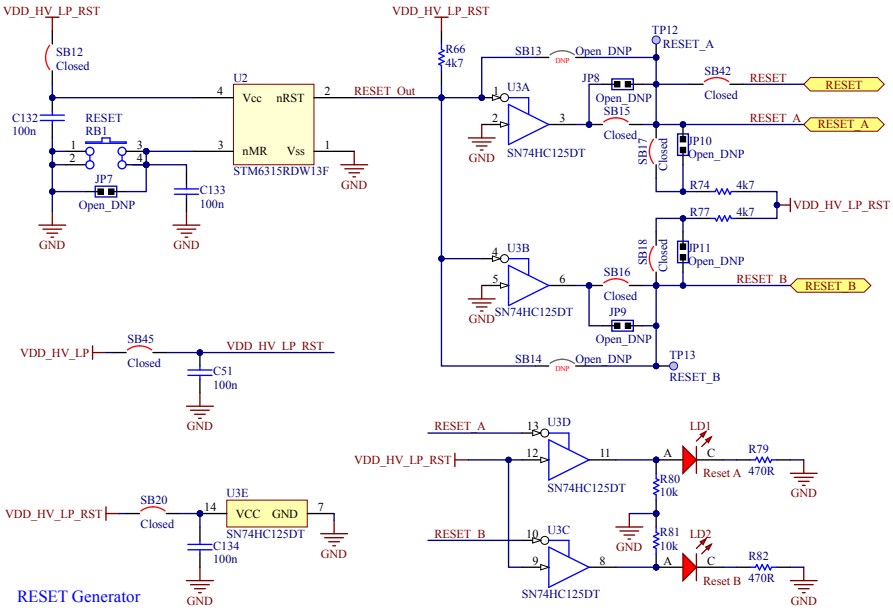
1. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*
2. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

5.5 Reset circuit

The reset circuit is performed using the STM6315 device.

The following picture shows the schema of the evaluation board reset circuit.

Figure 6. Reset circuit schema



To use and perform the reset driving there are different solder bridges:

Table 3. Reset configuration jumpers

Jumper	Description	Default	Position
RB1	Reset push button	Open	C1[1]
SB13	• Open: disconnect the RESET_A and the RESET signals from the reset out of the STM6315 device • Closed: directly connect the RESET_A and the RESET signals to the reset out of the STM6315 device	Open	C2[1]
SB14	• Open: disconnect the RESET_B signal from the reset out of the STM6315 device • Closed: directly connect the RESET_B signal to the reset out of the STM6315 device	Open	B2[2]
SB15	• Open: disconnect the external reset to RESET_A pin • Closed: connect the external reset to RESET_A pin	Closed	B2[2]
SB16	• Open: the external reset to RESET_B pin is disconnected • Closed: the external reset to RESET_B pin is disconnected	Closed	B2[2]
SB42	• Open: disconnect the external reset circuitry to the reset signal connected to the Ethernet • Closed: connect the external reset circuitry to the reset driver for ESR0 and PORST pins	Closed	C2[1]
JP7	Reset push button bypass	Open	C2[1]

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*
2. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*

5.6 Test mode configuration

The following picture shows the TESTMODE configuration schema.

Figure 7. Test mode configuration schema

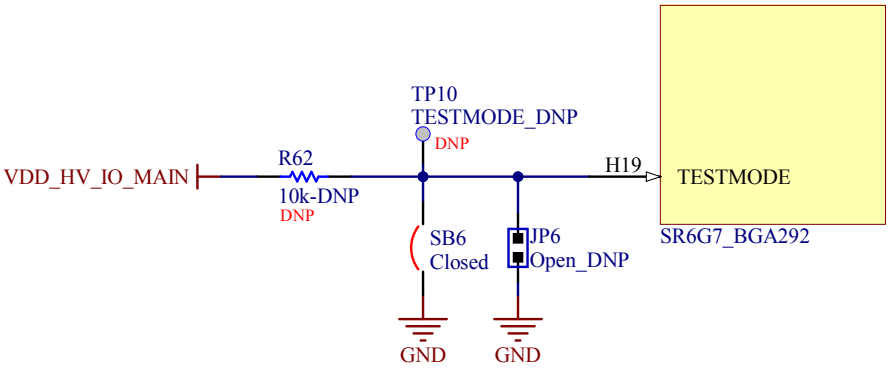


Table 4. Test mode

Jumper	Description	Default	Position
SB6	TESTMODE settings: • Open: TESTMODE pin is unconnected • Closed: TESTMODE pin is connected to GND	Closed	C2(1)

1. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*

5.7 External regulator configuration

This paragraph describes how to configure the board to allow the device to operate in the different configurations.

The configurations available are internal or external regulator mode by controlling the EXTREG_SEL pin. If EXTREG_SEL is connected to VDD_HV_LP, the external mode is selected. If EXTREG_SEL is connected to VSS, the internal mode is selected. This functionality is not available on all Stellar G family products. For the details of this product, refer to the datasheet document of the device used.

The following image shows the EXTREG_SEL configuration schema.

Figure 8. EXTREG_SEL configuration schema

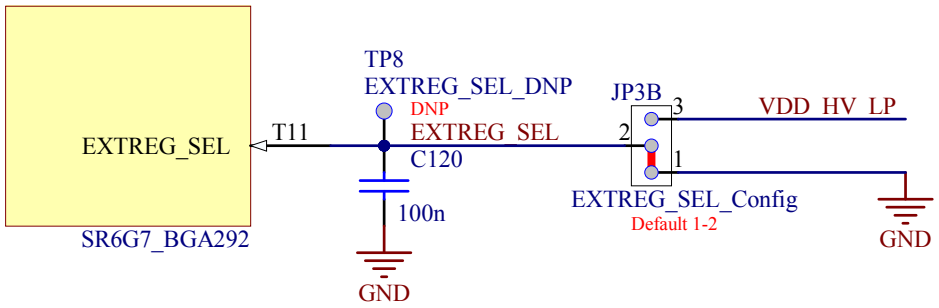


Table 5. EXTREG_SEL

Jumper	Description	Default	Position
JP3B	EXTREG_SEL settings: • 1-2: EXTREG_SEL connected to GND (internal regulator mode selected) • 2-3: EXTREG_SEL connected to VDD_HV_LP (external regulator mode selected)	1-2	B3(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6 Hardware description

6.1 1 Gb/s Ethernet 0 interface

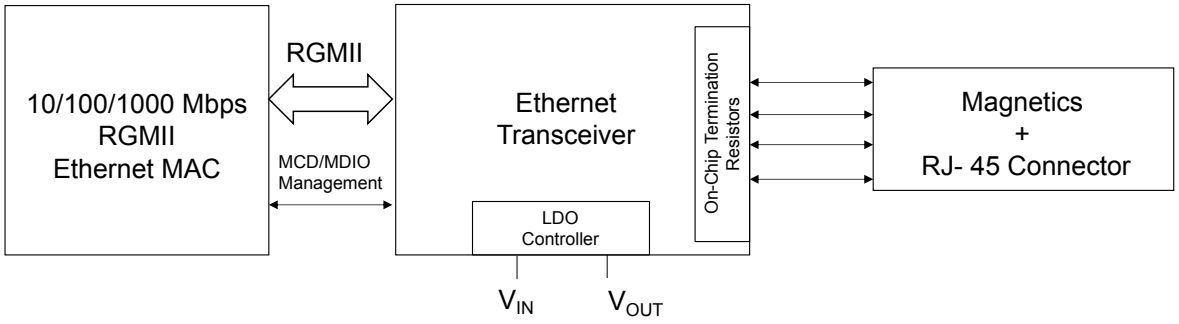
This paragraph describes the 1 Gb/s Ethernet 0 interface present on the board.

The Ethernet transceiver is KSZ9031RNXIA.

The Ethernet connector is RJ-45 with integrated magnetics.

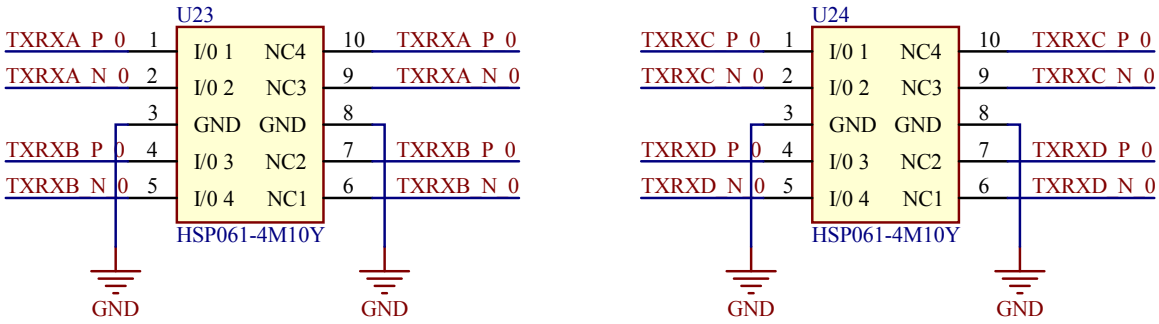
The following figure shows the functional diagram of the Ethernet interface.

Figure 9. 1 Gb/s Ethernet 0 functional diagram



The following figure shows the Ethernet ESD protection schema.

Figure 10. 1 Gb/s Ethernet 0 ESD protection schema



The following table describes all hardware of the 1 Gb/s Ethernet interface of the evaluation board, their position on PCB:

Table 6. 1 Gb/s Ethernet interface

Symbol	Description	Position
U23	ESD protection: HSP061-4M10Y	B1(1)
U24	ESD protection: HSP061-4M10Y	B1(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

The solder bridges detailed in the following table are used to configure the Ethernet 0 interfaces.

Table 7. Ethernet 0 configuration solder bridges

Jumper	Description	Default	Position
SB62	Ethernet 0 transceiver RESET_N filter configuration: • Open: disconnect the resistor-capacitor-diode (RCD) filter circuit • Closed: connect the resistor-capacitor-diode (RCD) filter circuit	Open	C1(1)
SB64	Ethernet 0 transceiver RESET_N configuration: • Open: use the resistor-capacitor-diode (RCD) filter • Closed: bypass the resistor-capacitor-diode (RCD) filter	Closed	C1(1)
SB65	Ethernet 0 transceiver LDO configuration: • Open: disconnect the 1V2_ETH_0 from the drain of the LDO MOSFET • Closed: connect the 1V2_ETH_0 from the drain of the LDO MOSFET	Closed	C1(1)
SB66	Ethernet 0 transceiver interrupt configuration: • Open: disconnect the transceiver Interrupt output • Closed: connect the transceiver Interrupt output to the ETH_0_PHY_INTR (PC11) of the device	Closed	B2(2)
SB67	Ethernet 0 transceiver clock 125 MHz configuration: • Open: disconnect the transceiver 125 MHz clock output • Closed: connect the transceiver 125 MHz clock output to the ETH_0_CLK_125 (PM2) of the device	Closed	B2(2)
SB68	Ethernet 0 transceiver MDIO configuration: • Closed: disconnect the transceiver MDIO • Closed: connect the transceiver MDIO to the ETH_0_MDIO (PM7) of the device	Closed	B2(2)
SB69	Ethernet 0 transceiver MDC configuration: • Open: disconnect the transceiver MDC • Closed: connect the transceiver MDC to the ETH_0_MDC (PM8) of the device	Closed	B2(2)
SB70	Ethernet 0 transceiver RGMII RXC (receive reference clock) configuration: • Open: disconnect the RGMII RXC (receive reference clock) output • Closed: connect the transceiver RGMII RXC (receive reference clock) output to the ETH_0_RX_CLK (PC10) of the device	Closed	B2(2)
SB71	Ethernet 0 transceiver RGMII RX_CTL configuration: • Open: disconnect the transceiver Interrupt output RGMII RX_CTL (receive control) output • Closed: connect the transceiver RGMII RX_CTL (receive control) output to the ETH_0_RX_DV (PM0) of the device	Closed	B2(2)
SB72	Ethernet 0 transceiver RGMII RD0 configuration: • Open: disconnect the transceiver RGMII RD0 (receive data 0) output • Closed: connect the transceiver RGMII RD0 (receive data 0) output to the ETH_0_RDATA0 (PC12) of the device	Closed	B2(2)
SB73	Ethernet 0 transceiver RGMII RD1 configuration: • Open: disconnect the transceiver RGMII RD1 (receive data 1) output • Closed: connect the transceiver RGMII RD1 (receive data 1) output to the ETH_0_RDATA1 (PC13) of the device	Closed	B2(2)
SB74	Ethernet 0 transceiver RGMII RD2 configuration: • Open: disconnect the transceiver RGMII RD2 (receive data 2) output • Closed: connect the transceiver RGMII RD2 (receive data 2) output to the ETH_0_RDATA2 (PM1) of the device	Closed	B2(2)
SB75	Ethernet 0 transceiver RGMII RD3 configuration: • Open: disconnect the transceiver RGMII RD3 (receive data 3) output • Closed: connect the transceiver RGMII RD3 (receive data 3) output to the ETH_0_RDATA3 (PK15) of the device	Closed	B2(2)

Jumper	Description	Default	Position
SB76	Ethernet 0 transceiver RGMII TX_CTL (transmit control) configuration: • Open: disconnect the transceiver RGMII TX_CTL (transmit control) input • Closed: connect the transceiver RGMII TX_CTL (transmit control) input to the ETH_0_TX_EN (PC14) of the device	Closed	B2(2)
SB77	Ethernet 0 transceiver RGMII TXC (transmit reference clock) configuration: • Open: disconnect the transceiver RGMII TXC (transmit reference clock) input • Closed: connect the transceiver RGMII TXC (transmit reference clock) input to the ETH_0_TX_CLK (PM6) of the device	Closed	B2(2)
SB78	Ethernet 0 transceiver RGMII TD0 (transmit data 0) configuration: • Open: disconnect the transceiver RGMII TD0 (transmit data 0) • Closed: connect the transceiver RGMII TD0 (transmit data 0) input to the ETH_0_TDATA0 (PC15) of the device	Closed	B2(2)
SB79	Ethernet 0 transceiver RGMII TD1 (transmit data 1) configuration: • Open: disconnect the transceiver RGMII TD1 (transmit data 1) • Closed: connect the transceiver RGMII TD1 (transmit data 1) to the ETH_0_TDATA1 (PE12) of the device	Closed	B2(2)
SB80	Ethernet 0 transceiver RGMII TD2 (transmit data 2) configuration: • Open: disconnect the transceiver RGMII TD2 (transmit data 2) • Closed: connect the transceiver RGMII TD2 (transmit data 2) to the ETH_0_TDATA2 (PM4) of the device	Closed	B2(2)
SB81	Ethernet 0 transceiver RGMII TD3 (transmit data 3) configuration: • Open: disconnect the transceiver RGMII TD3 (transmit data 3) • Closed: connect the transceiver RGMII TD3 (transmit data 3) to the ETH_0_TDATA3 (PM5) of the device	Closed	B2(2)

1. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*
2. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6.2 CAN interface

The SR6G7-EVBC4000P rev. A evaluation board has four MCP2542WFD high-speed CAN transceivers, two male standard DB9 connectors and one 4x2 header connector to provide physical CAN interfaces for the MCU.

The following table shows the CAN_0 DB9 connector pinout.

Table 8. CAN_0 DB9 connector pinout

Pin number (DB9)	Signal
1	N.C.
2	CAN_0_L
3	GND
4	N.C.
5	N.C.
6	GND
7	CAN_0_H
8	N.C.
9	N.C.

The following table shows the CAN_1 DB9 connector pinout (J5).

Table 9. CAN_1 DB9 connector pinout

Pin number (DB9)	Signal
1	N.C.
2	CAN_1_L
3	GND
4	N.C.
5	N.C.
6	GND
7	CAN_1_H
8	N.C.
9	N.C.

The following table shows the 4x2 header connector pinout (P5).

Table 10. 4x2 header CAN2 and CAN3 connector pinout

Pin number (DB9)	Signal
1	CAN_2_H
2	GND
3	CAN_2_L
4	GND
5	CAN_3_H
6	GND
7	CAN_3_L
8	GND

The jumpers and the solder bridges detailed in the following table are used to configure the CAN interfaces.

Table 11. CAN configuration jumpers and solder bridges

Jumper	Description	Default	Position
SB33	CAN 0 transceiver VIO supply configuration: • Open: disconnect the VDD_HV_IO_MAIN from the VIO of the CAN 0 transceiver • Closed: connect the VDD_HV_IO_MAIN to the VIO of the CAN 0 transceiver	Closed	D1(1)
SB34	CAN 0 transceiver VDD supply configuration: • Open: disconnect the VDD of the CAN 0 transceiver from the 5 V domain. • Closed: connect the VDD of the CAN 0 transceiver to the 5 V domain.	Closed	D1(1)
JP15A	CAN_0_STB configuration: • Open: disconnect PE7 from CAN_0_STB • Closed: connect PE7 to CAN_0_STB	Closed	A2(2)
JP15B	CAN_0_TX configuration: • Open: disconnect PE5 from CAN_0_TX • Closed: connect PE5 to CAN_0_TX	Closed	A1(2)
JP15C	CAN_0_RX configuration: • Open: disconnect PG14 from CAN_0_RX • Closed: connect PG14 to CAN_0_RX	Closed	A1(2)
JP16A	CAN_0_L termination resistor configuration: • Open: disconnect the termination resistor • Closed: connect CAN_0_L to a 60.4 Ω termination resistor	Closed	A1(2)
JP16B	CAN_0_H termination resistor configuration: • Open: disconnect the termination resistor • Closed: connect CAN_0_H to a 60.4 Ω termination resistor	Closed	A1(2)
SB35	CAN 1 transceiver VIO supply configuration: • Open: disconnect the VDD_HV_IO_MAIN from the VIO of the CAN 1 transceiver • Closed: connect the VDD_HV_IO_MAIN to the VIO of the CAN1 transceiver	Closed	D1(1)
SB36	CAN 1 transceiver VDD supply configuration: • Open: disconnect the VDD of the CAN 1 transceiver from the 5 V domain. • Closed: connect the VDD of the CAN 1 transceiver to the 5 V domain.	Closed	D1(1)
JP17A	CAN_1_STB configuration: • Open: disconnect PD9 from CAN_1_STB • Closed: connect PD9 to CAN_1_STB	Closed	A1(2)
JP17B	CAN_1_TX configuration: • Open: disconnect PD3 from CAN_1_TX • Closed: connect PD3 to CAN_1_TX	Closed	A1(2)
JP17C	CAN_1_RX configuration: • Open: connect PD2 to CAN_1_RX • Closed: dis connect PD2 to CAN_1_RX	Closed	A1(2)
JP18A	CAN_1_L termination resistor configuration: • Open: disconnect the termination resistor • Closed: connect CAN_1_L to a 60.4 Ω termination resistor	Closed	A1(2)
JP18B	CAN_1_H termination resistor configuration: • Open: disconnect the termination resistor • Closed: connect CAN_1_H to a 60.4 Ω termination resistor	Closed	A1(2)
SB37	CAN 2 transceiver VIO supply configuration: • Open: disconnect the VDD_HV_IO_MAIN from the VIO of the CAN transceiver • Closed: connect the VDD_HV_IO_MAIN to the VIO of the CAN transceiver	Closed	B4(1)

Jumper	Description	Default	Position
SB38	CAN 2 transceiver VDD supply configuration: • Open: disconnect the VDD of the U7 CAN 2 transceiver from the 5 V domain. • Closed: connect the VDD of the U7 CAN 2 transceiver to the 5 V domain.	Closed	B4(1)
JP19A	CAN_2_STB configuration: • Open: disconnect PL10 from CAN_2_STB • Closed: connect PL10 to CAN_2_STB	Closed	B4(2)
JP19B	CAN_2_TX configuration: • Open: disconnect PF0 from CAN_2_TX • Closed: connect PF0 to CAN_2_TX	Closed	B4(2)
JP19C	CAN_2_RX configuration: • Open: connect PF1 to CAN_2_RX • Closed: dis connect PF1 to CAN_2_RX	Closed	B4(2)
JP20A	CAN_2_L termination resistor configuration: • Open: disconnect the termination resistor • Closed: Connect CAN_2_L to a 60.4 Ω termination resistor	Closed	B4(2)
JP20B	CAN_2_H termination resistor configuration: • Open: disconnect the termination resistor • Closed: Connect CAN_2_H to a 60.4 Ω termination resistor	Closed	B4(2)
SB39	CAN 3 transceiver VIO supply configuration: • Open: disconnect the VDD_HV_IO_MAIN from the VIO of the AN transceiver • Closed: connect the VDD_HV_IO_MAIN to the VIO of the CAN transceiver	Closed	B4(1)
SB40	CAN 3 transceiver VDD supply configuration: • Open: disconnect the VDD of the CAN 3 transceiver from the 5 V domain. • Closed: connect the VDD of the CAN 3 transceiver to the 5 V domain.	Closed	B4(1)
JP21A	CAN_3_STB configuration: • Open: disconnect PA15 from CAN_3_STB • Closed: connect PA15 to CAN_3_STB	Closed	B4(2)
JP21B	CAN_3_TX configuration: • Open: disconnect PB9 from CAN_3_TX • Closed: connect PB9 to CAN_3_TX	Closed	B4(2)
JP21C	CAN_3_RX configuration: • Open: disconnect PA3 from CAN_3_RX • Closed: connect PA3 to CAN_3_RX	Closed	B4(2)
JP22A	CAN_3_L termination resistor configuration: • Open: disconnect the termination resistor • Closed: Connect CAN_3_L to a 60.4 Ω termination resistor	Closed	B4(2)
JP22B	CAN_3_H termination resistor configuration: • Open: disconnect the termination resistor • Closed: Connect CAN_3_H to a 60.4 Ω termination resistor	Closed	B4(2)

1. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*
2. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6.3 FlexRay interface

The SR6G7-EVBC4000P rev. A evaluation board is fitted with two FlexRAY transceivers , one female DB9 connector and some jumpers used to route the respective MCU signals to the physical interfaces.

The following picture shows the FlexRAY DB9 connector.

Figure 11. FlexRAY 0 and 1 DB9 female connector

The following table describes the pinout of the FlexRay 0 and 1 DB9 connector.

Table 12. FlexRay 0 and 1 DB9 connector pinout

Pin number	Signal
1	N.C.
2	BM0 (bus line minus 0)
3	GND
4	BM1 (bus line minus 1)
5	GND
6	N.C.
7	BP0 (bus line plus 0)
8	BP1 (bus line plus 1)
9	N.C.

The jumpers and the solder bridges detailed in the following table are used to configure the FlexRay interfaces.

Table 13. FlexRAY control jumpers and solder bridges

Jumper	Description	Default	Position
SB50	FlexRay 0 transceiver VCC and VBUF connection: • Open: FlexRay 0 transceiver VCC and VBUF not connected • Closed: FlexRay 0 transceiver VCC and VBUF connected to 5 V	Closed	D1(1)
SB51	FlexRay 0 transceiver VBAT connection: • Open: FlexRay 0 transceiver VBAT not connected • Closed: FlexRay 0 transceiver VBAT connected to 12 V	Closed	A1(2)
SB58	FlexRay 0 transceiver supply voltage: • Open: FlexRay 0 supply voltage transceiver not connected • Closed: FlexRay 0 supply voltage transceiver connected to VDD_HV_IO_MAIN	Closed	A1(2)
JP31A	Flex_TXD_0 connection: • Open: Flex_TXD_0 not connected • Closed: Flex_TXD_0 connected to PH7	Closed	A1(2)
JP31B	Flex_TXEN_0 connection: • Open: Flex_TXEN_0 not connected • Closed: Flex_TXEN_0 connected to PH8	Closed	A1(2)

Jumper	Description	Default	Position
JP31C	Flex_RXD_0 connection: • Open: Flex_RXD_0 not connected • Closed: Flex_RXD_0 connected to PH9	Closed	A1(2)
JP32A	FlexRay 0 BM input resistance: • Open: 47 Ω R_{Bus} not connected • Closed: 47 Ω R_{Bus} connected	Closed	A1(2)
JP32B	FlexRay 0 BP input resistance: • Open: 47 Ω R_{Bus} not connected Closed: 47 Ω R_{Bus} connected	Closed	A1(2)
SB52	FlexRay 1 transceiver VCC and VBUF connection: • Open: FlexRay 1 transceiver VCC and VBUF not connected • Closed: FlexRay 1 transceiver VCC and VBUF connected to 5 V	Closed	C1(1)
SB53	FlexRay 1 transceiver VBAT connection: • Open: FlexRay 1 transceiver VBAT not connected • Closed: FlexRay 1 transceiver VBAT connected to 12 V	Closed	B1(2)
SB59	FlexRay 1 transceiver supply voltage: • Open: FlexRay 1 supply voltage transceiver not connected • Closed: FlexRay 1 supply voltage transceiver connected to VDD_HV_IO_MAIN	Closed	B1(2)
JP31D	Flex_TXD_1 connection: • Open: Flex_TXD_1 not connected • Closed: Flex_TXD_1 connected to PH3	Closed	B1(2)
JP31E	Flex_TXEN_1 connection: • Open: Flex_TXEN_1 not connected • Closed: Flex_TXEN_1 connected to PH4	Closed	B1(2)
JP31F	Flex_RXD_1 connection: • Open: Flex_RXD_1 not connected • Closed: Flex_RXD_1 connected to PH10	Closed	B1(2)
JP33A	FlexRay 1 BM input resistance: • Open: 47 Ω R_{Bus} not connected • Closed: 47 Ω R_{Bus} connected	Closed	B1(2)
JP33B	FlexRay 1 BP input resistance: • Open: 47 Ω R_{Bus} not connected • Closed: 47 Ω R_{Bus} connected	Closed	B1(2)

1. *Refer to the Figure 20. SR6G7-EVBC4000P rev. A - bottom.*
2. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6.4 UART interface

The board contains an FT2232HL with two receivers and two drivers.

The connector is a MOLEX connector, SMT, right angle, USB MINI-B, 5 pins.

Each TX and RX pin has a jumper allowing the possibility to disconnect the default pin and connect another pin.

The following table shows the UART interface jumpers configuration.

Table 14. UART interface pin configuration

Jumper	Description	Default	Position
JP14A	UART_A_RX connection: • Open: UART_A_RX not connected • Closed: UART_A_RX connected to PD12	Closed	A4(1)
JP14B	UART_A_TX connection: • Open: UART_A_TX not connected • Closed: UART_A_TX connected to PD13	Closed	A4(1)
JP14C	UART_B_RX connection: • Open: UART_B_RX not connected • Closed: UART_B_RX connected to PJ4	Closed	A3(1)
JP14D	UART_B_TX connection: • Open: UART_B_TX not connected • Closed: UART_B_TX connected to PH6	Closed	A3(1)
SB24	TX_A_USB connection • Open: TX_A_USB not connected • Closed: TX_A_USB connected to UART_A_TX using a level shifter	Closed	A3(1)
SB25	RX_A_USB connection • Open: RX_A_USB not connected • Closed: RX_A_USB connected to UART_A_RX using a level shifter	Closed	A3(1)
SB26	USB A DTR and DSR connection • Open: DTR and DSR not connected • Closed: DTR and DSR connected	Closed	A3(1)
SB27	USB A DCD and RIconnection • Open: DCD and RI not connected • Closed: DCD and RI connected	Closed	A3(1)
SB30	TX_B_USB connection • Open: TX_B_USB not connected • Closed: TX_B_USB connected to UART_B_TX using a level shifter	Closed	A3(1)
SB31	RX_A_USB connection • Open: RX_B_USB not connected • Closed: RX_B_USB connected to UART_B_RX using a level shifter	Closed	A3(1)
SB28	USB B DTR and DSR connection • Open: DTR and DSR not connected • Closed: DTR and DSR connected	Closed	A3(1)
SB29	USB B DCD and RIconnection • Open: DCD and RI not connected • Closed: DCD and RI connected	Closed	A3(1)
SB32	USB GND connection • Open: USB_GND not connected • Closed: USB_GND connected to GND	Closed	A3(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

The following table shows the UART interface LEDs.

Table 15. UART interface LEDs

LED	Description	Position
LED3	RX_A_LED	A3(1)
LED4	TX_A_LED	
LED5	RX_B_LED	
LED6	TX_B_LED	

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6.5 LINFlexD interface

The SR6G7-EVBC4000P rev. A evaluation board is fitted with two dual channels LIN transceiver and one 2x4 header connector.

The following table shows the 2x4 header connector pinout (P8).

Table 16. LINFlexD header 2x4 pins connector pinout

Pin number	Signal
1	LIN_0
2	VBat_LIN_A
3	LIN_1
4	GND
5	LIN_2
6	VBat_LIN_B
7	LIN_3
8	GND

The jumpers detailed in the following table are used to configure the LINFlex interfaces.

Table 17. LINFlexD interface configuration jumpers and solder bridges

Jumper	Description	Default	Position
JP26A	LINFlex 0 sleep control input connection: • Open: LINFlex 0 sleep control input not connected. • Closed: LINFlex 0 sleep control input connected to VDD_HV_IO_MAIN.	Closed	A3(1)
JP26B	LINFlex 1 sleep control input connection: • Open: LINFlex 1 sleep control input not connected. • Closed: LINFlex 1 sleep control input connected to VDD_HV_IO_MAIN.	Closed	A3(1)
JP30A	LINFlex 2 sleep control input connection: • Open: LINFlex 2 sleep control input not connected. • Closed: LINFlex 2 sleep control input connected to VDD_HV_IO_MAIN.	Closed	A2(1)
JP30B	LINFlex 3 sleep control input connection: • Open: LINFlex 3 sleep control input not connected. • Closed: LINFlex 3 sleep control input connected to VDD_HV_IO_MAIN.	Closed	A2(1)
JP25A	LIN_0_RX connection: • Open: LIN_0_RX not connected • Closed: LIN_0_RX connected to PD0	Closed	A3(1)

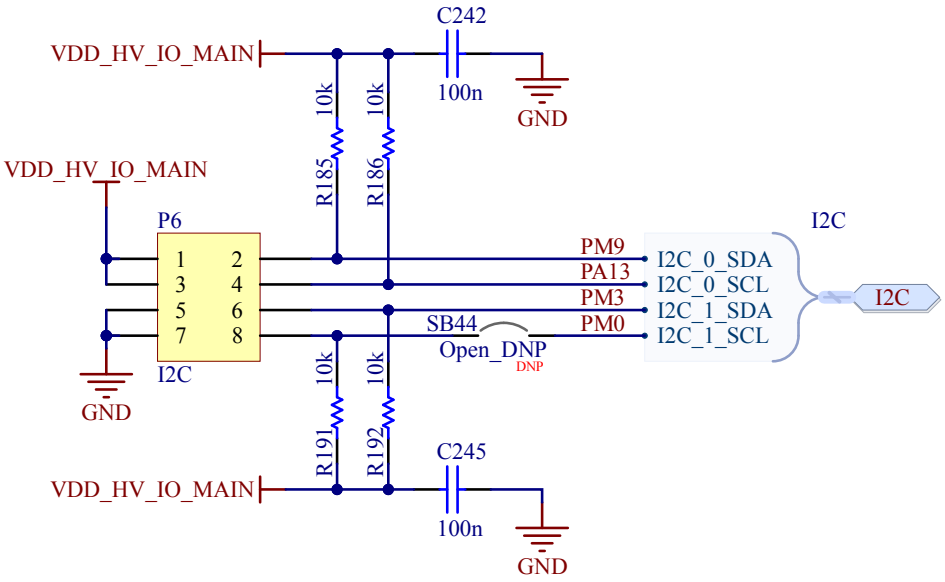
Jumper	Description	Default	Position
JP25B	LIN_0_TX connection: • Open: LIN_0_TX not connected • Closed: LIN_0_TX connected to PD1	Closed	A3(1)
JP25C	LIN_1_RX connection: • Open: LIN_1_RX not connected • Closed: LIN_1_RX connected to PA1	Closed	A3(1)
JP25D	LIN_1_TX connection: • Open: LIN_1_TX not connected • Closed: LIN_1_TX connected to PA0	Closed	A3(1)
JP28A	LIN_2_RX connection: • Open: LIN_2_RX not connected • Closed: LIN_2_RX connected to PA11	Closed	A3(1)
JP28B	LIN_2_TX connection: • Open: LIN_2_TX not connected • Closed: LIN_2_TX connected to PA10	Closed	A2(1)
JP28C	LIN_3_RX connection: • Open: LIN_3_RX not connected • Closed: LIN_3_RX connected to PC1	Closed	A2(1)
JP28D	LIN_3_TX connection: • Open: LIN_3_TX not connected • Closed: LIN_3_TX connected to PC2	Closed	A2(1)
JP27A	LIN_0_Config (master/slave): • 1-2: Master mode • 2-3: Slave mode	1-2 (Master mode)	A3(1)
JP27B	LIN_1_Config (master/slave): • 1-2: Master mode • 2-3: Slave mode	1-2 (Master mode)	A3(1)
JP29A	LIN_2_Config (master/slave): • 1-2: Master mode • 2-3: Slave mode	1-2 (Master mode)	A2(1)
JP29B	LIN_3_Config (master/slave): • 1-2: Master mode • 2-3: Slave mode	1-2 (Master mode)	A2(1)
SB48	VBat_LIN_A connection: • Open: VBat_LIN_A not connected • Closed: VBat_LIN_A connected to 12 V domain	Closed	A3(1)
SB49	VBat_LIN_B connection: • Open: VBat_LIN_B not connected • Closed: VBat_LIN_B connected to 12 V domain	Closed	A2(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6.6 I²C interface

This paragraph describes the embedded I²C interface present on the board.
The following figure shows the I²C schema.

Figure 12. I²C schema



The following table shows the 2x4 header connector pinout (P7).

Table 18. I²C header 2x4 pins connector pinout

Pin number	Signal
1	VDD_HV_IO_MAIN
2	I2C_0_SDA
3	VDD_HV_IO_MAIN
4	I2C_0_SCL
5	GND
6	I2C_1_SDA
7	GND
8	I2C_1_SCL

6.7 Debug connectors

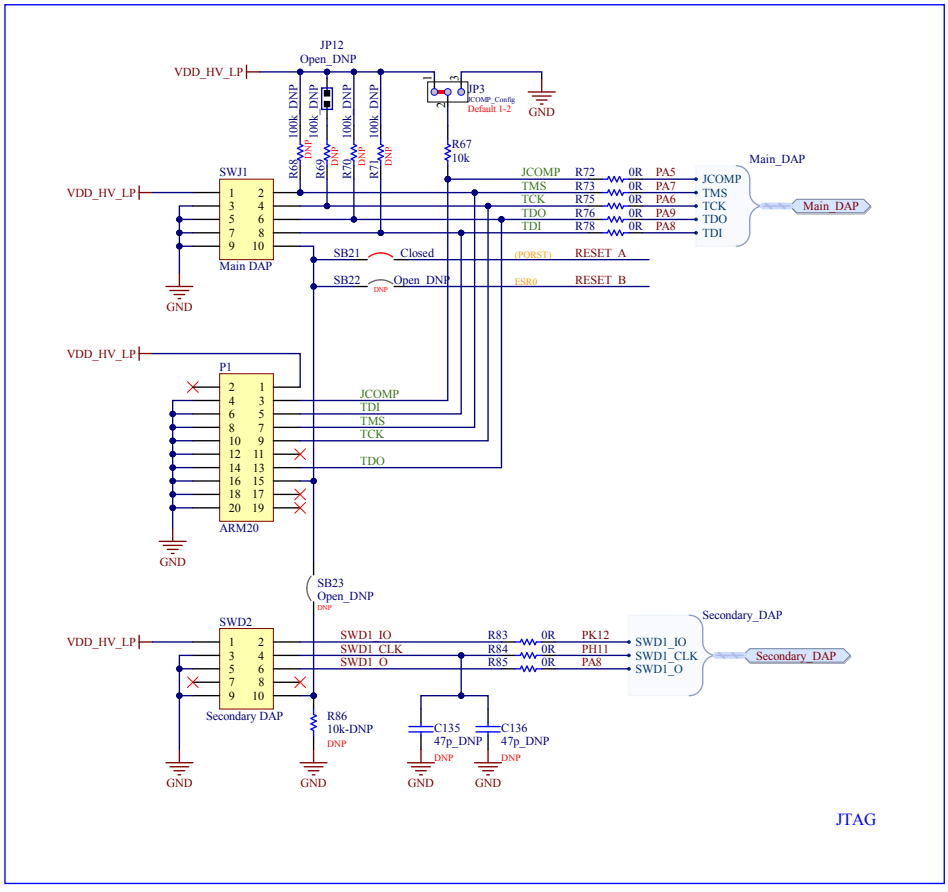
The SR6G7-EVBC4000P rev. A evaluation board has the following debug connectors:

Table 19. Debug connectors

Connectors	Description
SWJ1	10-pin header connector for JTAG/Main DAP interface
P1	20-pin ARM Connector for JTAG/Main DAP interface
SWD2	10-pin header connector for Secondary DAP interface
P3	12-pin header connector for SIPI 0 interface
P4	12-pin header connector for SIPI 1 interface
J15	NEXUS 2x20-pin connector for AURORA interface

The following figure shows the main DAP connectors and the secondary DAP connector schema.

Figure 13. Debug connectors schema



The following tables show the 2x5 and 2x10 header connectors pinout:

Table 20. SWJ1 main DAP header 2x5 pins connector pinout

Pin number	Signal
1	VDD_HV_IO_MAIN
2	TMS
3	GND
4	TCK
5	GND
6	TDO
7	GND
8	TDI
9	GND
10	Configurable pin between: • RESET_A • RESET_B

Table 21. P1 main DAP header 2x10 pins connector pinout

Pin number	Signal
1	VDD_HV_IO_MAIN
2	N.C.
3	JCOMP
4	GND
5	TDI
6	GND
7	TMS
8	GND
9	TCK
10	GND
11	N.C.
12	GND
13	TDO
14	GND
15	Configurable pin between: • RESET_A • RESET_B
16	GND
17	N.C.
18	GND
19	N.C.
20	GND

Table 22. SWD2 secondary DAP header 2x5 pins connector pinout

Pin number	Signal
1	VDD_HV_IO_MAIN
2	SWD1_IO
3	GND
4	SWD1_CLK
5	GND
6	SWD1_O
7	N.C.
8	N.C.
9	GND
10	Configurable pin between: • RESET_A • RESET_B • Pull down

The following table describes all jumpers, all 0R resistors and all solder bridges used to configure the JTAG/Main DAP and the secondary DAP ports of the board and their position on the PCB.

Table 23. JTAG/Main DAP and secondary DAP configuration

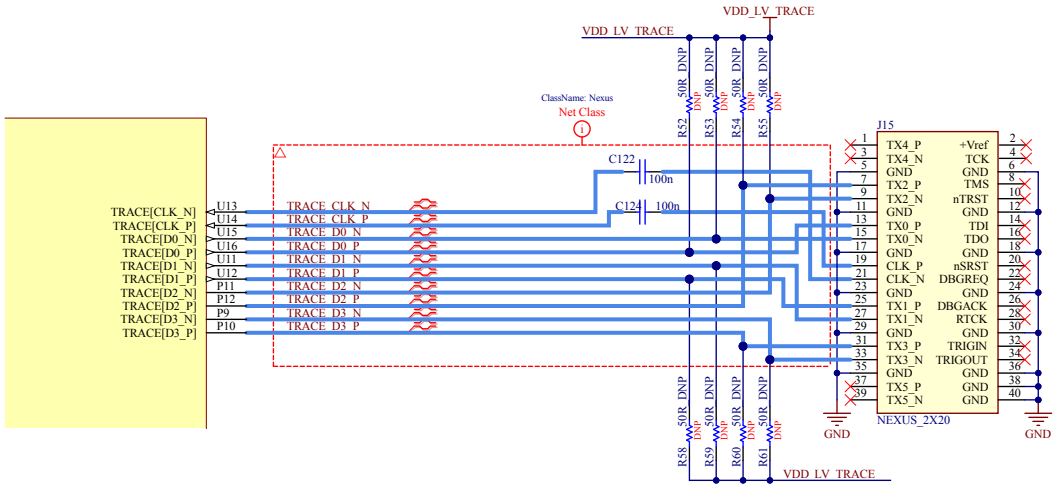
Reference	Description	Default	Position
JP3	JCOMP configuration: • 1-2: JCOMP connected to 10 kΩ pull-up resistor to VDD_HV_IO_MAIN • 2-3: JCOMP connected to 10 kΩ pull-down resistor.	1-2	C3(1)
R72	JCOMP connection configuration: • Mounted: PA5 connected to JCOMP • Not mounted: PA5 not connected to JCOMP	Mounted	C3(1)
R73	TMS configuration: • Mounted: PA7 connected to TMS • Not mounted: PA7 not connected to TMS	Mounted	C3(1)
R75	TCK configuration: • Mounted: PA6 connected to TCK • Not mounted: PA6 not connected to TCK	Mounted	C2(1)
R76	TDO configuration: • Mounted: PA9 connected to TDO • Not mounted: PA9 not connected to TDO	Mounted	C2(1)
R78	TDI configuration: • Mounted: PA8 connected to TDI • Not mounted: PA8 not connected to TDI	Mounted	C2(1)
R83	SWD1_IO configuration: • Mounted: PK12 connected to SWD1_IO • Not mounted: PK12 not connected to SWD1_IO	Mounted	C2(1)
R84	SWD1_CLK configuration: • Mounted: PK11 connected to SWD1_CLK • Not mounted: PK11 not connected to SWD1_CLK	Mounted	C2(1)
R85	SWD1_O configuration: • Mounted: PA8 connected to SWD1_O • Not mounted: PA8 not connected to SWD1_0	Mounted	C2(1)

Reference	Description	Default	Position
SB21	JTAG/Main DAP reset pin configuration: • Open: JTAG/Main DAP reset pin not connected to RESET_A • Closed: JTAG/Main DAP reset pin connected to RESET_A	Closed	C2(1)
SB22	JTAG/Main DAP reset pin configuration: • Open: JTAG/Main DAP reset pin not connected to RESET_B • Closed: JTAG/Main DAP reset pin connected to RESET_B	Open	C2(1)
SB23	Secondary DAP reset pin configuration: • Open: Secondary DAP reset pin not connected to JTAG/Main DAP reset pin • Closed: Secondary DAP reset pin connected to JTAG/Main DAP reset pin	Open	C2(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

The following figure shows the AURORA schema.

Figure 14. J15 AURORA schema



The following table shows the 2x4 header connector pinout.

Table 24. J15 AURORA 2x20 pins connector pinout

Pin number	Signal
1	N.C.
2	N.C.
3	N.C.
4	N.C.
5	N.C.
6	GND
7	TRACE_D2_P
8	N.C.
9	TRACE_D2_N
10	N.C.
11	GND
12	GND

Pin number	Signal
13	TRACE_D0_P
14	N.C.
15	TRACE_D0_N
16	N.C.
17	GND
18	GND
19	TRACE_CLK_P
20	N.C.
21	TRACE_CLK_N
22	N.C.
23	GND
24	GND
25	TRACE_D1_P
26	N.C.
27	TRACE_D1_N
28	N.C.
29	GND
30	GND
31	TRACE_D3_P
32	N.C.
33	TRACE_D3_N
34	N.C.
35	GND
36	GND
37	N.C.
38	GND
39	N.C.
40	GND

6.8 I/O port connectors

On the SR6G7-EVBC4000P rev. A evaluation board, all the MCU IO pins are available through 2x9 pins header connectors connected to each device I/O port.

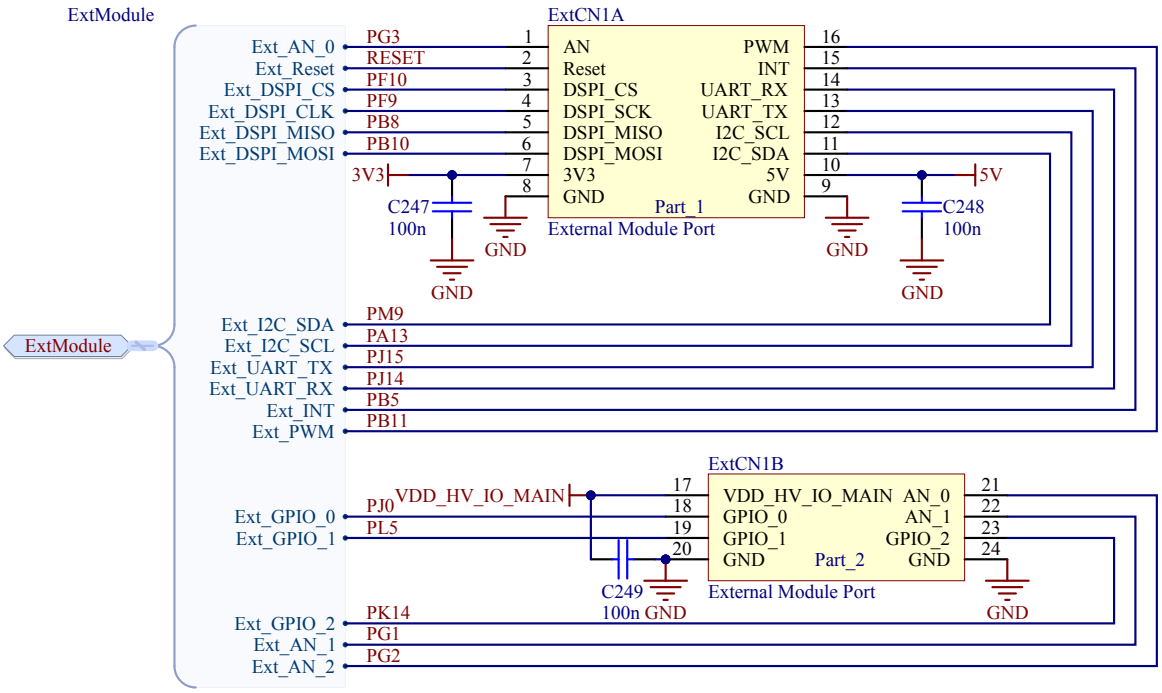
There are n.13 header connectors from port “A” to port “M”.

6.9 Extension module port

The SR6G7-EVBC4000P rev. A evaluation board is fitted with a 12x2 header connector.

The following figure shows the pinout of the connector.

Figure 15. Extension module connectors schema



The following table shows the connector pin mapping.

Table 25. External module connector pins mapping

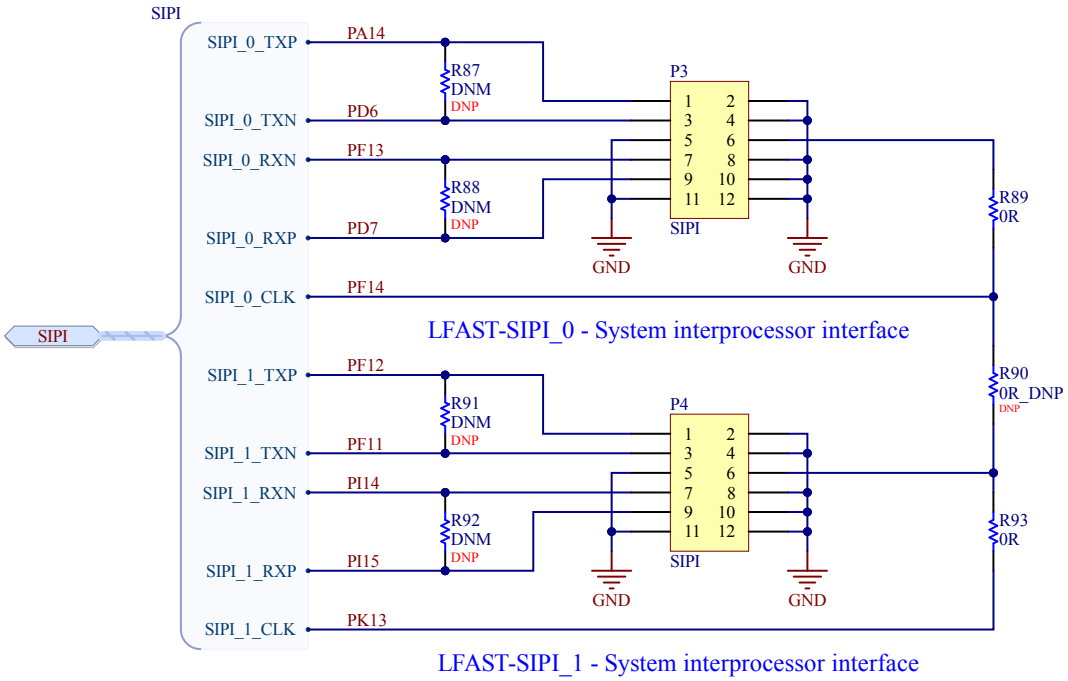
Pin number	Pin name	Port
1	Ext_AN_0	PG[03]
2	Ext_Reset	-
3	Ext_DSPI_CS	PF[10]
4	Ext_DSPI_CLK	PF[9]
5	Ext_DSPI_MISO	PB[8]
6	Ext_DSPI_MOSI	PB[10]
7	3V3	-
8	GND	-
9	GND	-
10	5V	-
11	Ext_I2C_SDA	PM[09]

Pin number	Pin name	Port
12	Ext_I2C_SCL	PA[13]
13	Ext_UART_TX	PJ[15]
14	Ext_UART_RX	PJ[14]
15	Ext_INT	PB[05]
16	Ext_PWM	PB[11]
17	VDD_HV_IO_MAIN	-
18	Ext_GPIO_0	PJ[00]
19	Ext_GPIO_1	PL[05]
20	GND	-
21	Ext_GPIO_2	PG[02]
22	Ext_AN_1	PG[01]
23	Ext_AN_2	PK[14]
24	GND	-

6.10 SIPI

On the SR6G7-EVBC4000P rev. A evaluation board there are two SIPI connectors.
The following figure shows the SIPI connection schema.

Figure 16. SIPI connectors schema



The following tables show the 2x5 header connectors pinout (P3->SIPI_0 P4->SIPI_1).

Table 26. SIPI_0 header 2x6 pins connector pinout

Pin number	Signal
1	SIPI_0_TXP (PA[14])
2	GND
3	SIPI_0_TXN (PD[6])
4	GND
5	GND
6	SIPI_0_CLK (PF[14])
7	SIPI_0_RXN (PF[13])
8	GND
9	SIPI_0_RXP (PD[7])
10	GND
11	GND
12	GND

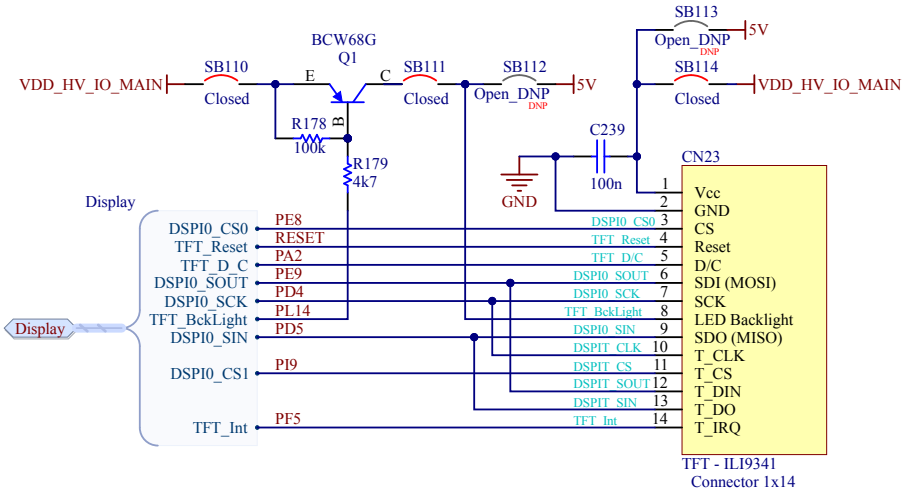
Table 27. SIPI_1 header 2x6 pins connector pinout

Pin number	Signal
1	SIPI_1_TXP (PF[12])
2	GND
3	SIPI_1_TXN (PF[11])
4	GND
5	GND
6	SIPI_1_CLK (PK[13])
7	SIPI_1_RXN (PI[14])
8	GND
9	SIPI_1_RXP (PI[15])
10	GND
11	GND
12	GND

6.11 Display port

The SR6G7-EVBC4000P rev. A evaluation board is fitted with a 14-pin TFT ILI9341 connector.
The following figure shows the pinout of the connector.

Figure 17. Display port schema



The following table shows the connector pin mapping.

Table 28. External module connector pins mapping

Pin number	Pin name	Port
1	V_{CC}	-
2	GND	-
3	DSPI0_CS0	PE[08]
4	Reset	-
5	TFT_D_C	PA[02]
6	DSPI0_SOUT	PE[09]
7	DSPI0_SCK	PD[04]
8	TFT_BckLight	PL[14]
9	DSPI0_SIN	PD[05]
10	DSPI1_CLK	PD[04]
11	DSPI1_CS0	PI[09]
12	DSPI1_SOUT	PE[09]
13	DSPI1_SIN	PD[05]
14	TFT_Int	PF[05]

6.12 User area

There is a user area on the SR6G7-EVBC4000P rev. A evaluation board, consisting of the following features:

- 8 LEDs
- 3 pushbuttons
- 2 potentiometers

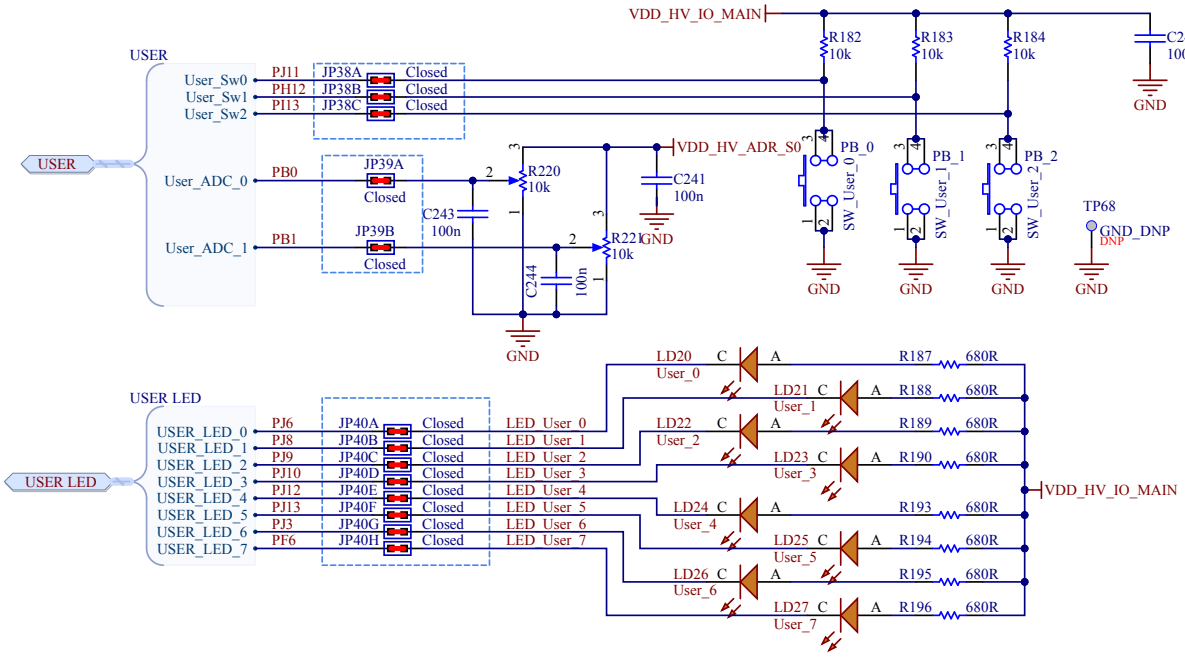
There are eight active low user LEDs D20, D21, D22, D23, D24, D25, LD26 and LD27. The LED inputs are pulled to VDD_HV_IO_MAIN through 680 Ω resistors.

There are three active high pushbuttons: PB_0, PB_1 and PB_2 which will drive VDD_HV_IO_MAIN onto the respective pins when pushed. The switch outputs are pulled to GND via 10 kΩ.

There are two potentiometers: R220 and R221 connected to JP39A and JP39B and they are adjustable between VDD_HV_ADR and GND.

The following figure shows the user area schema.

Figure 18. User area schema



The following table describes all jumpers used to configure the user area of the board and their position on PCB.

Table 29. User area interface configuration

Jumper	Description	Default	Position
JP38A	User_Sw0 (PJ11) configuration: • Open: User_Sw0 (PJ11) not connected • Closed: User_Sw0 (PJ11) connected to push button 1 (PB_1)	Closed	B4[1]
JP38B	User_Sw1 (PJ12) configuration: • Open: User_Sw1 (PH12) not connected • Closed: User_Sw1 (PH12) connected to push button 2 (PB_2)	Closed	B4[1]
JP38C	User_Sw2 (PJ13) configuration: • Open: User_Sw3 (PI13) not connected • Closed: User_Sw3 (PI13) connected to push button 1 (PB_3)	Closed	B4[1]

Jumper	Description	Default	Position
JP39A	User_ADC_0 (PB0) configuration: • Open: User_ADC_0 (PB0) not connected • Closed: User_ADC_0 (PB0) connected to potentiometer (R220)	Closed	B4(1)
JP39B	User_ADC_1 (PB1) configuration: • Open: User_ADC_1 (PB1) not connected • Closed: User_ADC_1 (PB1) connected to potentiometer (R221)	Closed	B4(1)
JP40A	User_LED_0 (PJ6) configuration: • Open: User_LED_0 (PJ6) not connected • Closed: User_LED_0 (PJ6) connected to LED (LD20)	Closed	B4(1)
JP40B	User_LED_1 (PJ8) configuration: • Open: User_LED_1 (PJ8) not connected • Closed: User_LED_1 (PJ8) connected to LED (LD21)	Closed	B4(1)
JP40C	User_LED_2 (PJ9) configuration: • Open: User_LED_2 (PJ9) not connected • Closed: User_LED_2 (PJ9) connected to LED (LD22)	Closed	B4(1)
JP40D	User_LED_3 (PJ10) configuration: • Open: User_LED_3 (PJ10) not connected • Closed: User_LED_3 (PJ10) connected to LED (LD23)	Closed	B4(1)
JP40E	User_LED_4 (PJ12) configuration: • Open: User_LED_4 (PJ12) not connected • Closed: User_LED_4 (PJ12) connected to LED (LD24)	Closed	B4(1)
JP40F	User_LED_5 (PJ13) configuration: • Open: User_LED_5 (PJ13) not connected • Closed: User_LED_5 (PJ13) connected to LED (LD25)	Closed	B4(1)
JP40G	User_LED_6 (PJ3) configuration: • Open: User_LED_5 (PJ3) not connected • Closed: User_LED_5 (PJ3) connected to LED (LD26)	Closed	B4(1)
JP40H	User_LED_7 (PF6) configuration: • Open: User_LED_5 (PF6) not connected • Closed: User_LED_5 (PF6) connected to LED (LD27)	Closed	B4(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

The following table shows the user area LEDs:

Table 30. User area LEDs

LED	Description	Position
LED20	User LED 0 connected to JP40A	B4(1)
LED21	User LED 1 connected to JP40B	B4(1)
LED22	User LED 2 connected to JP40C	B4(1)
LED23	User LED 3 connected to JP40D	B4(1)
LED24	User LED 4 connected to JP40E	B4(1)
LED25	User LED 5 connected to JP40F	B4(1)
LED26	User LED 6 connected to JP40G	B4(1)
LED27	User LED 7 connected to JP40H	B4(1)

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

6.13 Test points

Several test points of different shape and functionality are scattered around the SR6G7-EVBC4000P rev. A evaluation board to allow easy access to MCU and reference signals. This chapter summarizes and describes the available test points. Test points are listed and detailed in the following table.

Table 31. Test point

Test point	Description	Position
TP1	VDD_HV_ADx	B3(1)
TP2	VDD_HV_IO_MAIN	B2(1)
TP3	VDD_HV_NVM_PRG	C2(1)
TP4	VDD_LV_LP	B2(1)
TP5	VDD_LV	B2(1)
TP6	3V3_ADC	B4(1)
TP7	VDD_LV_IN	B2(1)
TP8	EXTREG_SEL	B3(1)
TP9	V_CVM	C3(1)
TP10	TESTMODE	C2(1)
TP11	V_Osc	C3(1)
TP12	RESET_A	C2(1)
TP13	RESET_B	C2(1)
TP14	3V3_USB	A1(1)
TP15	CAN_0_L	A1(1)
TP16	CAN_0_H	A1(1)
TP17	GND	A1(1)
TP18	CAN_1_L	A1(1)
TP19	CAN_1_H	A1(1)
TP20	GND	A1(1)
TP21	CAN_2_L	C4(1)
TP22	CAN_2_H	C4(1)
TP23	CAN_3_L	C4(1)
TP24	CAN_3_H	C4(1)
TP25	GND	A4(1)
TP26	5V_Ext	B4(1)
TP27	3V3_Ext	B4(1)
TP28	MCU Pin E14	B2(1)
TP29	MCU Pin D15	B2(1)
TP30	MCU Pin D14	B2(1)
TP35	VBat_LIN_A	A3(1)
TP36	VBat_LIN_B	A2(1)
TP37	FlexRay_0_BM	A1(1)
TP38	FlexRay_0_BP	A1(1)

Test point	Description	Position
TP39	GND	A1[1]
TP40	FlexRay_1_BP	A2[1]
TP41	FlexRay_1_BM	A2[1]
TP42	GND	A2[1]
TP49	VDD_Flex_0	A1[1]
TP50	VDD_Flex_1	B1[1]
TP53	ETH0_INT_N	B1[1]
TP54	AVDDH_0	B1[1]
TP55	DVDDH_0	B1[1]
TP56	AVDDL_0	B1[1]
TP57	AVDDL_0_PLL	B1[1]
TP58	DVDDL_0	B1[1]
TP59	GND	B1[1]
TP100	Vbatt	A4[1]
TP101	12 V	A4[1]
TP105	5 V	A4[1]

1. *Refer to the Figure 19. SR6G7-EVBC4000P rev. A - top.*

7 Layout overview

Figure 19. **SR6G7-EVBC4000P rev. A - top**

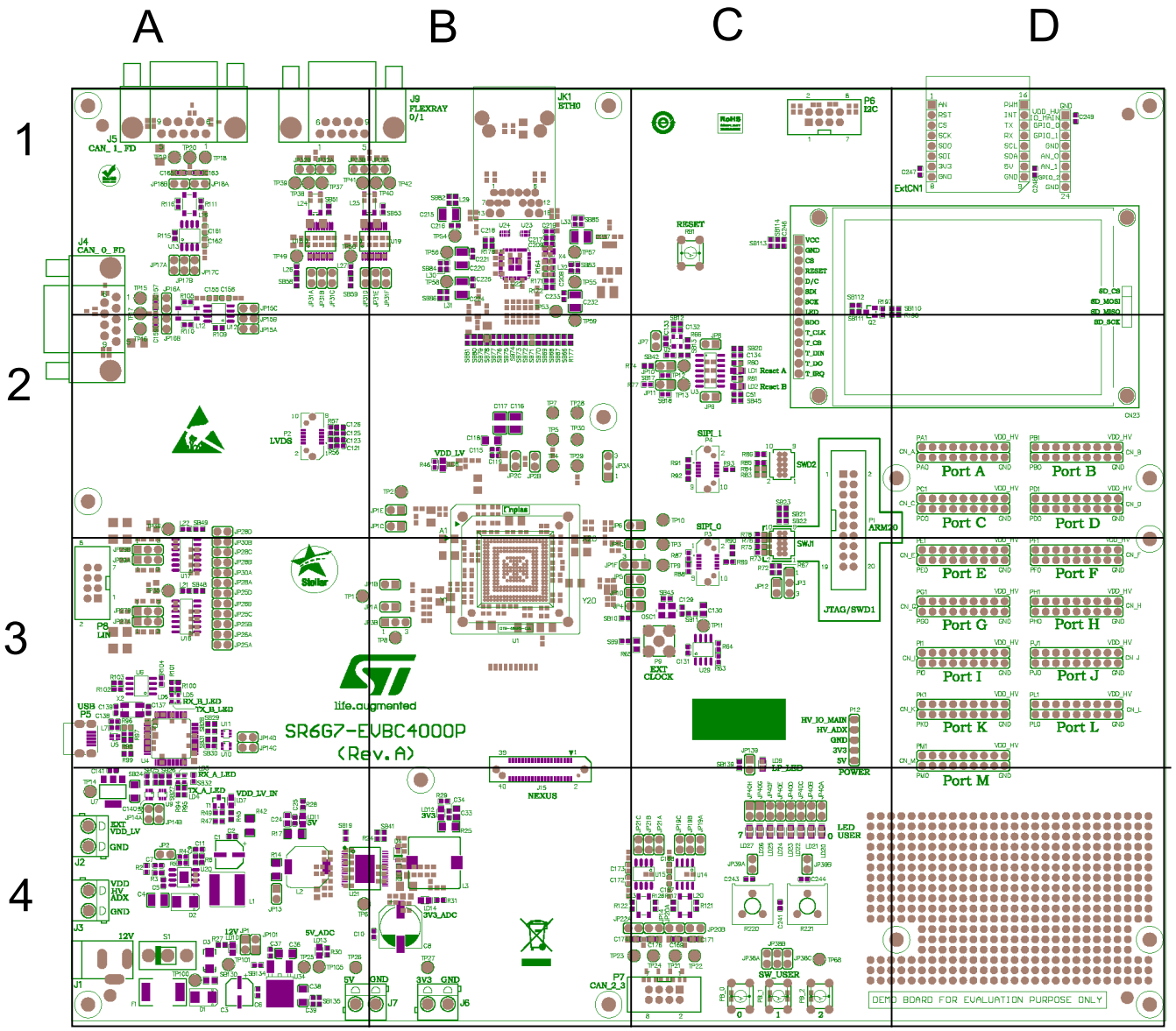
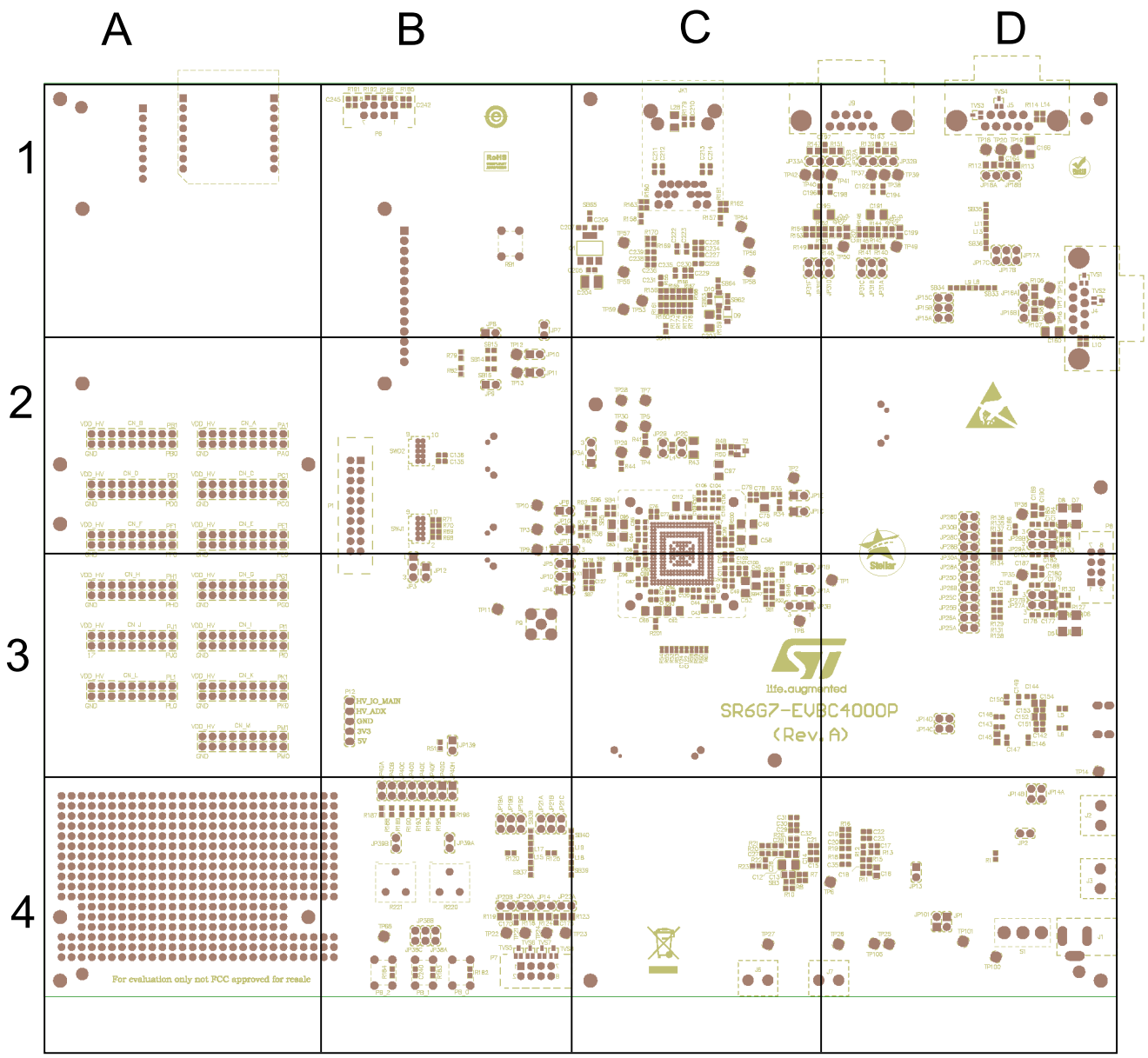


Figure 20. **SR6G7-EVBC4000P rev. A - bottom**



8 BOM

Table 32. **BOM**

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
1	C1	1	2BCAPELECSG00060	330 µF	EL-CAP-SMD-CASE-C6		SMD electrolytic capacitor
2	C2, C6, C10, C14, C19, C20, C25, C29, C30, C34, C37, C39, C51, C121, C123, C125, C126, C129, C131, C132, C133, C134, C138, C141, C142, C143, C144, C146, C147, C148, C149, C150, C151, C153, C155, C156, C161, C162, C167, C168, C172, C173, C181, C186, C188, C190, C200, C202, C205, C206, C210, C211, C212, C213, C214, C216, C217, C218, C219, C221, C222, C223, C225, C226, C227, C228, C229, C230, C231, C233, C234, C235, C236, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249	85	CAP_SMD_X7R	100 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
3	C3	1	2BCAPELECSG00060	47 µF	EL-CAP-SMD-CASE-D		SMD electrolytic capacitor
4	C4, C204, C215, C220, C224, C232, C237	7	CAP_SMD_X7R	47 µF	CAP-1210		SMD multilayer ceramic capacitor
5	C5	1	CAP_SMD_X7R	220 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
6	C7	1	CAP_SMD_X7R	15 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
7	C8	1	2BCAPELECSF00037	220 µF	EL-CAP-SMD-10X10.5		SMD electrolytic capacitor

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
8	C9	1	CAP_SMD_X7R	1.2 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
9	C11	1	CAP_SMD_X7R	68 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
10	C12, C36, C38, C140, C191, C195, C203	7	CAP_SMD_X7R	10 µF	CAP-1206		SMD multilayer ceramic capacitor automotive
11	C13	1	CAP_SMD_X7R	3.3 µF	CAP-0805-SMALL		SMD multilayer ceramic capacitor
12	C15, C21, C35	3	CAP_SMD_X7R	3.9 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
13	C16, C26	2	CAP_SMD_X7R	13 nF	CAP-0805-SMALL		SMD multilayer ceramic capacitor automotive
14	C17	1	CAP_SMD_X7R	1.3 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
15	C18	1	CAP_SMD_X7R	13 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
16	C22, C31	2	CAP_SMD_X7R	47 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
17	C23, C32, C178, C180, C183, C185	6	CAP_SMD_X7R	220 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
18	C24	1	CAP_SMD_X7R	2.2 µF	CAP-0805-SMALL		SMD multilayer ceramic capacitor automotive
19	C27	1	CAP_SMD_X7R	1.6 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
20	C28	1	CAP_SMD_X7R	43 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
21	C33, C145, C152, C154	4	CAP_SMD_X7R	4.7 µF	CAP-0805-SMALL		SMD multilayer ceramic capacitor automotive
22	C40, C43, C46, C52, C58, C63, C66, C75, C92, C95, C96, C97, C118	13	CAP_SMD_X7R	10 µF	CAP-1206-S		SMD multilayer ceramic capacitor
23	C41, C44	2	CAP_SMD_X7R	47 nF	CAP-0603-XS		SMD multilayer ceramic capacitor automotive
24	C42, C45, C48, C50, C60, C65, C68, C70, C77, C79, C85, C87, C94, C99, C101, C103, C105, C107, C109, C111, C114	21	CAP_SMD_X7R	10 nF	CAP-0603-XS		SMD multilayer ceramic capacitor automotive

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
25	C47, C49, C59, C64, C67, C69, C76, C78, C84, C86, C93, C98, C100, C102, C104, C106, C108, C110, C113, C115, C120	21	CAP_SMD_X7R	100 nF	CAP-0603-XS		SMD multilayer ceramic capacitor automotive
26	C112	1	CAP_SMD_X7R	2.2 µF	CAP-1206-S		SMD multilayer ceramic capacitor
27	C116, C117	2	CAP_SMD_X7R	22 µF	CAP-1210		SMD multilayer ceramic capacitor
28	C119	1	CAP_SMD_X7R	1 nF	CAP-0603-XS		SMD multilayer ceramic capacitor automotive
29	C122, C124	2	CAP_SMD_X7R	100 nF	CAP-0402-SMALL		SMD multilayer ceramic capacitor automotive
30	C127, C128	2	CAP_SMD_X7R	8 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
31	C130, C187, C189, C199, C201	5	CAP_SMD_X7R	1 uF	CAP-0805-SMALL		SMD multilayer ceramic capacitor automotive
32	C135, C136	2	CAP_SMD_X7R	47 pF	CAP-0603-SMALL	DNP	SMD multilayer ceramic capacitor
33	C137, C139	2	CAP_SMD_X7R	18 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
34	C157, C159, C163, C165, C169, C171, C174, C176	8	CAP_SMD_X7R	47 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
35	C158, C164, C170, C175, C193, C197	6	CAP_SMD_X7R	4.7 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
36	C160, C166	2	CAP_SMD_X7R	1 nF	CAP-1206	DNP	SMD multilayer ceramic capacitor
37	C177, C179, C182, C184	4	CAP_SMD_X7R	1 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
38	C192, C194, C196, C198, C208, C209	6	CAP_SMD_X7R	10 pF	CAP-0603-SMALL		SMD multilayer ceramic capacitor
39	C207	1	CAP_SMD_X7R	10 nF	CAP-0603-SMALL		SMD multilayer ceramic capacitor automotive
40	CN23	1	TFT Port	TFT - ILI9341	TFT-ILI9341		Female strip MULTICOMP, Single row, vertical
41	CN J	1	CONN_HDR_9X2	Port J	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
42	CN_A	1	CONN_HDR_9X2	Port A	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
43	CN_B	1	CONN_HDR_9X2	Port B	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
44	CN_C	1	CONN_HDR_9X2	Port C	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
45	CN_D	1	CONN_HDR_9X2	Port D	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
46	CN_E	1	CONN_HDR_9X2	Port E	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
47	CN_F	1	CONN_HDR_9X2	Port F	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
48	CN_G	1	CONN_HDR_9X2	Port G	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
49	CN_H	1	CONN_HDR_9X2	Port H	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
50	CN_I	1	CONN_HDR_9X2	Port I	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
51	CN_K	1	CONN_HDR_9X2	Port K	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
52	CN_L	1	CONN_HDR_9X2	Port L	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
53	CN_M	1	CONN_HDR_9X2	Port M	STRIP-9X2-M-V		Male strip 9x2 poles straight gold plated
54	D1	1	D Schottky	STPS340U	SMB_D		Schottky diode
55	D2	1	D Schottky	STPS2L25U	SMB_D		25 V, 2 A low drop power Schottky rectifier
56	D3	1	D Schottky	SMAJ24A	SMA	DNP	Schottky diode
57	D4	1	D Zener	MMSZ4684T1G	SOD-123		Zener diode
58	D5, D6, D7, D8	4	CMP-02540-000008-1	GF1A	SMA		SMD rectifier
59	D9	1	Diode	1N4148W	SOD-123		SMD rectifier
60	D10	1	Diode	1N4148W	SOD-123	DNP	SMD rectifier
61	ExtCN1	1	ExtenalModulePort	External Module Port	MIKROBUS-MODULE-EXTENDED		External module port
62	F1	1	Fuse 2	2A	SMD200F		Littlefuse SMD200F 2 polyswitch, SMD, 2A
63	FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8	8		Comment	FID-1MM-RND		
64	J1	1	COAX POWER	DC female (5.5/2.1mm)	PRESA_CC_2.1_FC68148		DC input
65	J2, J3, J6, J7	4	ARK_2	ARK_2	691101710002-WURTH		Screw connector terminal, single row, 5.00 pitch, 9 depth, 12.6 height, AWG 14-26, 16A
66	J4	1	2BCONNECTPG00211	CAN_ 0_TT_FD	DB9-HM		Connector DB9 male 90°
67	J5	1	2BCONNECTPG00211	DB9	DB9-HM		Connector DB9 male 90°
68	J9	1	2BCONNECTPG00211	FlexRay 0_1	DB9-HF		Connector DB9 female 90°

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
69	J15	1	NEXUS_2X20	NEXUS 2X20 pins	SAMTEC_ASP-130367-01		SAMTEC SMD connector ASP-130367-01
70	JK1	1	JK0-0136NL	JK0-0136NL	PULSE-JK0-0136NL		Connector MAGJACK 1 PORT 1000 BASE-T
71	JP1, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP139	11	Jumper 2.54	Open	STRIP-2-M-V	DNP	Male strip, single row, 2 poles, p = 2.54 mm
72	JP1A, JP1B, JP1C, JP1D, JP1E, JP1G, JP2B, JP2C, JP13, JP14, JP14A, JP14B, JP14C, JP14D, JP15B, JP15C, JP16A, JP16B, JP17B, JP17C, JP18A, JP18B, JP19B, JP19C, JP20A, JP20B, JP21B, JP21C, JP22A, JP25A, JP25B, JP25C, JP25D, JP26A, JP26B, JP28A, JP28B, JP28C, JP28D, JP30A, JP30B, JP31A, JP31B, JP31C, JP31D, JP31E, JP31F, JP32A, JP32B, JP33A, JP33B, JP38A, JP38B, JP38C, JP39A, JP39B, JP40A, JP40B, JP40C, JP40D, JP40E, JP40F, JP40G, JP40H, JP101	65	Jumper 2.54	Closed	STRIP-2-M-V		Male strip, single row, 2 poles, p = 2.54 mm
73	JP1F	1	Jumper 3x2.54	VDD_HV_INVM_PRG_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
74	JP2, JP15A, JP17A, JP19A, JP21A	5	Jumper 2.54	Open	STRIP-2-M-V		Male strip, single row, 2 poles, p = 2.54 mm
75	JP3	1	Jumper 3x2.54	JCOMP_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
76	JP3A	1	Jumper 3x2.54	D16_E15 Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
77	JP3B	1	Jumper 3x2.54	EXTREG_SEL_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
78	JP27A	1	Jumper 3x2.54	LIN0_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
79	JP27B	1	Jumper 3x2.54	LIN1_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
80	JP29A	1	Jumper 3x2.54	LIN2_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
81	JP29B	1	Jumper 3x2.54	LIN3_Config	STRIP-3-M-V		3xmale pin - 0.1" - Default 1-2
82	L1	1	2BINDCOILSF00117	4.7 µH	WURTH_74404084047_8X8-SIZE-8040		SMD automotive grade semi-shielded power inductor
83	L2	1	2BINDCOILSF00293	33 µH	COILCRAFT-MSS1048T		SMD high temperature power inductors - automotive
84	L3	1	2BINDCOILSF00276	22 µH	TDK_SLF12555		SMD inductors for power circuits wound ferrite
85	L4, L5, L6, L7, L8, L9, L11, L13, L15, L17, L18, L19, L21, L22, L26, L27, L29, L30, L31, L32, L33	21	Inductor	60 Ω at 100 MHz	0603-BEAD		SMD multilayer ferrite
86	L10, L14	2	Inductor	60 Ω at 100 MHz	0603-BEAD	DNP	SMD multilayer ferrite
87	L12, L16, L20, L23	4	ACT1210	ACT45B-510-2P	ACT45B_TDK_IND		SMD common mode inductor
88	L24, L25	2	Trans Ideal	ComMode Coil	MURATA-DLW43SH101		SMD inductor
89	L28	1	Inductor	HI1206N101R-10	1206-BEAD		SMD multilayer ferrite
90	LD1	1	LED2	Reset A	LED_SMD_0805_RED		SMD LED diode red - standard bright
91	LD2	1	LED2	Reset B	LED_SMD_0805_RED		SMD LED diode red - standard bright
92	LD3	1	LED2	RX_A_LED	LED_SMD_0603_ORANGE		SMD Micro LED®
93	LD4	1	LED2	TX_A_LED	LED_SMD_0603_ORANGE		SMD Micro LED®
94	LD5	1	LED2	RX_B_LED	LED_SMD_0603_ORANGE		SMD Micro LED®
95	LD6	1	LED2	TX_B_LED	LED_SMD_0603_ORANGE		SMD Micro LED®
96	LD7	1	LED2	VDD_LV_IN	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
97	LD8	1	LED2	VDD_LV	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
98	LD9	1	LED2	LP_LED	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
99	LD10	1	LED2	12V	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
100	LD11	1	LED2	5V	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
101	LD12	1	LED2	3V3	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
102	LD13	1	LED2	5V_ADC	LED_SMD_0805_GREEN		SMD LED diode green - standard bright

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
103	LD14	1	LED2	3V3_ADC	LED_SMD_0805_GREEN		SMD LED diode green - standard bright
104	LD20	1	LED2	User_0	LED_SMD_0805_AMBER		SMD LED diode amber
105	LD21	1	LED2	User_1	LED_SMD_0805_AMBER		SMD LED diode amber
106	LD22	1	LED2	User_2	LED_SMD_0805_AMBER		SMD LED diode amber
107	LD23	1	LED2	User_3	LED_SMD_0805_AMBER		SMD LED diode amber
108	LD24	1	LED2	User_4	LED_SMD_0805_AMBER		SMD LED diode amber
109	LD25	1	LED2	User_5	LED_SMD_0805_AMBER		SMD LED diode amber
110	LD26	1	LED2	User_6	LED_SMD_0805_AMBER		SMD LED diode amber
111	LD27	1	LED2	User_7	LED_SMD_0805_AMBER		SMD LED diode amber
112	LOGO, LOGO1	2		Comment	ROHS_LOGO-CHINA-COMPLIANT		
113	MTH4, MTH5, MTH6, MTH7, MTH8, MTH9, MTH10, MTH11, MTH12, MTH13, MTH14, MTH15, MTH16, MTH17	14		MTHOLE3.2	MTHOLE3.2-NYLON		
114	OSC1	1	50 MHz	8 MHz	QUARZO-SMD-KC5032A		SMD CMOS quartz oscillator
115	P1	1	Header 10X2	ARM20	CN-FLAT-20-V		Connector flat male 20 pins, straight low profile
116	P2	1	Header 6X2	LVDS	SAMTEC_ERF8-005-05.0-L-DV-L-TR		SAMTEC SMD Connector ERF8-005-05.0-L-DV-L-TR
117	P3, P4	2	Header 6X2	SIPI	SAMTEC_ERF8-005-05.0-L-DV-L-TR		SAMTEC SMD Connector ERF8-005-05.0-L-DV-L-TR
118	P5	1	USB_Port	USB_Port	CONN_MOLEX_51387-0578		MOLEX Connector SMT, right angle, USB MINI-B, 5pin
119	P6	1	Header 4X2	I^2C	CN-FLAT-8-V		Connector flat male 8 pins, straight
120	P7	1	Header 4X2	CAN_2_3	CN-FLAT-8-V		Connector flat male 8 pins, straight
121	P8	1	Header 4X2	LIN	CN-FLAT-8-V		Connector flat male 8 pins, straight
122	P9	1	2BCONCOAXPG00008	SMA	CON-COAX-SMA-V		Female RF SMA 180°
123	P12	1	CON5	Power	STRIP-5-M-V		Male strip 5 pins pitch 2.54 180° - Cut as necessary

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
124	PB_0	1	SW PUSHBUTTON	SW_User_0	ALPS-SKHHAJA010		Pushbutton for pcb 4 pins
125	PB_1	1	SW PUSHBUTTON	SW_User_1	ALPS-SKHHAJA010		Pushbutton for pcb 4 pins
126	PB_2	1	SW PUSHBUTTON	SW_User_2	ALPS-SKHHAJA010		Pushbutton for pcb 4 pins
127	Q1	1	MOSFET-P	NTF6P02T3G	SOT223_GDS_T		SMD P-channel Power MOSFET
128	Q2	1	PNP BCX52-16	BCW68G	SOT23_BEC_T		SMD PNP general purpose transistor
129	R1, R10, R32, R33, R34, R35, R37, R40, R44, R72, R73, R75, R76, R78, R83, R84, R85, R89, R93, R105, R108, R110, R111, R114, R116, R117, R121, R122, R126, R164, R169, R178, R179	33	Resistor_SMD	0 Ω	RES-0603-SMALL		SMD resistor
130	R2	1	Resistor_SMD	300 Ω	RES-0603-SMALL		SMD resistor automotive
131	R3, R13, R22, R27	4	Resistor_SMD	5.1 kΩ	RES-0603-SMALL		SMD resistor
132	R4	1	Resistor_SMD	8.2 kΩ	RES-0603-SMALL		SMD resistor
133	R5	1	Resistor_SMD	180 kΩ	RES-0603-SMALL	DNP	SMD resistor
134	R6	1	Resistor_SMD	1.1 kΩ	RES-0603-SMALL		SMD resistor automotive
135	R7	1	Resistor_SMD	464 kΩ	RES-0603-SMALL		SMD resistor automotive
136	R8	1	Resistor_SMD	200 kΩ	RES-0603-SMALL		SMD resistor
137	R9, R12	2	Resistor_SMD	910 Ω	RES-0603-SMALL		SMD resistor
138	R11	1	Resistor_SMD	1.3 kΩ	RES-0603-SMALL		SMD resistor automotive
139	R14, R17, R25, R42	4	Resistor_SMD	0 Ω	RES-1206		SMD resistor automotive
140	R15	1	Resistor_SMD	1.27 kΩ	RES-0603-SMALL		SMD resistor automotive
141	R16, R24, R66, R74, R77, R102, R103, R172, R198	9	Resistor_SMD	4.7 kΩ	RES-0603-SMALL		SMD resistor
142	R18, R26, R97, R98	4	Resistor_SMD	10 Ω	RES-0603-SMALL		SMD resistor

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
143	R19, R67, R80, R81, R128, R129, R131, R132, R134, R135, R137, R138, R140, R141, R142, R146, R148, R149, R150, R154, R155, R157, R158, R159, R165, R166, R167, R168, R171, R182, R183, R184, R185, R186, R191, R192	36	Resistor_SMD	10 kΩ	RES-0603-SMALL		SMD resistor
144	R20	1	Resistor_SMD	1.6 kΩ	RES-0603-SMALL		SMD resistor
145	R21	1	Resistor_SMD	750 Ω	RES-0603-SMALL		SMD resistor automotive
146	R23, R104, R177	3	Resistor_SMD	2.2 kΩ	RES-0603-SMALL		SMD resistor
147	R28, R30, R45, R46	4	Resistor_SMD	1.5 kΩ	RES-0603-SMALL		SMD resistor
148	R29, R31, R51, R187, R188, R189, R190, R193, R194, R195, R196	11	Resistor_SMD	680 Ω	RES-0603-SMALL		SMD resistor
149	R36, R38, R41, R90, R145, R153, R199, R200, R201	9	Resistor_SMD	0 Ω	RES-0603-SMALL	DNP	SMD resistor
150	R39	1	Resistor_SMD	0 Ω	RES-0603-XS		SMD resistor
151	R43	1	Resistor_SMD	0 Ω	RES-1206		SMD resistor automotive
152	R47, R48, R127, R130, R133, R136, R161	7	Resistor_SMD	1 kΩ	RES-0603-SMALL		SMD resistor
153	R49, R50, R197	3	Resistor_SMD	100 kΩ	RES-0603-SMALL		SMD resistor
154	R52, R53, R54, R55, R58, R59, R60, R61	8	Resistor_SMD	50 Ω	RES-0402-SMALL		SMD high frequency (up to 40 GHz) resistor
155	R56, R57	2	Resistor_SMD	100 Ω	RES-0603-SMALL	DNP	SMD resistor
156	R62, R86	2	Resistor_SMD	10 kΩ	RES-0603-SMALL	DNP	SMD resistor
157	R63	1	Resistor_SMD	124 Ω	RES-0603-SMALL		SMD resistor automotive
158	R64	1	Resistor_SMD	240 Ω	RES-0603-SMALL		SMD resistor
159	R65	1	Resistor_SMD	50 Ω	RES-0805-SMALL		SMD resistor automotive
160	R68, R69, R70, R71	4	Resistor_SMD	100 kΩ	RES-0603-SMALL	DNP	SMD resistor
161	R79, R82	2	Resistor_SMD	470 Ω	RES-0603-SMALL		SMD resistor

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
162	R87, R88, R91, R92	4	Resistor_SMD		RES-0603-SMALL	DNP	SMD resistor
163	R94, R95, R100, R101, R180, R181	6	Resistor_SMD	220 Ω	RES-0603-SMALL		SMD resistor automotive
164	R96	1	Resistor_SMD	12 kΩ	RES-0603-SMALL		SMD resistor
165	R99	1	Resistor_SMD	15 kΩ	RES-0603-SMALL		SMD resistor
166	R106, R107, R112, R113, R118, R119, R123, R124	8	Resistor_SMD	60.4 Ω	RES-0805-SMALL		SMD resistor
167	R109, R115, R120, R125, R144, R152	6	Resistor_SMD	47 kΩ	RES-0603-SMALL		SMD resistor
168	R139, R143, R147, R151	4	Resistor_SMD	47 Ω	RES-0805-SMALL		SMD resistor
169	R156	1	Resistor_SMD	10 kΩ	RES-0603-SMALL	DNP	SMD resistor
170	R160, R162, R163, R173, R174, R175, R176	7	Resistor_SMD	1 kΩ	RES-0603-SMALL	DNP	SMD resistor
171	R170	1	Resistor_SMD	12.1 kΩ	RES-0603-SMALL		SMD resistor automotive
172	R220, R221	2	RPot	10 kΩ	TRIM-3386F		Potentiometer
173	RB1	1	SW PUSHBUTTON	RESET	DIPTRONICS-DTS-65R-V		Pushbutton for pcb 4 pins - RED - H = 9.5 mm
174	S1	1	SWITCH	DC switch	NKK-CS12ANW03		Slide switch 2 positions ON-ON
175	SB1, SB2, SB3, SB4, SB5, SB6, SB7, SB8, SB11, SB12, SB15, SB16, SB17, SB18, SB19, SB20, SB21, SB24, SB25, SB26, SB27, SB28, SB29, SB30, SB31, SB32, SB33, SB34, SB35, SB36, SB37, SB38, SB39, SB40, SB41, SB42, SB43, SB45, SB47, SB48, SB49, SB50, SB51, SB52, SB53, SB58, SB59, SB64, SB65, SB66, SB67, SB68, SB69, SB70, SB71, SB72, SB73, SB74, SB75, SB76, SB77, SB78, SB79,	76	Circuit Breaker_Closed	Closed	RES-0603-SMALL		Circuit Breaker

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
	SB80, SB81, SB82, SB83, SB84, SB85, SB86, SB110, SB111, SB114, SB134, SB135, SB139						
176	SB9, SB10, SB13, SB14, SB22, SB23, SB44, SB46, SB62, SB63, SB112, SB113	12	Circuit Breaker_Open	Open	RES-0603-SMALL	DNP	Circuit breaker
177	SB130	1	Circuit Breaker_Closed	Closed	RES-0805-SMALL	Closed	Circuit breaker
178	SWD2	1	Header 5X2	Secondary DAP	FTSH-105-01-XXX-D-K		Debug connector 5x2 1.27 mm
179	SWJ1	1	Header 5X2	Main DAP	FTSH-105-01-XXX-D-K		Debug connector 5x2 1.27 mm
180	T1, T2	2	NPN	BC848	SOT23_BEC_T		NPN bipolar transistor
181	TP1	1	Test point	VDD_HV_ADx_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
182	TP2	1	Test point	VDD_HV_IO_MAIN_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
183	TP3	1	Test point	VDD_HV_NVM_PRG_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
184	TP4	1	Test point	VDD_LV_LP	TEST-RING-3.1-RED		PCB ring test point - red (drill 1.32 mm)
185	TP5	1	Test point	VDD_LV_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
186	TP6	1	Test point	3V3_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
187	TP7	1	Test point	VDD_LV_IN_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
188	TP8	1	Test point	EXTREG_SEL_DNP	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
189	TP9	1	Test point	CVM_DNP	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
190	TP10	1	Test point	TESTMODE_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
191	TP11	1	Test point	V_Osc_DNP	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
192	TP12	1	Test point	RESET_A	TEST-RING-3.1-WHITE		PCB ring test point - White (drill 1.32 mm)
193	TP13	1	Test point	RESET_B	TEST-RING-3.1-WHITE		PCB ring test point - White (drill 1.32 mm)
194	TP14	1	Test point	3V3_USB	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
195	TP15	1	Test point	CAN_0_L	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
196	TP16	1	Test point	CAN_0_H	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
197	TP17, TP20, TP39, TP42, TP59, TP68	6	Test point	GND	TEST-RING-3.1-BLACK	DNP	PCB ring test point - black (drill 1.32 mm)
198	TP18	1	Test point	CAN_1_L	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
199	TP19	1	Test point	CAN_1_H	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
200	TP21	1	Test point	CAN_2_L	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
201	TP22	1	Test point	CAN_2_H	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
202	TP23	1	Test point	CAN_3_L	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
203	TP24	1	Test point	CAN_3_H	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
204	TP25	1	Test point	GND	TEST-RING-3.1-BLACK		PCB ring test point - black (drill 1.32 mm)
205	TP26	1	Test point	5V_Ext	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
206	TP27	1	Test point	3V3_Ext	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
207	TP28	1	Test point	E14	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
208	TP29	1	Test point	D15	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
209	TP30	1	Test point	D14	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
210	TP35	1	Test point	VBat_LIN_0	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
211	TP36	1	Test point	VBat_LIN_B	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
212	TP37	1	Test point	BM_0	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
213	TP38	1	Test point	BP_0	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
214	TP40	1	Test point	BM_1	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
215	TP41	1	Test point	BP_1	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
216	TP49	1	Test point	VDD_Flex_0	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
217	TP50	1	Test point	VDD_Flex_1	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
218	TP53	1	Test point	INT_N	TEST-RING-3.1-WHITE	DNP	PCB ring test point - White (drill 1.32 mm)
219	TP54	1	Test point	AVDDH	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
220	TP55	1	Test point	DVDDH	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
221	TP56	1	Test point	A_VDDL	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
222	TP57	1	Test point	AVDDL_PLL	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
223	TP58	1	Test point	DVDDL	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
224	TP100	1	Test point	Vbatt+	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
225	TP101	1	Test point	12V	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
226	TP105	1	Test point	5V	TEST-RING-3.1-RED	DNP	PCB ring test point - red (drill 1.32 mm)
227	TVS1, TVS2, TVS3, TVS4, TVS5, TVS6, TVS7, TVS8	8	2BDIOTRANSF00061	ESD PROTECTION	SOT323-D-A-AA-A		SMD automotive dual-line TVS in SOT323-3L for CAN bus
228	U1	1	SR6G7_BGA292_Rev A	SR6G7_BGA292	292FPBGA_OTB-292(484RS)-0.8-002-00-ENPLAS		Socket BGA292 Pitch 0.8 mm OTB-292(484RS)-0.8-002-00
229	U2	1	STM6315RDW13F	STM6315RDW13F	SOT-143		SMD Reset circuit
230	U3	1	CMP-0440-00032-3	SN74HC125DT	SO14NB		SMD Quadruple Bus BµFfer Gates With 3-State Outputs
231	U4	1	FTDI2232	FT2232HL	TQFP64L		IC FTDI SMD USB HS DUAL UART/ FIFO LQFP64
232	U5	1	USBLC6-2P6	USBLC6-2P6	SOT-666		USBLC6-2P6
233	U6	1	M93S46RMN6	M93S46-WMN6P	SO8NB		1K (x16) Serial Microwire Bus EEPROM With Block Protection
234	U7	1	LD1117S33TR	LD1117S33TR	SOT223_GOI_H_VR		Volt. Reg. Low Drop out Lin. 3.3V SOT223
235	U8, U9, U10, U11	4	SN74LVC1T45	SN74LVC1T45	SC70-6		IC SMD single-bit dual-supply bus transceiver SC-70-6
236	U12, U13, U14, U15	4	MCP2542WFD	MCP2542WFD	SO8NB		SMD CAN FD transceiver with wake-up pattern (WUP) option
237	U16, U17	2	TJA1022T	TJA1022T	SO14NB		SMD dual LIN 2.2A/SAE J2602 transceiver
238	U18, U19	2	TJA1080	TJA1080ATS	SSOP20		SMD FlexRay transceiver
239	U20	1	A7986A	A7986A	HSOP8		DC-DC switching buck (step down) regulator, adjustable, 3A, HSOP-8
240	U21	1	L5963DN	L5963DN	POWERSSO36		Automotive dual monolithic switching regulator with LDO and HSD

#	Item	Qty.	Reference	Value	Footprint	Ass. Opt.	Description
241	U22	1	KSZ9031RNX	KSZ9031RNX	48QFN_7X7X0.85_0.5_EXPAD_3.5X3.5		SMD Gigabit Ethernet Transceiver with RGMII Support
242	U23, U24	2	HSP061-4M10Y	HSP061-4M10Y	UQFN10		SMD automotive 4-line ESD protection for high speed lines
243	U29	1	LM217LD	LM217LD	SO8NB		SMD low current 1.2 to 37 V adjustable voltage regulators
244	U34	1	REG_FIX	LD1117DT50	TO252_GOI_H_VR		Voltage regulator low drop out linear TO-252
245	X1	1	Crystal 4pin	40 MHz	QUARZO-SMD-ECS-2236Q		SMD quartz ECS
246	X2	1	XTAL	12 MHZ	QUARZO-SMD-TXC-7B-SERIES		Crystal oscillator
247	X4	1	Crystal 4pin	25 MHz	QUARZO-SMD-ECS-33B		SMD ECX-33B SMD crystal automotive
248	C1	1	2BCAPELECSG00060	330 µF	EL-CAP-SMD-CASE-C6		SMD electrolytic capacitor

9 Schematics

Figure 21. **MAIN**

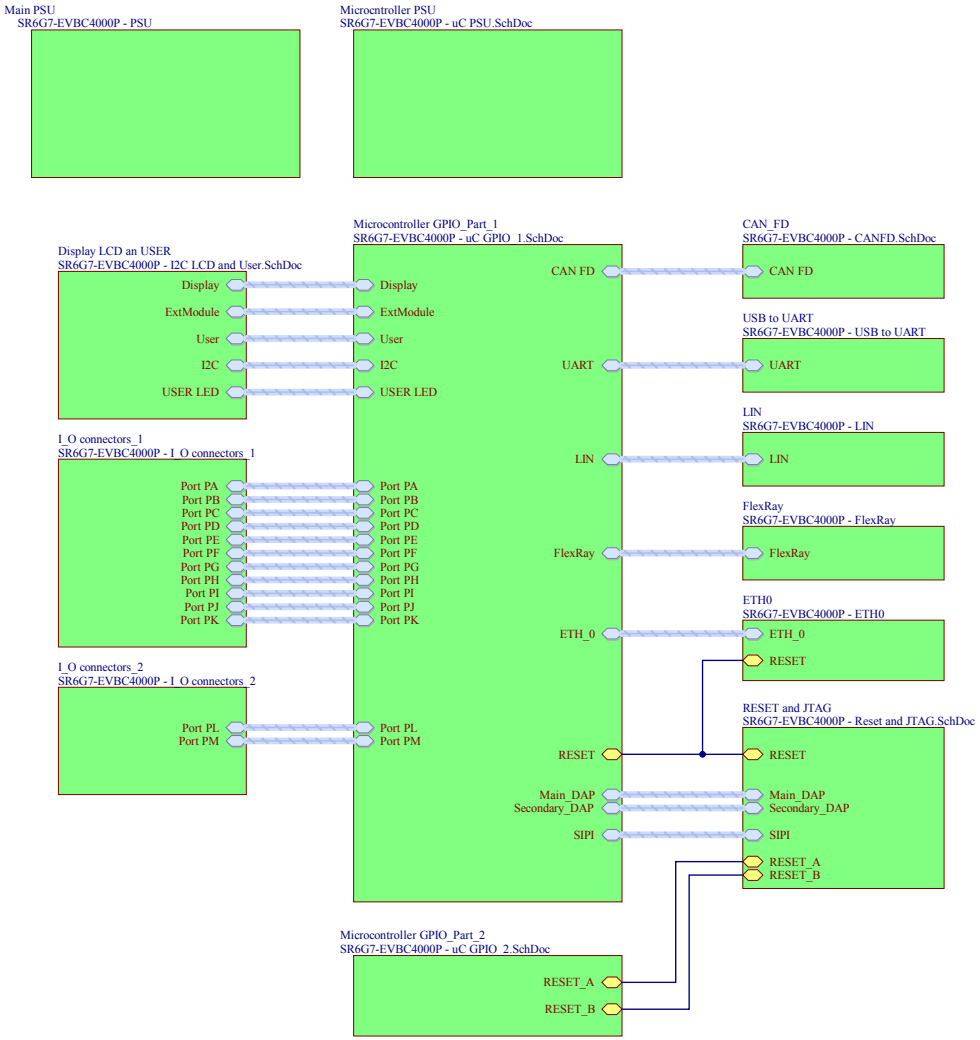


Figure 22. Power supply

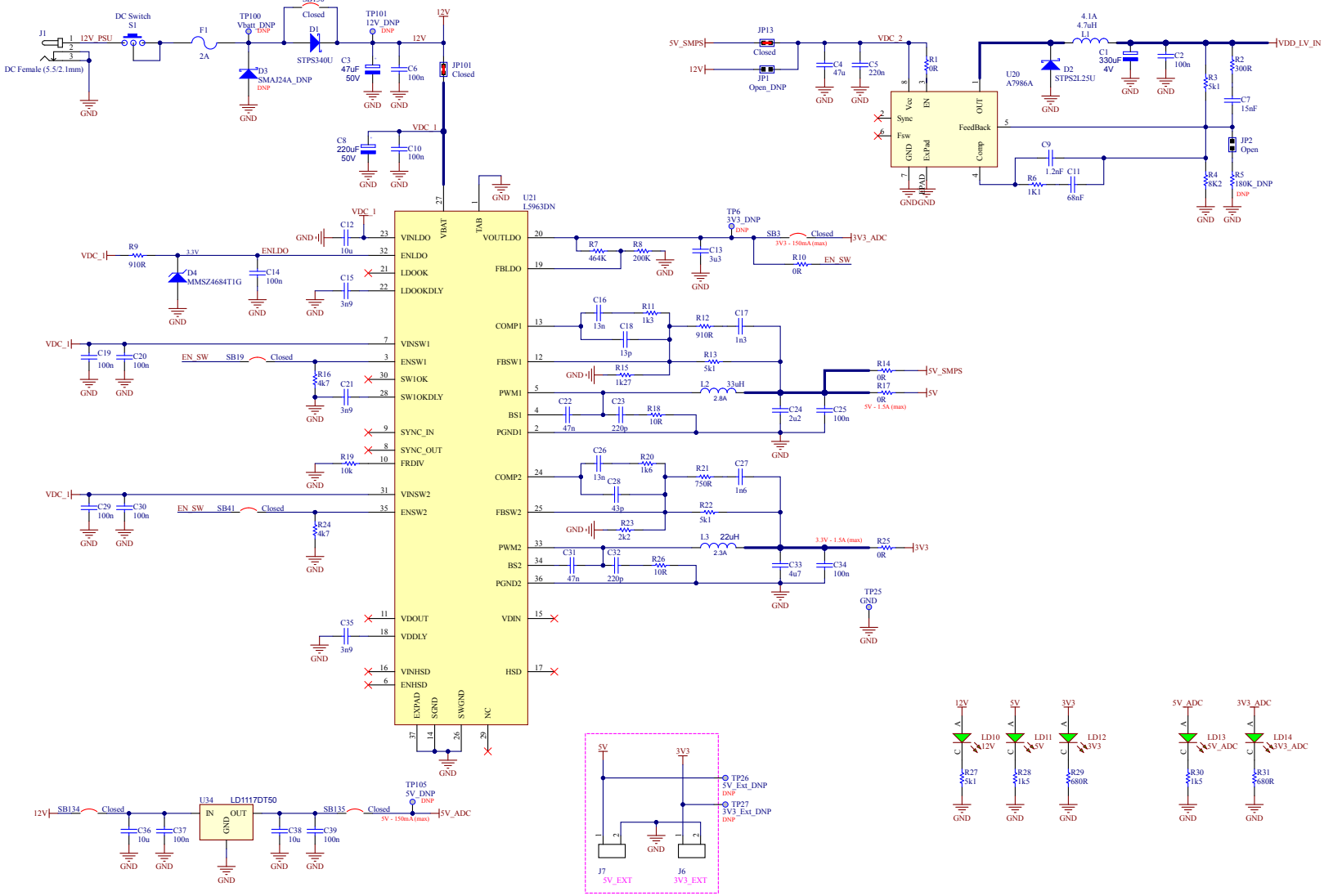


Figure 23. uC PSU

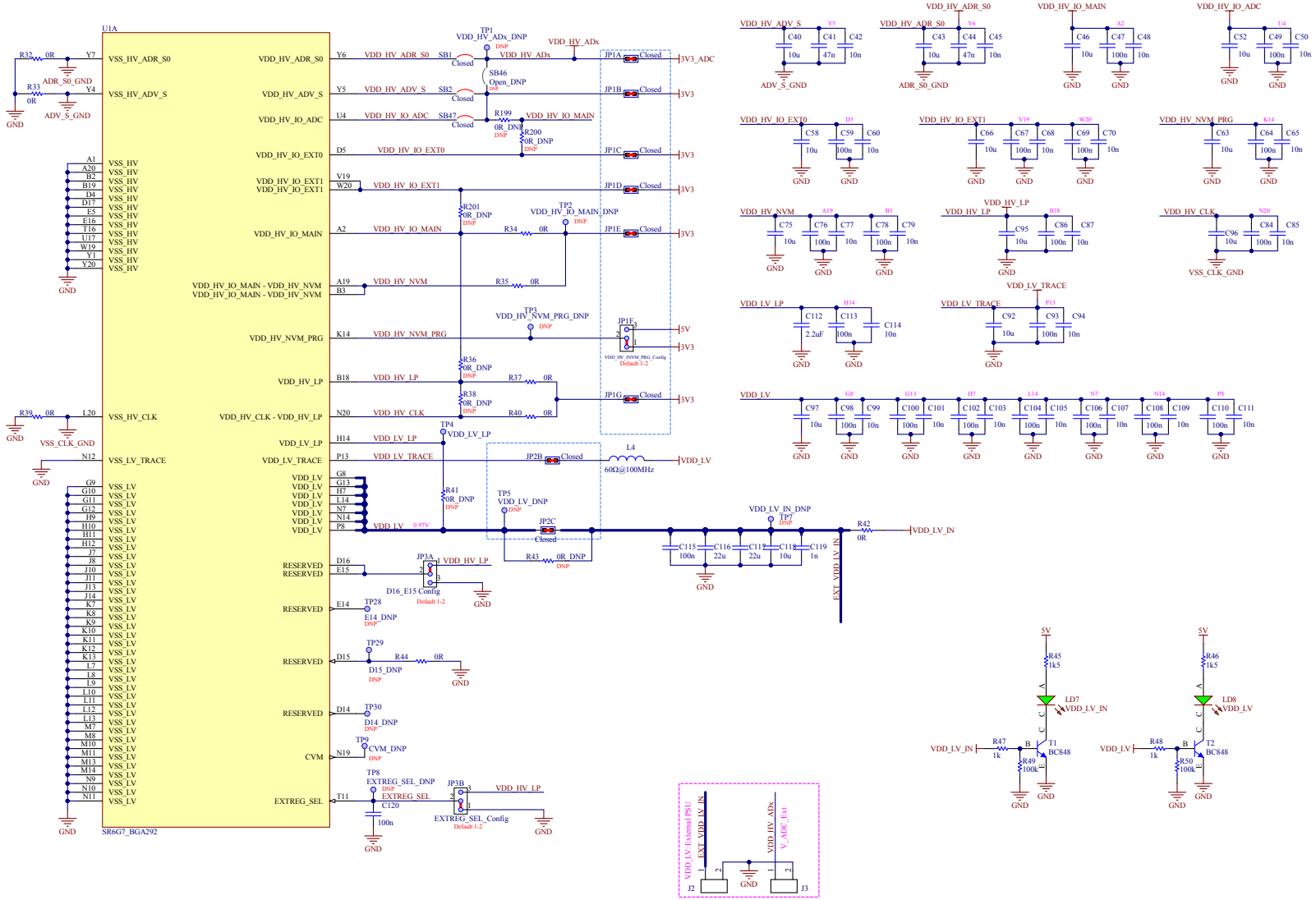


Figure 24. uC GPIO_1

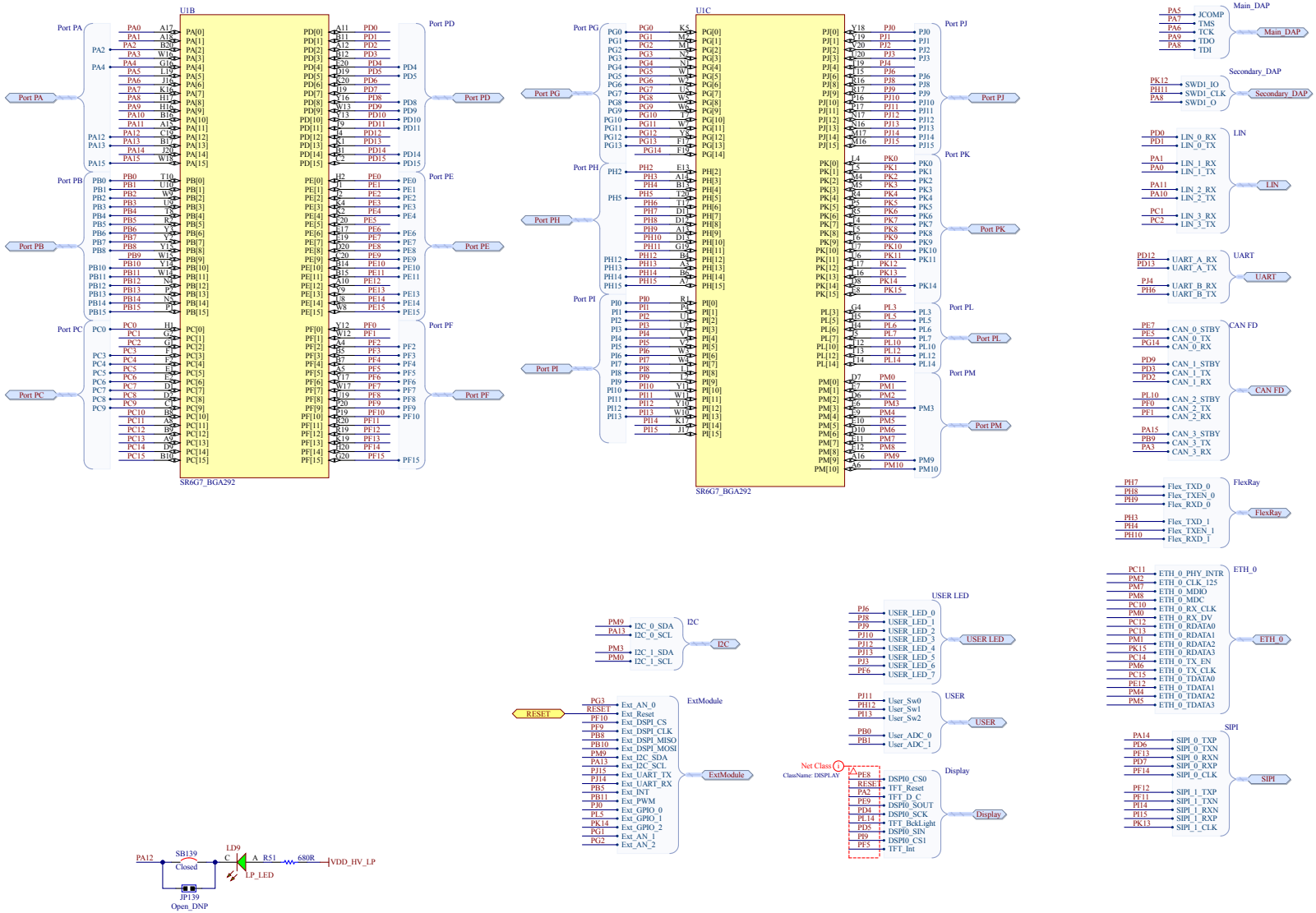


Figure 25. uC GPIO_2

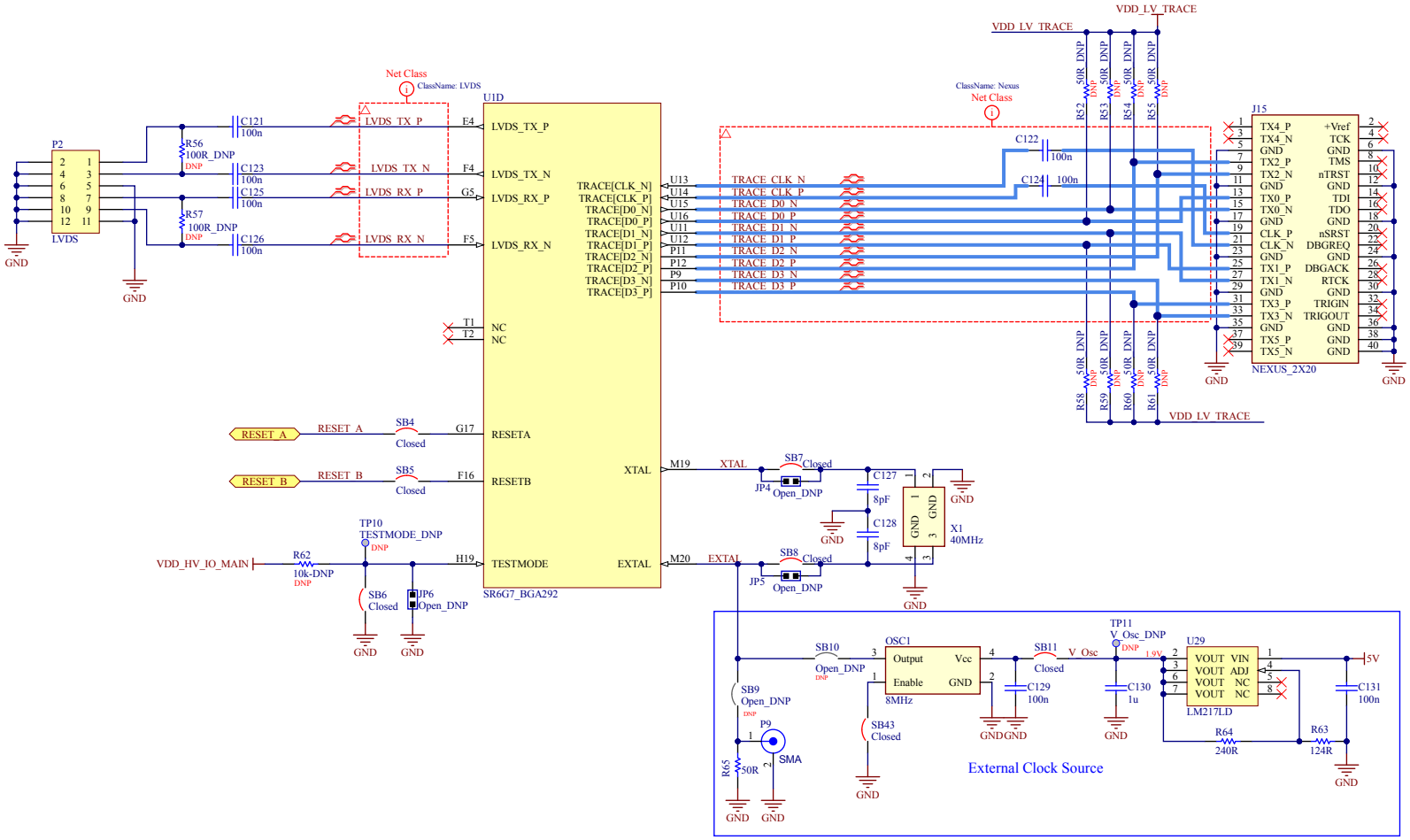
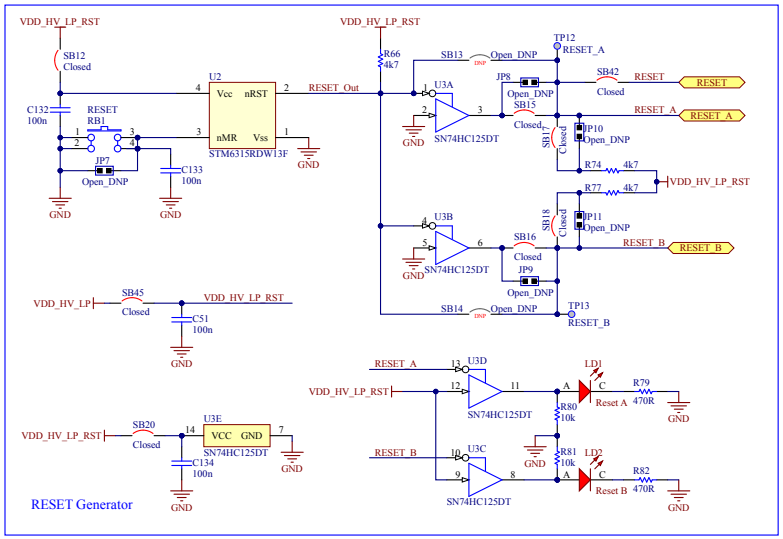
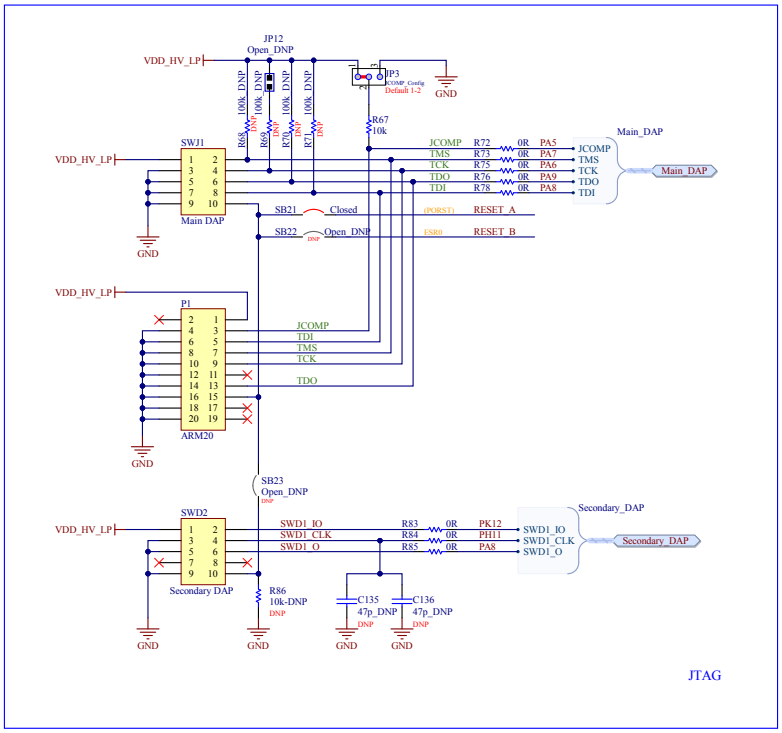


Figure 26. Reset and clock





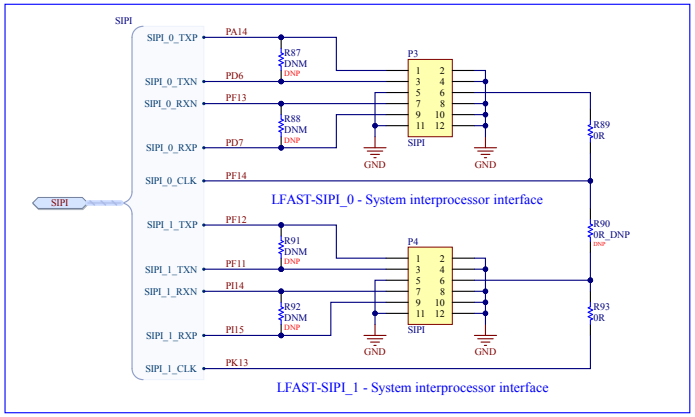


Figure 27. USB to UART

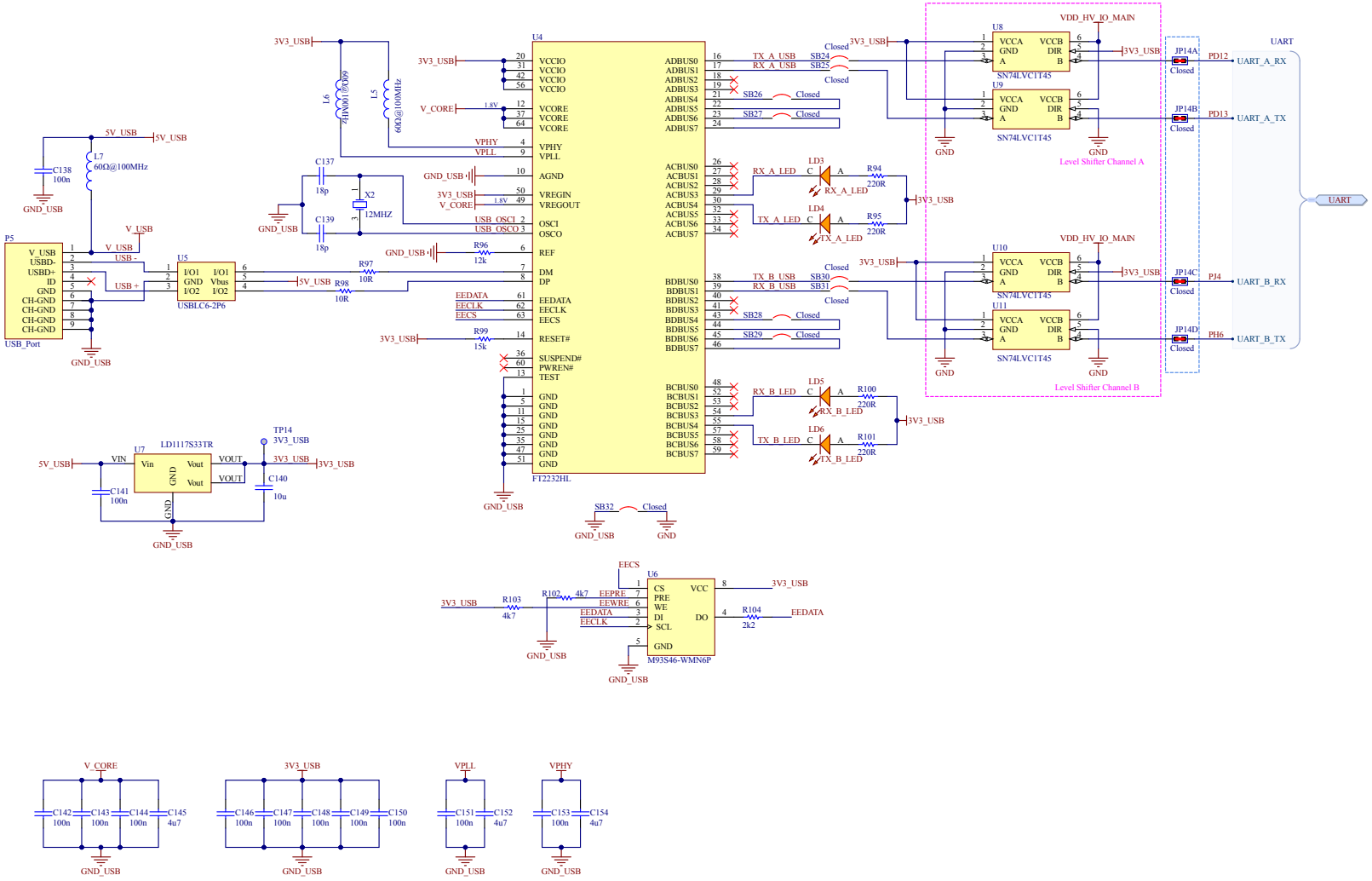


Figure 28. CANFD

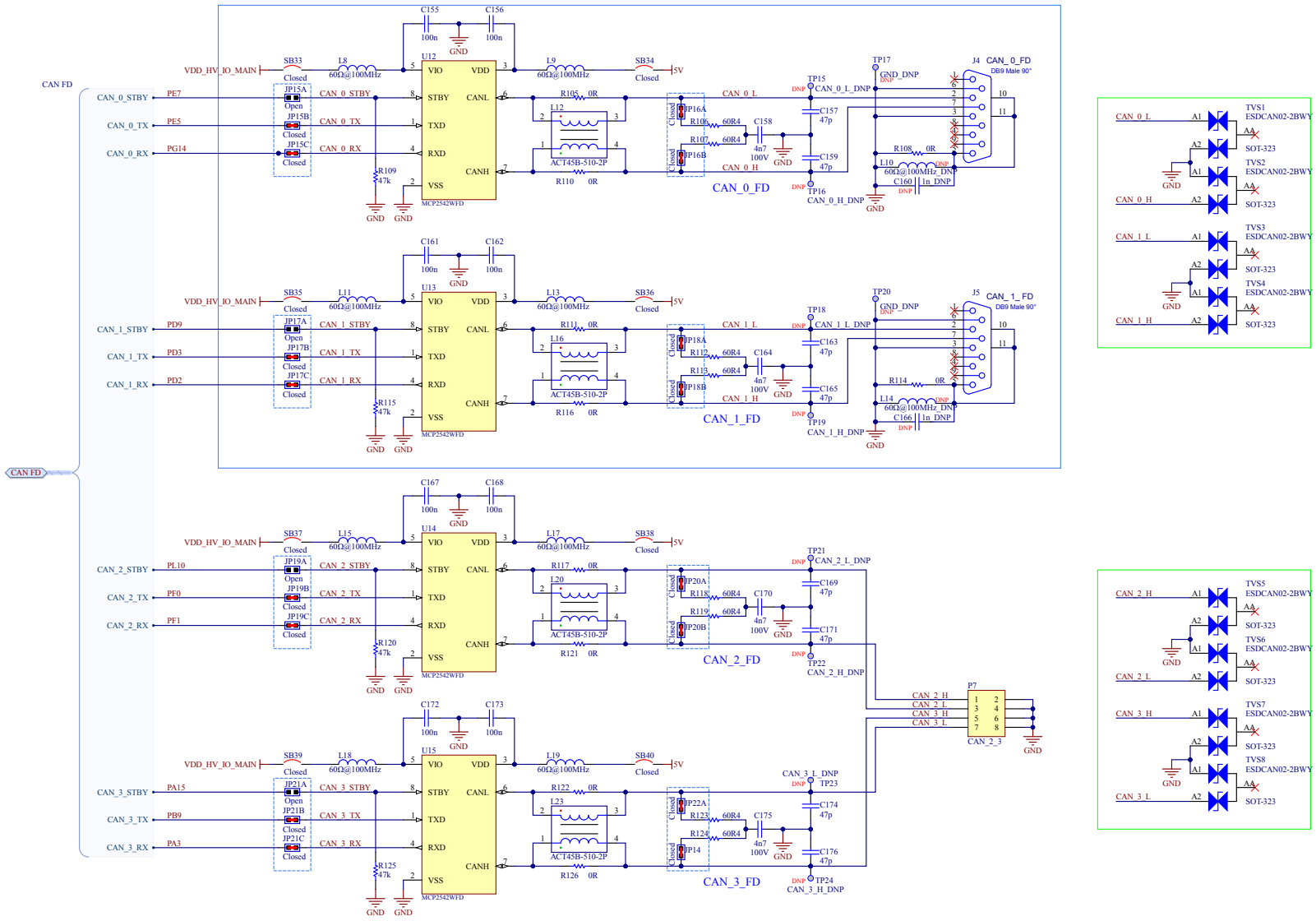


Figure 29. **LIN**

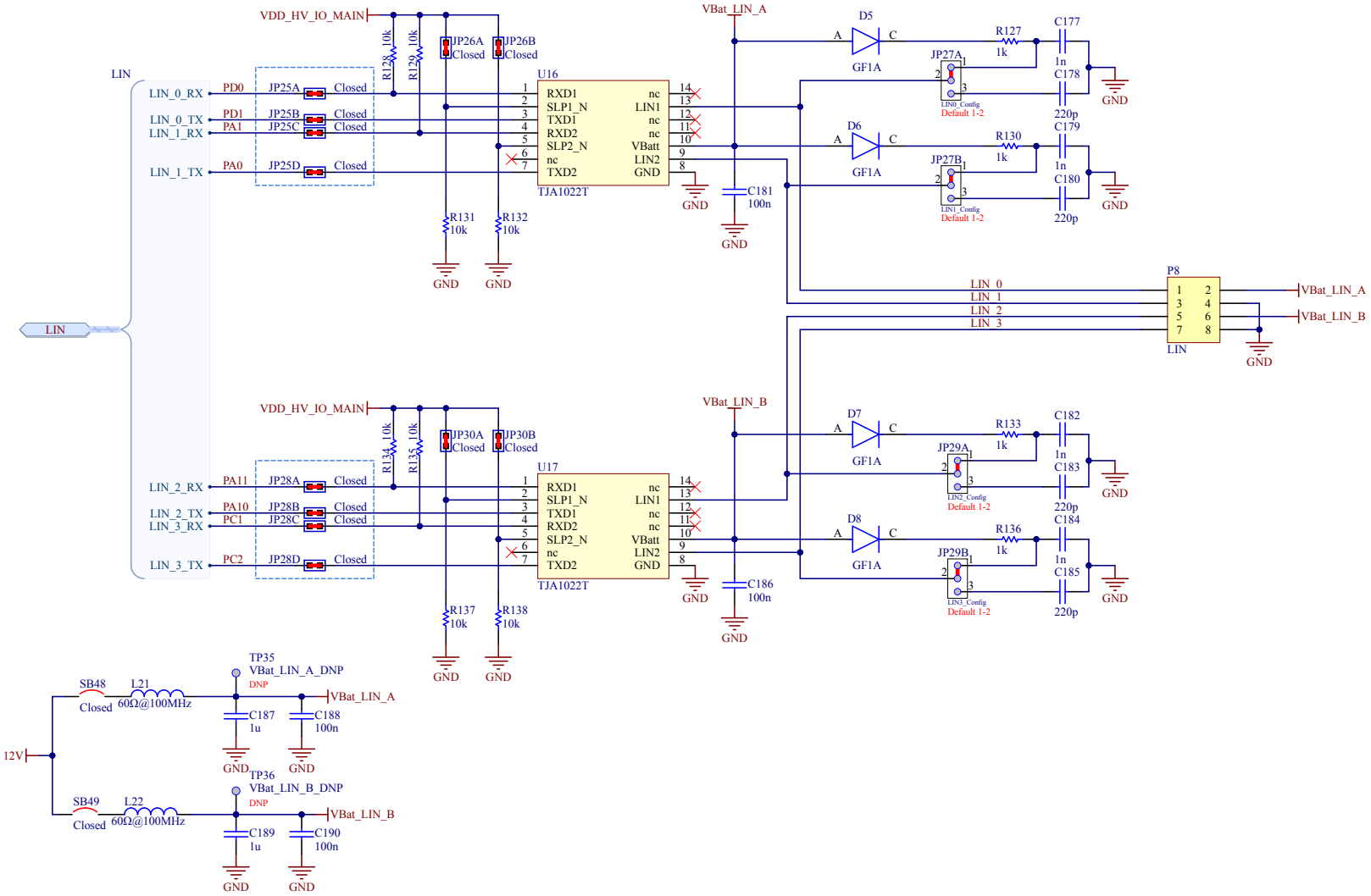


Figure 30. FlexRay

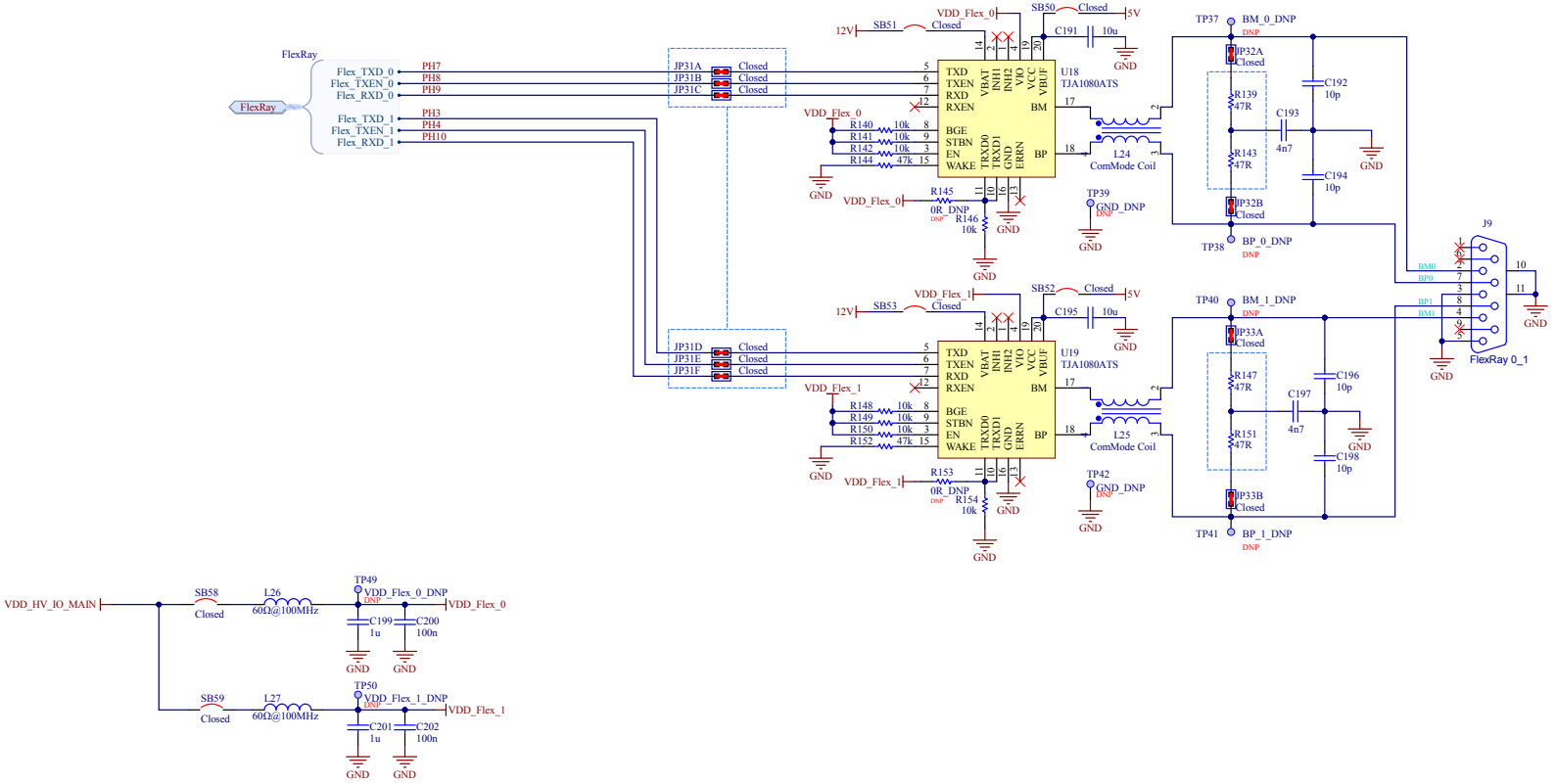


Figure 31. Ethernet 0

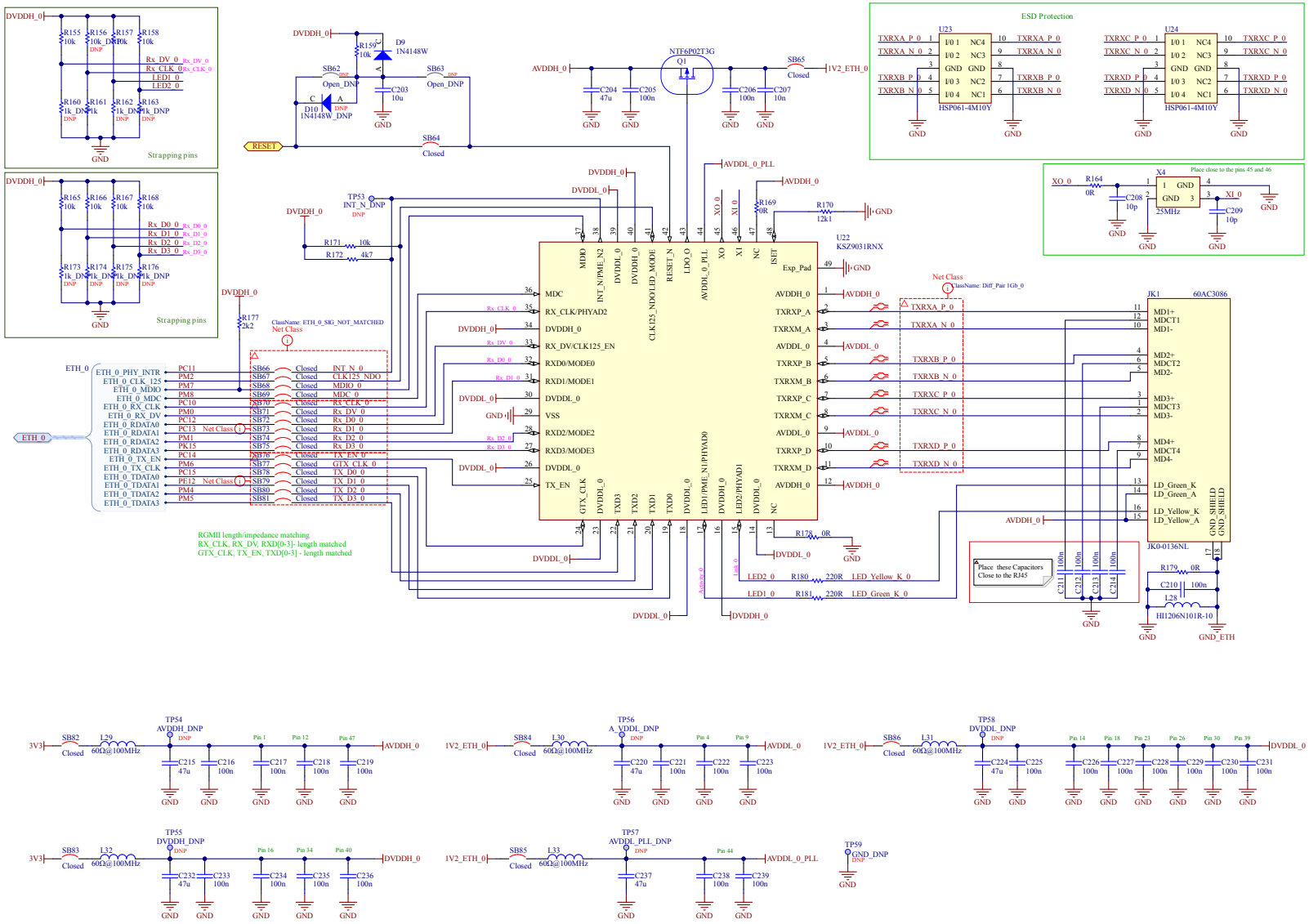


Figure 32. I²C user LCD

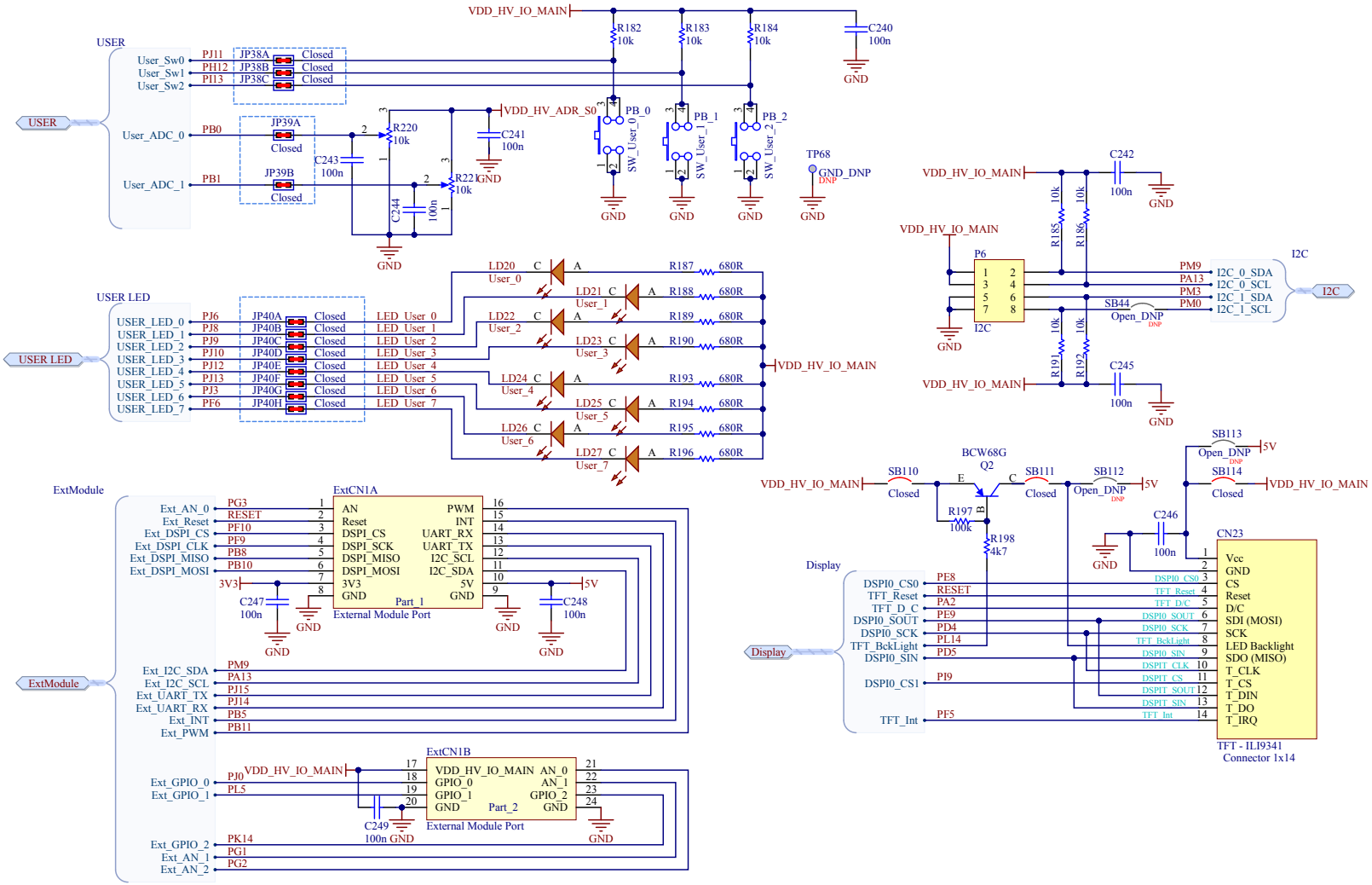


Figure 33. IO user_1

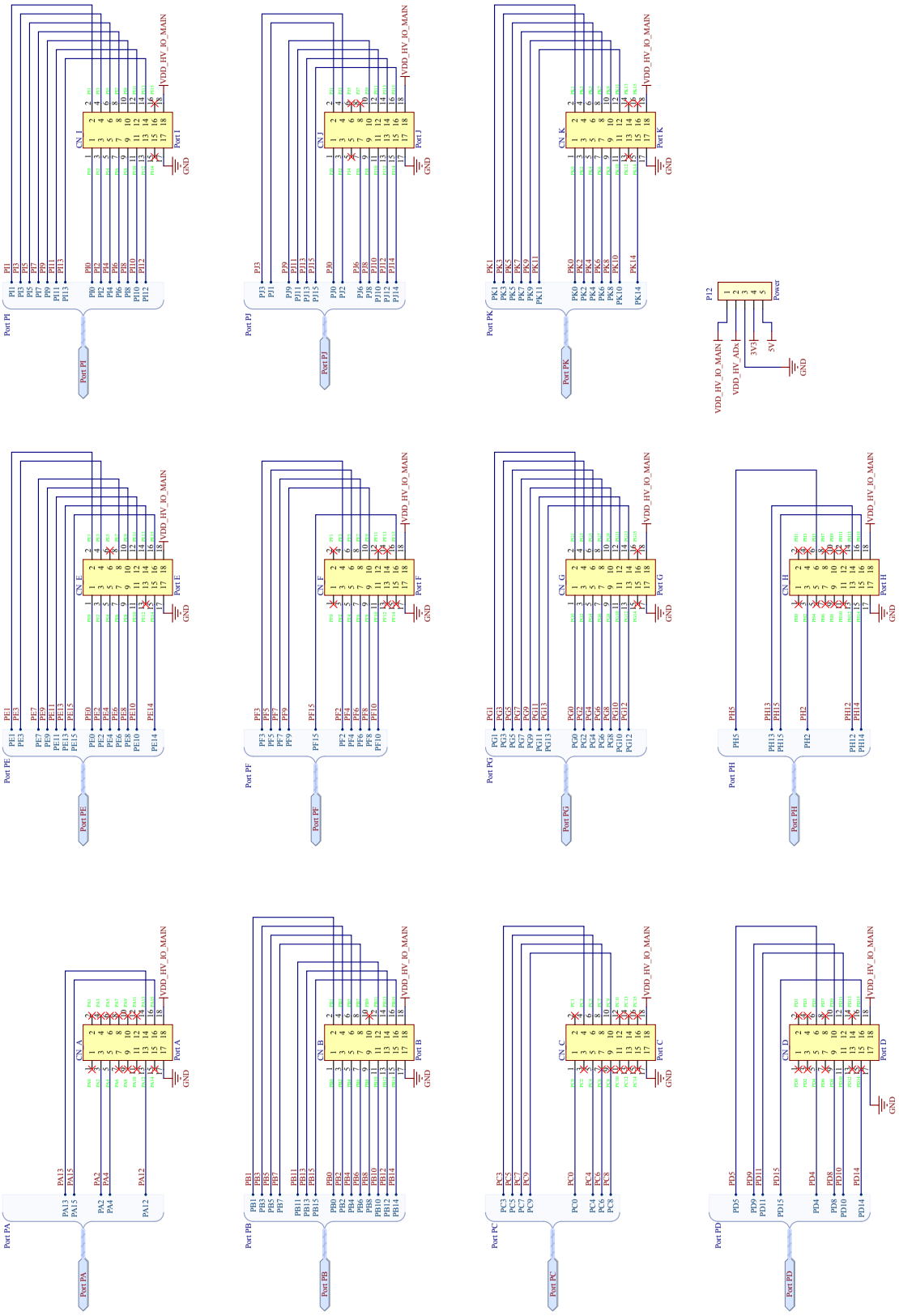
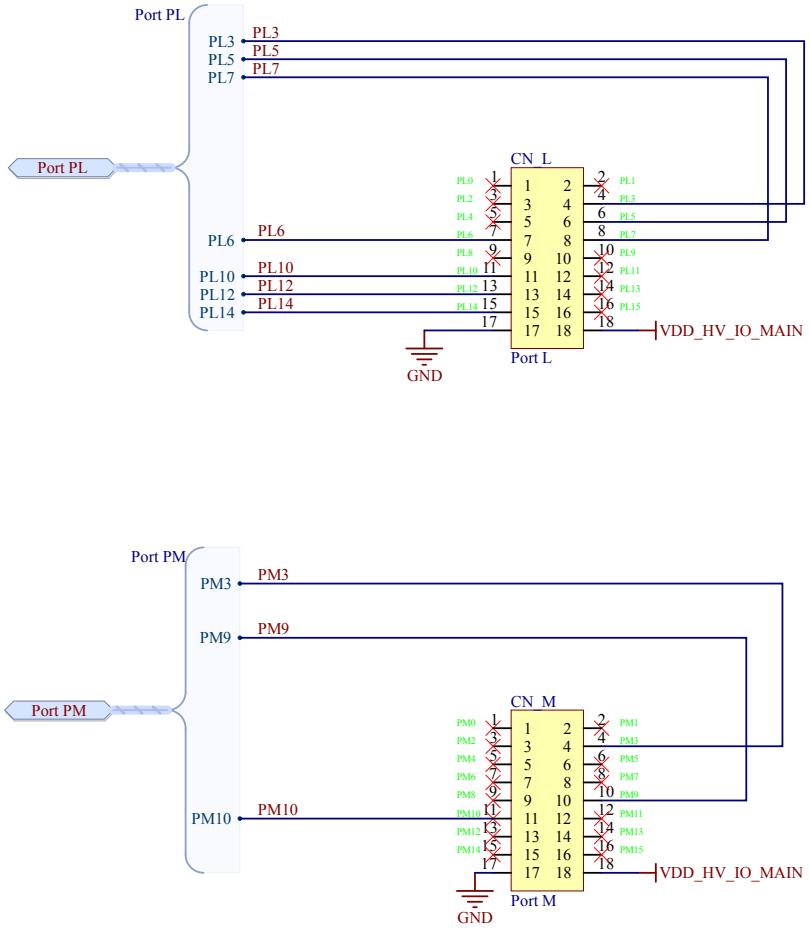


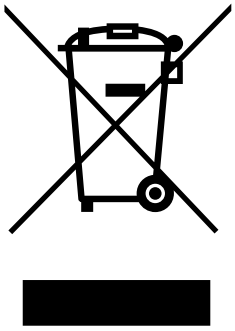
Figure 34. IO user_2



10 Product disposal

Disposal of this product: WEEE (Waste Electrical and Electronic Equipment)

(Applicable in Europe)



This symbol on the product, accessories, or accompanying documents indicates that the product and its electronic accessories must not be disposed of with household waste at the end of their working life.

To prevent possible harm to the environment and human health from uncontrolled waste disposal, separate these items from other types of waste and recycle them responsibly at a designated collection point to promote the sustainable reuse of material resources.

Household users:

Contact the retailer that you purchased the product from or your local authority for details of your nearest designated collection point.

Business users:

Contact your dealer or supplier for further information.

Revision history

Table 33. **Document revision history**

Date	Revision	Changes
02-Oct-2023	1	Initial release.
26-Aug-2025	2	Removed "ST restricted" watermark. Updated Section 3: Handling precautions. Added Section 10: Product disposal.

Contents

List of tables

List of figures