25 kW, dual active bridge bidirectional power converter for EV charging and battery energy storage systems

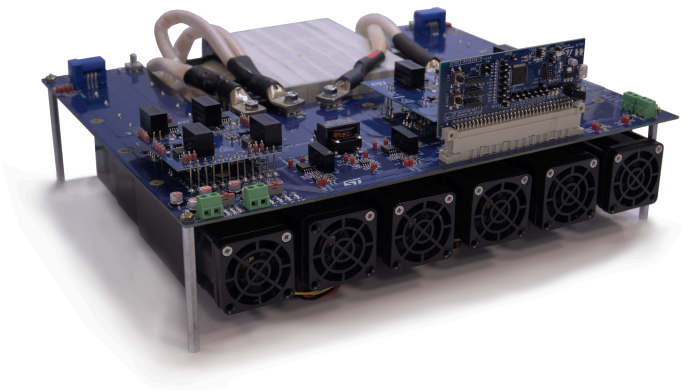
Introduction

This reference design represents a complete solution for high power bidirectional DC-DC power converter in dual active bridge topology based on ACEPACK2 SiC power modules. An STM32G474 MCU Mixed-Signal digital platform optimized for Digital Power is used to control the power converter. The latest generation SiC power modules and high-frequency operation (100 kHz) ensure very high performance and design optimization. Soft switching DAB behavior is managed by modulation techniques according to load/voltage variation.

This reference design consists of the following separate modules:

- STDES-DABBIDIRP: main power board with ACEPACK 2 SiC power modules, a full bridge A2F12M12W2-F1 and two A2H6M12W3-F for primary HV side and secondary LV side, respectively. The power board design also includes bulk capacitors, sensing sections, and auxiliary power supply.
- STDES-DABBIDIRDF: driver board for full bridge ACEPACK 2 A2F12M12W2-F1 SiC power modules based on STGAP2SiCS Galvanically isolated 4 A single gate driver for SiC MOSFETs
- STDES-DABBIDIRDH: two driver boards for half bridges ACEPACK2 A2H6M12W3-F SiC power modules based on STGAP2SiCS galvanically isolated 4 A single gate driver for SiC MOSFETs
- STDES-PFCBIDIRC: control board based on the STM32G4 series microcontroller with connectors for communication and programming, and test-points and status indicators for testing and monitoring.

Figure 1. STDES-DABBIDIR reference design board



The latest technology SiC MOSFETs power modules used at high switching frequency (100 kHz) and the topology structure allow nearly 98% efficiency and the use of smaller and more cost-effective passive power components.

This high efficiency bidirectional isolated DC-DC converter is designed for several end applications such as electric vehicles (EV) and industrial battery chargers, and industrial equipment requiring very high efficiency and reliability.

1 Safety and compliance information

- The reference design uses voltage levels that can cause serious injury and even death.
- Due to the high-power density, the components on the board as well as the heat sink can be heated to a very high temperature, which can cause a burning risk when touched directly.
- This board is intended for use by experienced power electronics professionals who understand the necessary precautions against potential dangers and risks while operating this board, even when it is not powered.

Important: *The STDES-DABBIDIR evaluation board is designed for demonstration purposes only and is not intended for domestic or industrial installations.*

Danger: *The high voltage levels used to operate the STDES-DABBIDIR evaluation board may provoke a serious electrical shock. This evaluation board must be used in a suitable laboratory by qualified personnel only, familiar with the installation, use, and maintenance of power electrical systems. During operation, do not touch the board as some of its components may reach very high temperatures.*

2 Overview

2.1 Features

- Reference design modular kit:
  - Main power board
  - Driving board (1xHV side 2xLV side)
  - STM32G474RET3 control board
- Dual active bridge DC-DC power converter:
  - Nominal DC input voltage 800 V
  - Nominal DC output voltage 400 V
  - Nominal power 25 kW
  - Switching frequency 100 kHz
  - Peak efficiency 98.4%
- Main features:
  - ACEPACK 2 SiC power module to optimize power section integration and thermal dissipation
  - Bidirectional capability
  - Extended soft switching behavior enabled by enhanced modulation techniques management
  - Isolated SiC gate driver
  - STM32G4 family MCU for customizable full digital solution
  - Inrush current control and soft startup
- High frequency operation with SiC MOSFETs:
  - High efficiency ~99%
  - Smaller and lighter passive elements

Figure 2. STDES-DABBIDIR reference design overview

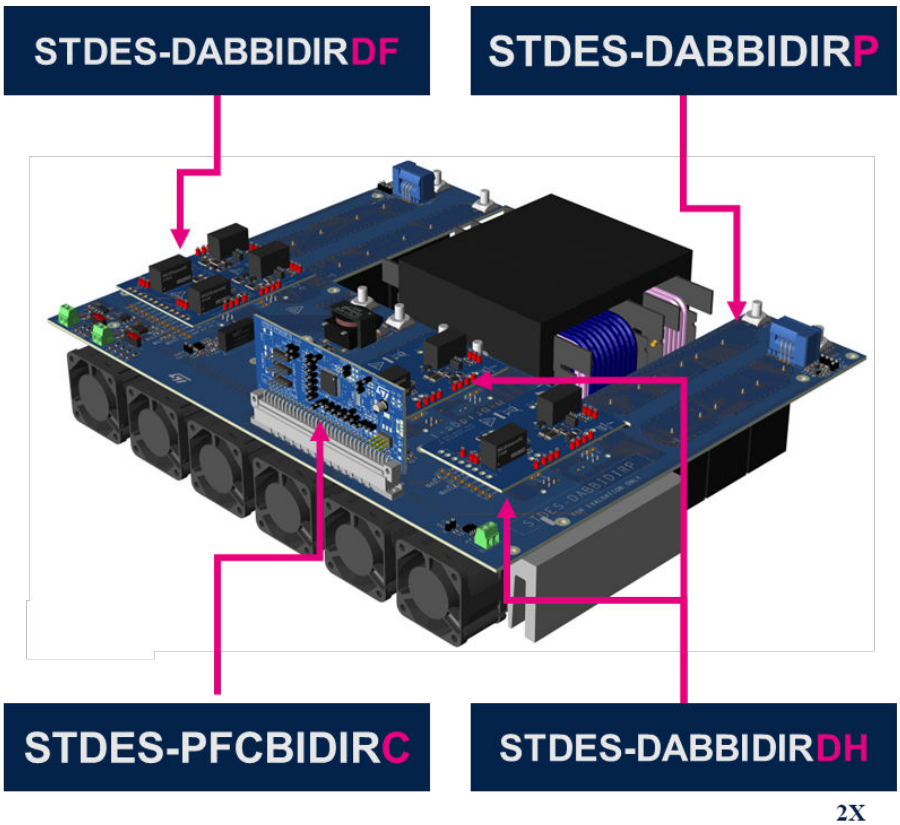
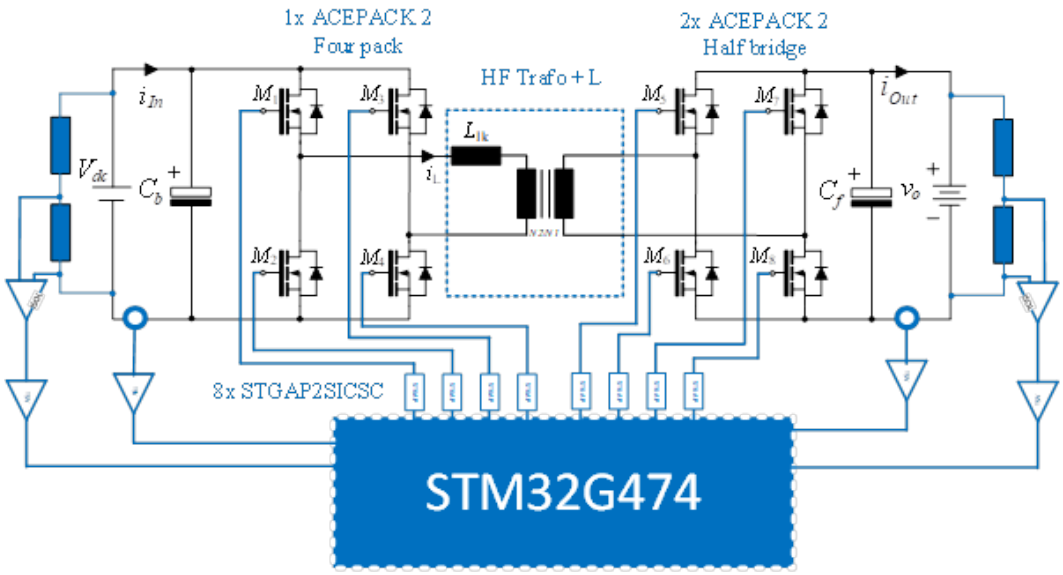


Figure 3. **STDES-DC2DCDAB block diagram**



2.2 Main characteristics

Table 1. **Main characteristics**

Description	Symbol	Min.	Typ.	Max.	Unit	Comments
HV DC Voltage	V_{DCHV}	720	800	880	V	
LV DC Voltage	V_{DCLV}		400		V	
Maximum output power	$P_{out_{MAX}}$		25		kW	At nominal voltages
Switching frequency	f_{SW}		70		kHz	
Peak efficiency	n		>98		%	At nominal voltages

2.3 Dual active bridge topology

The dual active bridge is a bidirectional, dc-dc converter that includes two full bridges, a high frequency transformer, energy transfer inductor, and dc-link capacitors. Due to the symmetry of this converter, with identical primary and secondary bridges, it is capable of bidirectional power flow control.

Each full-bridge consists of two totem-poled switching devices configuration, driven with complimentary signals. The switching frequency of these complimentary devices is referred to as the switching frequency of the converter.

The topology is shown in Figure 3, where Vin and Vout are the dc-link voltages and Lk is the actual resonance inductance, which includes leakage inductance of the transformer plus any additional auxiliary energy transfer inductance. Equivalent AC primary and secondary voltages are controlled by the actual configuration of semiconductor switches M1-M8.

With insulated gate bipolar transistor (IGBT) implementations, switching cells are traditionally implemented with antiparallel diodes and snubber capacitors to direct current commutation on switching events and to allow zero voltage switching (ZVS) through the snubber capacitor and energy transfer inductance resonance.

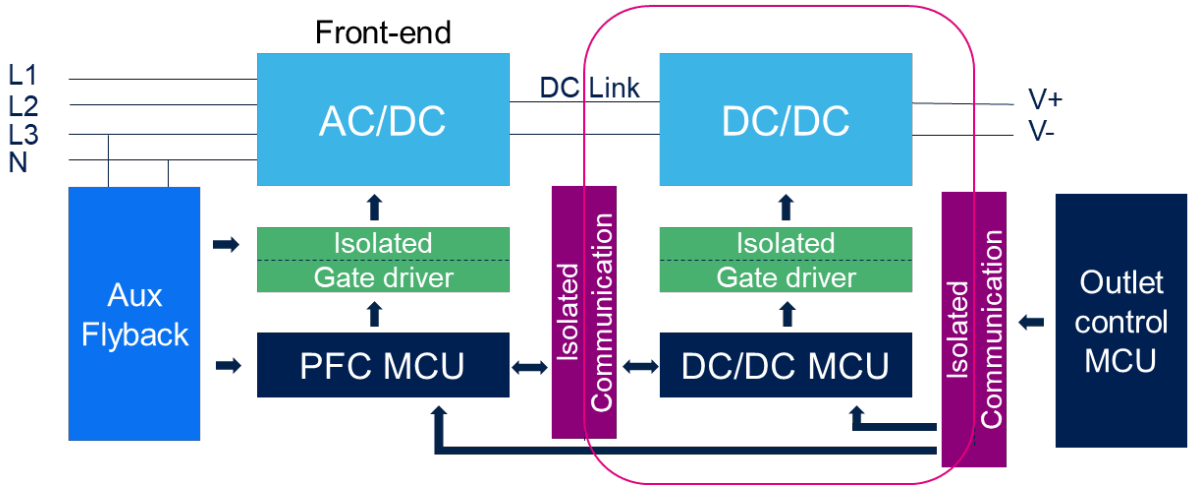
Now, high-voltage MOSFETs are selected for DAB designs because their intrinsic body diode and drain-to-source output capacitance take the place of external components and help reduce the part count of the converter.

Wide bandgap power MOSFETs such as silicon carbide (SiC) are commonly used for high-power DABs to increase switching frequency operation of the converter and increase power density in DAB applications.

2.4 Typical application

A typical application of DAB power converter is the EV battery DC charger. A three phase system suitable for the proposed power level is shown in the following figure.

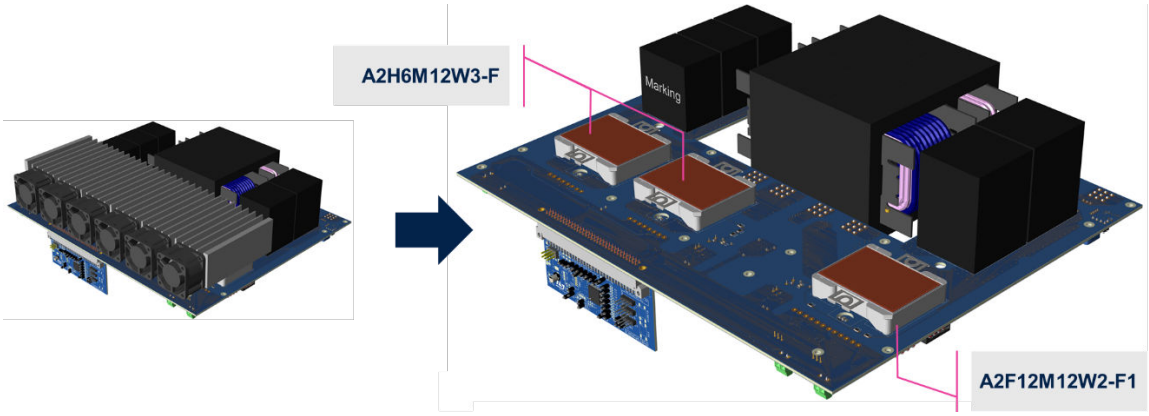
Figure 4. Typical DC battery charger architecture



The DC fast charger consists of a three-phase active front end (AFE) rectifier that provides a regulated DC link from a universal three-phase AC input. The current from the grid must be high quality current to fulfill the power quality requirements. The DAB operation ensures isolation and bidirectional operation required by the downstream DC-DC converter.

The full-bridge A2F12M12W2-F and half-bridge A2H6M12W3 ACEPACK 2 SiC power modules selected for primary and secondary side, respectively, ensure very high integration for this topology.

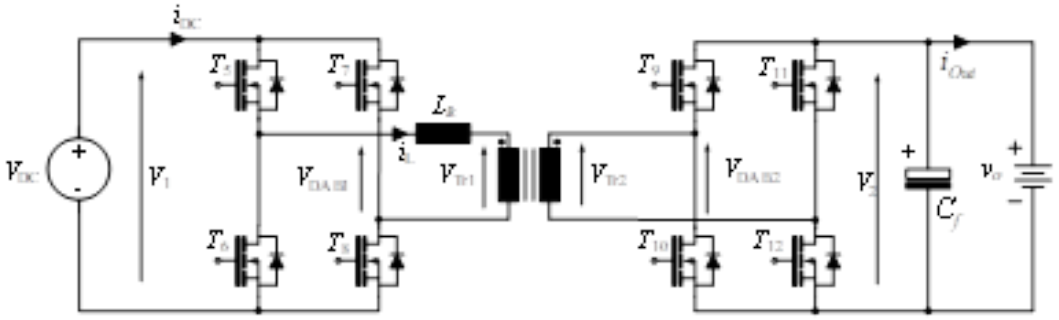
Figure 5. SiC power module assembly



3 DAB converter operation

The DAB converter contains two voltage sourced full bridge circuits that are connected to the inductor L and the high frequency transformer. To transfer power, time varying voltages $v_{AC1}(t) = v_{DAB1}(t)$ and $v_{AC2}(t) = v_{DAB2}(t)$ must be provided by the full bridge circuits to both, the high frequency transformer, and the converter inductor L.

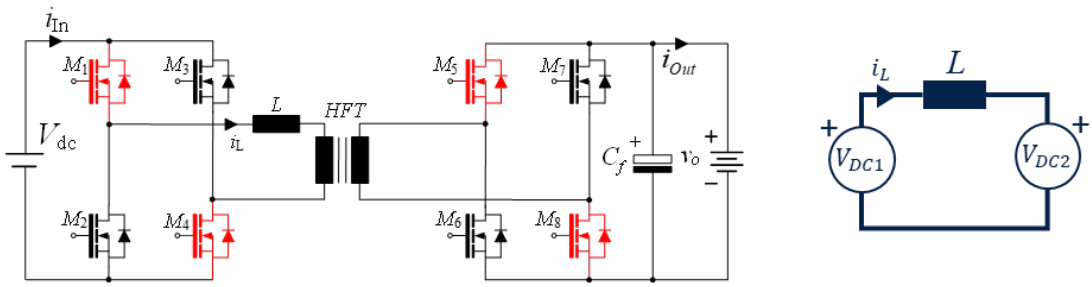
Figure 6. DAB topology



$$v_{DAB1}(t) = \begin{cases} +V_1 & I \quad T_1, T_4 on \& T_2, T_3 off \\ 0 & II \quad T_1, T_4 on \& T_2, T_3 off \\ & III \quad T_1, T_4 off \& T_2, T_3 on \\ -V_1 & IV \quad T_1, T_4 on \& T_2, T_3 off \end{cases} \quad (1)$$

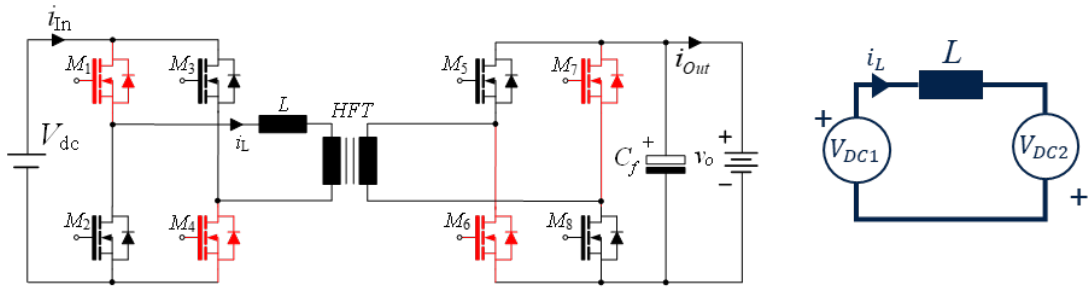
$$v_{DAB2}(t) = \begin{cases} +V_2 & I \quad T_5, T_8 on \& T_6, T_7 off \\ 0 & II \quad T_5, T_8 on \& T_6, T_7 off \\ & III \quad T_5, T_8 off \& T_6, T_7 on \\ -V_2 & IV \quad T_5, T_8 on \& T_6, T_7 off \end{cases} \quad (2)$$

Figure 7. **DAB operation (combo)**



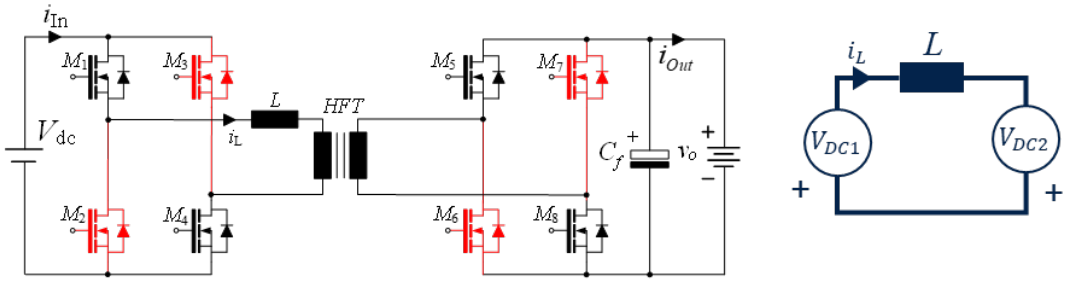
$$v_{\mathrm{DAB1}}(t) = +V_1\ T_1, T_4\ on\ \&\ T_2, T_3\ off$$

$$v_{\mathrm{DAB2}}(t) = +V_2\ T_5, T_8 on\ \&\ T_6, T_7\ off$$



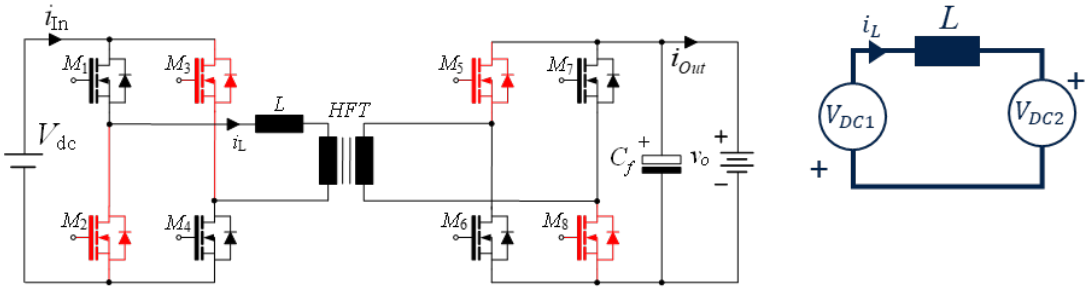
$$v_{\mathrm{DAB1}}(t) = +V_1\ T_1, T_4\ on\ \&\ T_2, T_3\ off$$

$$v_{\mathrm{DAB2}}(t) = -V_2\ T_5, T_8 \mathrm{off}\ \&\ T_6, T_7\ on$$



$$v_{\mathrm{DAB1}}(t) = -V_1\ T_1, T_4\ off\ \&\ T_2, T_3\ on$$

$$v_{\mathrm{DAB2}}(t) = -V_2\ T_5, T_8 off\ \&\ T_6, T_7\ on$$



$$v_{\mathrm{DAB1}}(t) = -V_1\ T_1, T_4\ off\ \&\ T_2, T_3\ on$$

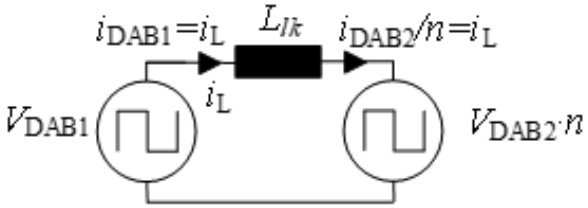
$$v_{\mathrm{DAB2}}(t) = +\ T_5, T_8 on\ \&\ T_6, T_7\ off$$

The HV and LV side full-bridge circuits can therefore be replaced by the respective voltage sources $v_{AC1}(t) = v_{DAB1}(t)$ and $v_{AC2}(t) = v_{DAB2}(t)$ to simplify the analysis of the DAB converter.

Figure 8. Simplified diagram of DAB

The primary side referred equivalent circuit diagram is shown below.

Figure 9. Primary side referred simplified diagram of DAB



According to the simplified circuit, the inductance voltage depends on the AC voltage of the full bridges.

$$v_{Lk}(t) = v_{DAB1}(t) - nv_{DAB2}(t) \tag{3}$$

Then we obtain the inductor current.

$$i_L(t) = i_L(t_0) + \frac{1}{L}\int_0^{\frac{T_s}{2}} v_{Lk}(t)dt \forall t_0 < t_1 \tag{4}$$

We now consider the instantaneous power for both sides.

(5)

$$\begin{cases} p_1(t) = v_{DAB1}(t)i_L(t) \\ p_2(t) = nv_{DAB2}(t)i_L(t) \end{cases}$$

The average power over one switching cycle T_s , $T_s = 1/f_s$, is finally calculated.

$$\begin{cases} P_1 = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} p_1(t)dt \\ P_2 = \frac{1}{T_s}\int_{t_0}^{t_0+T_s} p_2(t)dt \end{cases} \tag{6}$$

As equivalent AC bridge voltages can be represented by two sinusoidal waveforms with phase shift φ :

$$\begin{cases} V_1(t) = V_1 cos(\omega t) \\ V_2(t) = V_2 cos(\omega t - \varphi) \end{cases} \tag{7}$$

For inductor current, the equivalent phasor is:

$$\bar{I}_L = \frac{\bar{V}_1 - \bar{V}_2}{j\omega L_{lk}} = \frac{V_1 \angle 0 - nV_2 \angle \varphi}{j\omega L_{lk}} \tag{8}$$

That for time and considering $\frac{\cos}{j} = sin$ becomes:

$$i_L(t) = \frac{V_1}{\omega L_{lk}} sin(\omega t) - \frac{nV_2}{\omega L_{lk}} sin(\omega t - \varphi) \quad (9)$$

Next we obtain instantaneous output power:

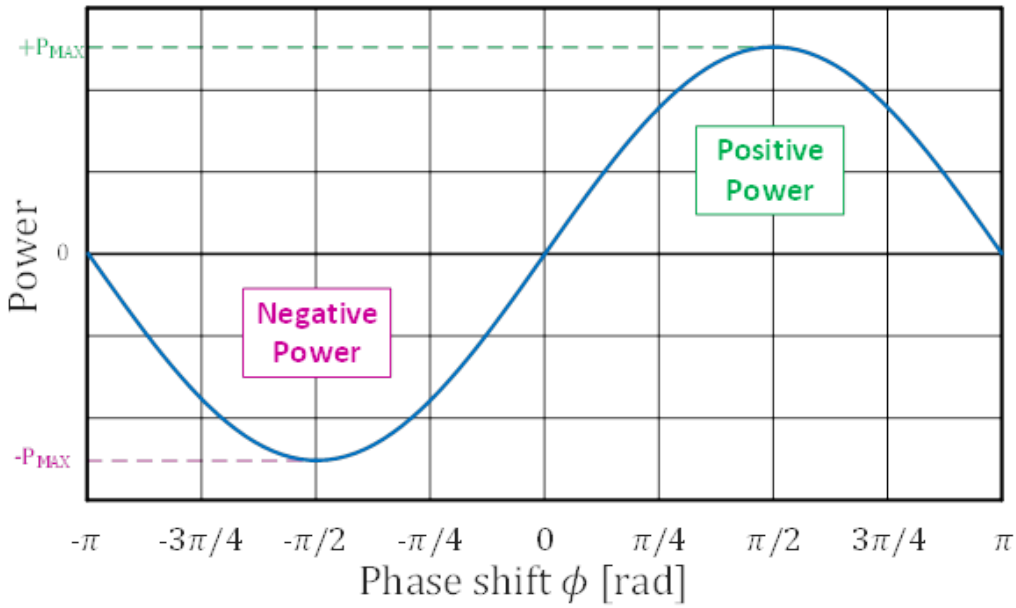
$$p_2(t) = \frac{nV_1V_2}{\omega L_{lk}} cos(\omega t - \varphi) sin(\omega t) \quad (10)$$

Which averaged over the switching period T becomes:

$$P_2 = \langle p_2(t) \rangle_{\frac{1}{T}} = \frac{1}{T}\int_0^T p_2(t)dt = \frac{\boldsymbol{nV_1V_2}}{\boldsymbol{2\pi f_s L_{lk}}} \boldsymbol{sin(\varphi)} \quad (11)$$

As shown by the equation, the DAB allows power flow in both directions according to the sign of the phase shift. Power transfer is modulated according to the amplitude of the phase shift, with maximum at $\varphi = \pm\frac{\pi}{2}$.

Figure 10. Power transfer vs phase shift in DAB



In addition, according to this relation, the power level of the DAB converter is thus typically adjusted using one or more of the following control parameters.

1. The phase shift, ϕ, between $v_{DAB1}(t)$ and $v_{DAB2}(t)$, with −π < ϕ < π
2. The duty cycle, D1, of $v_{DAB1}(t)$, with 0 < D1 < 1/2
3. The duty cycle, D2, of $v_{DAB2}(t)$, with 0 < D2 < 1/2
4. The switching frequency f_s

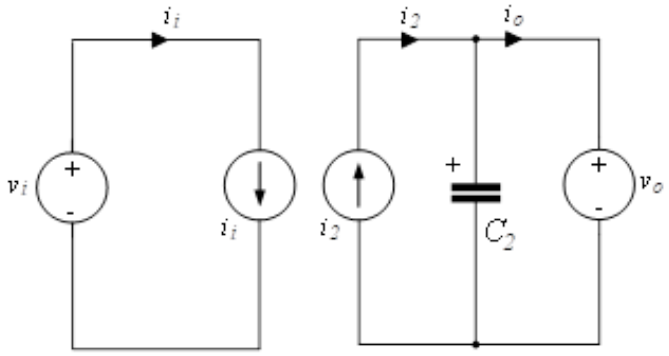
Defining the phase shift duty ratio $D = \frac{\varphi_{rad}}{\pi}$, the actual power transfer can be derived from the following equation.

$$Pout = \frac{nV_{DC_1}V_{DC_2}}{2Lf_s} D(1-D)$$

To define the control strategy of the DAB converter and the control parameters, knowledge of the equivalent dynamic model of the converter must be considered.

The equivalent average model of the DAB can be described by the following schematic and equivalent controlled source mathematical representation.

Figure 11. **Average model of the DAB**



$$I_2 = \frac{nV_i}{2Lf_s}D(1-D)$$

$$I_{i,avg} = \frac{nV_o}{2Lf_s}D(1-D)$$

To obtain the small-signal model, perturbation is injected to define the effects of the parameters on the equation.

$$i_{i,avg} = I_{i,avg} + \widehat{i_{i,avg}}$$
$$i_2 = I_2 + \widehat{i_2}$$

$$\widehat{i_{i,avg}} = \left.\frac{\partial i_{i,avg}}{\partial d}\right|_Q \hat{d} + \left.\frac{\partial i_{i,avg}}{\partial v_o}\right|_Q \widehat{v_o} = F_1\hat{d} + F_2\widehat{v_o}$$
$$\widehat{i_2} = \left.\frac{\partial i_2}{\partial d}\right|_Q \hat{d} + \left.\frac{\partial i_2}{\partial v_i}\right|_Q \widehat{v_o} = F_3\hat{d} + F_4\widehat{v_o}$$

$$F_1 = \left.\frac{\partial i_{i,avg}}{\partial d}\right|_Q = \frac{nV_o}{2Lf_s}(1-2|d|) \quad F_2 = \left.\frac{\partial i_{i,avg}}{\partial v_o}\right|_Q = \frac{nV_o}{2Lf_s}d(1-|d|)$$
$$F_3 = \left.\frac{\partial i_2}{\partial d}\right|_Q = \frac{nV_i}{2Lf_s}(1-2|d|) \qquad F_4 = \left.\frac{\partial i_2}{\partial v_i}\right|_Q = \frac{nV_i}{2Lf_s}d(1-|d|)$$

Thanks to input capacitance and PFC stage regulation, input voltage perturbation may be neglected.

$$F_4 = \left.\frac{\partial i_2}{\partial v_i}\right|_Q = \frac{nV_i}{2Lf_s}d(1-|d|) \cong 0$$

The output capacitor ripple voltage is now included through the following equation.

$$C_2\frac{d\widehat{v_o}}{dt} = \widehat{i_2} - \widehat{i_{i,avg}}$$

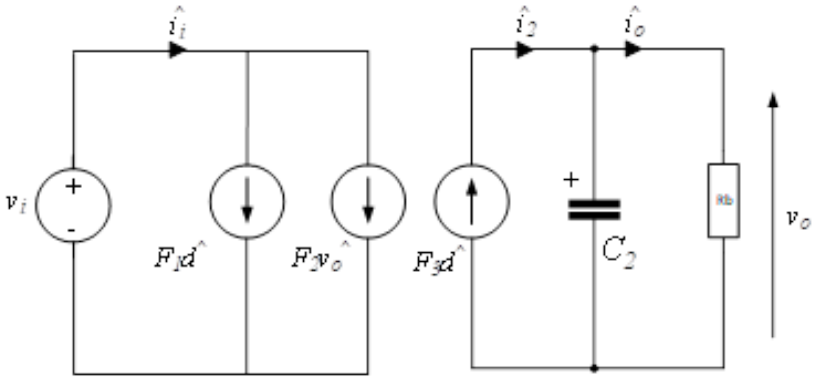
The final equivalent small signal circuit is then obtained.

$$\widehat{i_{i,avg}} = F_1\hat{d} + F_2\widehat{v_o} = \frac{nV_o}{2Lf_s}(1-2|d|)\hat{d} + \frac{nV_o}{2Lf_s}d(1-|d|)\widehat{v_o}$$

$$\widehat{i_2} = F_3\hat{d} = \frac{nV_i}{2Lf_s}(1-2|d|)\hat{d}$$

$$C_2\frac{d\widehat{v_o}}{dt} = \widehat{i_2} - \widehat{i_{i,avg}}$$

Figure 12. **Simplified small signal equivalent circuit of DAB converter**



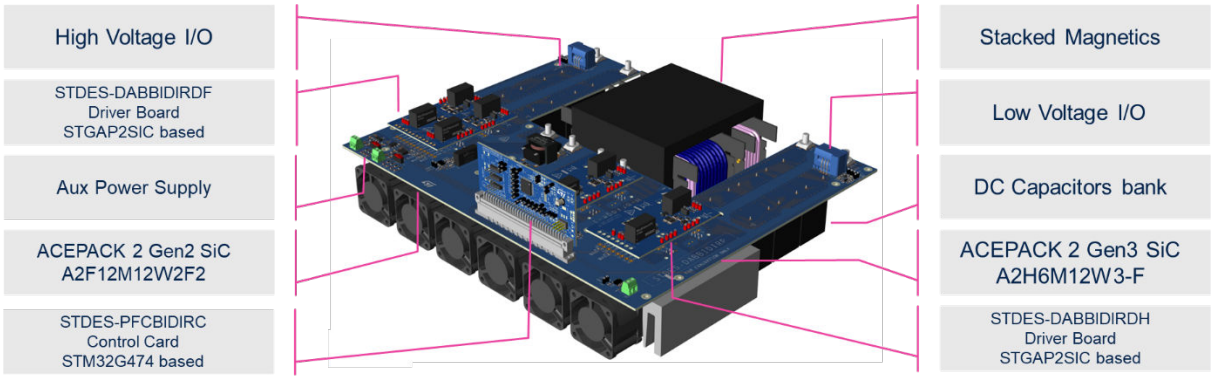
4 STDES-DABBIDIR reference design overview

4.1 Power stage of the STDES-DABBIDIR reference design

STDES-DABBIDIRP consists of a dual active bridge converter topology implementing ACEPACK 2 SiC power modules in the power section.

The driving section is based on two different PCB modules to optimize the driving path of each module. Fan cooling is used to simplify the evaluation of the reference design platform.

Figure 13. Power stage blocks



4.2 Driving stage of the STDES-DABBIDIR reference design

Two different driving boards are proposed to feed the driving signal to ACEPACK 2 SiC power modules. Both solutions are based on STGAP2SICS gate drivers for SiC technology.

The STGAP2SICS single gate driver provides galvanic isolation between the gate driving channel and the low voltage control and interface circuitry. The gate driver is characterized by 4 A capability and rail-to-rail outputs, making the device also suitable for mid and high-power applications such as power conversion and motor driver inverters in industrial applications. The configuration featuring a single output pin and Miller clamp function prevents gate spikes during fast commutations in half-bridge topologies.

The device integrates UVLO protection with optimized value for SiC MOSFETs and thermal shutdown to facilitate the design of highly reliable systems. Dual input pins allow the selection of signal polarity control and implementation of hardware interlocking protection to avoid cross-conduction in case of controller malfunction.

Figure 14. **STDES-DABBIDIRDF driver board based on 4xSTGAP2SIC**

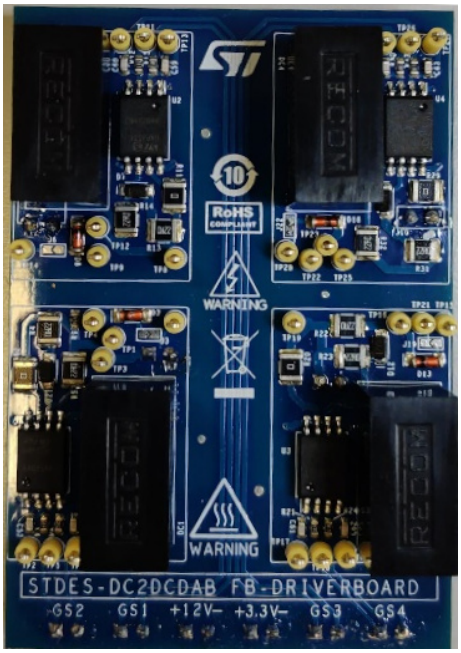
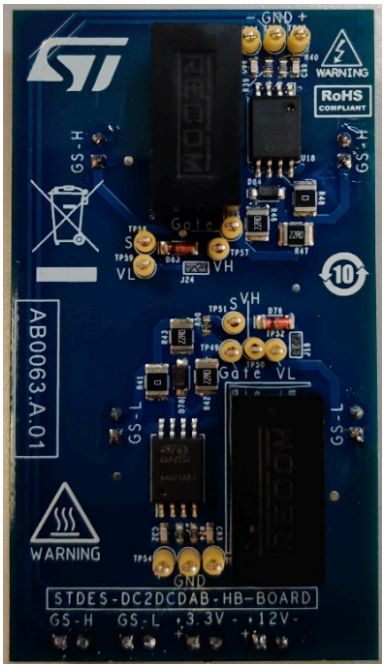


Figure 15. **STDES-DABBIDIRDH driver board based on 2xSTGAP2SIC**



4.3 Control stage of the STDES-DABBIDIR reference design

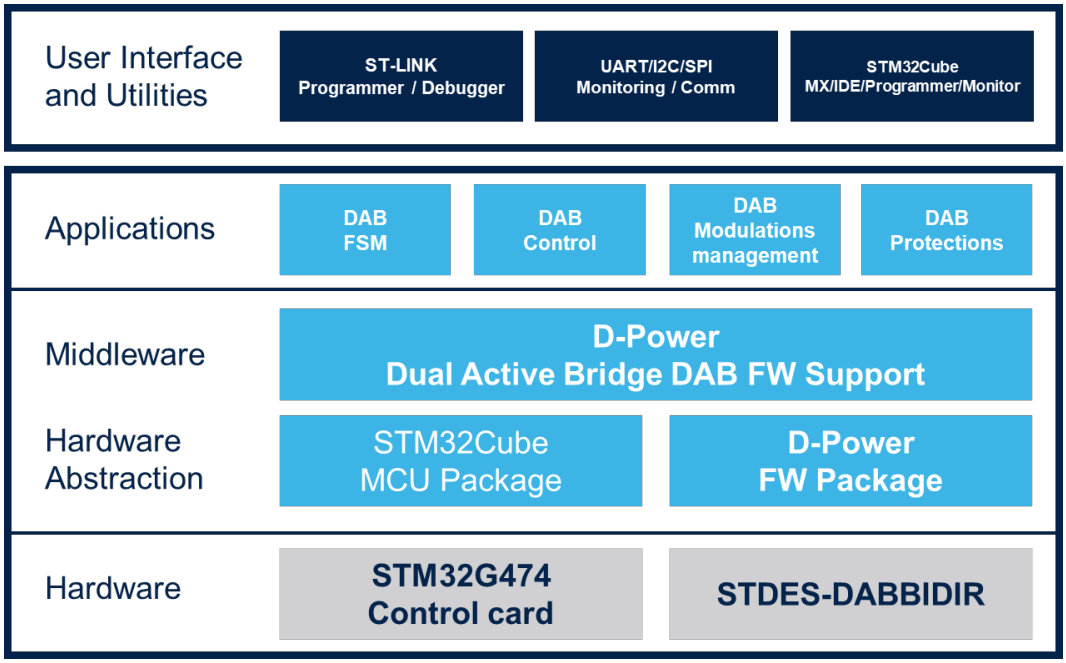
The control stage is based on STM32G474RE MCU devices with high-performance Arm® Cortex®-M4 32-bit RISC core. The Cortex-M4 core features a single-precision floating-point unit (FPU), which supports all the Arm single-precision data-processing instructions and all the data types. It also implements a full set of digital signal processing (DSP) instructions and a memory protection unit (MPU) to enhance application security.

Reference design firmware is provided to help evaluate the full functionality of this power platform. The digital power converter architecture and STM32Cube environments help optimize the implementation and use of the source code.

The hardware abstraction and middleware layers contain the peripheral and application-related functions to manage and extend the functionality.

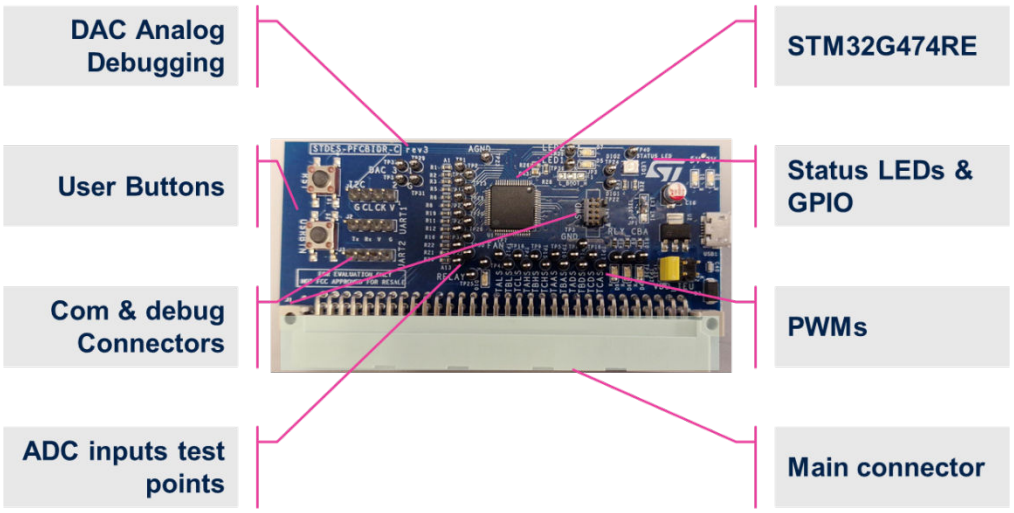
The application layer allows us to manage operation features such as startup procedure load management, control, and protection, as well as the finite state machine.

Figure 16. **STDES-DABBIDIR FW architecture**



The general purpose STDES-PFCBIDIR control board based on the STM32G474 MCU is suitable for various high-power applications. This control board supports additional communication and debugging features such as I2C, UART, status LEDs, and analog monitoring, to extend the usage of the MCU peripherals.

Figure 17. **Control stage blocks**



5 STDES-DABBIDIR hardware implementation

5.1 Input/output requirements

5.1.1 Maximum input power

The maximum input power related to high voltage is obtained according to maximum output (low-voltage side) and worst-case efficiency considered.

$$P_{in\_max} = \frac{P_{out\_max}}{\boldsymbol{\eta_w}} = \frac{28kW}{95\%} = 29{,}4kW \quad (12)$$

5.1.2 Maximum DC input current

The maximum DC input current with the variation of the Vin value is now considered. When Vin is minimal, the maximum DC input current is obtained.

$$I_{in\_max} = \frac{P_{in}}{V_{in\_min}} = \frac{29{,}4kW}{720V} = 40.93A \quad (13)$$

5.1.3 Nominal DC input current

The maximum DC input current with the variation of the Vin value is now considered. When Vin is minimal, the maximum DC input current is obtained.

$$I_{in} = \frac{P_{in}}{V_{in\_nom}} = \frac{29{,}4kW}{800} = 36.84A \quad (14)$$

5.1.4 Minimum DC input current

The mean input current changes with the variation of the Vin value. When Vin is minimal, the maximum average current is obtained.

$$I_{in} = \frac{P_{in}}{V_{in\_max}} = \frac{29{,}4kW}{880} = 33{,}49A \quad (15)$$

5.1.5 Maximum DC output current

The maximum DC output current is obtained from the typical output voltage at maximum output power.

$$I_{out} = \frac{P_{max}}{V_{out\_nom}} = \frac{28000}{450} = 62.22A \quad (16)$$

5.1.6 Minimum DC output current

The minimum DC output current is obtained from the maximum output voltage at maximum output power.

$$I_{out} = \frac{P_{out\_max}}{V_{out\_max}} = \frac{28000}{500} = 56A \quad (17)$$

5.1.7 Nominal DC output current

The nominal DC output current is obtained for the typical output voltage at nominal output power.

$$I_{out} = \frac{P_{out}}{V_{out\_nom}} = \frac{25000}{450} = 55.55A \quad (18)$$

5.2 Sensing circuitry

5.2.1 HV voltage sensing

The high-voltage-side voltage is obtained using a two-stage sensor circuit isolated architecture. The first stage represents an isolated op amp that allows measurement of the HV through a voltage divider with an isolation barrier.

Isol-Op-AMP output is limited in volts and is scaled with a second stage of op amps with appropriate gain and bias.

Figure 18. HV voltage sensing equivalent circuit.

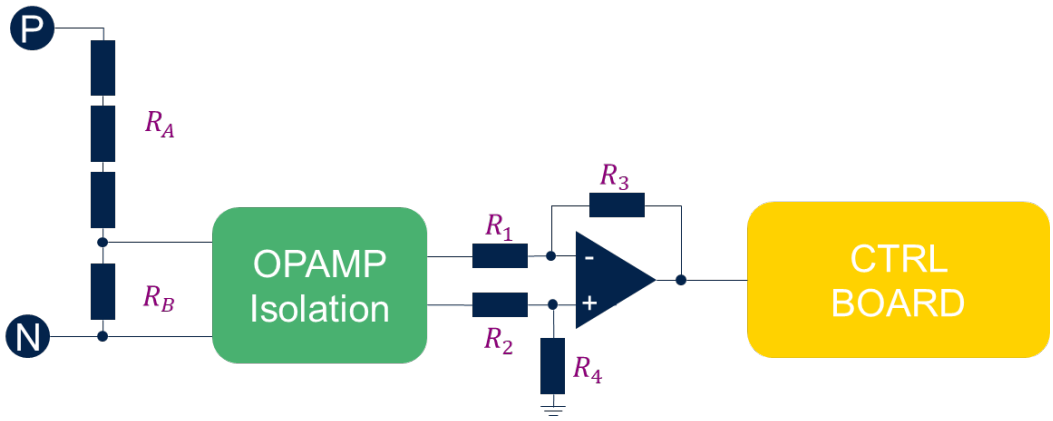
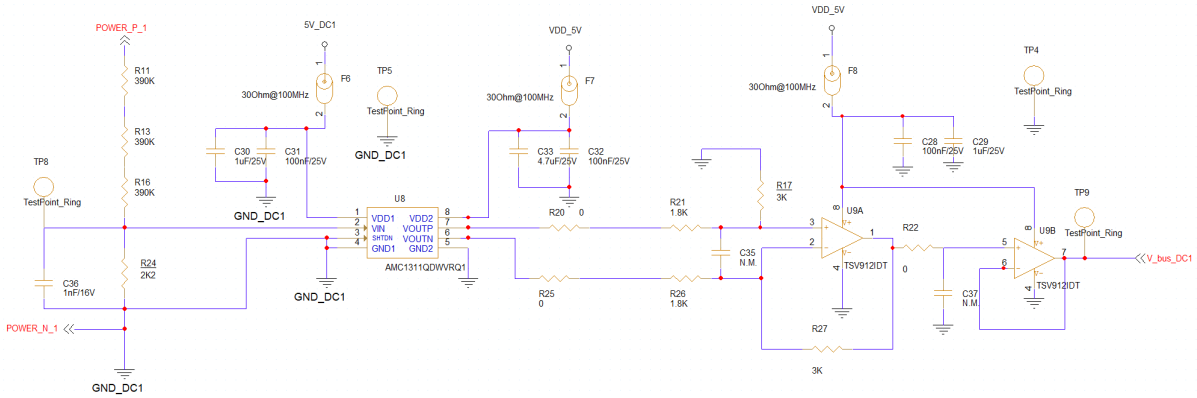


Figure 19. STDES-DABBIDIR HV sensing circuit



To define the maximum high-voltage-side measurement, the maximum voltage range is considered.

Table 2. HV-side input voltages

Parameters	Value	Description
Vin_nom	800 V	Nominal input Voltage
Vin_min	720 V	Min. input voltage
Vin_max	880 V	Max. input voltage

High voltage maximum voltage range is considered with +20% margin.

$$V_{SenseMax}^{DC1} = V_{Max}^{DC1} + 20\%V_{Max}^{DC1} = 880*1.2 = 1056 \cong 1050V$$

The maximum voltage of the isolated op amp must be guaranteed at HV max sense voltage.

$$V_{Max}^{isolOA} = 2V$$

From this, voltage divider transfer function is obtained.

$$k_{div}^{DC1} = \frac{V_{Max}^{isolOA}}{V_{Max}^{DC1}} = \frac{2}{1050} = 1.905e^{-3}$$

The resistor values of voltage divider are now calculated.

$$R_B = 22k\Omega$$

$$R_A = \frac{1 - k_{div}^{DC1}}{k_{div}^{DC1}} R_B = 11.53M\Omega \cong 3x3.90k\Omega$$

Note: Isolated op amp unity and voltage gain must be followed by proper signal conditioning to fulfill ADC range requirements.

Table 3. HV sensing input and output voltage range

Parameters	Value	Description
V_{out_max}	3.3 V	Maximum value of the voltage range of the microcontroller ADC
V_{in_max}	2 V	Op amp maximum input voltage | maximum output voltage of ISO op amp

According to these input and output values, the voltage gain of signal conditioning is defined.

$$K = \frac{V_{out\_max}}{V_{in\_max}} = \frac{3.3V}{2V} = 1.65$$

The differential amplifier configuration is designed according to the voltage gain requirement.

Table 4. STDES-DABBIDIR effective value of HV sensing

Parameters	Value	Description
V_{HV_range}	$0V - 1050V$	HV voltage range
V_{ADC_range}	$0V - 3.3V$	ADC signal range
G_{Tv_HVDC}	$3.13e^{-3}\frac{V}{V}$	k_{eq} conditioning circuit gain
G_{ADC_Bits}	$1240\frac{Bits}{V}$	ADC peripheral digital gain factor with 12-bit precision and VDDA=3.3V
B_{Tv_HVDC}	$0V$	Bias term of conditioning circuit gain
B_{ADC_Bits}	$0Bits$	Offset term of ADC peripheral
$G_{Tv\_HVDC\_tot}$	$3.881\frac{Bits}{V}$	Overall conditioning circuit gain
$B_{Tv\_HVDC\_tot}$	$0Bits$	Overall offset term
$invG_{Tv\_HVDC\_tot}$	$0.2576\frac{V}{Bits}$	Reciprocal overall conditioning circuit gain

5.2.2 LV voltage sensing

The low-voltage-side voltage is obtained using a two-stage sensor circuit isolated architecture. The first stage represents an isolated op amp that allows measurement of the HV through a voltage divider with an isolation barrier.

Isol-Op-AMP output is limited in volts and is scaled with a second stage of op amps with appropriate gain and bias.

Figure 20. **LV sensing equivalent circuit**

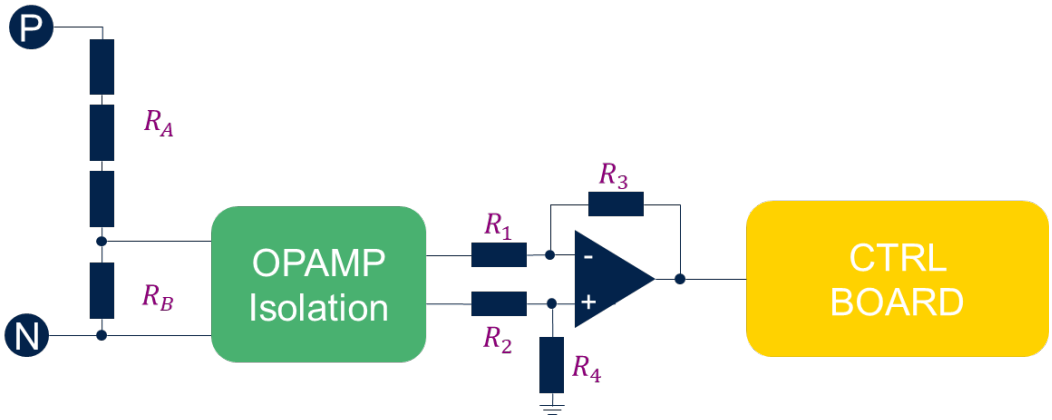
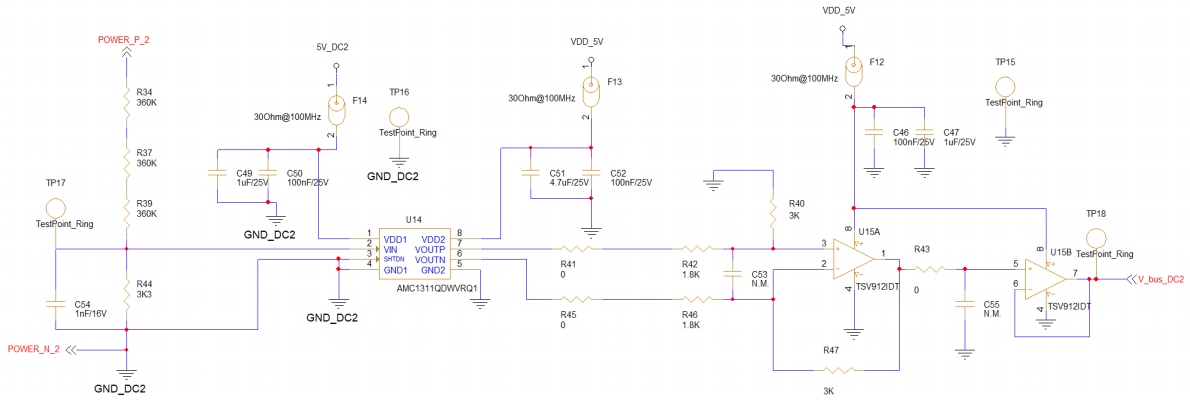


Figure 21. **STDES-DABBIDIR LV sensing circuit**



To define the maximum high voltage side measurement, the maximum voltage range is considered.

Table 5. **HV-side output voltages**

Parameters	Value	Description
Vout_nom	450 V	Nominal output Voltage
Vout_min	250 V	Min. output voltage
Vout_max	500 V	Max. output voltage

The high voltage maximum voltage range is considered with +20% margin.

$$V_{SenseMax}^{DCLV} = V_{Max}^{DCLV} + 30\%V_{Max}^{DCLV} = 500*1.3 = 650 \cong 660V$$

The isolated op amp maximum voltage must be guaranteed at LV max sense voltage.

$$V_{Max}^{AMC1311} = 2V$$

From this voltage, the divider transfer function is derived.

$$k_{div}^{DCLV} = \frac{V_{Max}^{AMC1311}}{V_{Max}^{DCLV}} = \frac{2}{660} = 3.03e^{-3}$$

The resistor values of the voltage divider are calculated.

$$R_B = 33k\Omega$$

$$R_A = \frac{1 - k_{div}^{DC1}}{k_{div}^{DC1}} R_B = 10.86M\Omega \cong 3x3.60k\Omega$$

Note: Isolated op amp unity and voltage gain must be followed by proper signal conditioning to fulfill ADC range requirements.

Table 6. LV sensing input and output voltage range

Parameters	Value	Description
V_{out_max}	3.3 V	Maximum value of the voltage range of the microcontroller ADC
V_{in_max}	2 V	Op amp maximum input voltage | maximum output voltage of ISO op amp

From the input and output values, the voltage gain for signal conditioning is defined.

$$K = \frac{V_{out\_max}}{V_{in\_max}} = \frac{3.3V}{2V} = 1.65$$

The differential amplifier configuration is designed according to the voltage gain requirement.

Table 7. STDES-DABBIDIR effective value of LV sensing

Parameters	Value	Description
V_{LV_range}	$0V - 660V$	LV voltage range
V_{ADC_range}	$0V - 3.3V$	ADC signal range
G_{Tv_LVDC}	$5.07e^{-3}\frac{V}{V}$	k_{eq} conditioning circuit gain
G_{ADC_Bits}	$1240\frac{Bits}{V}$	ADC peripheral digital gain factor with 12-bit precision and VDDA=3.3V
B_{Tv_LVDC}	$0V$	Bias term of conditioning circuit gain
B_{ADC_Bits}	$0Bits$	Offset term of ADC peripheral
$G_{Tv\_LVDC\_tot}$	$6.296\frac{Bits}{V}$	Overall conditioning circuit gain
$B_{Tv\_LVDC\_tot}$	$0Bits$	Overall offset term
$invG_{Tv\_LVDC\_tot}$	$0.1688\frac{V}{Bits}$	Reciprocal overall conditioning circuit gain

5.2.3 HV current sensing

HV-side current measurement is obtained through an isolated Hall effect current transducer.
The equivalent circuit is shown below.

Figure 22. **HV current sensing equivalent circuit**

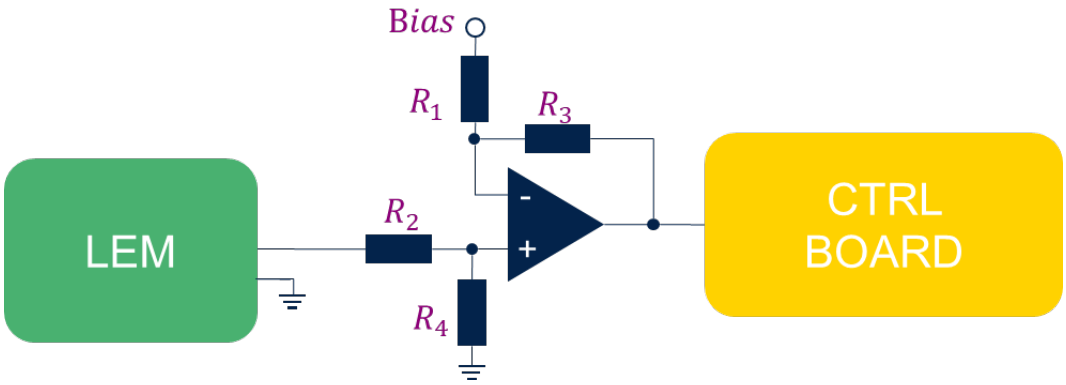
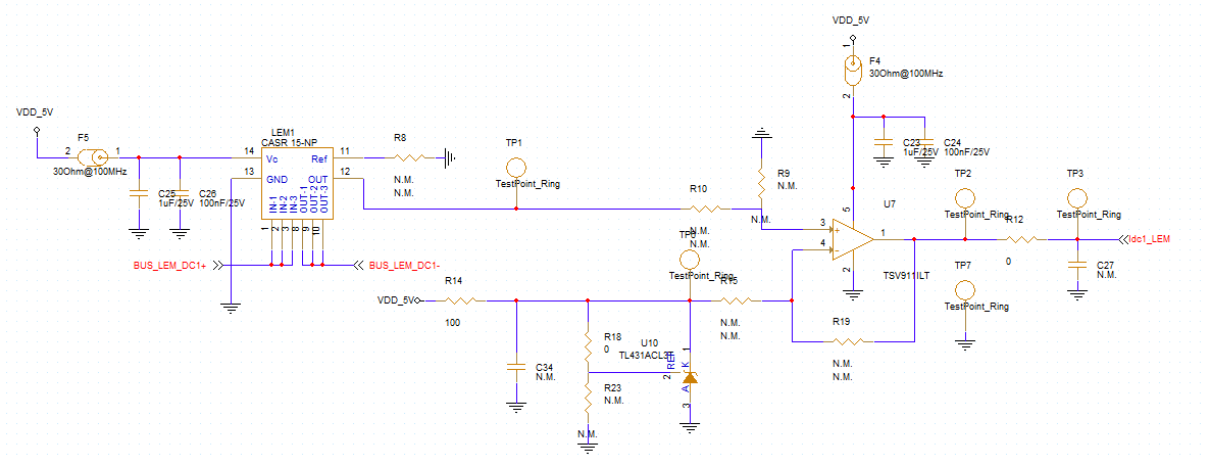


Figure 23. **STDES-DABBIDIR HV current sensing circuit**



To define the maximum high-voltage-side current measurement range, the maximum current range is considered.

Table 8. **HV-side current**

Parameters	Value	Description
I_{in_max}	$\pm 40.93A$	Max. input current at $V_{in\_min} = 720V$ and $Pin\_max = \pm 29{,}4kW$

The HV-side maximum voltage range is considered with +15% margin.

$$I_{SenseMax}^{DCHV} = I_{Max}^{DCHV} + 15\%V_{Max}^{DCIV} = \pm 40.93\text{A}*1.15 = \pm 47.07 \cong \pm 48A$$

We check this against the sensor limitation.

$I_{PM}^{CASR15NP} > I_{SenseMax}^{DCHV} \rightarrow \pm 51A > \pm 48A$ PASSED

The internal voltage reference of the Hall effect sensor is used. According to this, the sensor output voltage is shifted by Vref=2.5V.

The equivalent transfer function is given.

$$BIAS_{Hall} = 2.5V$$

$$GAIN_{Hall} = \frac{0.625}{IPN_{CASR15NP}} = \frac{0.625}{15} = 41.66e^{-3}\frac{V}{A}$$

$$V_{LEM_{out}}^{HV} = BIAS_{Hall} + GAIN_{Hall}I_{SenseMax}^{DCHV} = \left(41.66e^{-3}\frac{V}{A} \cdot \pm 48A\right) + 2.5V = \begin{cases} 4.5V \\ 0.5V \end{cases}$$

To adapt sensor the output voltage to the ADC range, op amp conditioning is required.

Table 9. Parameters for HV-side op amp conditioning

Parameter	Value	Description
I_{HV_range}	$\pm 48A$	HV-side current measurement range required
$V^{HV}_{LEM_{out}\_range}$	$0.5V to 4.5V$	Op amp input voltage range/output voltage range of hall sensor
$V_{OA\_out\_range}$	0-3.3 V	Maximum value of the voltage range of the microcontroller ADC

According to the input output specs, voltage gain and offset of signal conditioning is defined.

$$V_{out} = \left[\left(\frac{R_4}{R_2 + R_4}\right)\left(1 + \frac{R_3}{R_1}\right)\right]V_{in} - \frac{R_3}{R_1}V_{bias}$$

Finally, the transfer function is obtained.

$$GAINopamp = \left[\left(\frac{R_4}{R_2 + R_4}\right)\left(1 + \frac{R_3}{R_1}\right)\right] = \left[\left(\frac{10k\Omega}{4.12k\Omega + 10k\Omega}\right)\left(1 + \frac{1.65k\Omega}{10k\Omega}\right)\right] = 0.8251\frac{V}{V}$$

$$GAINeq = GAINopamp \cdot GAIN_{Hall} = 0.8251\frac{V}{V} \cdot 41.66e^{-3}\frac{V}{A} = 0.03437\frac{V}{A}$$

$$BIASopamp = -\frac{R_3}{R_1}V_{bias} = -0.165 \cdot 2.5V = -0.4125V$$

$$BIASeq = (BIAS_{Hall} \cdot GAINopamp) + BIASopamp = (2.5V \cdot 0.8251) - 0.4125V = 1.65V$$

$$V^{DCHV}_{OAout} = I^{DCHV}_{Sense} \cdot GAINeq + BIASeq$$

$$V_{Bits} = K_{12bits} \cdot V_{ADC} = \frac{2^{12} - 1}{3.3} \cdot V_{ADC} = 1240 \cdot V_{ADC}$$

$$G_{Ti\_HVDC\_tot} = GAINeq \cdot K_{12bits} = 42.65\frac{Bits}{A}$$

The digital transducer transfer function becomes:

$$V^{DCHV}_{OAout} = I^{DCHV}_{Sense} \cdot GAINeq + BIASeq$$

Sensing specifications are collected.

Table 10. Theoretical overall parameters of HV current sensing

Parameters	Value	Description
I_{HV_range}	$\pm 48A$	LV Voltage range
V_{ADC_range}	$0V - 3.3V$	ADC signal range
G_{Ti_HVDC}	$0.03437\frac{V}{A}$	k_{eq} conditioning circuit gain
G_{ADC_Bits}	$1240\frac{Bits}{V}$	ADC peripheral digital gain factor with 12-bit precision and VDDA=3.3V
B_{Ti_HVDC}	$1.65V$	Bias term of conditioning circuit gain
B_{ADC_Bits}	$2047Bits$	Offset term of ADC peripheral
$G_{Ti\_HVDC\_tot}$	$42.65\frac{Bits}{A}$	Overall conditioning circuit gain
$B_{Ti\_HVDC\_tot}$	$2047Bits$	Overall offset term
$invG_{Ti\_HVDC\_tot}$	$0.0234\frac{A}{Bits}$	Reciprocal overall conditioning circuit gain

The design overview is also included.

$$\begin{cases} R_1 = 10k\Omega 0.1\% \\ R_2 = 4.12k\Omega 0.1\% \\ R_3 = 1.65k\Omega 0.1\% \\ R_4 = 10k\Omega 0.1\% \end{cases} \rightarrow \begin{cases} AINopamp = \left[\left(\frac{R_4}{R_2+R_4}\right)\left(1+\frac{R_3}{R_1}\right)\right] = 0.8251\frac{V}{V} \\ Geq = Gopamp \cdot G_{Hall} = 0.8251\frac{V}{V} \cdot 41.66e^{-3}\frac{V}{A} = 0.03437\frac{V}{A} \\ 7 \\ \boldsymbol{G_{Tv}} = GAINeq \cdot K_{12bits} = 42.65\frac{Bits}{A} \end{cases}$$

5.2.4 LV current sensing

LV-side current measurement is obtained through an isolated Hall effect current transducer.
The equivalent circuit is shown below.

Figure 24. LV Current sensing equivalent circuit

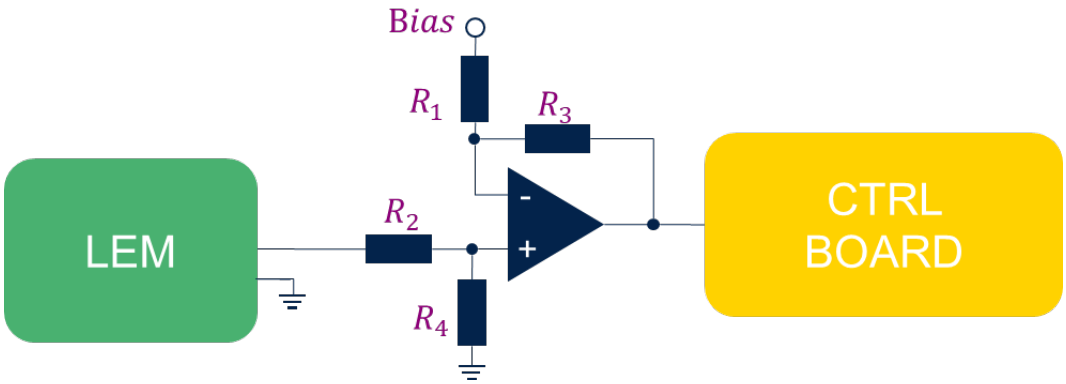
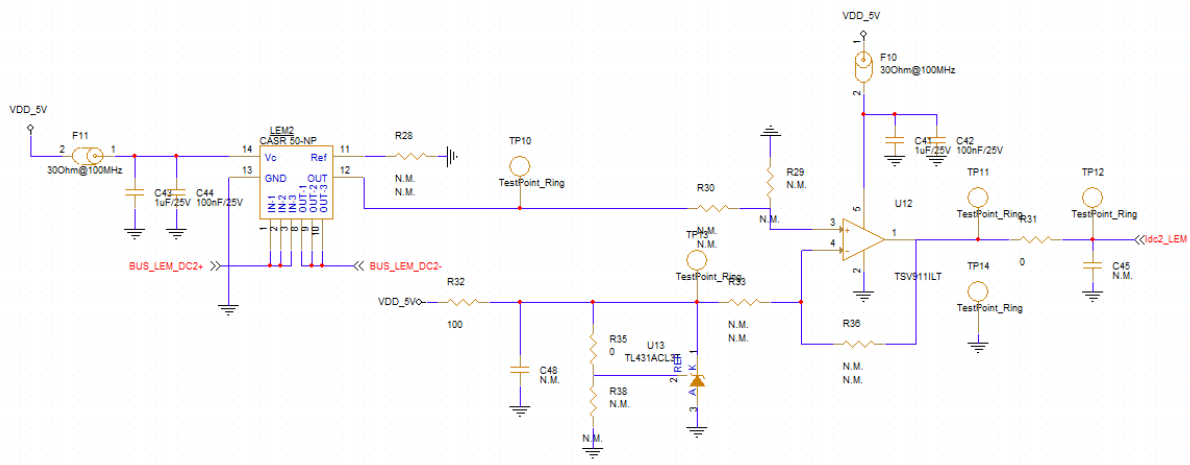


Figure 25. STDES-DABBIDIR LV current sensing circuit



To define the maximum low-voltage-side current measurement range, the maximum current range is considered.

Table 11. LV-side current

Parameters	Value	Description
I_{out_max}	$\pm 62.22A$	Max. LV-side current at $V_{in\_min} = 450V$ and $Pin\_max = \pm 28kW$

The low voltage maximum current range is considered with +30% margin.

$$I_{SenseMax}^{DCLV} = I_{Max}^{DCLV} + 15\%V_{Max}^{DCLV} = \pm 62.22\text{A}*1.3 = \pm 80.88 \cong \pm 82A$$

This value is checked against the sensor limitation.

$$I_{PM}^{CASR50NP} > I_{SenseMax}^{DCHV} \rightarrow \pm 150A > \pm 82A$$

The internal voltage reference of Hall effect sensor is used. According to this, the sensor output voltage is shifted by Vref=2.5V.
The equivalent transfer function is given.

$$BIAS_{Hall} = 2.5V$$

$$GAIN_{Hall} = \frac{0.625}{IPN_{CASR15NP}} = \frac{0.625}{50} = 12.5e^{-3}\frac{V}{A}$$

$$V_{LEM_{out}}^{LV} = BIAS_{Hall} + GAIN_{Hall} I_{SenseMax}^{DCLV} = \left(12.5e^{-3}\frac{V}{A} \cdot \pm 82A\right) + 2.5V = \begin{cases} 3.525V \\ 1.475V \end{cases}$$

To adapt the sensor output voltage to ADC range, op amp conditioning is required.

Table 12. Parameters for LV-side op amp conditioning

Parameter	Value	Description
I_{HV_range}	$\pm 82A$	HV side Current measurement range required
$V_{LEM_{out}\_range}^{HV}$	$1.475V to 3.525V$	Op amp input voltage range/output voltage range of hall sensor
$V_{OA\_out\_range}$	0-3.3 V	Maximum value of the voltage range of the microcontroller ADC

According to the input and output values, the voltage gain and offset for signal conditioning are defined.

$$V_{out} = \left[\left(\frac{R_4}{R_2 + R_4}\right)\left(1 + \frac{R_3}{R_1}\right)\right]V_{in} - \frac{R_3}{R_1}V_{bias}$$

The differential amplifier configuration is designed according to the voltage gain and bias requirements.
By setting R_1 , it is possible to calculate R_2, R_3 and R_4 with the following relationships:

$$R_1 = 13.7k\Omega$$

$$R_2 = 4.22k\Omega$$

$$R_3 = R_1 \cdot Y = 13.7k\Omega \cdot 0.9498 = 13.01k\Omega$$

$$R_4 = R_2 \cdot \left(\frac{X}{1 - X}\right) = 19.98k\Omega$$

Finally, the transfer function is obtained

$$GAINopamp = \left[\left(\frac{R_4}{R_2 + R_4}\right)\left(1 + \frac{R_3}{R_1}\right)\right] = \left[\left(\frac{19.98k\Omega}{4.22k\Omega + 19.98k\Omega}\right)\left(1 + \frac{13.01k\Omega}{13.7k\Omega}\right)\right] = 1.6096\frac{V}{V}$$

$$GAINeq = GAINopamp \cdot GAIN_{Hall} = 1.6096\frac{V}{V} \cdot 12.5e^{-3}\frac{V}{A} = 0.02012\frac{V}{A}$$

$$BIASopamp = -\frac{R_3}{R_1}V_{bias} = -0.9498 \cdot 2.5V = 2.3745V$$

$$BIASeq = (BIAS_{Hall} \cdot GAINopamp) + BIASopamp = (2.5V \cdot 1.6096) - 2.3745V = 1.6495V$$

$$V_{OAout}^{DCHV} = I_{Sense}^{DCHV} \cdot GAINeq + BIASeq$$

We now take digital conversion into account.

$$V_{Bits} = K_{12bits} \cdot V_{ADC} = \frac{2^{12} - 1}{3.3} \cdot V_{ADC} = 1240 \cdot V_{ADC}$$

$$G_{Tv\_LVDC\_tot} = GAINeq \cdot K_{12bits} = 24.9488\frac{Bits}{A}$$

The digital transducer transfer function becomes.

$$V_{OAout}^{DCHV} = I_{Sense}^{DCHV} \cdot GAINeq + BIASeq$$

The sensing specifications are collected.

Table 13. Theoretical overall parameters of HV current sensing

Parameters	Value	Description
I_{LV_range}	$\pm 82A$	LV voltage range
V_{ADC_range}	$0V - 3.3V$	ADC signal range
G_{Ti_LVDC}	$0.02012\frac{V}{A}$	k_{eq} conditioning circuit gain
G_{ADC_Bits}	$1240\frac{Bits}{V}$	ADC peripheral digital gain factor with 12-bit precision and VDDA=3.3V
B_{Ti_LVDC}	$1.65V$	Bias term of conditioning circuit gain
B_{ADC_Bits}	$2047Bits$	Offset term of ADC peripheral
$G_{Ti\_LVDC\_tot}$	$24.9488\frac{Bits}{A}$	Overall conditioning circuit gain
$B_{Ti\_LVDC\_tot}$	$2047Bits$	Overall offset term
$invG_{Ti\_LVDC\_tot}$	$0.0401\frac{A}{Bits}$	Reciprocal overall conditioning circuit gain

5.3 Magnetics design requirements

From the power converter specifications, the magnetic parameters are calculated.

Table 14. Parameters for magnetic design

Parameters		Value	Dimension	Description
Vin_nom		800	V	Nominal HV-side input voltage
Vout_nom		450	V	Nominal LV-side output voltage
Pout_nom		25	kW	Nominal power
Pout_max		28	kW	Maximum power
fsw		100	kHz	Switching frequency

5.3.1 Transformer turn ratio

In order to optimize the operation of the high frequency transformer, transformer ratio is obtained from the primary and secondary nominal voltages.

$$n = \frac{N_1}{N_2} = \frac{V_{in\_nom}}{V_{out\_nom}} = \frac{800}{450} = 1.78 \quad (19)$$

5.3.2 Total resonance inductance

To design DAB resonance inductance, nominal power is considered. According to the DAB theoretical aspects section, to manage full power operation, a single phase shift modulation technique is now considered. Ignoring the detrimental effects of efficiency parameters, the power flow equation is proposed.

$$P = P_1 = P_2 = \frac{N{*}V_{in\_nom}{*}V_{out\_nom}{*}\varphi{*}(\pi - |\varphi|)}{2{*}\pi^2{*}F_{sw}{*}L_K} \quad (20)$$

To obtain the max power transfer $\frac{\partial P}{\partial \varphi} = 0$ is imposed, then $\varphi = \frac{\pi}{2}$ allow to manage maximum power.

$$|P_{max}| = \frac{N*V_{in\_nom}*V_{out\_nom}}{8*F_{sw}*L_K} \tag{21}$$

Then:

$$L_K = \frac{n*V_{in\_nom}*V_{out\_nom}}{8*F_{sw}*P_{max}} = \frac{1{,}78*800*450}{8*100k*28k} = 28{,}6uH \tag{22}$$

The max leakage inductor current ($\varphi = \pi/2$) is:

$$|ILk_{max}| = \frac{\pi*(n*V_{out\_nom} - V_{in\_nom}) - 2*\varphi*n*V_{out\_nom}}{4*\pi*F_{sw}*L_k} =$$

$$= \frac{\pi*((1.78*450) - 800) - \left(2*\left(\frac{\pi}{2}\right)*1.78*450\right)}{4*\pi*100000*28.61*10^{-6}} = 69.90A \tag{23}$$

The max input current is:

$$I_{prim\_max} = ILk_{max} \tag{24}$$

The MAX output current is:

$$I_{sec\_max} = n*I_{prim\_max} = 124.43A \tag{25}$$

5.3.3 Transformer peak magnetic field estimation

To define the magnetic structure and core loss estimations, the magnetic field amplitude must be calculated.

Table 15. Parameters for transformer peak magnetic field estimation

Parameters	Value	Dimension	Description
N_P	800	V	Nominal LV-side output voltage
A_e	392	mm^2	Effective area of single ferrite
N_{core}	5	-	Number of stacked core elements
$A_{e,tot}$	1960(1960e-6)	$mm^2(m^2)$	Total effective area of ferrite block
f_{sw}	100	kHz	Switching frequency

$$\Delta B_{max} = \frac{1}{N_P A_e} n V_{out} \frac{1/2}{f_{sw}} =$$

$$= \frac{1}{9*1960*10^{-6}} *1.79*450 \frac{1/2}{100*10^3} = 228mT \tag{26}$$

$$B_{max} = \frac{228mT}{2} = 114mT \tag{27}$$

5.3.4 Auxiliary inductance - peak magnetic field estimation

$$\Delta B_{max} = \frac{1}{N_L A_e} V_{lk} \frac{1/2}{f_{sw}} = \frac{1}{7*1960*10^{-6}} *800 \frac{1/2}{100*10^3} = = 72.88*\Big(\left(1250*5*10^{-6}\right) + \left(350*5*10^{-6}\right) = 2*92.9mT\Big) \tag{28}$$

5.3.5 Transformer – Magnetizing inductance

The magnetizing inductance of HFT does not participate in the active power transfer, so it is designed with a magnetizing current <2% of the rated current.

$$I_m \leq 2\% I_{in} = 2\% \frac{P_{in}}{V_{in\_nom}} = 2\% \frac{29kW}{800\text{V}} = 2\% 36.84\ A \rightarrow$$

$$I_m \leq 0.7A$$

We now consider the inductance current.

$$I_{mpp} = \frac{1}{L_m}\int_0^{\frac{T_{sw}}{2}} V_{in} dt = \frac{V_{in}}{L_m}\int_0^{\frac{T_{sw}}{2}} dt = \frac{V_{in}}{L_m}\frac{T_{sw}}{2} = \frac{V_{in}}{2f_{sw}L_m}$$

$$I_{mpp} = \frac{V_{in}}{2f_{sw}L_m} \rightarrow 2I_m = \frac{V_{in}}{2f_{sw}L_m} \rightarrow I_m = \frac{V_{in}}{4f_{sw}L_m}$$

The actual magnetizing inductance can now be calculated.

$$L_m \leq \frac{V_{in}}{4f_{sw}I_m} = \frac{800}{4100kHz0.73A} \rightarrow$$

$$L_m \geq 2.739mH$$

5.3.6 Magnetics section design proposal

According to the design requirements, the actual design details are shown below.

Figure 26. Frenetic 32011-04-Design-Report (design requirements section)

1. Design Requirements

The present document provides a mergence (Transformer + Series Inductor) design based on the specifications provided by ST and summarized in Table1.

Mergence Specifications	
Parameter	**Value**
Topology	DAB
Power	25 kW
Frequency	100 kHz
Input Voltage	720 V – 880 V
Output Voltage	250 - 500 V
Output Current	56 A – 112 A
Power Loss	170 W
Turns Ratio	1.78:1
Magnetizing Inductance	Free
Series Inductance	28.6 µH
Standard	IEC 60664-1
Creepage Distance	10 mm
Clearance Distance	5.5 mm
Dimensions	Free
Cooling	Forced Air 3 m/s

Table 1. Main Specifications.

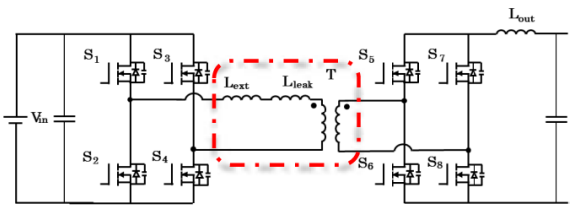


Figure 1. DAB Schematic Circuit.

Considering the specifications, Frenetic has a design based on 5 stacked cores of E80/38/20.

To maximize the performance of the converter, a sandwich interleaving arrangement is selected as the best solution to reduce AC proximity losses and to improve the coupling between the windings of the transformer.

Figure 27. Frenetic 32011-04 Transformer winding

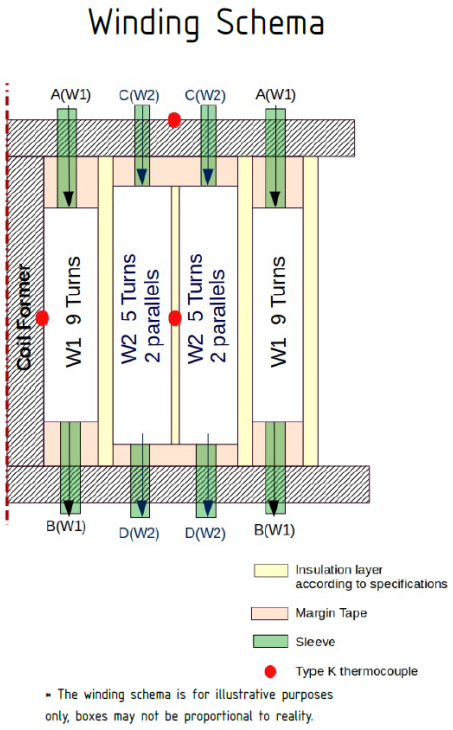
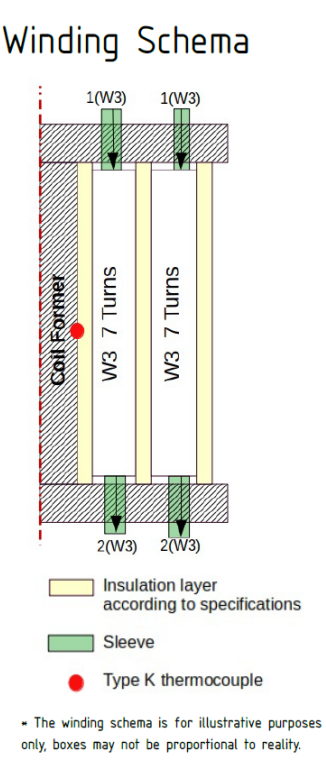
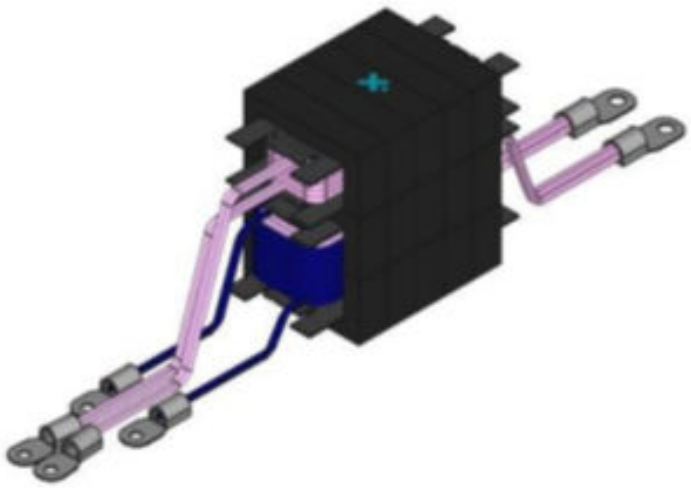


Figure 28. Frenetic 32011-04 Auxiliary inductor windings



The following figure provides a 3D view.

Figure 29. 3D image of transformer



Unique magnetic core elements were considered to reduce the volume and weight.

Figure 30. **3D model of transformer**

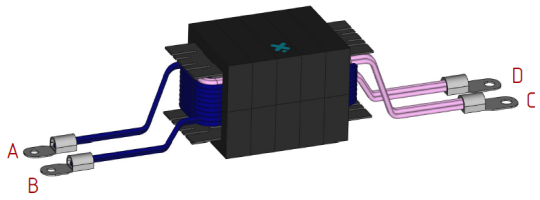
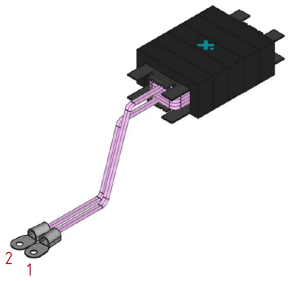


Figure 31. **3D model of auxiliary inductor**



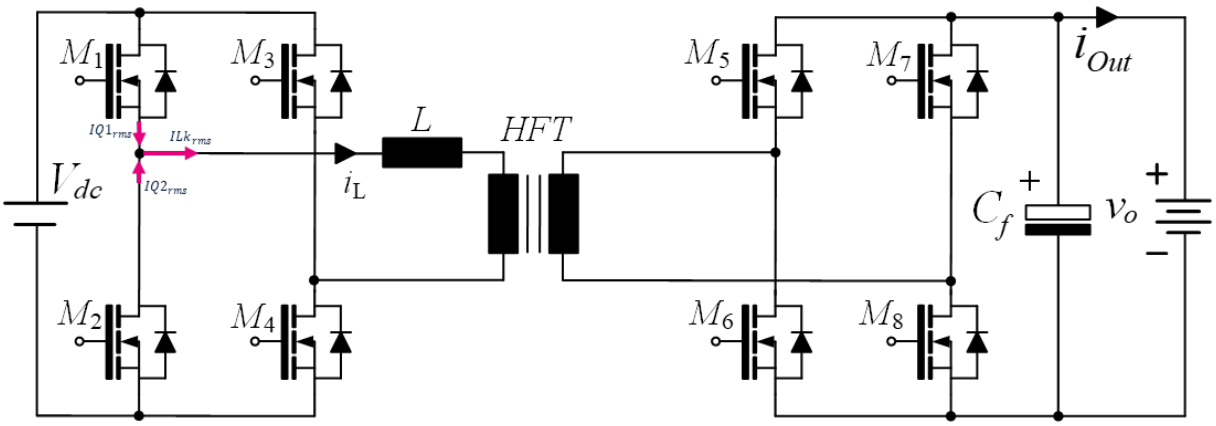
5.4 Power section

5.4.1 Power device current stress

The conduction losses are calculated using the rms switch currents $IQ1_{rms}$ and $IQ5_{rms}$ for the HV-side switches, PS_{cond}^{HV} , and the LV-side switches, PS_{cond}^{LV} , respectively.

As every switch conducts current during half of the cycle time $T_{sw} = 1/f_{sw}$ in steady state operation, the rms switch currents are easily obtained from the rms inductor current ILk_{rms}

Figure 32. **Switch RMS current equivalent circuit**



According to the selected modulation techniques, each half bridge operates at 50% duty cycle, so the rms currents are equal.

$$Hp.LegDuty50\% \rightarrow IQ1_{rms} = IQ2_{rms}$$

By LKC, the relation between inductor and switch currents can be identified.

$$ILk_{rms} = \sqrt{IQ1_{rms}{}^2 + IQ2_{rms}{}^2} = \sqrt{2IQ_{rms}{}^2} = \sqrt{2}IQ_{rms}$$

$$\downarrow$$

$$ILk_{rms} = \sqrt{2}IQ_{rms}$$

By LKC, the relation between inductor and switch currents can be identified.

$$IQ1_{rms} = IQ3_{rms} = \frac{ILk_{rms}}{\sqrt{2}} \quad IQ5_{rms} = IQ7_{rms} = \frac{ILk_{rms}/n}{\sqrt{2}}$$

$$IQ2_{rms} = IQ4_{rms} = \frac{ILk_{rms}}{\sqrt{2}} \quad IQ6_{rms} = IQ8_{rms} = \frac{ILk_{rms}/n}{\sqrt{2}}$$

5.4.2 Power switches conduction losses

High-voltage-side conduction losses are obtained from each contribution.

$$PS_{cond}^{HV} = 4*R_{DS(on)}*IQ1_{rms}{}^{2}$$

Secondary low-voltage estimation is also obtained.

$$PS_{cond}^{LV} = 4*R_{DS(on)}*IQ5_{rms}{}^{2}$$

The total switches conduction losses are obtained.

$$PS_{cond}^{TOT} = PS_{cond}^{HV} + PS_{cond}^{LV}$$

5.4.3 Power switch switching losses

The calculation of the switching losses is more demanding as they do not only depend on the selected power MOSFETs themselves. Surrounding parasitic components like PCB stray inductances may also influence the switching losses considerably.

Only power switching power losses are considered here.

Very low switching losses are obtained when ZVS/ZCS is achieved. In contrast, hard switching operation leads to excessive semiconductor losses and must be avoided when using advanced modulation methods or additional circuitry.

$$P_{SW}{}^{HV} = 4f_{sw}E_{On,Q_{HV}}(I,V) + 4f_{sw}E_{Off,Q_{HV}}(I,V)$$

$$P_{SW}{}^{LV} = 4f_{sw}E_{On,Q_{LV}}(I,V) + 4f_{sw}E_{Off,Q_{HV}}(I,V)$$

The total switches switching losses are obtained.

$$P_{SW}^{TOT} = P_{SW}{}^{HV} + P_{SW}{}^{LV}$$

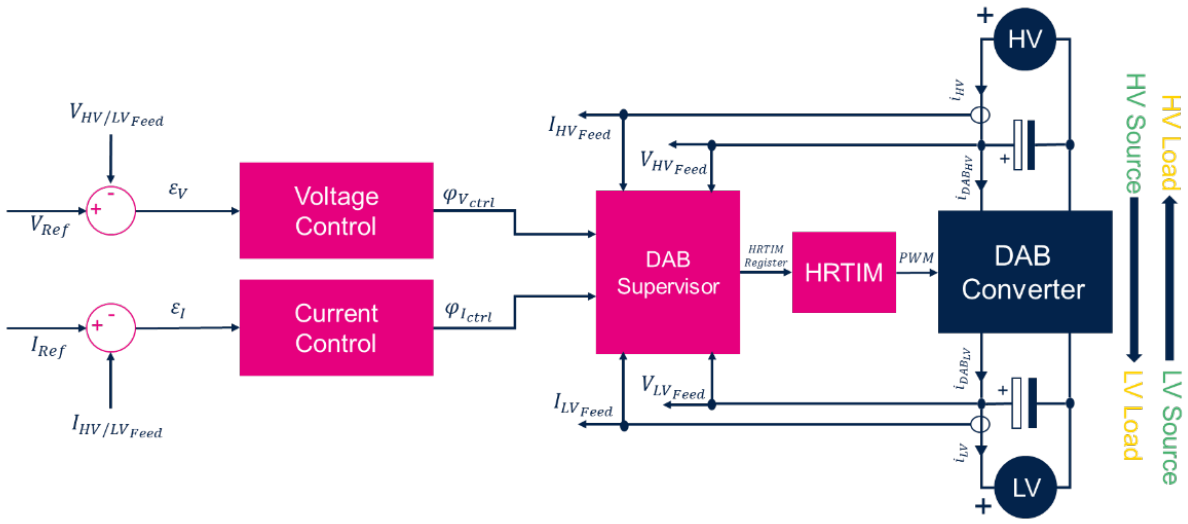
6 STDES-DABBIDIR control implementation

A typical EV charger control platform consists of two different control implementations to fulfill battery charging requirements: current control is used during the first part of charging profile, and voltage control is typically required to complete the charging profile. Both control solutions are therefore proposed for the STDES-DABBIDIR reference design control implementation.

An easy and robust proportional integrator (PI) regulator is considered to follow the reference value. Comparing references and feedback for voltages and currents, control variables are obtained to address the requirements.

According to the theoretical description of the DAB converter model, the actual control terms are represented by the phase shift, so phase shifting is obtained from each control block to manage the modulator blocks adopted to configure the high-resolution timer of the STM32G474 according to the phase shifting demand. In addition, “DAB Supervisor” blocks are proposed to manage other features such as protections, monitoring, and modulations techniques.

Figure 33. Control block diagram



6.1 Software implementation

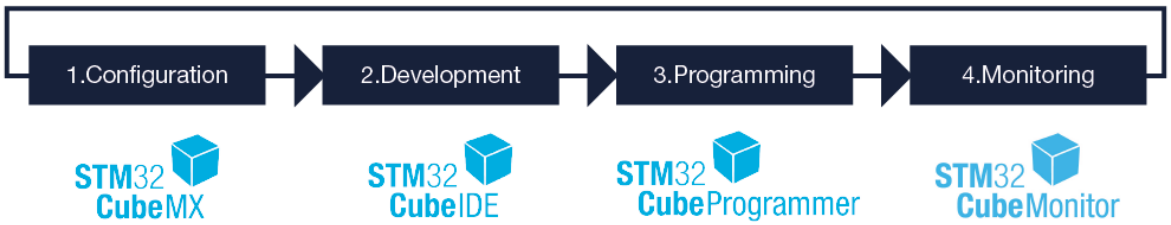
The STDES-DABBIDIR is controlled by the STM32G474RE MCU. The firmware package is based on the STM32Cube ecosystem shown in Figure 34.

Starting from STM32CUBEMX all used peripherals and pins are activated and configured according to the basic project. The application firmware is supported and tested using STM32CubeIDE IAR and KEIL development environment.

After the development, the MCU can be programmer with IDE or with STM32CubeProgrammer. To monitor and control the application, a GUI based on STM32CubeMonitor can be used.

The firmware described in this documentation development is based on STM32CubeG4 Firmware Package V1.4.0.

Figure 34. CUBE ecosystem development flow

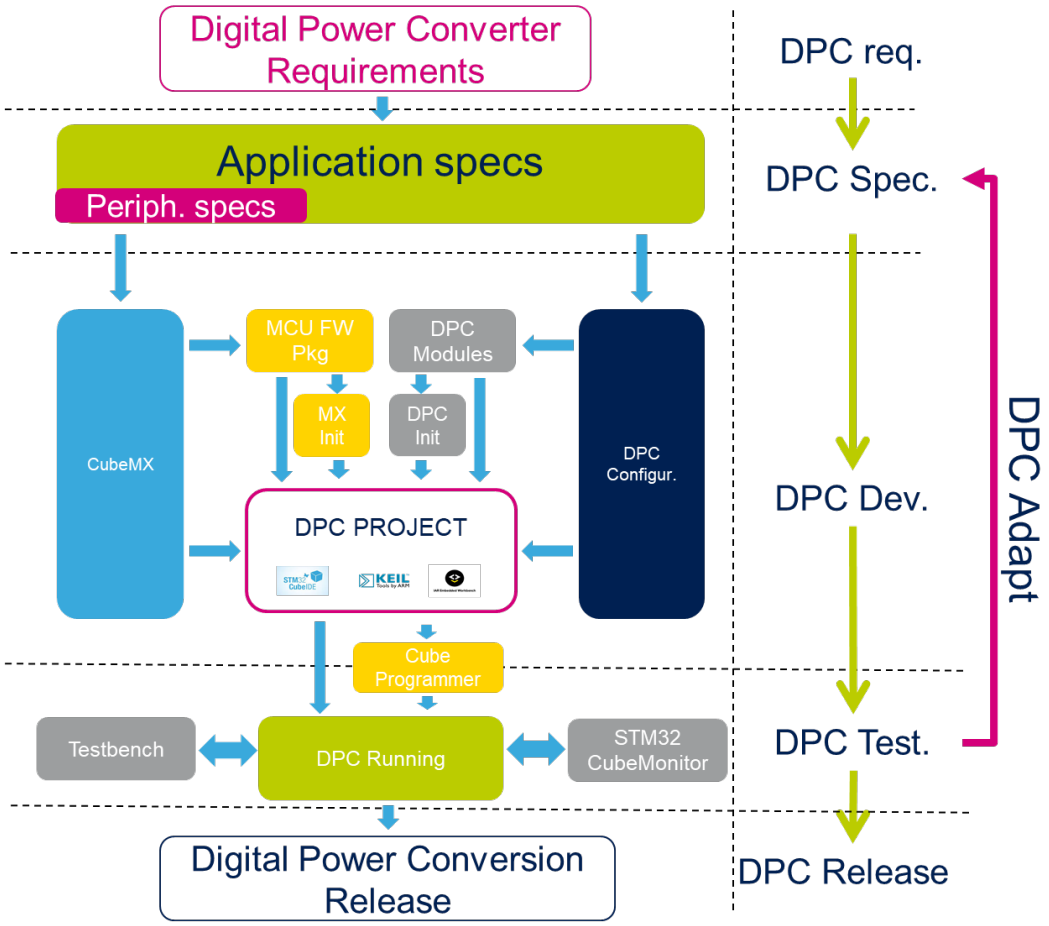


An extensive range of generic and specific firmware modules are available to support digital power conversion. Figure 35 shows the general development flow to obtain power conversion used for STDES-PFCBIDIR firmware development. This workflow allows us to start from power conversion requirements. This information is reinterpreted in application specifications that contain information linked to the MCU peripheral and DPC application configuration.

According to the previous information, a CubeMX project with appropriate “config” and “init” are provided. Then the required DPC module is included and configured.

CubeMX generated the IDE project for development. The MCU is flashed directly with IDE or using STM32CubeProgrammer. Finally, the DPC application is tested and debugged with appropriate instrumentation and STM32CubeMonitor. Digital Power converter firmware is released if compliant, and DPC is adapted.

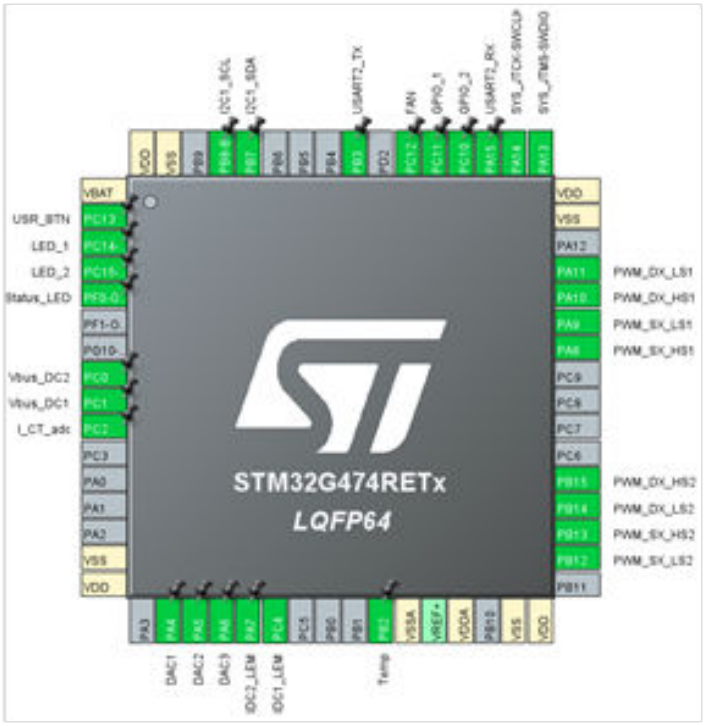
Figure 35. DPC development flow



6.2 Peripheral configuration STM32CubeMX

STM32CubeMX is a graphical tool that is used to configure STM32 microcontrollers and to generate the corresponding initialization C code for the chosen development tools. The overall pinout configuration of the STM32G474RE is shown. The STM32CubeMX configuration tool simplifies pin association and functionality to avoid any peripheral conflicts.

Figure 36. **STM32G474 MCU pinout configuration for STDES-DABBIDIR**



6.2.1 High-resolution timer

A brief representation of the high-resolution timer configuration is shown below. Accurate parameter configuration is visible in the STM32CubeMX project files.

Figure 37. **Generic phase shift - HRTIM block diagram**

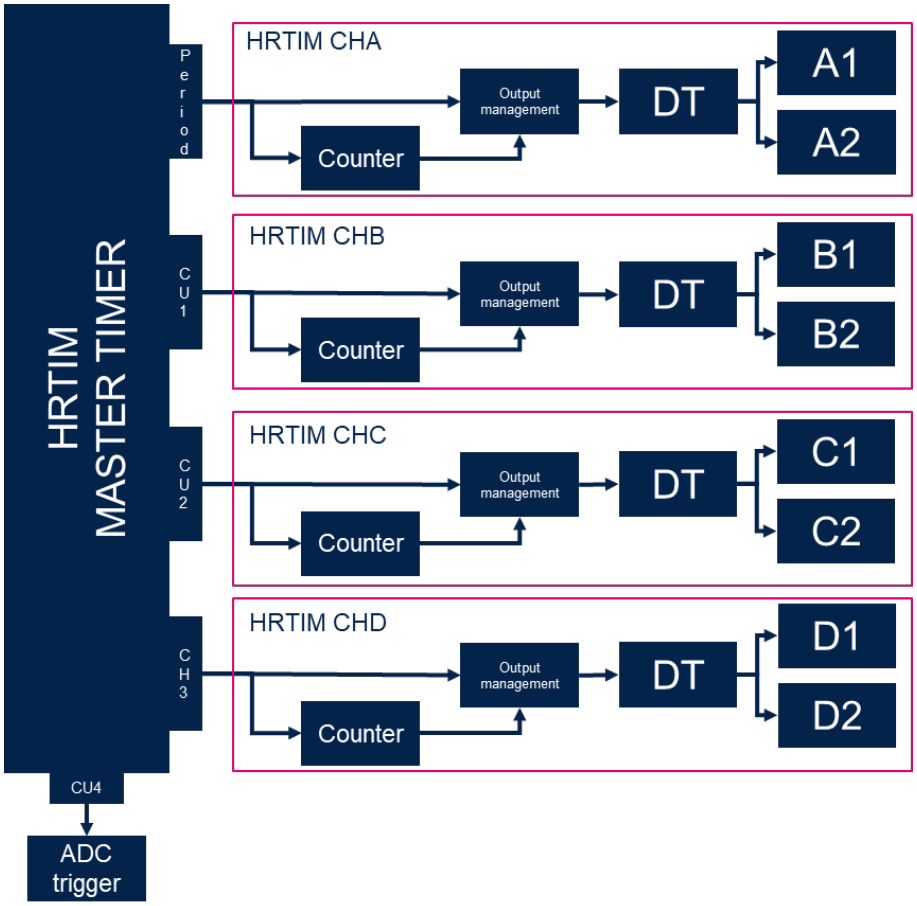
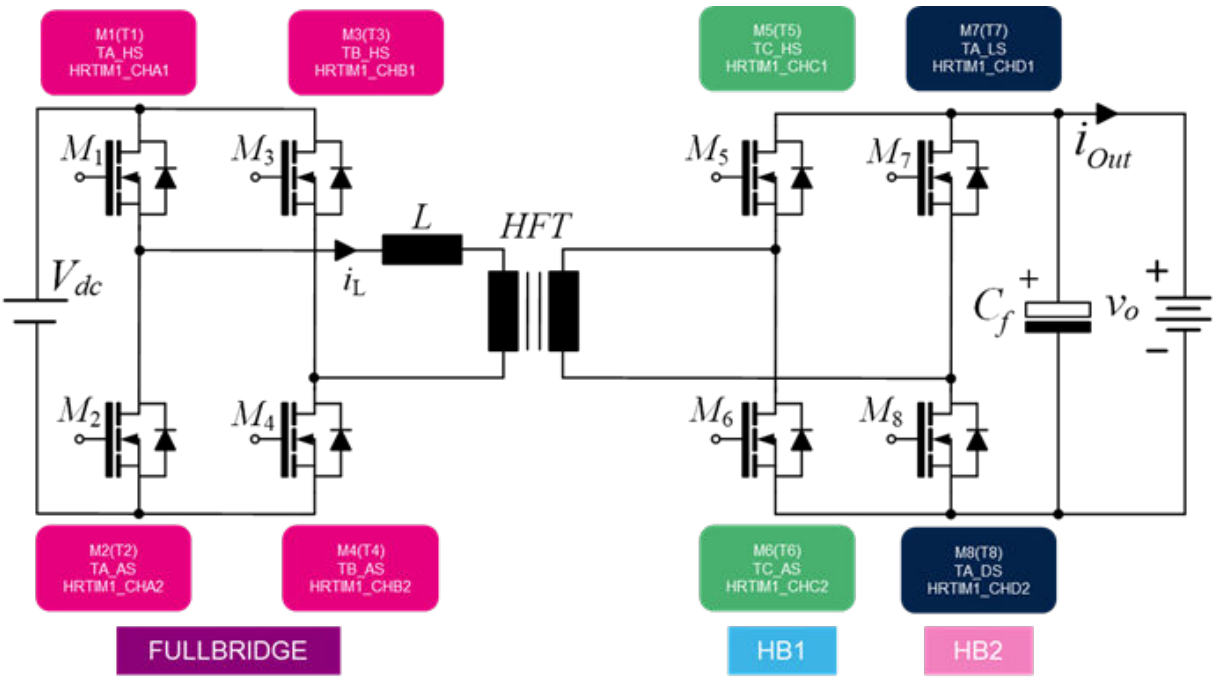
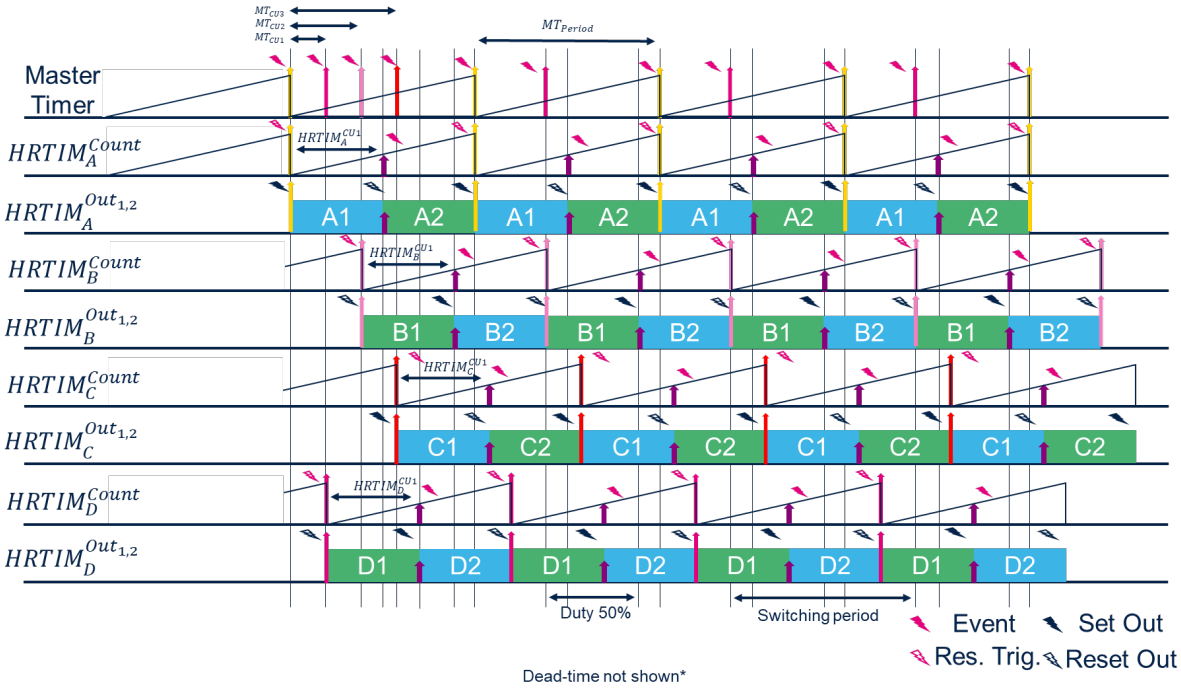


Figure 38. **HRTIM pin assignment**



An example of the switching pattern managed according to HRTIM peripheral of the STM32G474 is shown below, with primary and secondary legs of the DAB topology synchronized to the phase shifting requirements of the Master Timer Compare Unit. Dead time insertion and nominal 50% duty cycle of each leg is also managed through hardware configuration of the A-B-C-D channels of the HRTIM.

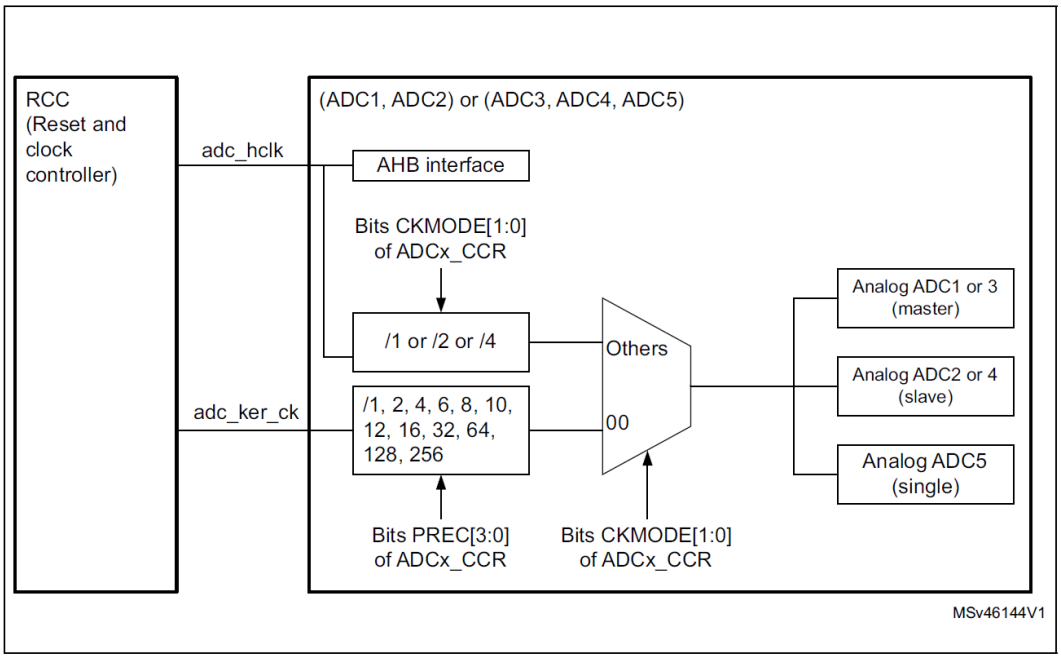
Figure 39. HRTIM modulation pattern



6.2.2 ADC configuration and triggering

Additional details about the peripheral are also proposed for the ADC.

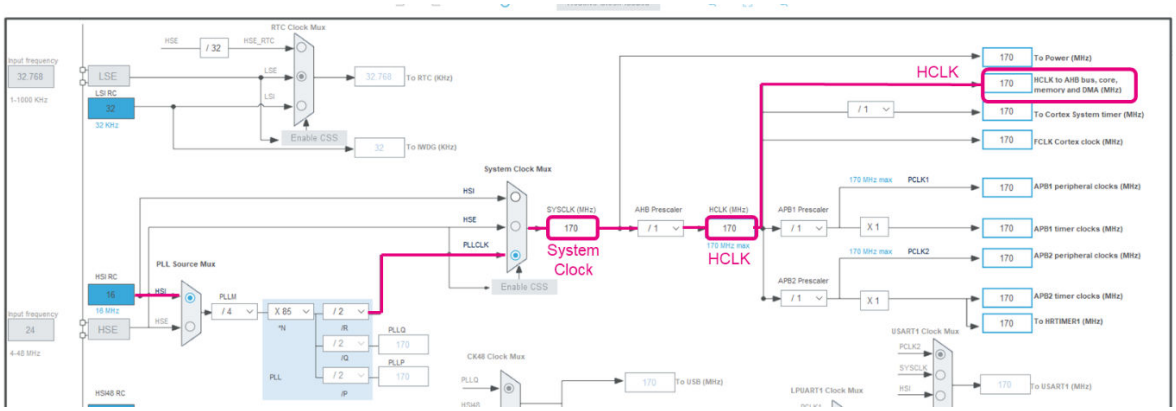
Figure 40. ADC clock scheme



6.2.2.1 *ADC timing - actual configuration*

We use STM32CubeMX to select the clock sources for the ADC peripherals.

Figure 41. ADC clock source selection (STM32CubeMX)



$$f_{sysclk} = 170MHz$$

$$f_{hclk} = \frac{f_{sysclk}}{AHB_{psc}} = \frac{170MHz}{1} = 170MHz \quad (29)$$

ADC 1 and ADC2 are requested for this application. Both are configured as shown below.

Figure 42. CubeMX ADC Settings

ADC_Settings	
Clock Prescaler	Synchronous clock mode divided by 4
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Gain Compensation	0
Scan Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Low Power Auto Wait	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Enabled
Overrun behaviour	Overrun data preserved

Clock Prescaler

Configuration related to CKMODE[1:0] and PRESC[3:0]

Table 16. Clock Prescaler settings

Register	Value
PRESC[3:0]	0010 (input ADC clock divided by 4)
CKMODE[1:0]: ADC clock mode	11: adc_hclk/4 (Synchronous clock mode)

$$f_{adc_{clk}} = \frac{f_{hclk}}{PRESC[3:0]} = \frac{170MHz}{4} = 42.5MHz$$

$$T_{adc_{clk}} = \frac{1}{f_{adc_{clk}}} = \frac{1}{42.5MHz} = 23{,}529nSec \quad (30)$$

Resolution

RES[1:0]= 12 -> 12.5 ADC clock cycles is considered for each channel and the ADC peripherals.

$$T_{sar} = RES_{clkcycle} T_{adc\_clk} = 12.5 \frac{1}{42.5MHz} = 294{,}1\text{nSec}$$

6.2.2.2 *Trigger and sampling*

Considering the “clean” area available in single phase shift modulation (SPS), the total conversion time must be lower than a quarter of the switching period.

Figure 43. SPS ADC sampling requirement

$$t_{adc_{trigger}} > \frac{1/f_{PWM}}{4} 7{,}5uSec \quad (31)$$

$$t_{adc_{clean}} < \frac{1/f_{PWM}}{4} = 2{,}5uSec \quad (32)$$

According to the PWM frequency and modulation technique, a specific trigger time is selected.

Figure 44. STM32CubeMX ADC1 Regular conversion configuration

ADC_Regular_ConversionMode	
Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	High Resolution Timer Trigger 1 event
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1

Figure 45. **STM32CubeMX ADC2 regular conversion configuration**

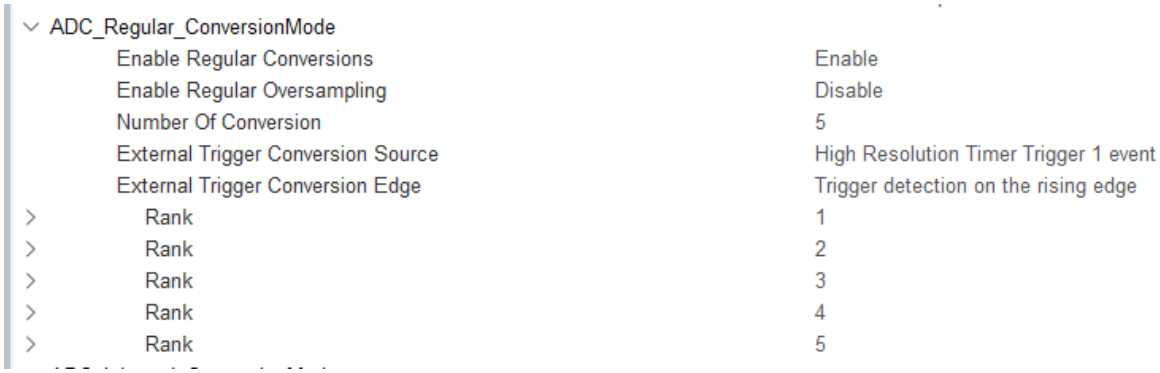


Figure 46. **HRTIM ADC trigger CubeMX configuration**

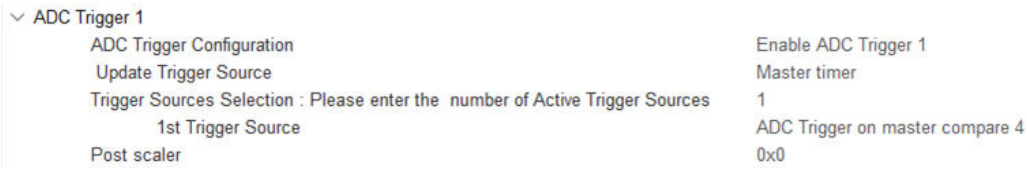


Figure 47. **HRTIM compare unit enabled for ADC triggering**

To guarantee the proposed $t_{adc_{trigger}}$ timed conversion request, an external trigger conversion is configured.

Table 17. **ADC and timer configuration**

	ADC Configuration					HRTIM Configuration		
ADC	N° of conversion	Regular Conversion	Regular Oversampling	Ext Trig. Source	Ext Trig. Edge	Update Trigger Source	Trigger Source Selection	Trigger Source
ADC1	1	Enable	Disable	HRTIM Trigger1 event	Rising	Master Timer	1	Master Compare 4
ADC2	5	Enable	Disable	HRTIM Trigger1 event	Rising	Master Timer	1	Master Compare 4

The converter signals are connected to the ADCs according to the following table.

Table 18. **Converter signal connections**

Phase	PORT	ADC	CH	DMA	RANK	FUNCTION
VDAB1	PC1	ADC2	CH7	DMA1CH4	4	ADC2 IN7
IDAB1	PC4	ADC2	CH5	DMA1CH4	2	ADC2 IN4
VDAB2	PC0	ADC2	CH6	DMA1CH4	3	ADC2 IN6
IDAB2	PA7	ADC2	CH4	DMA1CH4	1	ADC2 IN4
Ilk	PC2	ADC1	CH8	DMA1CH3	1	ADC1 IN8

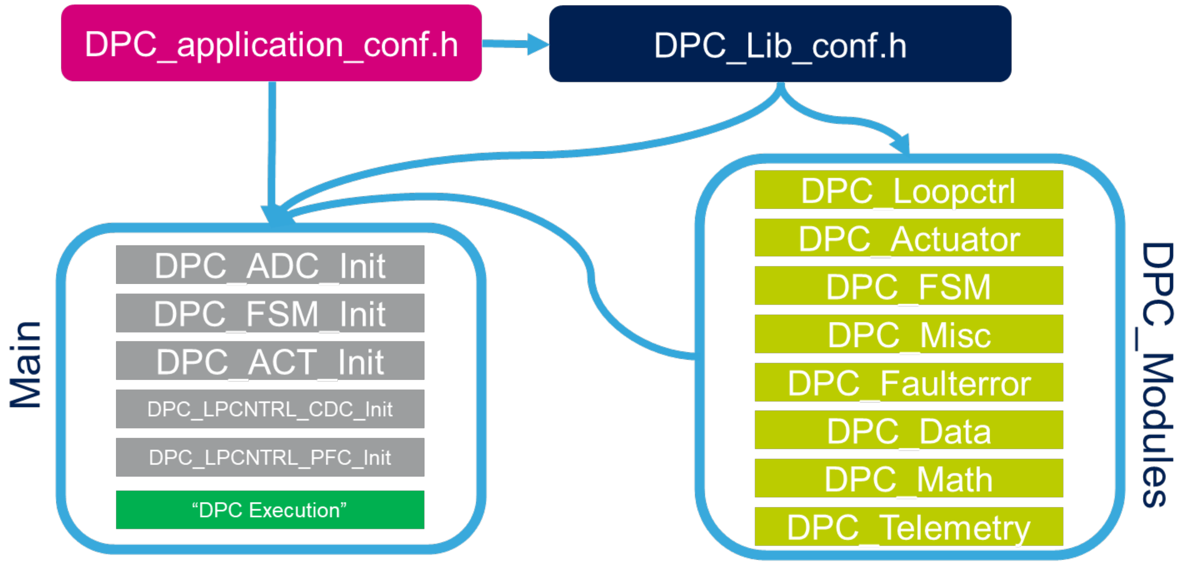
Phase	PORT	ADC	CH	DMA	RANK	FUNCTION
TEMP	PB2	ADC2	CH12	DMA1CH4	5	ADC2 IN12
Temp-INT	INT	ADC1	TEMP	DMA1CH3	8	ADC1-TEMP

6.2.3 Configuration files

STDES-DABBIDIR power converter configuration is based on two main configuration files, shown in the figure below:

- “DPC_application_conf.h” contains the application-specific DEFINE (i.e., ADC gain factor PI regulator gain, FSM configuration, control reference value, etc.
- “DPC_Lib_conf.h” contains the configuration parameters associated with MCU peripheral configuration

Figure 48. STDES-DABBIDIR configuration file



After the “MX” initialization function, the DPC initialization function are called to configure each specific application struct, as shown in the figure below.

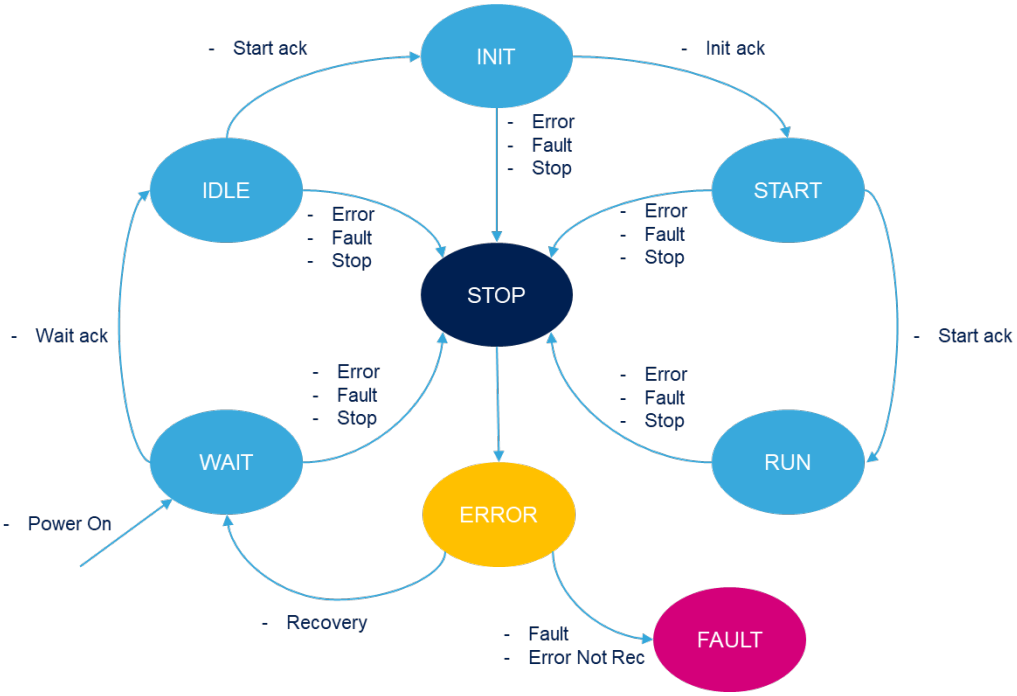
Figure 49. Application Init functions

```
/**
* @}
*/
void DPC_APPLICATION_Init(void)
{
  /* PACK CODE BEGIN 2 */

  DPC_Display_Init();
  DPC_MISC_OB_Init();
  DPC_DAB_ADC_Init(&DAB.DPC_ADC_Conf,G_VDC1,B_VDC1,G_IDC1,B_IDC1,G_VDC2,B_VDC2,G_IDC2,B_IDC2);    ///
  DAB.StartUpCheck=StartUpCheck_INIT;    ///
  DAB.pDAB_CTRL.DPC_DTG_DAB1_bin=DPC_ACT_Calc_DeadTime(DPC_DT_DAB1);    /// Find the op
  DAB.pDAB_CTRL.DPC_DTG_DAB2_bin=DPC_ACT_Calc_DeadTime(DPC_DT_DAB2);    /// Find the op
  DPC_ACT_DAB_Conf_DeadTime(DAB.pDAB_CTRL.DPC_DTG_DAB1_bin,DAB.pDAB_CTRL.DPC_DTG_DAB2_bin);    /// Set
  DPC_MISC_APPL_Timer_Init(APPL_Tim1, RefreshTime_DESIDERED);    /// Function us
  DPC_MISC_APPL_Timer_Init(APPL_Tim2, RefreshTime_TO_DESIDERED);    /// Function us
  DPC_MISC_APPL_Timer_Init(APPL_Tim3, RefreshTime2_DESIDERED);    /// Function us
  DPC_MISC_APPL_Timer_Init(APPL_Tim5, RefreshTime3_DESIDERED);    /// Function us
  DPC_MISC_Analog_Start();
  DPC_ACT_Init(DPC_BURST_PWM_FREQ,PWM_FREQ,DPC_PWM_INIT,&DAB.tDPC_PWM);
  DPC_PI_Init(&DAB.pDAB_CTRL.VOLTAGECTRL.pPI_VDC_CTRL,DPC_VCTRL_KP,DPC_VCTRL_KI,DPC_PI_VDC_TS,DPC_VCTRL_PI_sat_up,DPC_VCTRL_PI_sat_down,DPC_VCTRL_PI_SAT_EN,DPC_VCTRL_PI_AW_EN,DPC_VCTRL_PI_AWTG,DPC_PI_VDC_RES_VAL);
  DPC_PI_Init(&DAB.pDAB_CTRL.CURRENTCTRL.pPI_IDC_CTRL,DPC_ICTRL_KP,DPC_ICTRL_KI,DPC_PI_IDC_TS,DPC_ICTRL_PI_sat_up,DPC_ICTRL_PI_sat_down,DPC_ICTRL_PI_SAT_EN,DPC_ICTRL_PI_AW_EN,DPC_ICTRL_PI_AWTG,DPC_PI_IDC_RES_VAL);
  DPC_MISC_DCSource_Init(&DAB.DC_Source_Limit,DPC_VDC_HV_OVP,DPC_VDCHV_UV,DPC_VDCHV_UVLO,DPC_VDCHV_MIN,DPC_IDCHV_OCP,&DAB.DPC_ADC_Conf);    ///
  DPC_MISC_DAB_DCLoad_Init(&DAB.DC_Load_Limit,DPC_VDC_LV_OVP,DPC_NO_LOAD_CURR,DPC_LOW_LOAD_CURR,DPC_IDCLV_OC,&DAB.DPC_ADC_Conf);    /// INIT DC
  DPC_LPCNTRL_DAB_Init(&DAB.pDAB_CTRL,DPC_CTRL_INIT,DPC_DAB_VDC,DPC_DAB_IDC,&DAB.DPC_ADC_Conf);    /// INIT Inrush
  DPC_FSM_Init(&DAB.PC_State,DPC_PC_State_Init,&DAB.FSM_Run_State,DPC_FSM_RUN_INIT);    /// Finite stat
  DPC_LCT_Inrush_Init(&DAB.INRUSH_CTRL,INRUSH_VREF_V,INRUSH_DELTA_MAX,INRUSH_DELTA_MIN,DPC_INRUSH_NO_LOAD_CURR,DPC_INRS_EN,&DAB.DPC_ADC_Conf);    ///
  DPC_LCT_BurstCtrl_Init(&DAB.BURST_CTRL,DPC_BURST_EN,RUN_BURST_VREF_V,RUN_BURST_VHIST,DPC_NO_LOAD_CURR,DPC_LOW_LOAD_CURR,DPC_BURST_DUTY_NL,DPC_BURST_DUTY_LL,&DAB.DPC_ADC_Conf);    /// INIT BURST
  DPC_DAC_Init(&DAB.DAC_CH,DAC_CH1_INIT,DAC_CH2_INIT,DAC_CH3_INIT,DAC_G_CH1_Init,DAC_G_CH2_Init,DAC_G_CH3_Init,DAC_B_CH1_Init,DAC_B_CH2_Init,DAC_B_CH3_Init);    /// DAC debuggi
  DPC_FSM_State_Init(DPC_FSM_STATE_INIT);    /// Finite stat
  DPC_TO_Init();    /// Timeout mod
  DPC_ADC_TrigSet(TRIGGER_TIME_EVENT);    ///
  DPC_MISC_Appl_Timer_Start();    /// ###########  WARNING MUST BE THE LAST operation to prevent jump by interrupt  ##########

  /* PACK CODE END 2 */

}
```

6.2.4 Finite state machine

The STDES-DABBIDIR control supervisor is developed by a passthrough implementation of the finite state machine with event and status shown in the following figure.

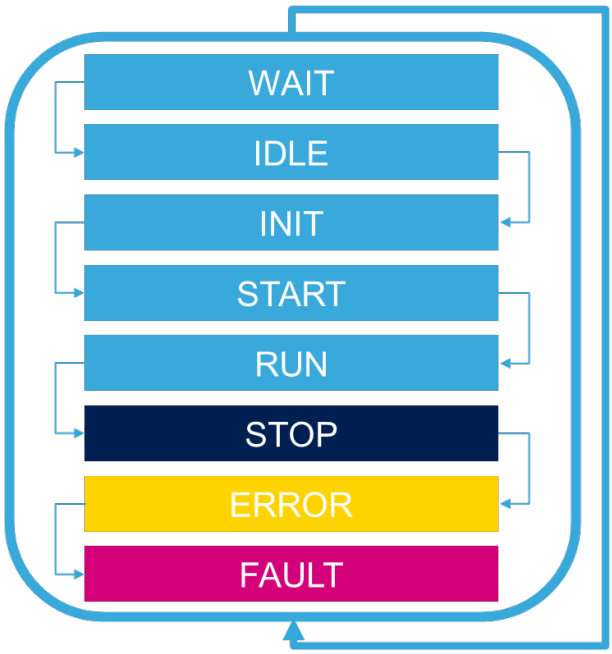
Figure 50. Finite state machine bubble representation



The FSM firmware modules provide a specific “weak” function for any state. The weak function provides a simple change of state to the following state. If any state is not used, the FSM main function allows a bypass to move forward automatically (Figure 51).

The STDES-DABBIDIR provides a typical FSM execution to obtain a typical startup procedure of the converter. The nominal operation is managed with the FSM and the ERROR and FAULT states are supported.

Figure 51. STDES-DABBIDIR FSM application service execution



7 How to manage the STDES-DABBIDIR reference design

This section describes how to configure and evaluate the power platform. Preliminary information regarding the typical test bench and testing procedures are provided in the following sections.

7.1 System setup requirement

To perform functions of the STDES-DABBIDIR, the following equipment is needed:

- Programmable DC source
- DC electronic load
- Power analyzer
- Digital oscilloscope

In addition to the hardware equipment, additional software tools are suggested to fully evaluate the reference environment.

A fully integrated design environment like STM32CUBEIDE allows evaluation and management of software source code and STM32G474 peripheral configuration. In addition, thanks to STM32CubeMX, support for other IDEs such as EWARM and AMR Keil is available as well.

Table 19. Software compatibility

Tools	Version
STM32CubeMX	v.6.6 or above
STM32CubeIDE	v.1.8 or above
IAR EWARM	v.9.20.2 or above
Arm Keil	v5.36 or above

7.2 Safety precautions and protective equipment

Important: The STDES-DABBIDIR evaluation board is designed for demonstration purposes only and is not intended for domestic or industrial installations.

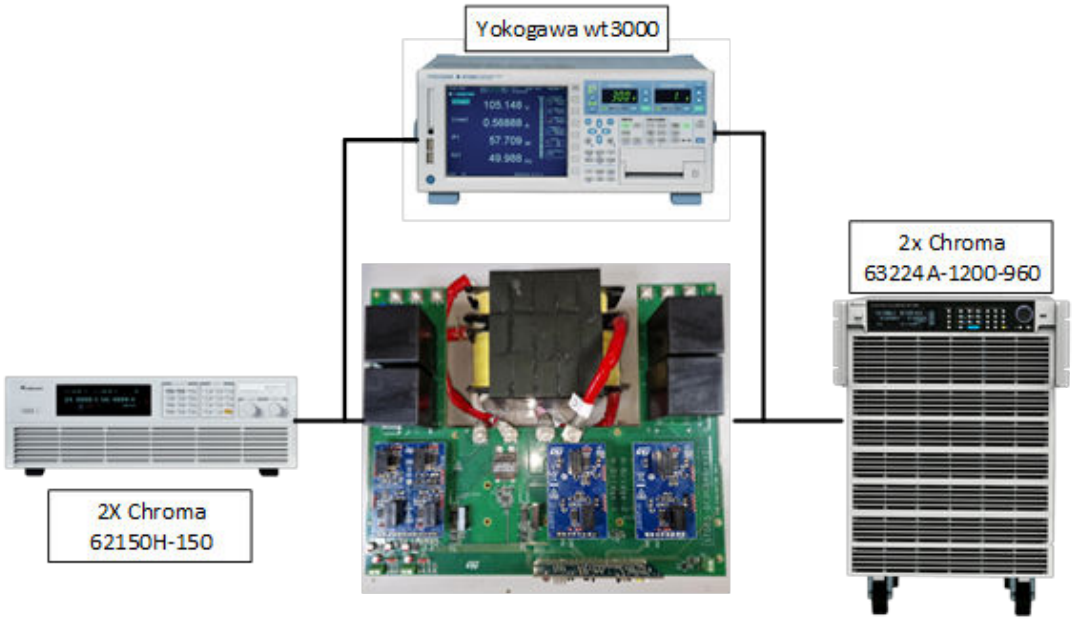
Danger: *The high voltage levels used to operate the STDES-DABBIDIR evaluation board may provoke a serious electrical shock. This evaluation board must be used in a suitable laboratory by qualified personnel only, familiar with the installation, use, and maintenance of power electrical systems. During operation, do not touch the board as some of its components could reach very high temperatures.*

7.3 How to use the STDES-DABBIDIR

STDES-DABBIDIR is a high-power, high-voltage application and an appropriate testbench is required for safety operation.

A typical configuration of test bench is proposed here.

Figure 52. **Power equipment connection example**



7.4 How to connect the STDES-DABBIDIR

Before testing the reference design, the following actions and checks must be considered.

Step 1. Connect or verify the proper connection of HF transformer as described into the specific section.

Step 2. Insert or verify the STDES-DABBIDIRDF into the driving board connectors located into left side.

Step 3. Insert or verify the two STDES-DABBIDIRDH into the driving board connectors located into right side.

Step 4. Insert or verify the STDES-PFCBIDIR into the control board connector located on the bottom-right side.

Step 5. Connect 12V external power supply into the “12V” connector located in the bottom-left corner.

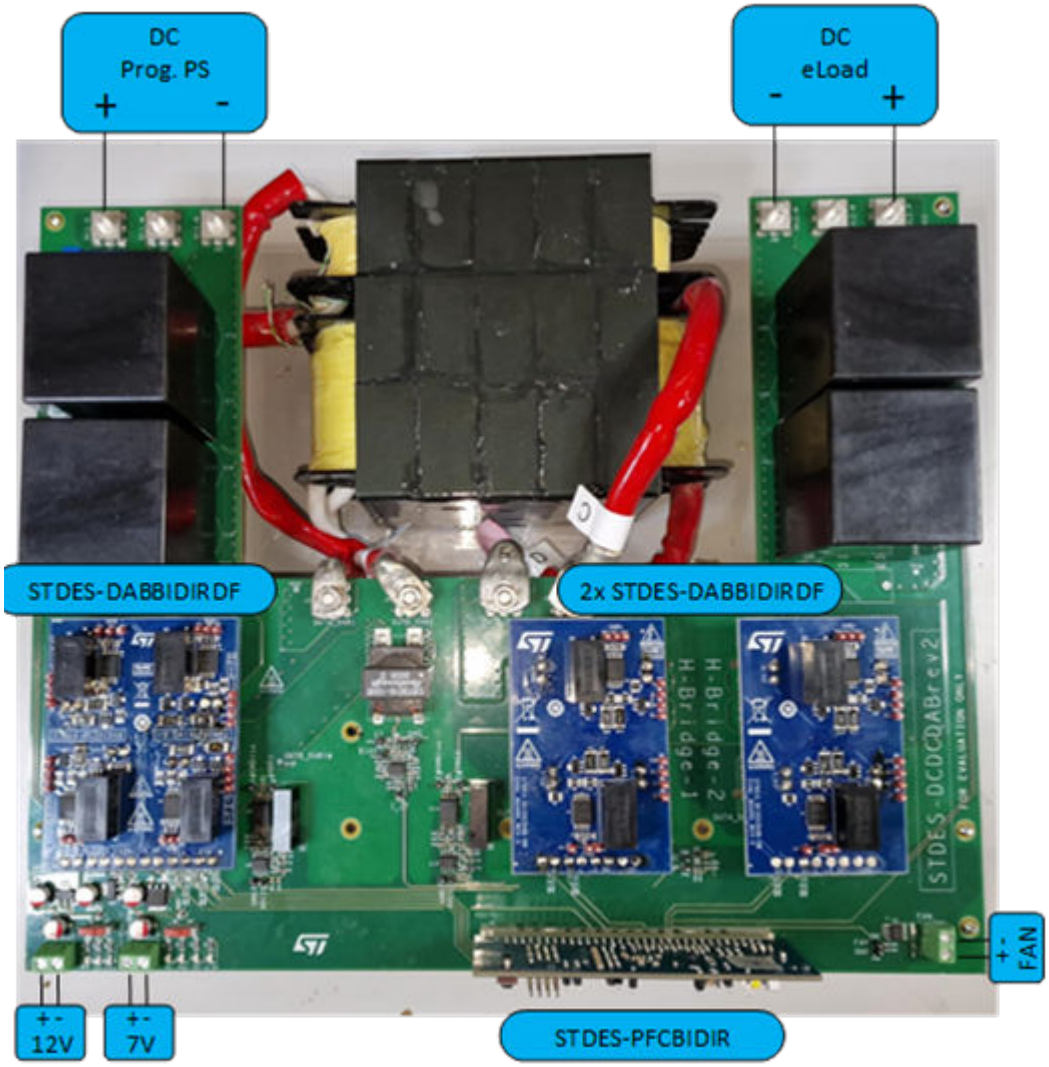
Step 6. Connect 7V external power supply into the “7V” connector located in the bottom-left corner.

Step 7. Connect the Programmable DC power supply in the top-left corner connectors. Polarity must be checked according to the image description.

Step 8. Connect the Programmable DC e-Load in the top-right corner connectors. Polarity must be checked according to the image description.

The control card based on STM32G474 MCU is directly powered by the main board. The required MCU 3.3V is provided by internal LDO.

Figure 53. **Connecting the STDES-DABBIDIR**



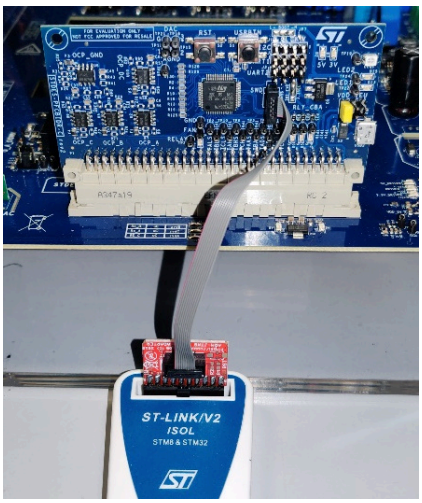
7.5 How to set up the STDES-DABBIDIR

The MCU could be programmed, monitored, and debugged using different SW/HW tools. ST-Link V2/isol and a typical 20 to10-pin JTAG adapter is used to connect the platform with a PC.

The following procedure shows how to flash and debug the reference platform from a generic configuration; referr to dedicated sections to configure the actual configuration for specific tests.

Figure 54. **ST-LINK/V2 ISOL + adapter**

Figure 55. **ST-LINK/V2 ISOL connection**



Step 1. Install and configure the preferred IDEs

Step 2. Apply 7V and 12V external supply voltage

Step 3. Connect STlink hardware debugger

Step 4. Open project according to IDE selection

Step 5. The “main.c” file is in project/Application/User path.

Step 6. “Download and debug” button performs programming procedure and start-up the debugging connection.

Step 7. “Run button” to start the code execution.

Step 8.

Figure 56. **IAR EWARM program procedure**

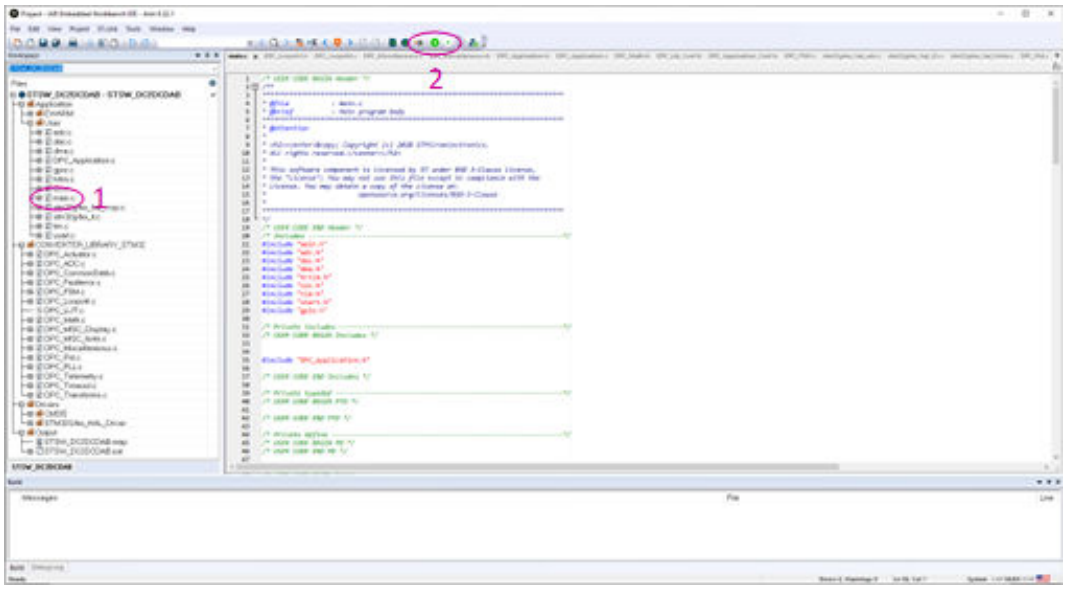
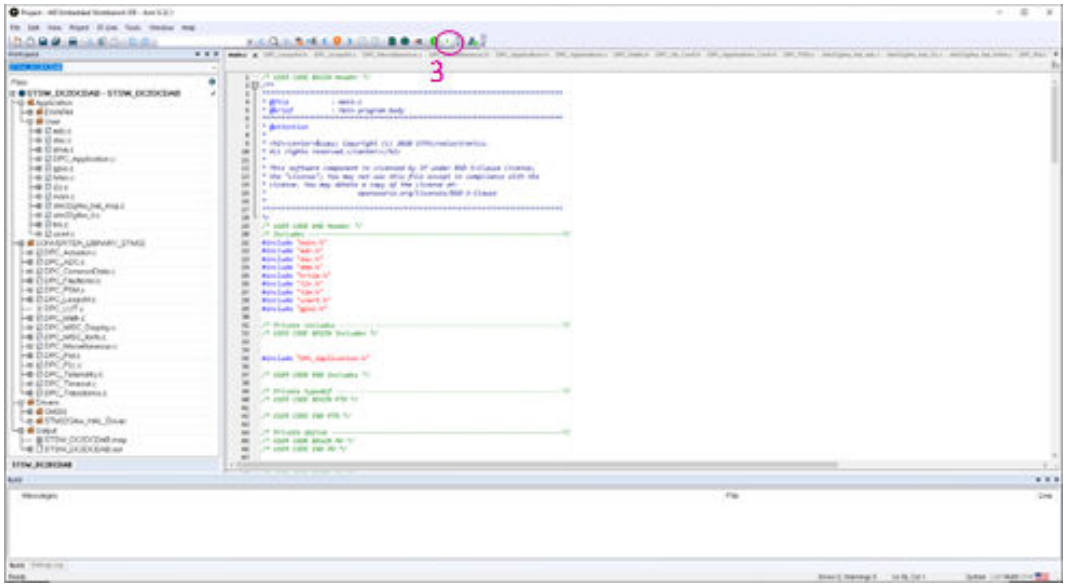


Figure 57. **IAR EWARM debug procedure**



Example 1 :

Several parameters can be adapted in order to evaluate and customize the application operating condition. The main parameters are depicted in the next table showing the default configuration proposed in the source code firmware example.

Some examples are proposed in this chapter, and specific configuration of these parameters are proposed to emulate the same behavior described for each.

Table 20. **Control section firmware configuration defines**

Parameters	Value type	Min	Default	Max	Unit	Comments
DPC_CTRL_INIT	DAB_OPEN_LOOP DAB_CURRENT_LOOP DAB_VOLTAGE_LOOP	-	DAB_OPEN_LOOP	-	enum	
DPC_PWM_INIT	PWM_Armed PWM_Safe	400			enum	
StartUpCheck_INIT	StartUpCheck_Disabled StartUpCheck_Enabled		StartUpCheck_Disabled		enum	Startup management
DPC_INRS_EN	SET RESET		RESET			
DPC_BURST_EN	SET RESET		RESET			
DPC_DAB_VDC_OUT	float	0	50	880	V	Target DC output voltage
DPC_DAB_IDC_OUT	float	0	1	60	A	Target DC output current

In addition to the operating mode parameters, a dedicated parameter section is proposed for the protection feature configuration. The default configuration is also given.

Table 21. Hardware protection firmware configuration defines

Parameters	Value type	Min	Default	Max	Unit
DPC_VDCHV_OVP	float	-	900	-	V
DPC_VDCHV_UV	float	-	40	-	V
DPC_VDCHV_UVLO	float	-	30	-	V
DPC_VDCHV_MIN	float	-	20	-	V
DPC_IDCHV_OCP	float	-	50	-	A
DPC_IDCLV_OCP	float	-	550	-	A
DPC_VDCLV_OVP	float	-	100	-	V

The STSW-DABBIDIR source code firmware package represents the control section of STDES-DABBIDIR. By using hardware section configuration of the FW, different hardware configuration proposed by the CTMs can also be supported. The main parameters such as switching frequency, dead time, sensing parameters, and magnetics section can be customized.

Table 22. Hardware parameters firmware configuration defines

Parameters	Value type	Min	Default	Max	Unit	Comments
TRAFO_TURN_RATIO	float	-	1.78	-	N1/N2	Transformer turn ratio
INDUCTANCE	float	-	28e-6	-		Auxiliary inductance
PWM_FREQ	Uint16_t	-	100000	-		Switching Frequency of converter expressed in [Hz]
DPC_DT_DAB1	float	-	0.4e-6	-		Dead Time [Expressed in sec]
DPC_DT_DAB2	float	-	0.4e-6	-		Dead Time [Expressed in sec]
G_VDC1	float	-	3.901	-		Gain terms of the DC input voltage sensing
B_VDC1	float	-	0	-		Bias terms of the DC input voltage sensing
G_IDC1	float	-	42.67	-		Gain terms of the DC input current sensing
B_IDC1	float	-	2048	-		Bias terms of the DC input current sensing
G_VDC2	float	-	6.296	-		Gain terms of the DC output voltage sensing
B_VDC2	float	-	0	-		Bias terms of the DC output voltage sensing
G_IDC2	float	-	24.948	-		Gain terms of the DC output current sensing
B_IDC2	float	-	2048	-		Bias terms of the DC output current sensing

7.6 How to operate the STDES-DABBIDIR

This section provides examples of operating modes. Several setups are proposed to help evaluate and become familiar with the various features of the reference design.

7.6.1 Mode 1 – open loop, driving check

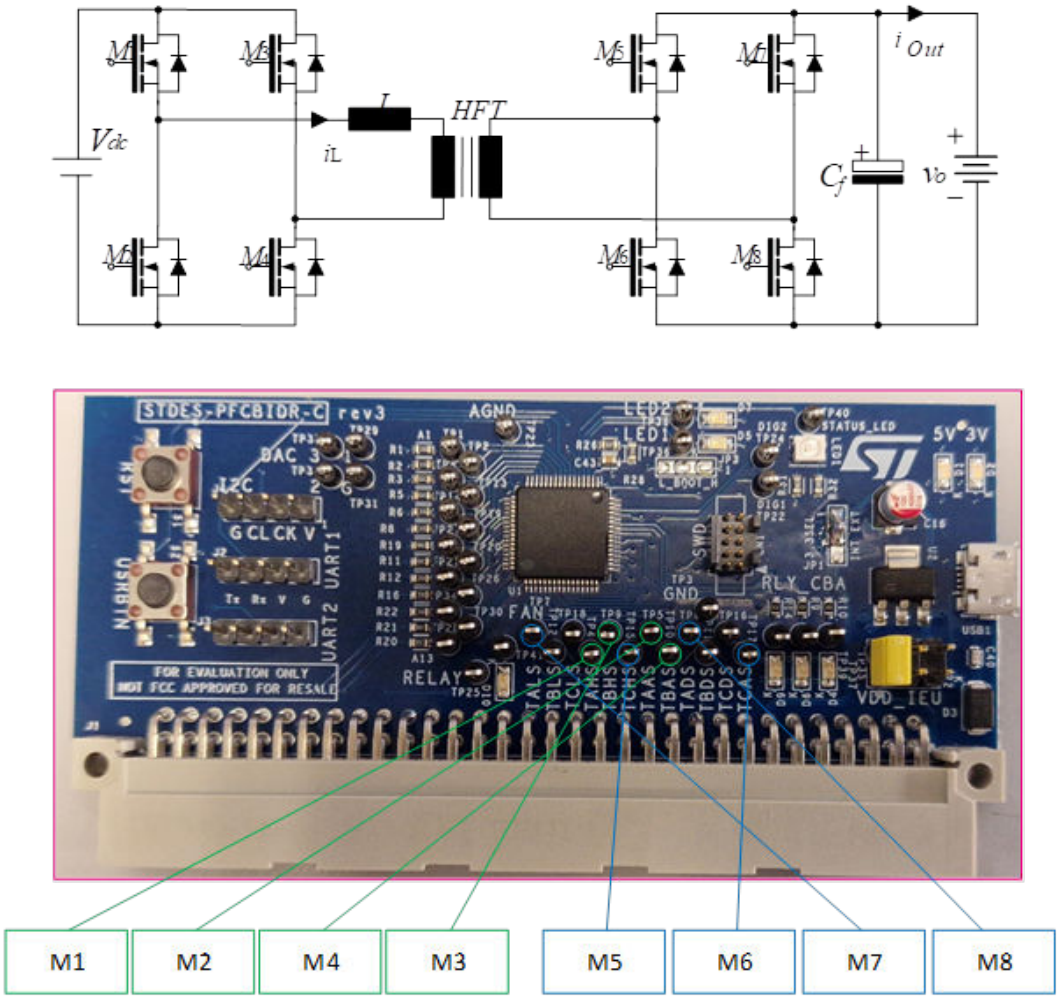
This test is for the driving section of the application. PWM signals are generated by HRTIM according to the STM32CubeMX peripheral configuration.

Dead time and switching frequency are managed by “PWM_FREQ”, “DPC_DT_DAB1” and “DPC_DT_DAB2” of “DPC_Appplication_Conf.h” file.

No high-power equipment is required during this test.

MCU and gate driver section phase shift between primary and secondary can be verified during this test.

Figure 58. **Mode 1 test configuration**



An example of the default configuration is given. Swathing frequency and dead time are configured in “DPC_Application_Conf.h” and the expected waveforms are provided.

Step 1. Configure the firmware parameters and flash the MCU.

Table 23. **Mode 1 test parameters**

Parameters	Location	Value
DPC_CTRL_INIT	DPC_Application_Conf.h	DAB_OPEN_LOOP
DPC_PWM_INIT	DPC_Application_Conf.h	PWM_Armed
StartUpCheck_INIT	DPC_Application_Conf.h	StartUpCheck_Disabled
DPC_INRS_EN	DPC_Application_Conf.h	RESET
DPC_BURST_EN	DPC_Application_Conf.h	RESET
PhSh_CTRL_MAN_norm	DAB. pDAB_CTRL.PhSh_CTRL_MAN_norm	0.25

Step 2. Go to the debugging mode in the preferred IDE software.

Step 3. If emergency shoot down is required, DPC_FSM_NEW_State can be set to “DPC_FSM_FAULT” to disable PWM as well as phase shifting and energy transfer.

Example 1 :

Table 24. Example of frequency and dead time configuration

Parameters	Location	Value
PWM_FREQ	DPC_Application_Conf.h	100000
DPC_DT_DAB1	DPC_Application_Conf.h	0.4e-6
DPC_DT_DAB2	DPC_Application_Conf.h	0.4e-6

Figure 59. Typical PWM and driving voltages

7.6.2 Mode 2 – open loop, phase shift power operation.

This test is for the power and sensing section of the application.

Power equipment (programmable DC power supply and DC eDLoad) is required for this test. DPI and protection shields are mandatory to prevent injury. Power analyzer can be connected during this test to evaluate efficiency in specific operating points.

The PWM signals are generated by HRTIM according to the STM32CubeMX peripheral configuration.

Dead time and switching frequency are managed by “PWM_FREQ”, “DPC_DT_DAB1” and “DPC_DT_DAB2” of “DPC_Appplication_Conf.h” file.

MCU and gate driver sections phase shift between primary and secondary can be verified during this test.

Step 1. Configure firmware parameters and flash the MCU.

Table 25. Mode 2 test parameters

Parametrs	Location	Value
DPC_CTRL_INIT	DPC_Application_Conf.h	DAB_OPEN_LOOP
DPC_PWM_INIT	DPC_Application_Conf.h	PWM_Armed
StartUpCheck_INIT	DPC_Application_Conf.h	StartUpCheck_Disabled
DPC_INRS_EN	DPC_Application_Conf.h	RESET
DPC_BURST_EN	DPC_Application_Conf.h	RESET
PhSh_CTRL_MAN_norm	DAB. pDAB_CTRL.PhSh_CTRL_MAN_norm	Variable during this test

Step 2. Select and enable Constant Current mode “CC” in the High Power eLoad.

Step 3. Set current reference to 9A.

Step 4. Go to the debugging mode in the preferred IDE software.

Step 5. Set to 0.06 in DAB. pDAB_CTRL.PhSh_CTRL_MAN_norm.

Step 6. Slowly increase the DC power supply up to 400V.
The eLoad voltage will also increase up to 210V.

Step 7. Slowly increase the eLoad up to 16A.
The eLoad voltage will decrease.

Step 8. Slowly increase the DC power supply up to 800V.
The eLoad voltage will also increase up to 420V.

Step 9. By slowly changing phase shifting and the eLoad current requirements, the actual power level configuration can be adjusted to evaluate several configurations.

Step 10. Decrease the DC power supply until 0V is reached.
The eLoad voltage will decrease.

Step 11. If emergency shoot down is required, DPC_FSM_NEW_State can be set to “DPC_FSM_FAULT” to disable PWM as well as phase shifting and energy transfer.

Figure 60. Open loop, phase shift power operation Vin=400V Vout=210V PS=0.06 Iload=9A

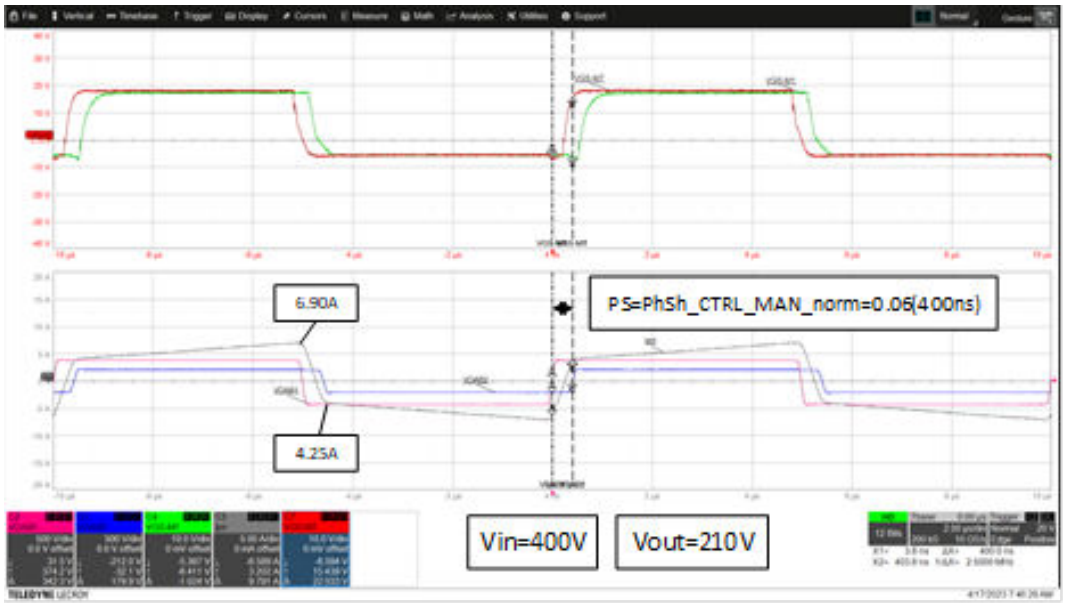
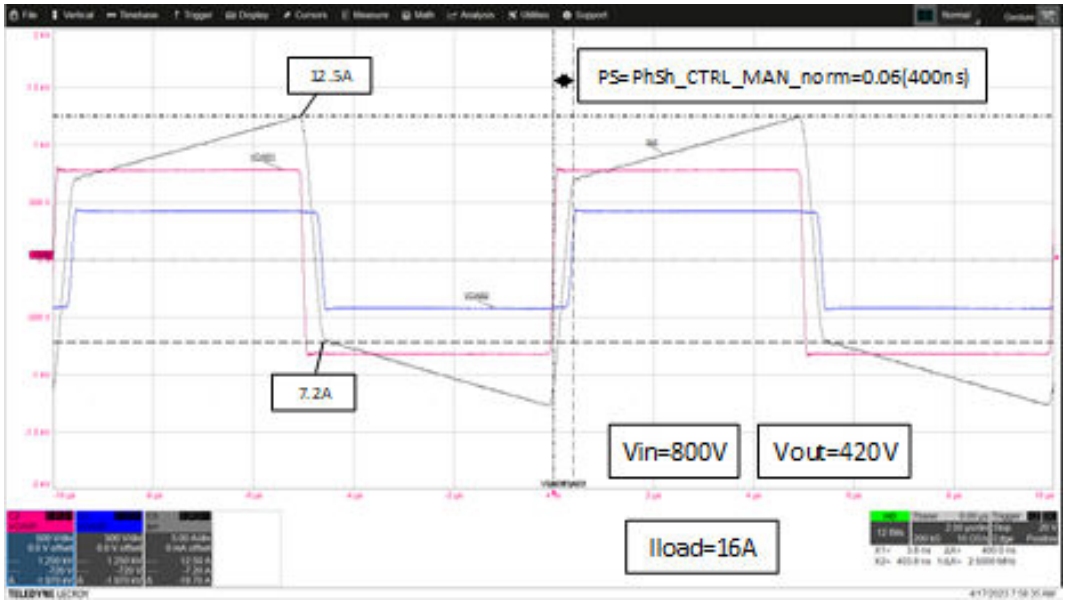


Figure 61. **Open loop, phase shift power operation Vin=800V Vout=420V PS=0.06 Iload=16A**



7.6.3 Mode 3 – closed loop, voltage control

This test allows evaluation of the overall performance in voltage control mode of the application.

Power equipment (Programmable DC Power Supply and DC eDLoad) is required for this test. DPI and protection shields are mandatory to prevent any injury. Power analyzer can be connected during this test to evaluate efficiency into specific operating points.

PWM signals are generated by HRTIM according to the STM32CubeMX peripheral configuration.

Dead time and switching frequency are managed by “PWM_FREQ”, “DPC_DT_DAB1” and “DPC_DT_DAB2” of “DPC_Appplication_Conf.h” file.

Step 1. Configure the firmware parameters and flash the MCU.

Table 26. **Mode 3 test parameters**

Parametrs	Location	Value
DPC_CTRL_INIT	DPC_Application_Conf.h	DAB_VOLTAGE_LOOP
DPC_PWM_INIT	DPC_Application_Conf.h	PWM_Armed
StartUpCheck_INIT	DPC_Application_Conf.h	StartUpCheck_Disabled
DPC_INRS_EN	DPC_Application_Conf.h	RESET
DPC_BURST_EN	DPC_Application_Conf.h	RESET
fDAB_VDC_RefNext_V	DAB.pDAB_CTRL.pDAB_VCTRL_SlewRate. fDAB_VDC_RefNext_V	Variable during this test

Step 2. Select and enable Constant Current mode “CC” in the High Power eLoad

Step 3. Set current reference to 1A.

Step 4. Go to the debugging mode by using the preferred IDE tool (“Live mode”).

Step 5. Set to 250 in DAB.pDAB_CTRL.pDAB_VCTRL_SlewRate. fDAB_VDC_RefNext_V

Step 6. Slowly increase the DC power supply up to 800V
The eLoad power will also increase.

Step 7. Adapt the current reference of the eLoad to evaluate the operating mode at different power level.

Step 8. The DC output voltage can also be adapted by changing “fDAB_VDC_RefNext_V”.
The actual output voltage reference changes linearly according to the slew rate configuration.

Step 9. If emergency shoot down is required, DPC_FSM_NEW_State can be set to “DPC_FSM_FAULT” to disable PWM as well as phase shifting and energy transfer.

Some operating examples are shown below:

Figure 62. Open loop, phase shift power operation Vin=800V Vout=330V(VCTRL) Iload=17A

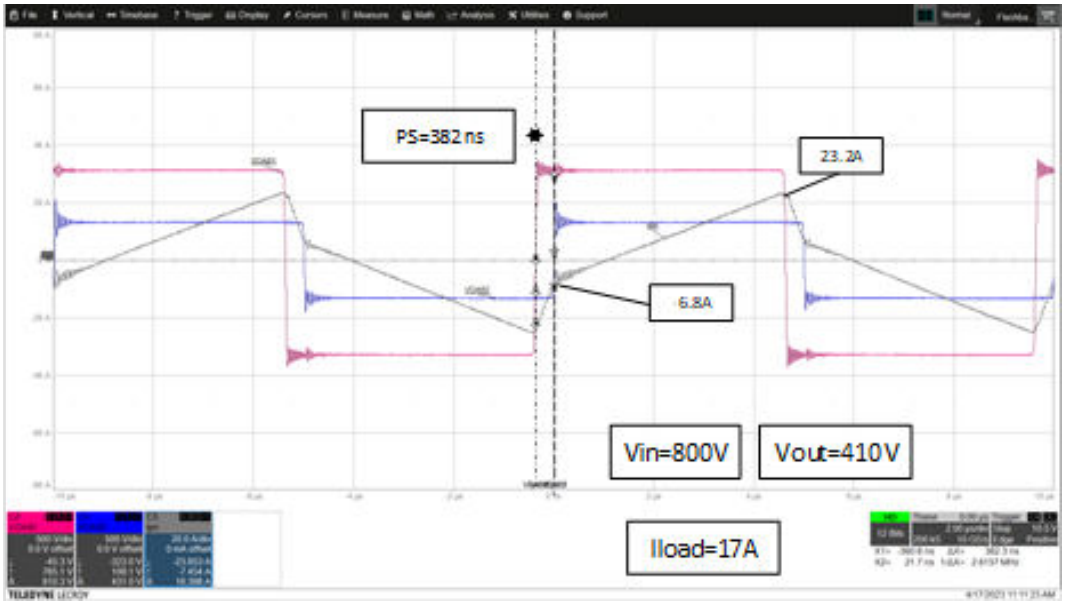


Figure 63. Open loop, phase shift power operation Vin=800V Vout=410V(VCTRL) Iload=15A

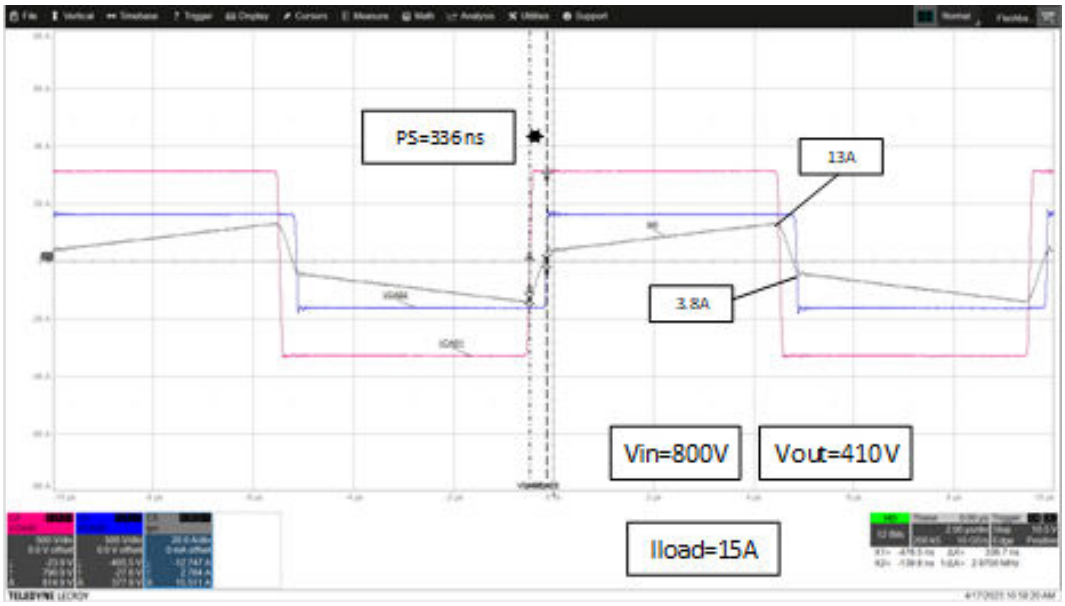
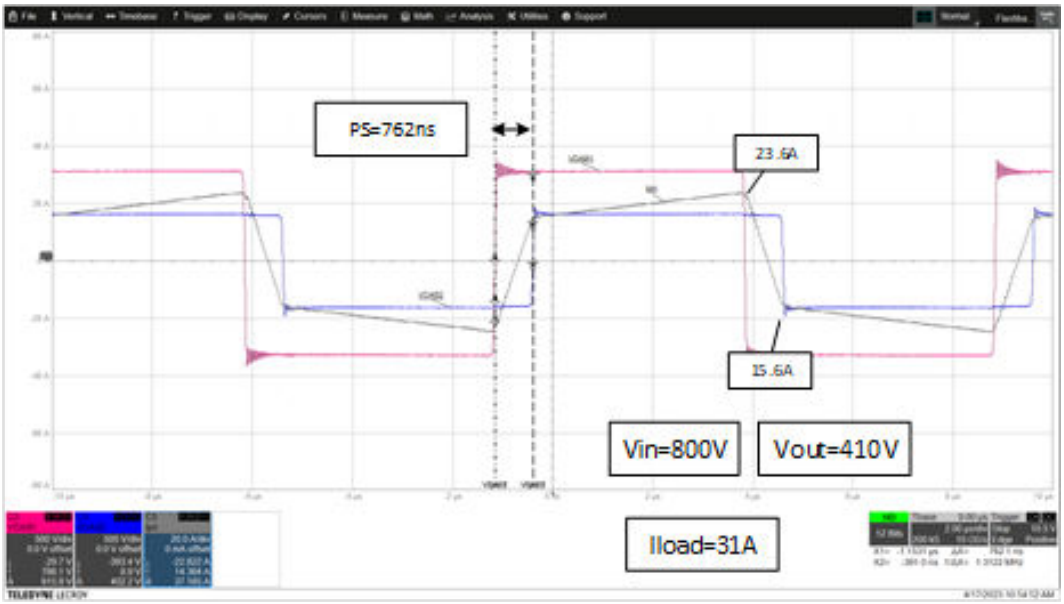


Figure 64. **Open loop, phase shift power operation Vin=800V Vout=410V(VCTRL) Iload=31A**



7.6.4 Mode 4 – closed loop, current control

This test allows evaluation of the overall performance of the application in current control mode.

Power equipment (Programmable DC Power Supply and DC eDLoad) is required for this test. DPI and protection shields are mandatory to prevent injury. Power analyzer can be connected during this test to evaluate efficiency in specific operating points.

PWM signals are generated by HRTIM according to the STM32CubeMX peripheral configuration.

Dead time and switching frequency are managed by “PWM_FREQ”, “DPC_DT_DAB1” and “DPC_DT_DAB2” of “DPC_Appplication_Conf.h” file.

Step 1. Configure the firmware parameters and flash the MCU.

Table 27. **Mode 4 test parameters**

Parameters	Location	Value
DPC_CTRL_INIT	DPC_Application_Conf.h	DAB_CURRENT_LOOP
DPC_PWM_INIT	DPC_Application_Conf.h	PWM_Armed
StartUpCheck_INIT	DPC_Application_Conf.h	StartUpCheck_Disabled
DPC_INRS_EN	DPC_Application_Conf.h	RESET
DPC_BURST_EN	DPC_Application_Conf.h	RESET
fDAB_IDC_RefNext_V	DAB.pDAB_CTRL.pDAB_ICTRL_SlewRate. fDAB_IDC_RefNext_A	Variable during this test

Step 2. Select and enable Constant Current mode “CC” in the High Power eLoad

Step 3. Set current reference to 250V.

Step 4. Go to the debugging mode by using the preferred IDE tool.

Step 5. Set to 2 in DAB.pDAB_CTRL.pDAB_ICTRL_SlewRate. fDAB_IDC_RefNext_A

Step 6. Slowly increase the DC power supply up to 800V; the eLoad power will also increase.

Step 7. Adapt the voltage reference of the eLoad to evaluate the operating mode at different power levels.

Step 8. The DC output current can also be adapted by changing “fDAB_IDC_RefNext_A”. The actual output current reference changes linearly according to the slew rate configuration.

Step 9. If emergency shoot down is required, DPC_FSM_NEW_State can be set to “DPC_FSM_FAULT” to disable PWM as well as phase shifting and energy transfer.

8 STDES-DABBIDIR results

This section provides an additional overview of the reference design.

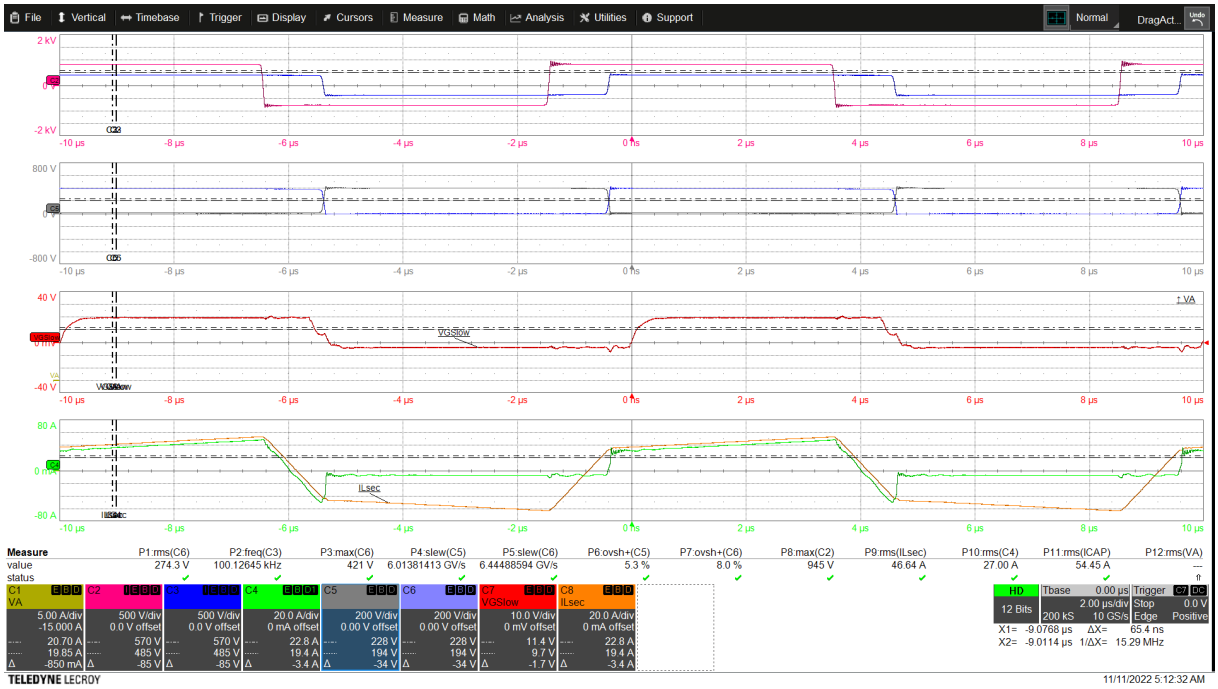
8.1 Charging mode waveforms

Waveforms analysis at:

- Vin=800V
- Vout=400V
- fsw=100kHz
- IDCload=40Amps
- Voltage regulation operating mode

Figure 65. Switching waveform

C1=DC load current C2=VDAB1 C3=VDAB2 C4=IDM7 C5=VDSM7 C6=VDSM8 C7=VGSM7 C8=ILsec

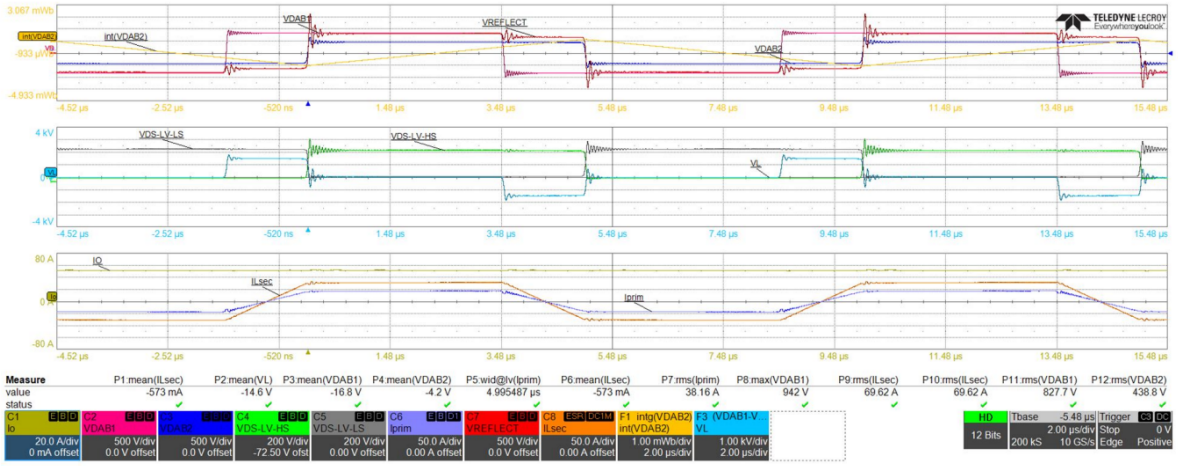


Waveforms analysis at:

- Vin=830V
- Vout=440V
- fsw=100kHz
- IDCload=56.3A
- Voltage regulation operating mode

Figure 66. Maximum power waveforms

C1=DC load current C2=VDAB1 C3=VDAB2 C4=VDS_LV_HS C5= VDS_LV_LS C6=Iprim C7=VREFL C8=ILsec F3=VL

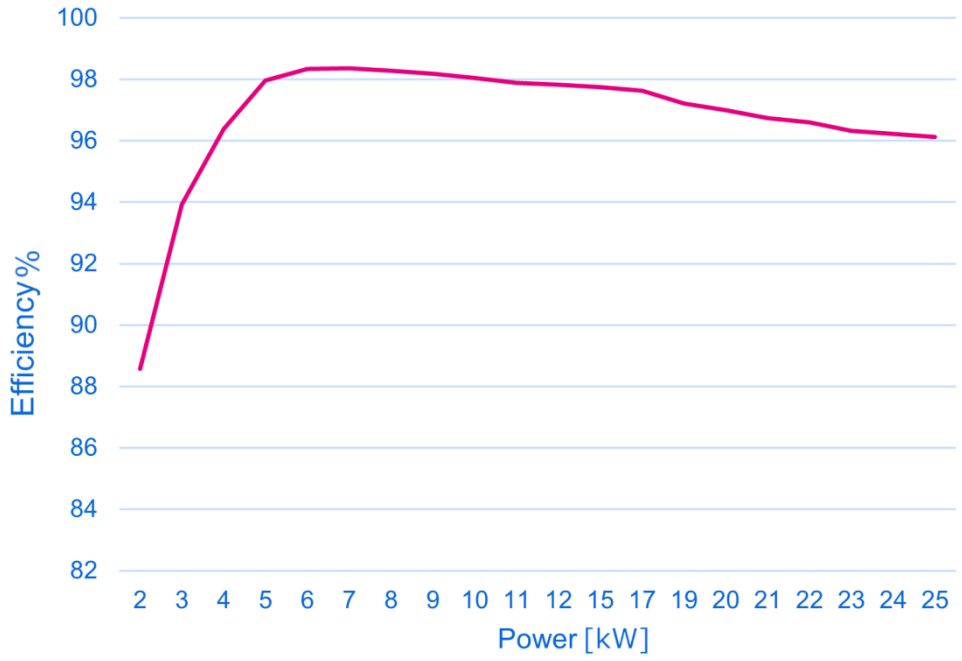


8.2 Efficiency

Efficiency characterization at:

- Vin=800V
- Vout=440V
- fsw=100kHz
- Voltage regulation operating mode
- Iload=4.5-56.3 A (Constant current)

Figure 67. STDESDABBIDIR Efficiency



9 Schematic diagrams

Figure 68. **STDES-DABBIDIR - main board circuit schematic (1 of 6)**

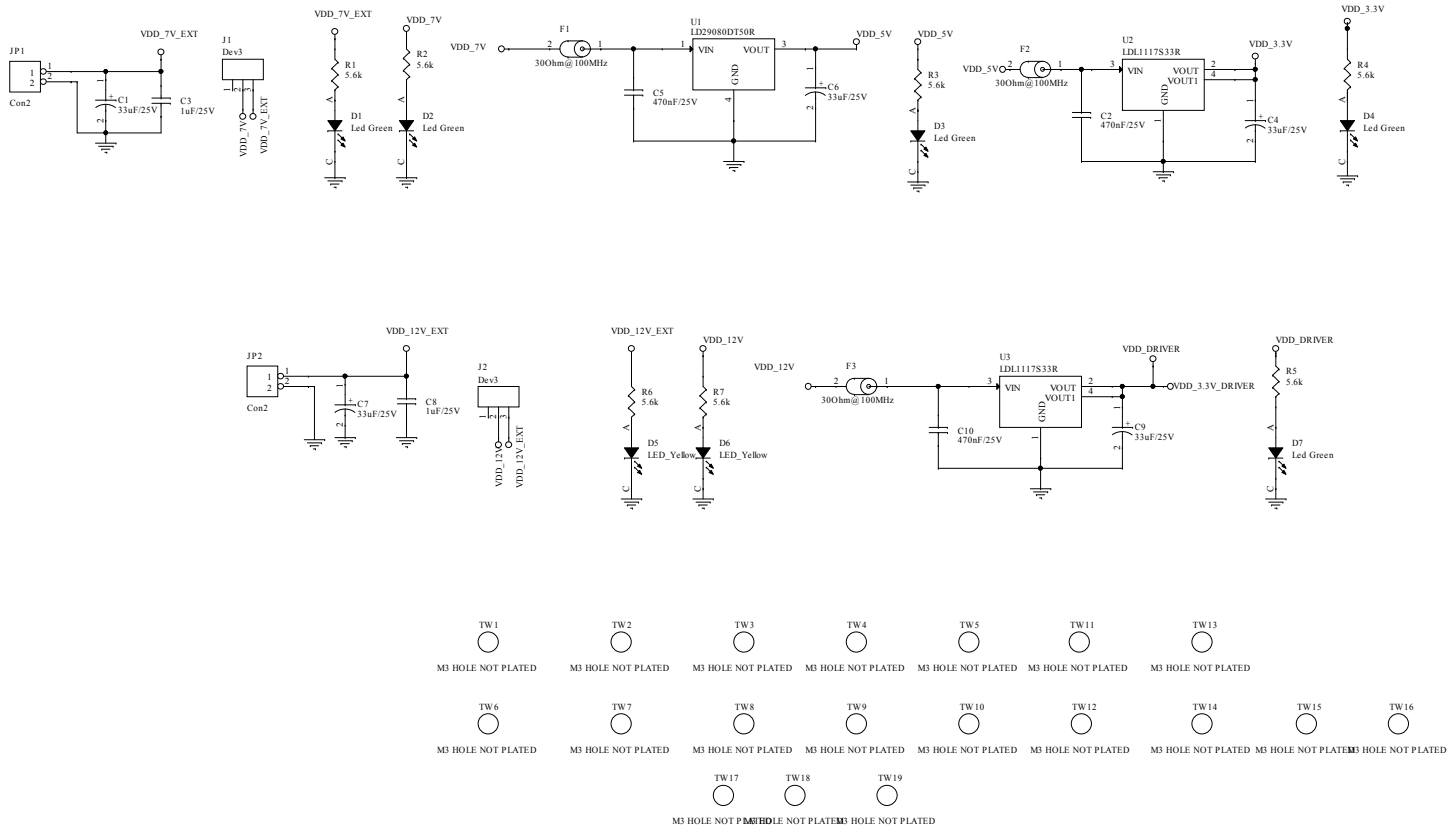


Figure 69. STDES-DABBIDIR - main board circuit schematic (2 of 6)

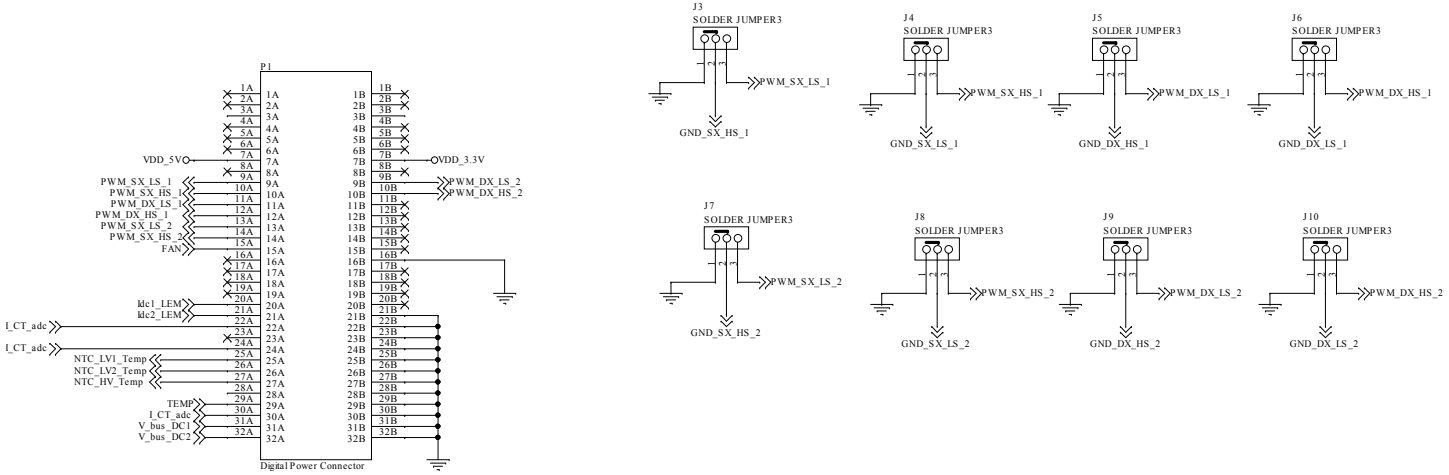


Figure 70. STDES-DABBIDIR - main board circuit schematic (3 of 6)

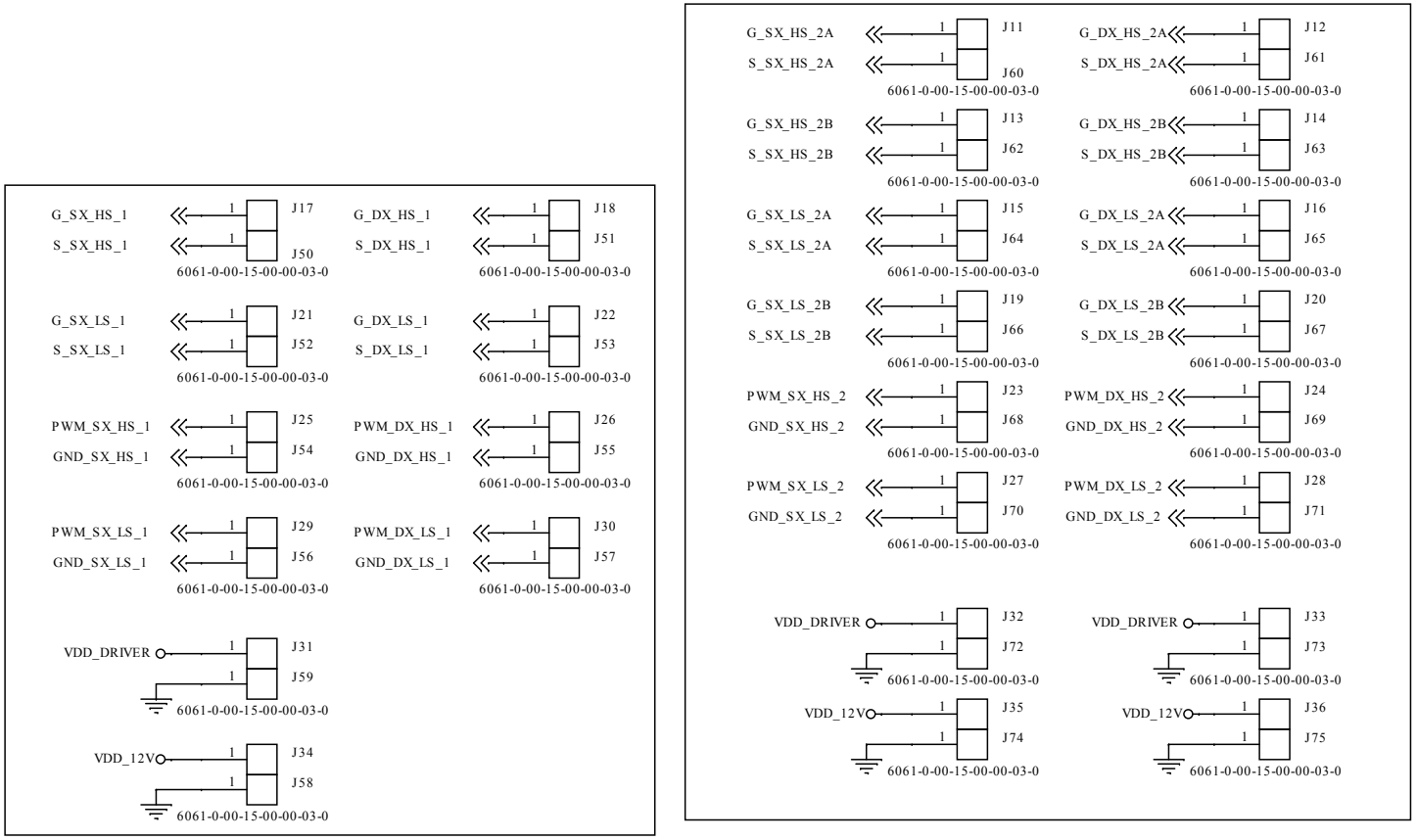


Figure 71. STDES-DABBIDIR - main board circuit schematic (4 of 6)

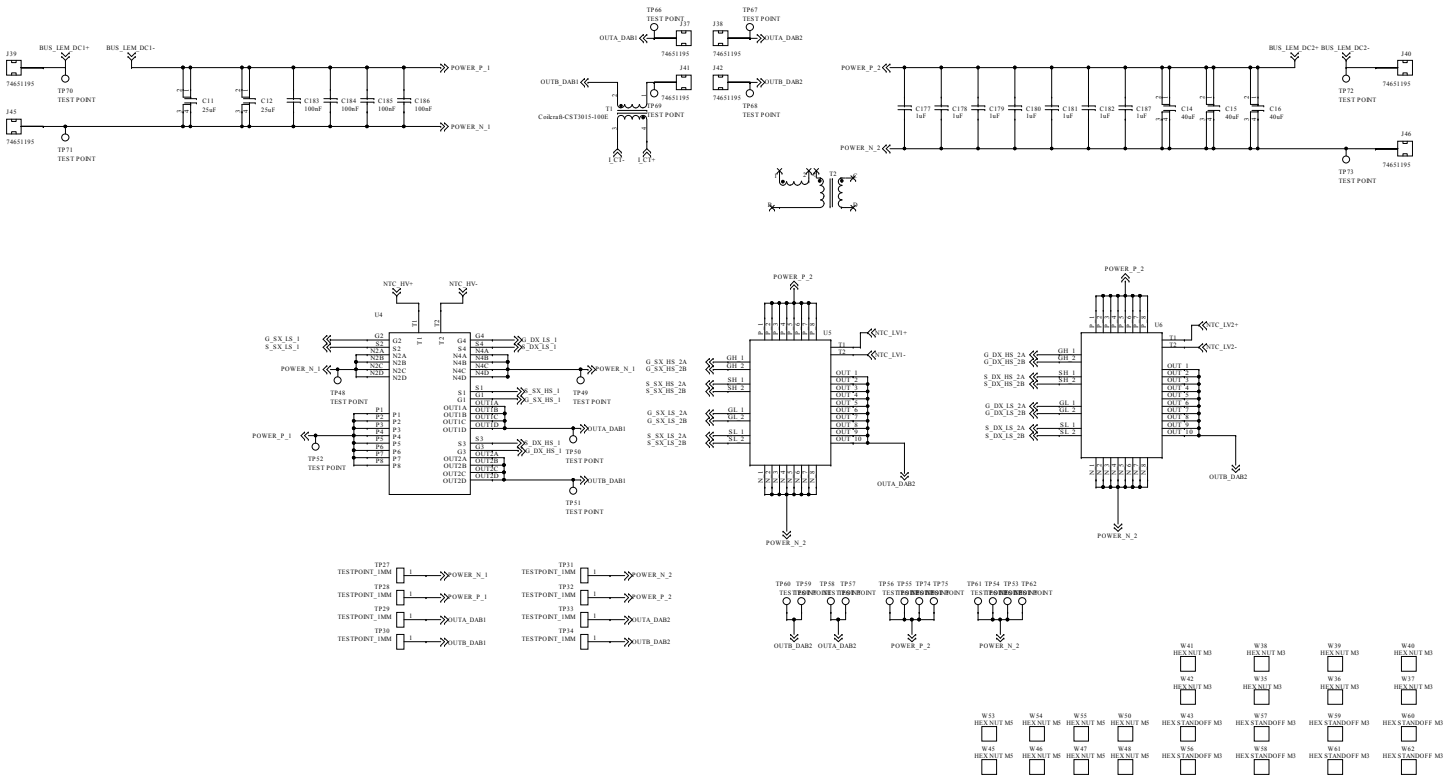


Figure 72. STDES-DABBIDIR - main board circuit schematic (5 of 6)

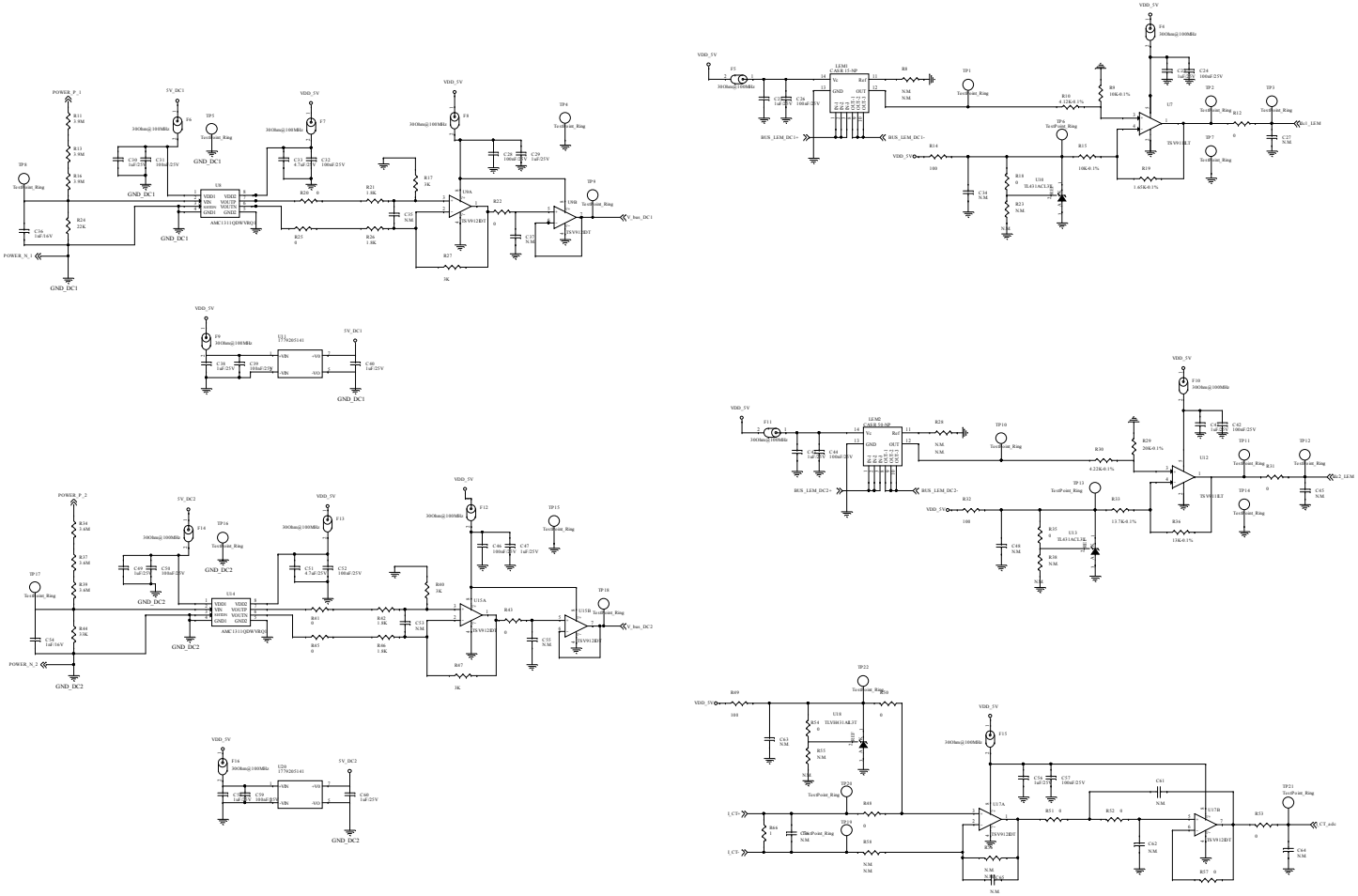


Figure 73. STDES-DABBIDIR - main board circuit schematic (6 of 6)

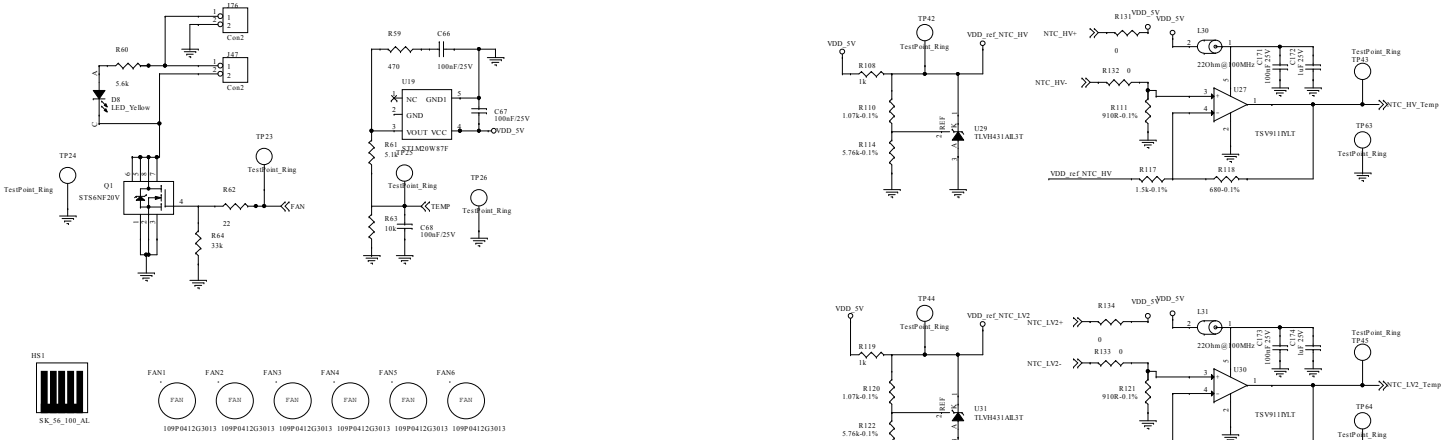


Figure 74. STDES-DABBIDIR - driver board for full bridge circuit schematic

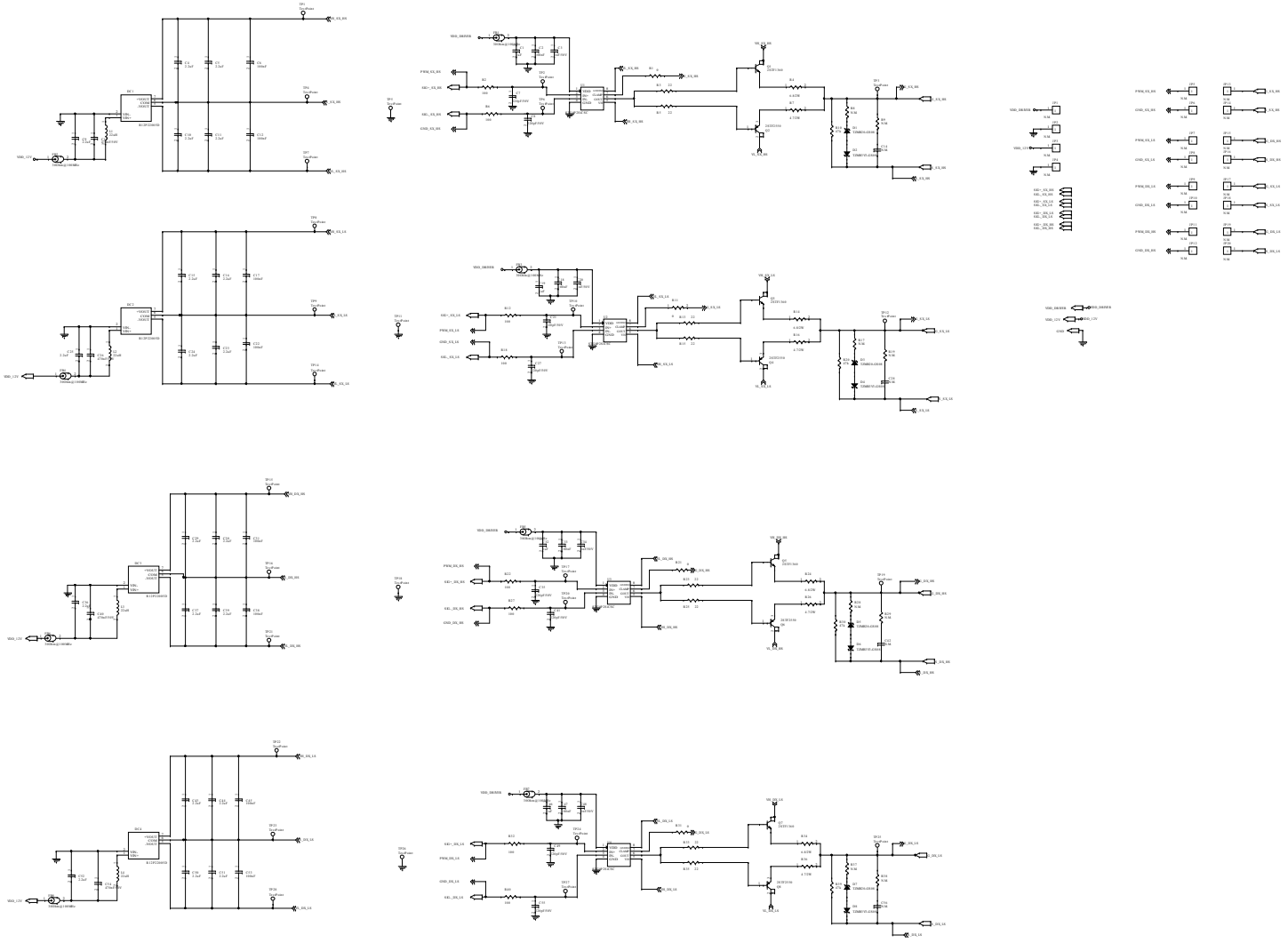


Figure 75. **STDES-DABBIDIR - driver board for half bridge circuit schematic (1 of 2)**

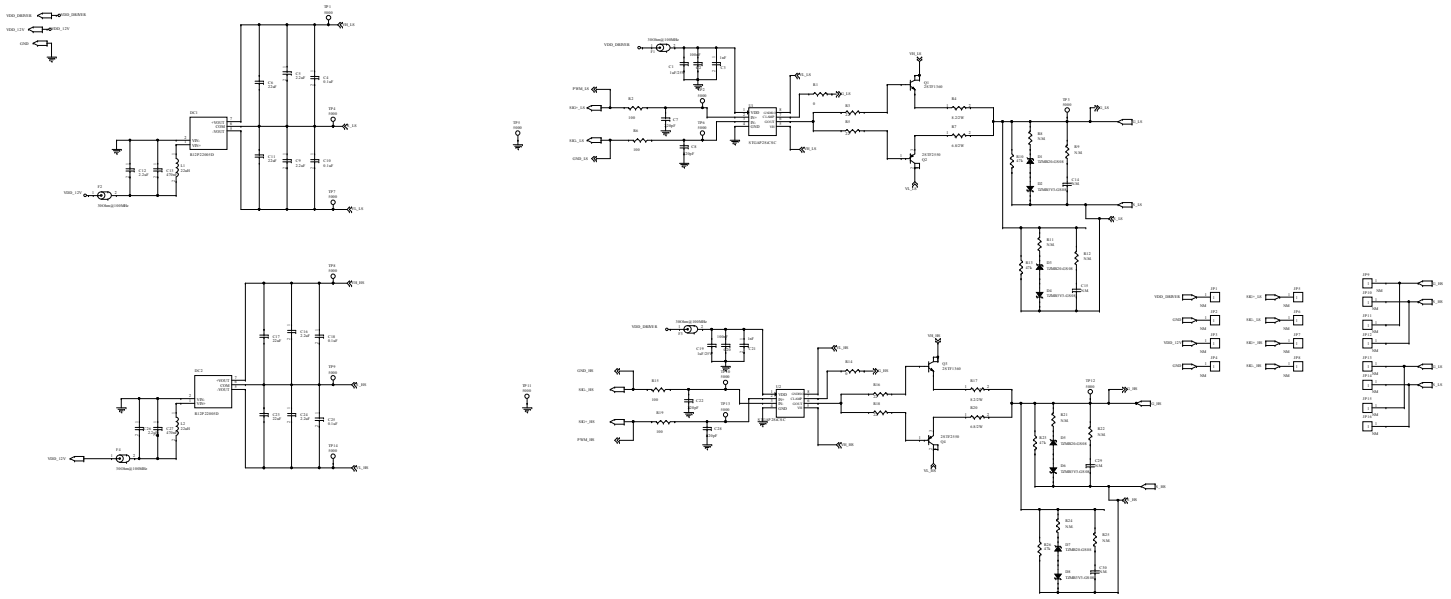


Figure 76. **STDES-DABBIDIR - driver board for half bridge circuit schematic (1 of 1)**

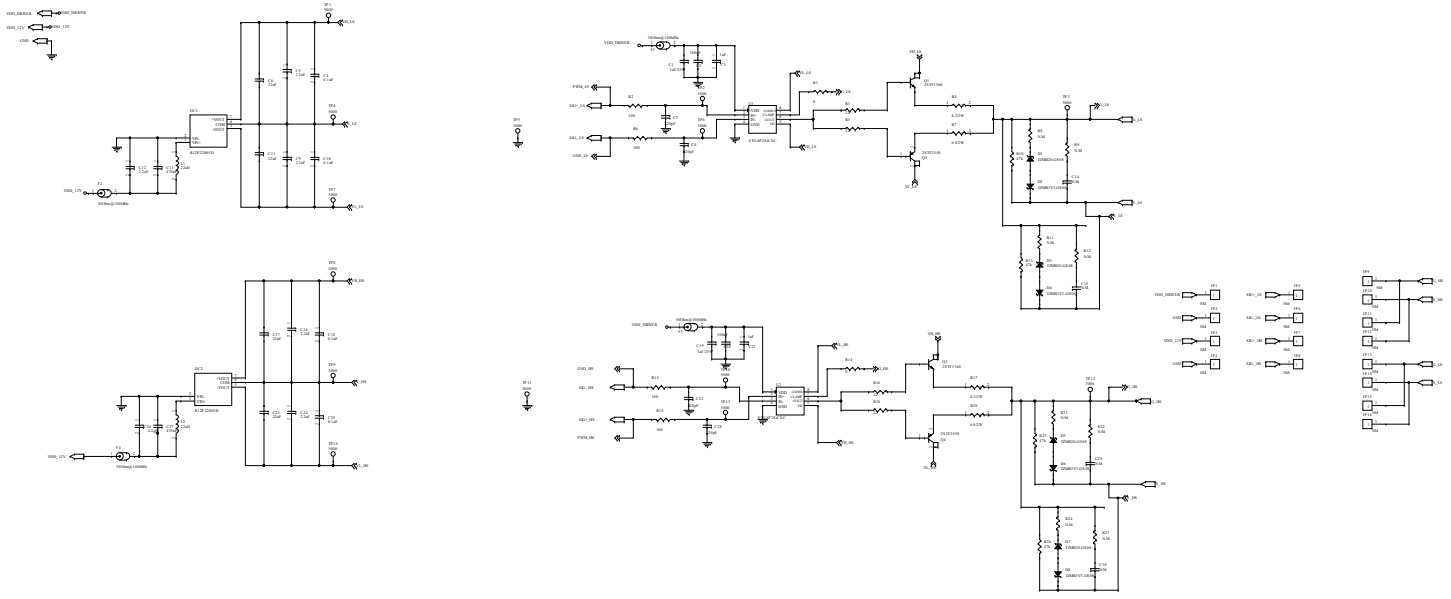
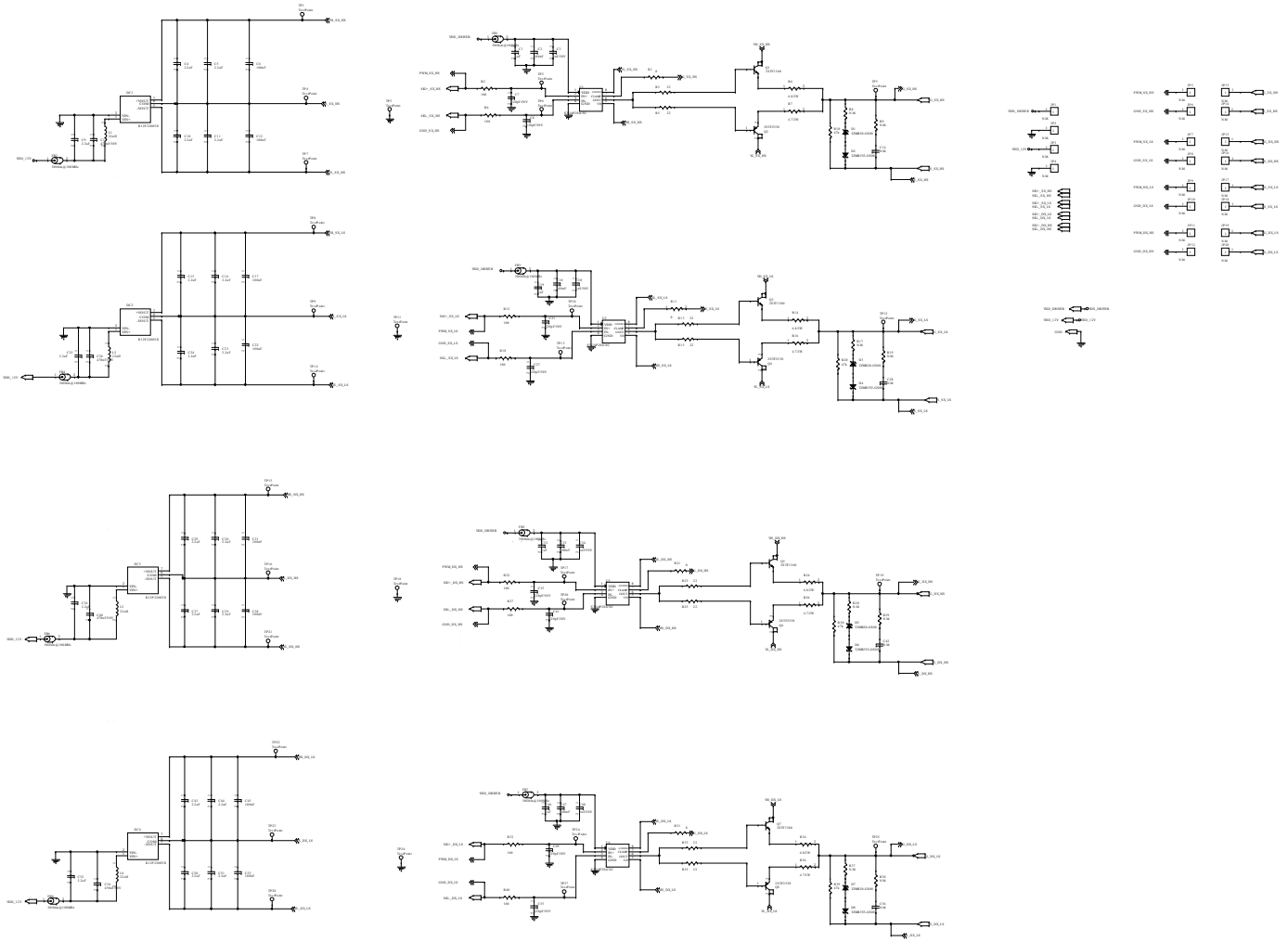


Figure 77. **STDES-DABBIDIR - control board circuit schematic**



10 Bill of materials

Table 28. STDES-DABBIDIR bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	1	Table 29. Main board bill of materials	-	Main board	ST	Not available for separate sale
2	1	Table 30. Driver board for full bridge bill of materials	-	Driver board for full bridge	ST	Not available for separate sale
3	2	Table 31. Driver board for half bridge bill of materials	-	Driver board for half bridge	ST	Not available for separate sale
4	1	Table 32. STDES-DABBIDIR control board	-	Control board	ST	Not available for separate sale

Table 29. Main board bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	5	C1 C4 C6 C7 C9	33uF/25V	Cap Pol Radial (Electrolytic); 6.60 mm X 6.60 mm X 5.50 mm H body	WURTH	865230443004
2	3	C2 C5 C10	470nF/25V	CAPACITOR CERAMIC SMD 0603	WURTH	885012206075
3	15	C3 C8 C23 C25 C29 C30 C38 C40 C41 C43 C47 C49 C56 C58 C60	1uF/25V	CAPACITOR CERAMIC SMD 0603	WURTH	885012206076
4	2	C11 C12	25uF	WCAP-FTDB DC-Link Capacitor,32.5mm,25uF	WURTH	890744428006CS
5	3	C14 C15 C16	40uF	WCAP-FTDB DC-Link Capacitor,32.5mm,40uF	WURTH	890764428004CS
6	16	C24 C26 C28 C31 C32 C39 C42 C44 C46 C50 C52 C57 C59 C66 C67 C68	100nF/25V	CAPACITOR CERAMIC SMD 0603	WURTH	885012206071
7	14	C27 C34 C35 C37 C45 C48 C53 C55 C61 C62 C63 C64 C65 C76	N.M.	CAPACITOR CERAMIC SMD 0603	ANY	ANY
8	2	C33 C51	4.7uF/25V	CAPACITOR CERAMIC SMD 0603	WURTH	885012106012

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
9	2	C36 C54	1nF/16V	CAPACITOR CERAMIC SMD 0603	WURTH	885012006029
10	3	C171 C173 C175	100nF 25V	CAPACITOR CERAMIC SMD 0603	Würth Elektronik	885012206071R
11	3	C172 C174 C176	1uF 25V	CAPACITOR CERAMIC SMD 0603	Würth Elektronik	885012206076
12	7	C177 C178 C179 C180 C181 C182 C187	1uF	CAPACITOR CERAMIC SMD 2220	WURTH	885342214001
13	4	C183 C184 C185 C186	100nF	CAPACITOR CERAMIC SMD 2220	WURTH	885342214173
14	5	D1 D2 D3 D4 D7	Led Green	LED GREEN CLEAR 0805 SMD	Wurth	150080YS75000
15	3	D5 D6 D8	LED_Yellow	LED YELLOW CLEAR 0805 SMD	Wurth	150080GS75000
16	16	F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16	30Ohm@100MHz	FERRITE BEAD 30 OHM 0805 1LN	WURTH	742792030
17	6	FAN1 FAN2 FAN3 FAN4 FAN5 FAN6	109P0412G3013	Sanyo Denki 109P Series Axial Fan, 12 V dc, DC Operation, 25.1m³/h, 3.72W, 40 x 40 x 28mm	Sanyo Denki	109P0412G3013
18	1	HS1	SK_56_100_AL	SK 56 100 AL | FISCHER ELEKTRONIK	fischerelektronik	SK 56 100 AL
19	2	J1 J2	Dev3	SWITCH SLIDE SPDT 500MA 12V	WURTH	450301014042
20	8	J3 J4 J5 J6 J7 J8 J9 J10	SOLDER JUMPER3	TIN DROP JUMPER 0603 3pin		
21	52	J11 J12 J13 J14 J15 J16 J17 J18 J19 J20 J21 J22 J23 J24 J25 J26 J27 J28 J29 J30 J31 J32 J33 J34 J35 J36 J50 J51 J52 J53 J54 J55 J56 J57 J58 J59 J60 J61 J62 J63 J64 J65 J66 J67 J68 J69 J70 J71 J72 J73 J74 J75	6061-0-00-15-00-00-03-0	Circuit Board Hardware - PCB RECPT. GOLD/ NICKEL .106 IN. PRESSFIT	Mill-Max	6061-0-00-15-00-00-03-0

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
22	8	J37 J38 J39 J40 J41 J42 J45 J46	74651195	Power to the Board 10MM 40A SOLDER SCREW M4	WURTH	74651195
23	2	J47 J76	Con2	CONN TERM BLOCK 2POS 5.08MM PCB	Wurth	691213510002
24	2	JP1 JP2	Con2	CONN TERM BLOCK 2POS 5.08MM PCB	Wurth	691213510002
25	3	L30 L31 L32	22Ohm@100MHz		Würth Elektronik	742792021
26	1	LEM1	CASR 15-NP	SENSOR CURRENT HALL 15A AC/DC	LEM USA Inc.	CASR 15-NP
27	1	LEM2	CASR 50-NP	SENSOR CURRENT HALL 15A AC/DC	LEM USA Inc.	CASR 50-NP
28	1	P1	CON64AB	Connector Erni 284166 32X2 female	ERNI	284166
29	1	Q1	STS6NF20V, SO-8	MOSFET N-CH 20V 6A 8SOIC	ST	STS6NF20V
30	7	R1 R2 R3 R4 R5 R6 R7	5.6k	CHIP RESISTOR SMD 1% 1/4W 1206	ANY	ANY
31	7	R8 R23 R28 R38 R55 R56 R58	N.M.	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
32	2	R9 R15	10K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
33	1	R10	4.12K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
34	3	R11 R13 R16	3.9M	CHIP RESISTOR SMD 1% 1/4W 1206	ANY	ANY
35	14	R12 R18 R20 R22 R25 R31 R35 R41 R43 R45 R48 R50 R53 R54	0	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
36	3	R14 R32 R49	100	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
37	4	R17 R27 R40 R47	3K	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
38	1	R19	1.65K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
39	4	R21 R26 R42 R46	1.8K	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
40	1	R24	22K	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
41	1	R29	20K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
42	1	R30	4.22K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
43	1	R33	13.7K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
44	3	R34 R37 R39	3.6M	CHIP RESISTOR SMD 1% 1/4W 1206	ANY	ANY
45	1	R36	13K-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
46	2	R44 R64	33K	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
47	3	R51 R52 R57	0	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
48	1	R59	470	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
49	1	R60	5.6k	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
50	1	R61	5.1k	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
51	1	R62	22	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
52	1	R63	10k	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
53	1	R66	1	CHIP RESISTOR SMD 2512	ANY	ANY
54	3	R108 R119 R125	1k	CHIP RESISTOR SMD 1% 1/10W 0603		
55	3	R110 R120 R126	1.07k-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603		
56	3	R111 R121 R127	910R-0.1%	CHIP RESISTOR SMD 0.1% 1/10W 0603		
57	3	R114 R122 R128	5.76k-0.1%	CHIP RESISTOR SMD 1% 1/10W 0603		
58	3	R117 R123 R129	1.5k-0.1%	CHIP RESISTOR SMD 0.1% 1/10W 0603		
59	3	R118 R124 R130	680-0.1%	CHIP RESISTOR SMD 0.1% 1/10W 0603		
60	6	R131 R132 R133 R134 R135 R136	0	CHIP RESISTOR SMD 0.1% 1/10W 0603		
61	1	T1	Coilcraft-CST3015-100E	Tranf,Radio 1:100,80A	Coilcraft	CST3015-100E
62	1	T2	Frenetic_32011-04			
63	22	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22	TestPoint_Ring	TestPoint RIng	ANY	ANY
64	4	TP23 TP24 TP25 TP26	TestPoint_Ring	TestPoint RIng	ANY	ANY
65	8	TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34	TESTPOINT_1MM			

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
66	9	TP42 TP43 TP44 TP45 TP46 TP47 TP63 TP64 TP65	TestPoint_Ring	Polo terminale RS Pro, diam. foro 1mm, Bronzo fosforoso	ANY	ANY
67	25	TP48 TP49 TP50 TP51 TP52 TP53 TP54 TP55 TP56 TP57 TP58 TP59 TP60 TP61 TP62 TP66 TP67 TP68 TP69 TP70 TP71 TP72 TP73 TP74 TP75	TEST POINT	PC TEST POINT NATURAL	Harwin Inc.	S1751-46R
68	19	TW1 TW2 TW3 TW4 TW5 TW6 TW7 TW8 TW9 TW10 TW11 TW12 TW13 TW14 TW15 TW16 TW17 TW18 TW19	M3 HOLE NOT PLATED	Mounting Hole M3 not plated - Pan Head		
69	1	U1	LD29080DT50R , DPAK	IC REG LINEAR 5V 800MA DPAK	ST	LD29080DT50R
70	2	U10 U13	TL431ACL3T, SOT23	IC VREF SHUNT ADJ SOT23-3	ST	TL431ACL3T
71	2	U11 U20	1779205141	DC DC CONVERTER 5V 1W	WURTH	1779205141
72	2	U12 U7	TSV911ILT, SOT23-5L	IC OPAMP GP 8MHZ RRO SOT23-5	ST	TSV911ILT
73	2	U14 U8	AMC1311QDW VRQ1	IC ISOLATION 8SOIC	Texas Instruments	AMC1311QDWVRQ1
74	3	U15 U17 U9	TSV912IDT, SO-8	IC OPAMP GP 8MHZ RRO 8SO	ST	TSV912IDT
75	2	U2 U3	LDL1117S33R, SOT-223	IC REG LINEAR 3.3V 800MA SOT223	ST	LDL1117S33R
76	1	U4	A2F12M12W2-F1, ACEPACK 2	ACEPACK™ 2 – Full-bridge - 1200V, 12mO SiC	ST	A2F12M12W2-F1
77	2	U5 U6	A2H6M12W3	ACEPACK™ 2 - Half-bridge - 1200V, 6mO SiC MOSFET Gen2 and NTC	ST	A2H6M12W3
78	1	U18	TLVH431AIL3T, SOT23	IC VREF SHUNT ADJ SOT23-3	ST	TLVH431AIL3T

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
79	1	U19	STLM20W87F, SOT323-5L	SENS TEMP ANLG VOLT SOT-323-5	ST	STLM20W87F
80	3	U27 U30 U32	TSV911IYLT, SOT23-5L	IC OPAMP GP 8MHZ RRO SOT23-5	ST	TSV911IYLT
81	3	U29 U31 U33	TLVH431AIL3T, SOT23	IC VREF SHUNT ADJ SOT23-3	ST	TLVH431AIL3T
82	8	W35 W36 W37 W38 W39 W40 W41 W42	HEX NUT M3	HEX NUT M3	ANY	
83	8	W43 W56 W57 W58 W59 W60 W61 W62	HEX STANDOFF M3	HEX STANDOFF M3X0.5 STEEL 50MM	WURTH	971500321
84	8	W45 W46 W47 W48 W50 W53 W54 W55	HEX NUT M5	HEX NUT M5	ANY	

Table 30. Driver board for full bridge bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	4	C1 C19 C32 C46	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603	Wurth Electronics Inc.	885012206076
2	12	C2 C6 C12 C17 C18 C22 C31 C33 C38 C45 C47 C53	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603	Wurth Electronics Inc.	885012206095
3	4	C3 C20 C34 C48	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603	Wurth Electronics Inc.	885012006063
4	20	C4 C5 C9 C10 C11 C15 C16 C23 C24 C25 C29 C30 C36 C37 C39 C43 C44 C50 C51 C52	0805 (2012 Metric)	CAPACITOR CERAMIC SMD 0805	Wurth Electronics Inc.	885012207079
5	8	C7 C8 C21 C27 C35 C41 C49 C55	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603	Wurth Electronics Inc.	885012006059
6	4	C13 C26 C40 C54	0805 (2012 Metric)	CAPACITOR CERAMIC SMD 0805	Wurth Electronics Inc.	885012207102
7	4	C14 C28 C42 C56		N.M.	ANY	
8	4	D1 D3 D5 D7	DO-213AC, MINI-MELF, SOD-80	DIODE ZENER 20V 500MW SOD80	Vishay Semiconductor Diodes Division	TZMB20-GS08
9	4	D2 D4 D6 D8	DO-213AC, MINI-MELF, SOD-80	DIODE ZENER 3.3V 500MW SOD80	Vishay Semiconductor Diodes Division	TZMB3V3-GS08

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
10	4	DC1 DC2 DC3 DC4	0.77" L x 0.39" W x 0.49" H (19.5mm x 9.8mm x 12.5mm)	CONV DC/DC 2W 12VIN +20/-5VOUT T	Recom Power	R12P22005D
11	8	FB1 FB2 FB3 FB4 FB5 FB6 FB7 FB8	0805 (2012 Metric)	FERRITE BEAD 30 OHM 0805 1LN	Wurth Electronics Inc.	74279206
12	20	JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10 JP11 JP12 JP13 JP14 JP15 JP16 JP17 JP18 JP19 JP20		IC & Component Sockets .060" Dia St Pins	Mill-Max	3560-1-00-15-00-00-03-0
13	4	L1 L2 L3 L4	0805 (2012 Metric)	FIXED IND 22UH 130MA 3.7 OHM SMD	Taiyo Yuden	LBC2012T220M
14	4	Q1 Q3 Q5 Q7	TO-243AA, SOT-89	TRANS NPN 60V 3A SOT-89	ST	2STF1360
15	4	Q2 Q4 Q6 Q8	TO-243AA, SOT-89	TRANS PNP 50V 5A SOT 89	ST	2STF2550
16	3	R1 R21 R31	1210 (3225 Metric)	CHIP RESISTOR SMD	ANY	ANY
17	8	R2 R6 R12 R18 R22 R27 R32 R40	0603 (1608 Metric)	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
18	8	R3 R5 R13 R15 R23 R25 R33 R35	1210 (3225 Metric)	CHIP RESISTOR SMD	ANY	ANY
19	4	R4 R14 R24 R34	2512 (6332 metric)	CHIP RESISTOR SMD	ANY	ANY
20	4	R7 R16 R26 R36	2512 (6332 metric)	CHIP RESISTOR SMD	ANY	ANY
21	8	R8 R9 R17 R19 R28 R29 R37 R38	0603 (1608 Metric)	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
22	4	R10 R20 R30 R39	0603 (1608 Metric)	CHIP RESISTOR SMD 1% 1/10W 0603	ANY	ANY
23	1	R11	1206 (3216 Metric)	CHIP RESISTOR SMD 5% 1/4W 1206	ANY	ANY

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
24	28	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28	0.100" Dia x 0.180" L (2.54mm x 4.57mm)	TEST POINT PC MINI .040"D RED	ANY	ANY
25	4	U1 U2 U3 U4	8-SOIC (0.295", 7.50mm Width), SO 8 WIDE 300	Galvanically isolated 4 A single gate driver for SiC MOSFETs	ST	STGAP2SICSC

Table 31. Driver board for half bridge bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	2	C1 C19	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603 (MLCC) GRM 1µF, ±10%, 25V cc, SMD	Wurth Electronics Inc.	885012206076
2	2	C2 C20	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603 (MLCC) GRM 100nF, ±10%, 25V cc, SMD	Wurth Electronics Inc.	885012206071
3	1	C3	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603 (MLCC) C 1nF, ±10%, 25V cc, SMD	Wurth Electronics Inc.	885012006044
4	4	C4 C10 C18 C25	0603 (1608 Metric)	CAP CER 0.1UF 50V X7R 0603	Wurth Electronics Inc.	885012206095
5	6	C5 C9 C12 C16 C24 C26	0805 (2012 Metric)	CAP CER 2.2UF 50V X7R 0805	Wurth Electronics Inc.	885012207079
6	4	C6 C11 C17 C23	1210 (3225 Metric)	CAP CER 22UF 25V X5R 1210	Würth Elektronik	885012109014
7	4	C7 C8 C22 C28	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603 (MLCC) C 220pF, ±5%, 1kV cc, SMD	Wurth Electronics Inc.	885012006059
8	2	C13 C27	0805 (2012 Metric)	CAPACITOR CERAMIC SMD 0805	Wurth Electronics Inc.	885012207102
9	4	C14 C15 C29 C30		N.M.	ANY	

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
10	1	C21	0603 (1608 Metric)	CAPACITOR CERAMIC SMD 0603 (MLCC) C 1nF, ±10%, 25V cc, SMD	Wurth Electronics Inc.	885012006044
	4	D1 D3 D5 D7	DO-213AC, MINI-MELF, SOD-80	DIODE ZENER 20V 500MW SOD80	Vishay Semiconductor Diodes Division	TZMB20-GS08
12	4	D2 D4 D6 D8	DO-213AC, MINI-MELF, SOD-80	DIODE ZENER 3.3V 500MW SOD80	Vishay Semiconductor Diodes Division	TZMB3V3-GS08
13	2	DC1 DC2	0.77" L x 0.39" W x 0.49" H (19.5mm x 9.8mm x 12.5mm)	CONV DC/DC 2W 12VIN +20/-5VOUT T	RECOM	R12P22005D
14	4	F1 F2 F3 F4	0805 (2012 Metric)	FERRITE BEAD 30 OHM 0805 1LN	Wurth Electronics Inc.	742792030
15	16	JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10 JP11 JP12 JP13 JP14 JP15 JP16		IC & Component Sockets .060" Dia St Pins	Mill-Max	3560-1-00-15-00-00-03-0
16	2	L1 L2	0805 (2012 Metric)	FIXED IND 22UH 130MA 3.7 OHM SMD	Taiyo Yuden	LBC2012T220M
17	2	Q1 Q3	TO-243AA, SOT-89	TRANS NPN 60V 3A SOT-89	ST	2STF1360
18	2	Q2 Q4	TO-243AA, SOT-89	TRANS PNP 50V 5A SOT 89	ST	2STF2550
19	2	R1 R14	1210 (3225 Metric)	CHIP RESISTOR SMD		
20	4	R2 R6 R15 R19		Resistore SMD Bourns 100O ±1%, 0,1W, 0603, serie CR0603	ANY	ANY
21	4	R3 R5 R16 R18	1210 (3225 Metric)	CHIP RESISTOR SMD		
22	2	R4 R17	2512 (6332 metric)	CHIP RESISTOR SMD		
23	2	R7 R20	2512 (6332 metric)	CHIP RESISTOR SMD		
24	8	R8 R9 R11 R12 R21 R22 R24 R25		N.M.	N.M.	N.M.
25	4	R10 R13 R23 R26	0603 (1608 Metric)	CHIP RESISTOR SMD 1% 1/10W 0603		

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
26	14	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14	0.100" Dia x 0.180" L (2.54mm x 4.57mm)	TEST POINT PC MINI .040"D RED	ANY	ANY
27	2	U1 U2	8-SOIC (0.295", 7.50mm Width), SO 8 WIDE 300	Galvanically isolated 4 A single gate driver for SiC MOSFETs	ST	STGAP2SICSC

Table 32. STDES-DABBIDIR control board

Item	Q.ty	Ref.	Value	Description	Manufacturer	Order code
1	1	CN56	Jtag_SWD_Adapter	10 Way, 2 Row, Vertical Pin Header	Wurth	62201021121
2	20	C3,C6,C7,C28,C34,C36,C37,C45,C48,C49,C51,C52,C53,C55,C59,C61,C62,C65,C66,C134	100nF	Multilayer Ceramic Capacitor MLCC	Wurth	885012206046
3	7	C2,C27,C35,C47,C50,C58,C64	1uF	Multilayer Ceramic Capacitor MLCC	Wurth	885012206076
4	17	C11,C12,C13,C14,C20,C21,C22,C24,C30,C31,C32,C33,C38,C40,C42,C43,C140	100pF	Multilayer Ceramic Capacitor MLCC	Wurth	885012006057
5	1	C135	220nF	Multilayer Ceramic Capacitor MLCC	ANY	ANY
6	1	C18	470nF	Multilayer Ceramic Capacitor MLCC	Wurth	885012207102
7	3	C15,C23,C29	2.2nF	Multilayer Ceramic Capacitor MLCC	KEMET	C0603C222J5GACTU
8	1	C133	10uF	Multilayer Ceramic Capacitor MLCC	ANY	ANY
9	7	D2,D4,D5,D9,D12,D13,D15	GREEN	Green LED	Wurth	150080GS75000
10	2	D3,D10	SMAJ5.0A-TR, SMA	Uni-Directional TVS Diode,	ST	SMAJ5.0A-TR
11	1	D7	RED	Red LED	Wurth	150080RS75000
12	5	F1,F2,F3,F4,F5	22Ohm@100MHz	Ferrite Beads	Wurth	742792021

Item	Q.ty	Ref.	Value	Description	Manufacturer	Order code
13	2	JP1,JP7	3JP_pcb	Solder Jumper Selector	Solder Jumper Selector	Solder Jumper Selector
14	1	JP2	STRIP_2X3	Solder Jumper Selector	Solder Jumper Selector	Solder Jumper Selector
15	1	J1	i2C	4 Way, 1 Row, Straight Pin Header	Wurth	61300411121
16	2	J2,J3	CON4	4 Way, 1 Row, Straight Pin Header	Wurth	61300411121
17	1	LED1	SMTL4-SBC	LED Bivar, Verde, rosso, SMD, 2,4 V, 2 Led, PLCC 4	BIVAR	SMTL4-SBC
18	1	L1	WE-CBF	Ferrite Bead	WE	74279262
19	1	P1	CON 64 male	Multipole plug	ERNI	533406
20	13	R2,R4,R5,R8,R10,R13,R16,R19,R44,R125,R128,R129,R130	10k	Thick Film SMD Resistor	ANY	ANY
21	36	R6,R7,R9,R12,R14,R15,R20,R21,R22,R24,R25,R26,R27,R28,R29,R31,R33,R34,R36,R38,R40,R41,R42,R43,R47,R48,R49,R52,R54,R55,R57,R58,R59,R60,R61,R62	N.M.	RESISTOR	ANY	ANY
22	10	R17,R39,R45,R46,R50,R51,R53,R56,R131,R133	1k	Thick Film SMD	ANY	ANY
23	7	R23,R30,R35,R126,R127,R134,R135	0	Thick Film SMD Resistor	ANY	ANY
24	2	S1,S2	te_fsm4jsma	Button Tactile Switch, Single Pole Single Throw (SPST)	TE Connectivity	FSM4JSMATR
25	26	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22,TP24,TP25,TP26,TP27	TestPoint	Test Terminal	ANY	ANY
26	1	USB2	microUSB	Micro USB Connector Receptacle	MOLEX	47346-0001
27	5	U2,U5,U6,U9,U10	TSV912IDT, SO-8	Op Amp	ST	TSV912IDT

Item	Q.ty	Ref.	Value	Description	Manufacturer	Order code
28	1	U3	LD29080S33R, PPACK 5	LDO Voltage Regulators	ST	LD29080S33R
29	1	U23	STM32G474RETx_3TTC_EVAL, LQFP 64 10x10x1.4 mm	STM32G474RET3	ST	STM32G474RE
30	1	U22	ESDAL, SOT23-3L	Dual-Element Uni-Directional TVS Diode	ST	ESDA6V1L
31	1	PCB	FR4 4 LAYER	PCB FR4- 4 Layer size 98x48x1.6mm		

Revision history

Table 33. **Document revision history**

Date	Version	Changes
04-Dec-2023	1	Initial release.
19-Nov-2025	2	Updated Section 5.3.2: Total resonance inductance

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