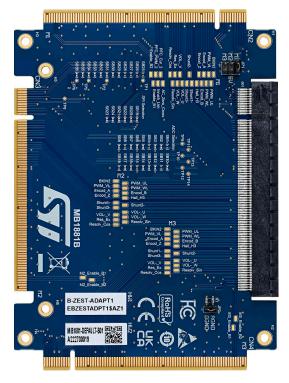


### Adapter board for STM32 ZeST motor-control boards

#### Introduction

The B-ZEST-ADAPT1 adapter board expands the abilities of control cards using a V2 motor-control connector (PCIe x16) by splitting the command signals into three connectors, enabling up to three power board management.

Figure 1. B-ZEST-ADAPT1 top view



Pictures are not contractual.

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Figure 2. B-ZEST-ADAPT1 bottom view





#### 1 Features

- V2 motor-control connector splitter to three connectors allowing up to three motor board operation
- Signal configuration through solder bridges (SPI, ADC)
- Separate analog and digital ground planes for isolated operations with compatible boards

B-ZEST-ADAPT1 adapter board connects motor-control boards with embedded STM32 32-bit microcontrollers based on the Arm<sup>®</sup> Cortex<sup>®</sup>-M processor.

This board is compatible with the new generation of STM32 motor-control boards, to be used in association with B-G473E-ZEST1S and B-DRIVE-LVLP01. For further information, refer to the STM32 motor-control ecosystem webpage at <a href="https://www.st.com">www.st.com</a>.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

arm

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## 2 Ordering information

To order the B-ZEST-ADAPT1 adapter board, refer to Table 1.

Table 1. List of available products

Order code	Board reference
B-ZEST-ADAPT1	MB1881

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## 3 Conventions

Table 2 provides the conventions used for the ON and OFF settings in the present document.

Table 2. ON/OFF convention

Convention	Definition	
Jumper JPx ON	Jumper fitted	
Jumper JPx OFF	Jumper not fitted	
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2	
Solder bridge SBx ON	SBx connections closed by 0 $\Omega$ resistor	
Solder bridge SBx OFF	SBx connections left open	
Resistor Rx ON	Resistor soldered	
Resistor Rx OFF	Resistor not soldered	
Capacitor Cx ON	Capacitor soldered	
Capacitor Cx OFF	Capacitor not soldered	

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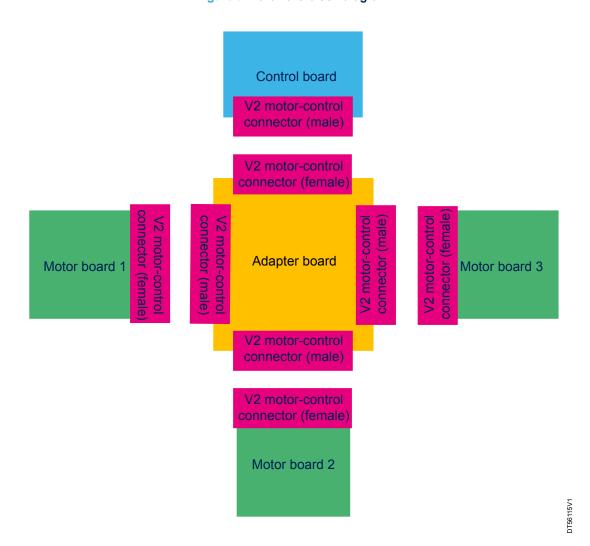
#### 4 Hardware layout and configuration

The purpose of the B-ZEST-ADAPT1 adapter board is to extend the signals from a control board using the V2 motor-control connector to up to three motor boards.

Figure 3 illustrates how a complete system (one control board, one adapter board, and three motor boards) must be connected.

Figure 4 gives a picture of a complete system.

Figure 3. Hardware block diagram



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Figure 4. Full system picture





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#### 4.1 PCB layout

Figure 5. Adapter board top view



Figure 5 shows in pink the solder bridges setting the signal configuration according to Table 4 and Table 5.

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Figure 6. Adapter board bottom view

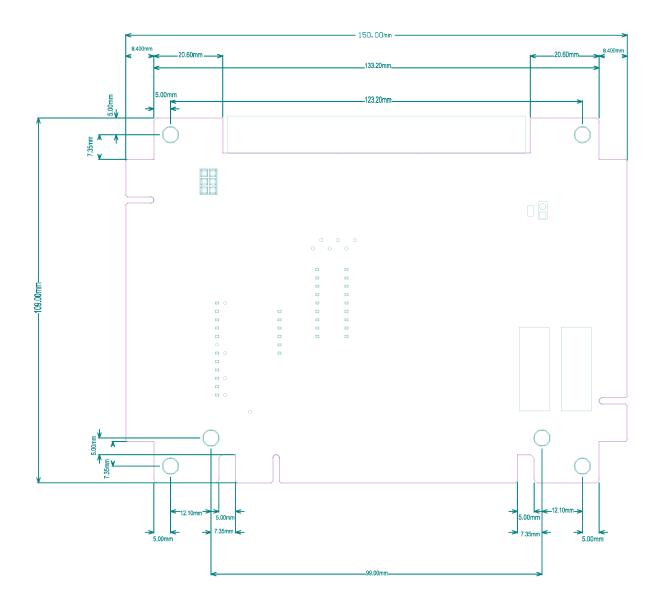


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## 4.2 Mechanical drawing

Figure 7. B-ZEST-ADAPT1adapter board mechanical drawing (in millimeters)



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#### 4.3 Default settings

Table 3. Jumpers default setting

Jumper	Default state	Comment
JP1	[5-6]	Control board powered from the M1 board
JP2	ON	Joined AGND/DGND

Table 4. Solder bridge default settings for ADC channel selection

Solder bridge	Default state	Comment	
SB1, SB2, and SB3	SB1 ON	ADC1 is linked to board M1	
351, 352, and 353	SB2 and SB3 OFF	ADCT IS IIIREU to board WT	
SB4, SB5, and SB6	SB4 ON	ADC2 is linked to board M1	
354, 353, and 350	SB5 and SB6 OFF	ADG2 is linked to board WT	
SB7, SB8, and SB9	SB8 ON	ADC3 is linked to board M2	
367, 360, and 369	SB7 and SB9 OFF	ADCS IS III KEU to board Wiz	
SB10, SB11, and SB12	SB11 ON	ADC4 is linked to board M2	
3510, 3511, and 3512	SB10 and SB12 OFF	ADO4 IS IIIREU to board Wiz	
SB13, SB14, and SB15	SB15 ON	ADC5 is linked to board M3	
OB 10, OB 14, and OB 13	SB13 and SB14 OFF	ADOS IS IIINCU to board Wis	
SB16, SB17, and SB18	SB18 ON	ADC6 is linked to board M3	
0510, 0517, and 0510	SB16 and SB17 OFF	ADOUG INTINGE TO DOUGH INTO	

Table 5. Solder bridge default settings for SPI channel selection

Solder bridge	Default state	Comment
SB25 and SB27	Both ON	SPI1 linked to board M1
SB29 and SB31	Both OFF	Not connected
SB33 and SB35	Both OFF	Not connected
SB26 and SB28	Both ON	SPI2 linked to board M1
SB30 and SB32	Both OFF	Not connected
SB34 and SB36	Both OFF	Not connected
SB19 and SB20	Both OFF	Not connected
SB21 and SB22	Both OFF	Not connected
SB23 and SB24	Both OFF	Not connected

Warning: Only one board must be enabled for an SPI connection to avoid conflict.

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## 4.4 Configuration

Table 6. ADC selection configuration

Channel	Solder bridge	State	Comment
100	SB1	ON	Connected to board M1
		OFF	Not connected
	CDO	ON	Connected to board M2
ADC1	SB2	OFF	Not connected
	SB3	ON	Connected to board M3
	563	OFF	Not connected
	SB4	ON	Connected to board M1
	5B4	OFF	Not connected
ADC2	SB5	ON	Connected to board M2
ADC2	565	OFF	Not connected
	SB6	ON	Connected to board M3
	SB0	OFF	Not connected
	CD7	ON	Connected to board M1
	SB7	OFF	Not connected
ADC3	SB8	ON	Connected to board M2
ADC3	SB0	OFF	Not connected
	CDO	ON	Connected to board M3
	SB9	OFF	Not connected
	0040	ON	Connected to board M1
	SB10	OFF	Not connected
ADC4	CD44	ON	Connected to board M2
ADC4	SB11	OFF	Not connected
	0040	ON	Connected to board M3
	SB12	OFF	Not connected
	0040	ON	Connected to board M1
	SB13	OFF	Not connected
ADOF	CD44	ON	Connected to board M2
ADC5	SB14	OFF	Not connected
	CD45	ON	Connected to board M3
	SB15	OFF	Not connected
	0040	ON	Connected to board M1
	SB16	OFF	Not connected
ADCC	05:-	ON	Connected to board M2
ADC6	SB17	OFF	Not connected
	SB18	ON	Connected to board M3
		OFF	Not connected
	· · · · · · · · · · · · · · · · · · ·	•	

Warning: Only one solder bridge must be ON for each channel to avoid conflict.

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The JP1 jumper is used to select which power board powers the control board.

Table 7. Power configuration (JP1)

JP1 <sup>(1)</sup>	Comment
[1-2]	Power from the M3 board
[3-4]	Power from the M2 board
[5-6]	Power from the M1 board

<sup>1.</sup> The default configuration is in bold.

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#### 5 Connectors

#### 5.1 PCle 16x control-board connector (CN1)

Figure 8. PCle 16x female connector

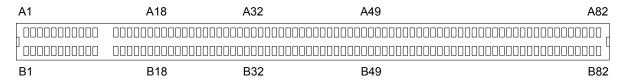


Table 8. PCI-e 16x pinout for the control-board connector (CN1)

-	Pin	A raw	B row
	1	SPI1_nSS	SPI1_MISO
	2	SPI1_SCK	SPI1_MOSI
	3	SPI2_nSS	SPI2_MISO
	4	SPI2_SCK	SPI2_MOSI
	5	5V_to_CTRLB	5V_to_CTRLB
	6	3V3_to_PWRB	VREF+
	7	DGND	DGND
	8	ID_Enable	AGND
	9	ADC1	ADC4
1x	10	ADC2	ADC5
	11	ADC3	ADC6
		Notch	
	12	M1_BKIN	M1_BKIN2
	13	M1_PWM_UH	M1_PWM_UL
	14	M1_PWM_VH	M1_PWM_VL
	15	M1_PWM_WH	M1_PWM_WL
	16	M1_Master_EN	M1_Encoder_A
	17	M1_Timer_ETR	M1_Encoder_B
	18	M1_Hall_H1	M1_Encoder_Z
	19	M1_Hall_H2	M1_Hall_H3
	20	DGND	DGND
	21	M1_SHUNT1+	M1_SHUNT1-
	22	M1_SHUNT2+	M1_SHUNT2-
	23	M1_SHUNT3+	M1_SHUNT3-
4x	24	AGND	AGND
	25	M1_VOL+_U	M1_VOLU
	26	M1_VOL+_V	M1_VOLV
	27	M1_VOL+_W	M1_VOLW
	28	M1_TEMP_ID	M1_Res.Ex
	29	M1_VBUS	M1_Resolver_Sin

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	Pin	A raw	B row
	30	M1_D_Brake	M1_Resolver_Cos
4x	31	DGND	DGND
	32	AGND	AGND
	33	AC_Voltage	AC_Zero_Crossing
	34	PFC_Current_1	PFC_Current_2
	35	PFC_BKIN_OC	Inrush_Lim
	36	PFC_PWM_1	PFC_PWM_2
	37	M2_BKIN	M2_BKIN2
	38	M2_PWM_UH	M2_PWM_UL
	39	M2_PWM_VH	M2_PWM_VL
	40	M2_PWM_WH	M2_PWM_WL
8x	41	M2_Master_EN	M2_Encoder_A
	42	M2_Timer_ETR	M2_Encoder_B
	43	M2_Hall_H1	M2_Encoder_Z
	44	M2_Hall_H2	M2_Hall_H3
	45	DGND	DGND
	46	M2_SHUNT1+	M2_SHUNT1-
	47	M2_SHUNT2+	M2_SHUNT2-
	48	M2_SHUNT3+	M2_SHUNT3-
	49	AGND	AGND
	50	M2_VOL+_U	M2_VOLU
	51	M2_VOL+_V	M2_VOLV
	52	M2_VOL+_W	M2_VOLW
	53	M2_TEMP_ID	M2_Res.Ex
	54	M2_VBUS	M2_Resolver_Sin
	55	M2_D_Brake	M2_Resolver_Cos
	56	DGND	DGND MO. RIKINO
	57	M3_BKIN	M3_BKIN2
	58	M3_PWM_UH	M3_PWM_UL
	59	M3_PWM_VH	M3_PWM_VL
16x	60	M3_PWM_WH	M3_PWM_WL
	61	M3_Master_EN	M3_Encoder_A
	62	M3_Timer_ETR	M3_Encoder_B
	63	M3_Hall_H1	M3_Encoder_Z
	64	M3_Hall_H2	M3_Hall_H3
	65	DGND	DGND
	66	M3_SHUNT1+	M3_SHUNT1-
	67	M3_SHUNT2+	M3_SHUNT2-
	68	M3_SHUNT3+	M3_SHUNT3-
	69	AGND	AGND
	70	M3_VOL+_U	M3_VOLU

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-	Pin	A raw	B row
	71	M3_VOL+_V	M3_VOLV
	72	M3_VOL+_W	M3_VOLW
	73	M3_TEMP_ID	M3_Res.Ex
	74	M3_VBUS	M3_Resolver_Sin
	75	M3_D_Brake	M3_Resolver_Cos
16x	76	DGND	AGND
TOX	77	M1_SPI_nSS	M1_Enable_B1
	78	M1_Enable_A	M1_Enable_B2
	79	M2_SPI_nSS	M2_Enable_B1
	80	M2_Enable_A	M2_Enable_B2
	81	M3_SPI_nSS	M3_Enable_B1
	82	M3_Enable_A	M3_Enable_B2

### 5.2 PCIe 16x motor-board connectors (CN2, CN3, and CN4)

Table 9. PCI-e 16x pin out for motor-board connectors (CN2, CN3, and CN4)

-	Pin	A raw	B raw	
	1	Mx_SPI1_nSS	Mx_SPI1_MISO	
	2	Mx_SPI1_SCK	Mx_SPI1_MOSI	
	3	Mx_SPI2_nSS	Mx_SPI2_MISO	
	4	Mx_SPI2_SCK	Mx_SPI2_MOSI	
	5	Mx_5V	Mx_5V	
	6	3V3_to_PWRB	VREF+	
	7	DGND	DGND	
	8	ID_Enable	AGND	
	9	Mx_ADC1	Mx_ADC4	
1x	10	Mx_ADC2	Mx_ADC5	
	11	Mx_ADC3	Mx_ADC6	
	Notch			
	12	Mx_BKIN	Mx_BKIN2	
	13	Mx_PWM_UH	Mx_PWM_UL	
	14	Mx_PWM_VH	Mx_PWM_VL	
	15	Mx_PWM_WH	Mx_PWM_WL	
	16	Mx_Master_EN	Mx_Encoder_A	
	17	Mx_Timer_ETR	Mx_Encoder_B	
	18	Mx_Hall_H1	Mx_Encoder_Z	
	19	Mx_Hall_H2	Mx_Hall_H3	
	20	DGND	DGND	
4x	21	Mx_SHUNT1+	Mx_SHUNT1-	
	22	Mx_SHUNT2+	Mx_SHUNT2-	
	23	Mx_SHUNT3+	Mx_SHUNT3-	

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	Pin	A raw	B raw
	24	AGND	AGND
	25	Mx_VOL+_U	Mx_VOLU
	26	 Mx_VOL+_V	Mx_VOLV
	27	 Mx_VOL+_W	Mx_VOLW
4x	28	Mx_TEMP_ID	Mx_Res.Ex
	29	Mx_VBUS	Mx_Resolver_Sin
	30	 Mx_D_Brake	Mx_Resolver_Cos
	31	DGND	DGND
	32	AGND	AGND
	33	AC_Voltage (Only for M1)	AC_Zero_Crossing (Only for M1)
	34	PFC_Current_1 (Only for M1)	PFC_Current_2 (Only for M1)
	35	PFC_BKIN_OC (Only for M1)	Inrush_Lim (Only for M1)
	36	PFC_PWM_1 (Only for M1)	PFC_PWM_2 (Only for M1)
	37	NC	NC
	38	NC	NC
	39	NC	NC
	40	NC	NC
8x	41	NC	NC
	42	NC	NC
	43	NC	NC
	44	NC	NC
	45	DGND	DGND
	46	NC	NC
	47	NC	NC
	48	NC	NC
	49	AGND	AGND
	50	NC	NC
	51	NC	NC
	52	NC	NC
	53	NC	NC
	54	NC	NC
	55	NC	NC
	56	DGND	DGND
16x	57	NC	NC
	58	NC	NC
	59	NC	NC
	60	NC	NC
	61	NC	NC
	62	NC	NC
	63	NC	NC
	64	NC	NC

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-	Pin	A raw	B raw
	65	DGND	DGND
	66	NC	NC
	67	NC	NC
	68	NC	NC
	69	AGND	AGND
	70	NC	NC
	71	NC	NC
	72	NC	NC
16x	73	NC	NC
TOX	74	NC	NC
	75	NC	NC
	76	DGND	AGND
	77	Mx_SPI_nSS	Mx_Enable_B1
	78	Mx_Enable_A	Mx_Enable_B2
	79	NC	NC
	80	NC	NC
	81	NC	NC
	82	NC	NC

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#### 6 B-ZEST-ADAPT1 product information

#### 6.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

 First sticker: product order code and product identification, generally placed on the main board featuring the target device.

Example:

Product order code Product identification

Second sticker: board reference with revision and serial number, available on each PCB.
 Example:





On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: "MBxxxx-Variant-yzz", where "MBxxxx" is the board reference, "Variant" (optional) identifies the mounting variant when several exist, "y" is the PCB revision, and "zz" is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as "ES" or "E" are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"ES" or "E" marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

#### 6.2 B-ZEST-ADAPT1 product history

**Table 10. Product history** 

Order code	Product identification	Product details	Product change description	Product limitations
B-ZEST-ADAPT1	BZESTADAPT1\$AZ1	Board: • MB1881-DEFAULT-B01	Initial revision	No limitation

#### 6.3 Board revision history

Table 11. Board revision history

Board reference	Board variant and revision	Board change description	Board limitations
MB1881	MB1881-DEFAULT-B01	Initial revision	No limitation

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### **Revision history**

Table 12. Document revision history

Date	Version	Changes
27-Jan-2023	1	Initial release.

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