Evaluation board with STM32U575AI MCU

Introduction

The STM32U575I-EV Evaluation board is designed as a complete demonstration and development platform for the STMicroelectronics Arm® Cortex®-M33 core-based microcontroller with Arm® TrustZone® and the Armv8-M mainline security extension.

The STM32U575I-EV Evaluation board is based on an ultra-low-power STM32U575AII6Q microcontroller with 2 Mbytes of flash memory and 786 Kbytes of SRAM, one external memory interface supporting an LCD interface, two Octo-SPI memory interfaces, one USB Type-C® 2.0 FS device and host with Power Delivery controller interface (UCPD) compliant with USB Type-C® r1.2 and USB PD specification r3.0, one camera interface, one SDMMC interface, one 14-bit and one 12-bit ADCs, two 12-bit DACs, two operational amplifiers, two ultralow-power comparators, four digital filters for sigma-delta modulation, up to 16 timers, touchkey capability, and SWD, JTAG, and ETM interface debugging support.

The full range of hardware features on the STM32U575I-EV Evaluation board helps the user to develop applications and evaluate all the peripherals, such as USB Type-C® connector with USB PD, motor control connector, CAN FD transceiver, USB 2.0 FS, RS-232, audio DAC, microphone ADC, dot-matrix TFT LCD, IrDA, IR LED, IR receiver, LDR, SRAM, camera interface, Octo-SPI flash memory, microSD™ card, sigma-delta modulators, smartcard slot, I²C, and EEPROM.

The daughterboard and extension connectors provide an easy way to connect a daughterboard or wrapping board for the user's specific application.

Furthermore, the onboard STLINK-V3E debugger provides out-of-the-box loading and debugging capabilities, as well as a USB Virtual COM port bridge.

Figure 1. STM32U575I-EV Evaluation board top view

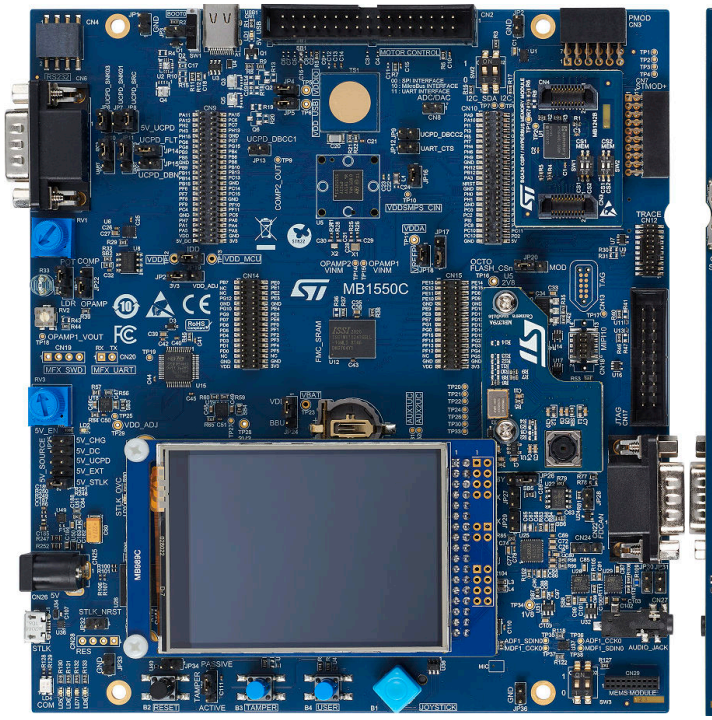
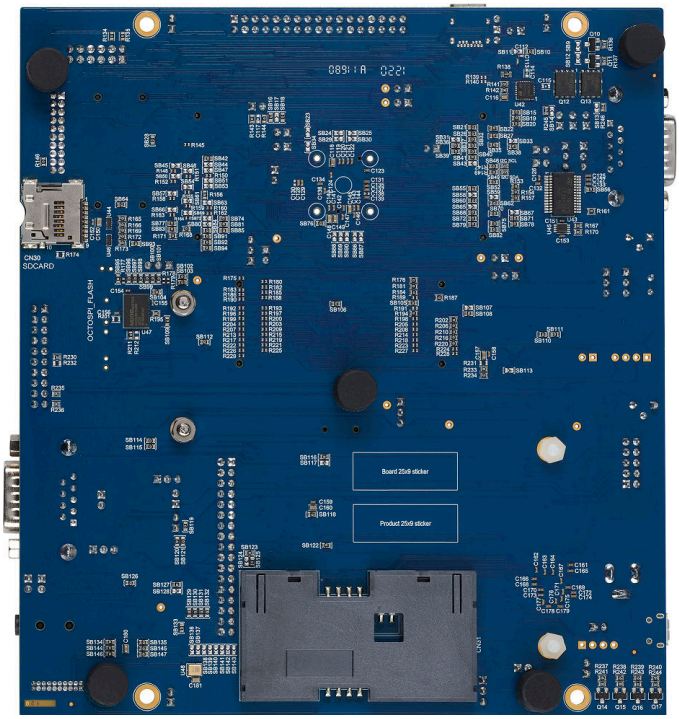


Figure 2. STM32U575I-EV Evaluation board bottom view



Pictures are not contractual.

1 Features

- STM32U575AII6Q Arm® Cortex®-M33 core-based microcontroller including Arm® TrustZone® with 2 Mbytes of flash memory, 786 Kbytes of SRAM, and an embedded SMPS in a UFBGA169 package
- 2.8” 240x320 pixel-262K color parallel port TFT LCD touch-panel module
- QSXGA 5-megapixel CMOS camera
- USB Type-C® FS, 5 V/500 mA sink and source power capability
- SAI audio codec
- MEMS digital microphone
- MEMS 3D accelerometer and 3D gyroscope
- Light-dependent resistor (LDR) and potentiometer for ADC
- 512-Mbit Octo-SPI flash memory, 16-Mbit SRAM, 128-Kbit I^2C EEPROM
- Power-metering demonstration with dual-channel sigma-delta modulator
- 4 user LEDs
- Reset, tamper, and user buttons
- 4-direction joystick with selection button
- Touchkey button
- Board connectors:
  - 5 V power jack
  - USB Type-C®
  - RS-232 communication and I^2C compatible serial interface
  - CAN FD
  - Stereo audio jack including analog microphone input
  - Connector for ADC input and DAC output
  - Smartcard socket
  - microSD™ card holder
  - Coin-battery cell holder for power backup
  - JTAG and ETM trace debugger connector
  - 8-bit camera expansion connector
  - Octo-SPI expansion connectors
  - Pmod™ and STMod+ expansion connectors
  - Audio MEMS expansion connector
  - Motor-control interface expansion connector
  - Expansion connectors for daughterboard or wire-wrap board
- Flexible power-supply options: ST-LINK USB V_{BUS}, USB connector, or external sources
- On-board STLINK-V3E debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeU5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR Embedded Workbench®, MDK-ARM, and STM32CubeIDE

Note: Arm and TrustZone are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the STM32U575I-EV Evaluation board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. List of available products

Order code	Board reference	Target STM32
STM32U575I-EV	• MB1550(1) • MB989(2) • MB1242(3) • MB1379(4)	STM32U575AII6Q

1. *Main board*
2. *LCD daughterboard*
3. *Octo-SPI memory daughterboard*
4. *Camera daughterboard*

2.1 Codification

The meaning of the codification is explained in Table 2.

Table 2. Codification explanation

STM32XXYYZ-EV	Description	Example: STM32U575I-EV
XX	MCU series in STM32 32-bit Arm Cortex MCUs	STM32U5 series
YY	MCU product line in the series	STM32U575/585
Z	STM32 flash memory size: • I for 2 Mbytes	2 Mbytes
EV	Evaluation board	Evaluation board

3 Development environment

3.1 System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

Note: *macOS® is a trademark of Apple Inc., registered in the U.S. and other countries and regions.*

Linux® is a registered trademark of Linus Torvalds.

Windows is a trademark of the Microsoft group of companies.

3.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench®(1)
- Keil® - MDK-ARM(1)
- STMicroelectronics - STM32CubeIDE

1. *On Windows® only.*

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

5 Delivery recommendations

Before the first use, make sure that no damage occurred to the board during shipment and that no socketed components are loosened in their sockets or fallen into the plastic bag. In particular, pay attention to the following components:

1. The MB989 LCD daughterboard is in its CN23 connector, and the LCD screw, spacer, and nut are in place.
2. The MB1242 Octo-SPI memory daughterboard is in its CN5/CN11 connectors.
3. The MB1379 CMOS camera daughterboard is in its CN16 connector and the LCD screw, spacer, and nut are in place.

6 Getting started

Follow the sequence below to configure the STM32U575I-EV Evaluation board and launch the demonstration application (refer to Figure 3 for component location):

1. Check the jumper position on the board (refer to Figure 6. Jumper default board configuration).
2. For the correct identification of the device interfaces from the host PC and before connecting the board, install the STLINK-V3E USB driver available on the *www.st.com* website.
3. Connect the STM32U575I-EV Evaluation board to a PC with a USB Type-A or USB Type-C® to Micro-B cable through the STLINK-V3E USB connector (CN26) to power the board.
4. The LD2 green LED (5V_PWR) lights up and the LD4 (COM) blinks.
5. Select the menu on the screen and play with the application.
6. Download the demonstration software and several software examples that help to use the STM32U575I-EV Evaluation board features. These are available on the *www.st.com* website.
7. Develop your application using the available examples.

7 Hardware layout and configuration

7.1 Hardware block diagram and board layout

The STM32U575I-EV Evaluation board is designed around the STM32U575AII6Q target microcontroller. Figure 3 illustrates STM32U575AII6Q connections with peripheral components. Figure 4 shows the location of the main components on the top side of the Evaluation board. Figure 5 shows the location of the main components on the bottom side of the Evaluation board.

Figure 3. Hardware block diagram

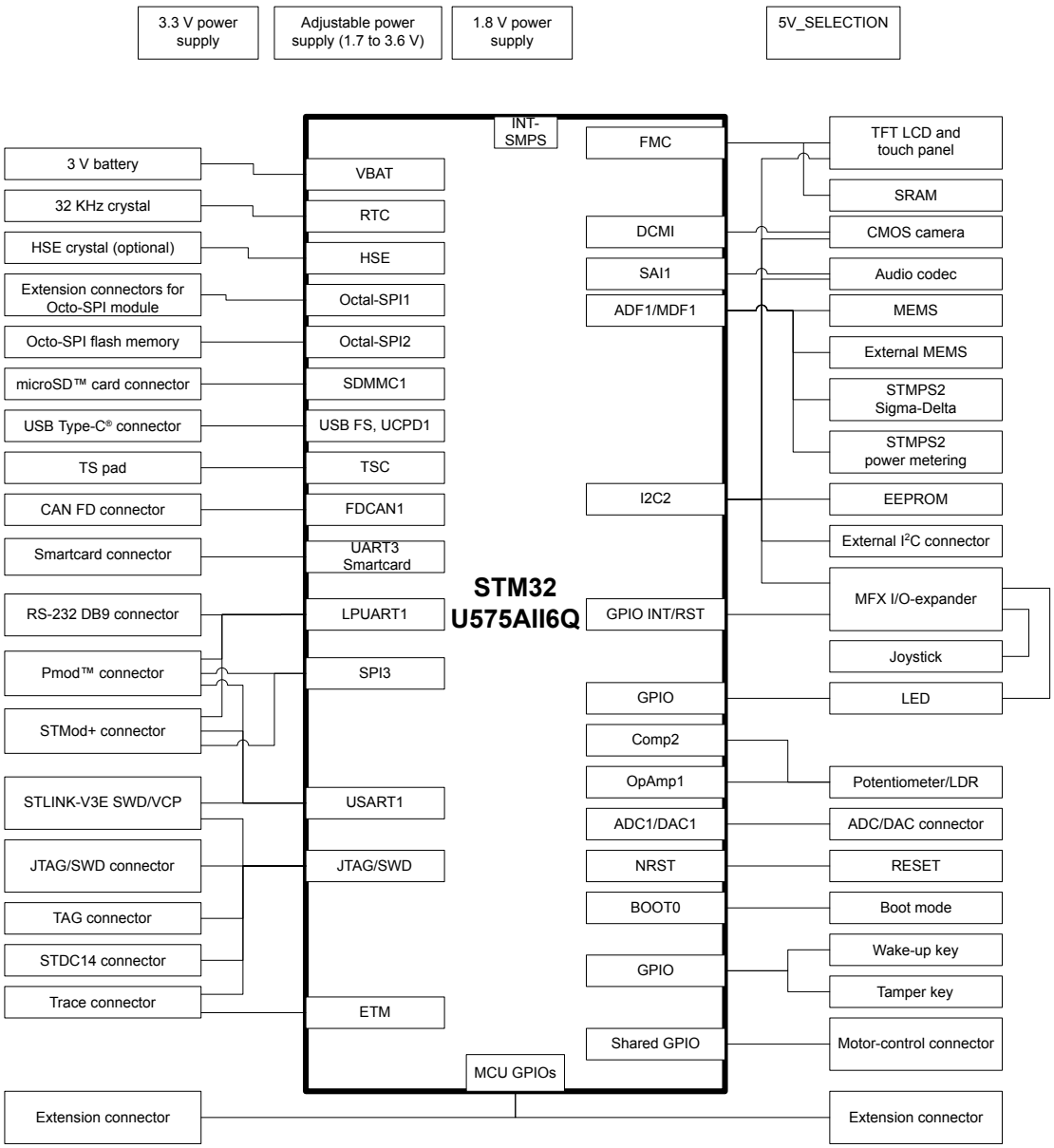


Figure 4. STM32U575I-EV PCB layout (top view)

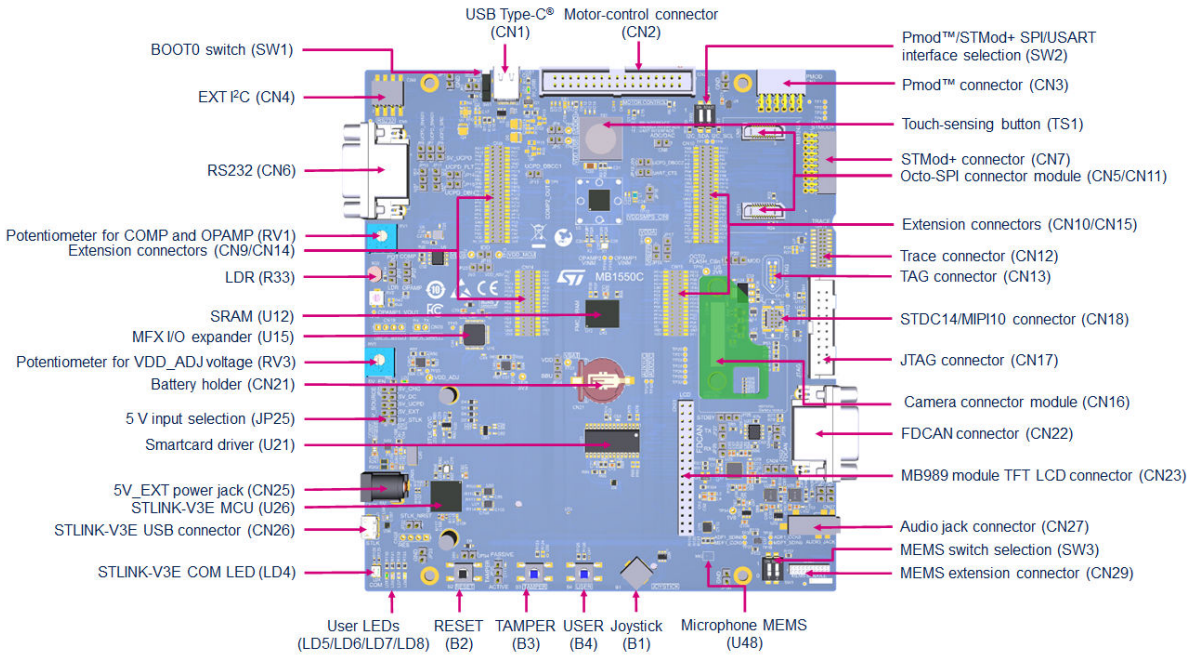
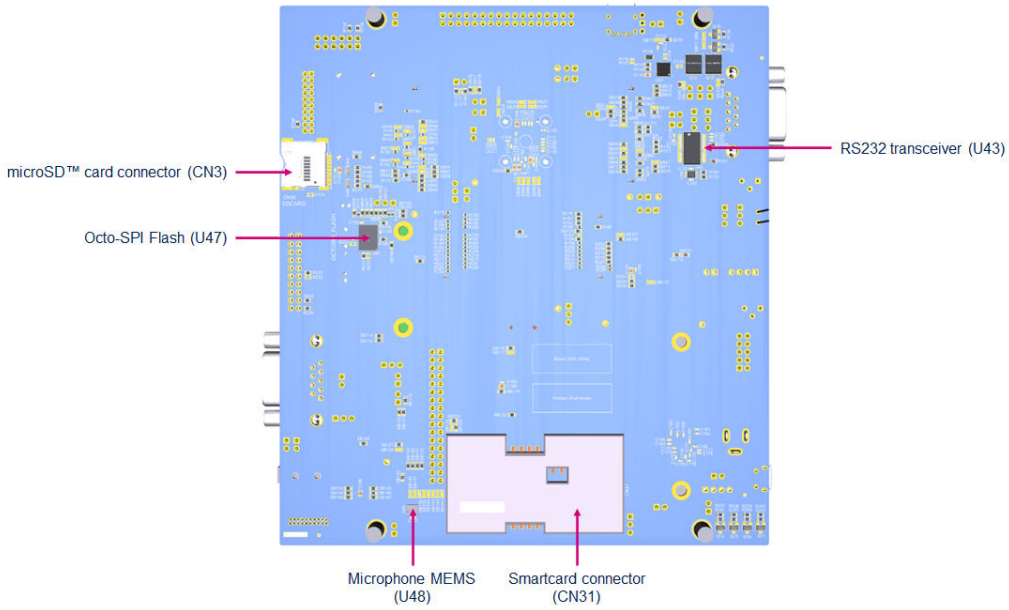


Figure 5. STM32U575I-EV PCB layout (bottom view)



7.2 Default board configuration

By default, the STM32U575I-EV Evaluation board is configured with VDD_MCU at 3.3 V. It is possible to set the board with VDD_MCU at 1.8 V. Before switching to 1.8 V, check that the extension module and external shield connected to the STM32U575I-EV Evaluation board are 1.8 V compatible.

Figure 6 summarizes the jumper default settings of the STM32U575I-EV Evaluation board.

Figure 6. Jumper default board configuration

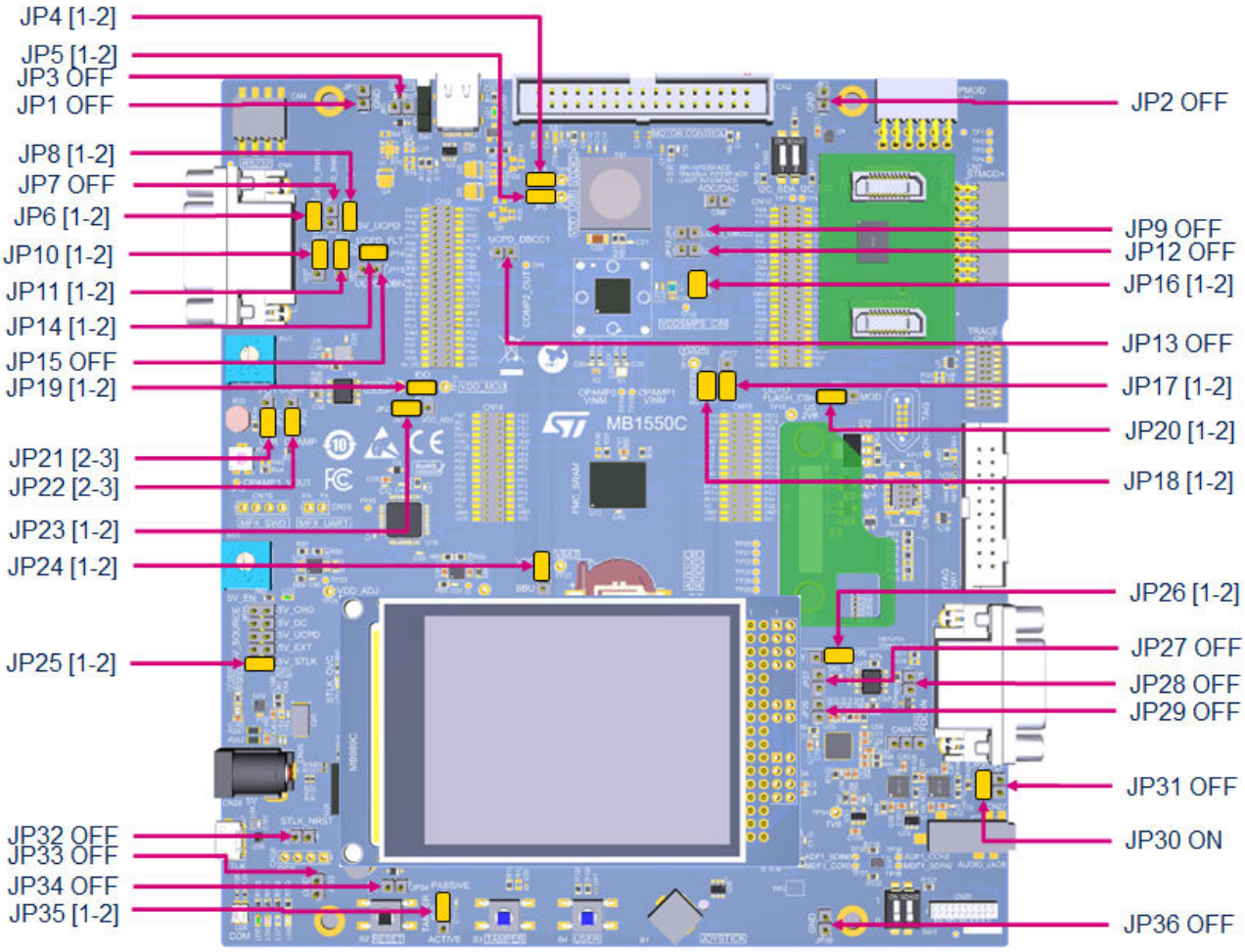


Figure 7 summarizes the switch default settings of the STM32U575I-EV Evaluation board.

Figure 7. Switch default board configuration

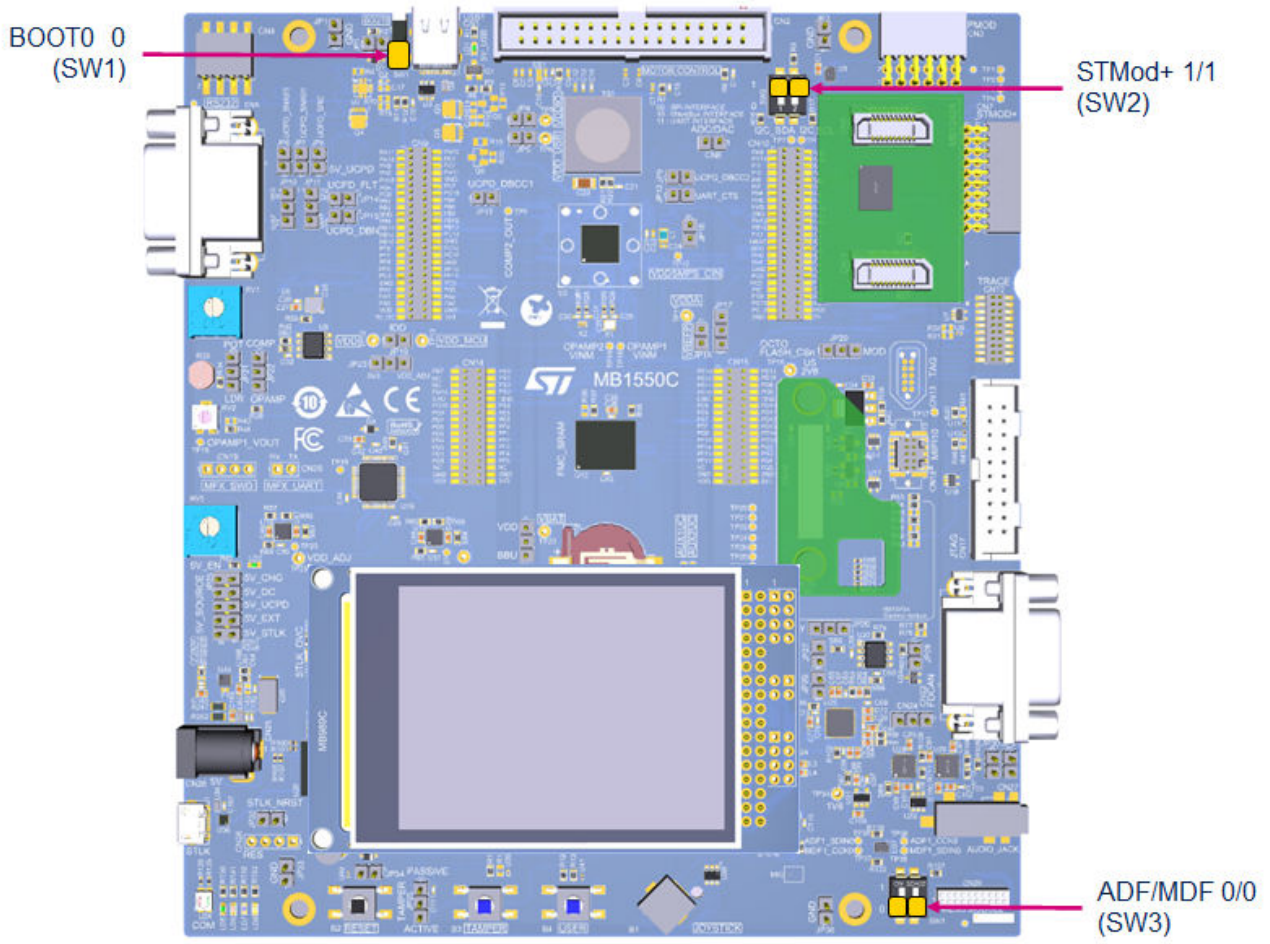


Table 4 describes the default jumper setting.

Table 4. Jumper default settings

Jumper	Function	Setting	Comment
JP1	GND probe	-	GND probe
JP2	GND probe	-	GND probe
JP3	BOOTLOADER_BOOT0 from USART	OFF	Boot 0 from USART not connected
JP4	VDDIO power source selection	ON	VDDIO connected to VDD_MCU
JP5	VDD_USB source selection	ON	VDD_USB connected to 3V3
JP6	5V_UCPD sink/source	ON	5V_UCPD connected to a SINK path
JP7	5V_UCPD sink/source	OFF	5V_UCPD not connected to TCPP01 SINK path
JP8	5V_UCPD sink/source	ON	5V_UCPD connected to TCPP03 SOURCE path
JP9	USB_DBCC2	OFF	USB_DBCC2 on PB14 not used
JP10	I^2C/UART selection	[1-2]	I2C_SCL on PG7 selected
JP11	I^2C/UART selection	[1-2]	I2C_SDA on PG8 selected
JP12	UART_CTS selection	OFF	UART_CTS not connected
JP13	USB_DBCC1	OFF	USB_DBCC1 on PB5 not used
JP14	UCPD_FLT selection	ON	UCPD_FLT on PB8 connected
JP15	UCPD_DBn	OFF	UCPD_DBn on PB9 not used
JP16	VDDSMPS_CIN power source selection	ON	VDDSMPS_CIN connected to VDD_MCU
JP17	VDDA power source selection	[1-2]	VDDA connected to VDD_MCU
JP18	VREFP power source selection	ON	VREFP connected to VDD_MCU
JP19	VDD_MCU IDD jumper	ON	VDD_MCU connected to VDD
JP20	OCTOSPI2 CSn selection	[1-2]	OCTOSPI2_NCs on PI5 used for OCTOSPI flash chip select
JP21	Potentiometer/LDR selection	[2-3]	LDR selected for COMP and OPAMP function
JP22	COMP/OPAMP selection	[2-3]	OPAMP function selected
JP23	VDD power source selection	[1-2]	VDD connected to 3V3
JP24	VBAT power source selection	[1-2]	VBAT connected to VDD
JP25	5V power source selection	[1-2]	5V connected to 5V_STLK source
JP26	FDCAN transceiver STBY selection	[1-2]	Normal mode selected
JP27	FDCAN_TX selection	OFF	FDCAN_TX not connected to PB9
JP28	FDCAN termination resistor	OFF	Termination resistor on the physical link is not connected
JP29	FDCAN_RX selection	OFF	FDCAN_RX not connected to PB8
JP30	STPMS2 for power metering data connection	ON	STPMS2 data connected to MDF interface
JP31	STPMS2 for sigma-delta data connection	OFF	STPMS2 data not connected to MDF interface
JP32	STLK_NRST	OFF	STLINK-V3E not in RESET mode
JP33	GND probe	-	GND probe
JP34	BOOTLOADER_RST from UART_DB9	OFF	RST from UART is not connected.
JP35	TAMPER selection	[1-2]	Tamper is connected to the TAMPER button. Passive mode
JP36	GND probe	-	GND probe

7.3 Embedded STLINK-V3E

7.3.1 Description

There are two different ways to program and debug the onboard STM32 MCU:

1. Using the embedded STLINK-V3E programming and debugging tool, which is on the STM32U575I-EV Evaluation board
2. Using an external debug tool connected to the STDC14/MIPI10 connector (CN18)

The STLINK-V3E makes the STM32U575I-EV Evaluation board Arm® Mbed Enabled™.

The embedded STLINK-V3E only supports SWD and VCP for STM32 devices:

- 5 V power supplied by the USB connector (CN26)
- USB 2.0 high-speed-compatible interface
- JTAG and SWD protocols compatible with 1.7 to 3.6 V application voltage and 5 V tolerant input I/Os
- Serial Wire Viewer (SWV) output
- STDC14/MIPI10 compatible connector (CN18)
- Status COM LED, which blinks during communication with the PC (LD4)
- Fault red OC LED alerting on USB overcurrent request (LD3)
- 5 V/500 mA output power supply capability with current limitation (U20)
- 5 V power green LED (LD2)

Table 5 describes the USB Micro-B connector (CN26) pinout.

Table 5. USB Micro-B connector (CN26) pinout

Pin	Pin name	Signal name	STLINK-V3E STM32 pin	Function
1	VBUS	5V_USB_CHGR	-	VBUS power
2	DM	USB_DEV_HS_CN_N	PB14	DM
3	DP	USB_DEV_HS_CN_P	PB15	DP
4	ID	-	-	Not used
5	GND	GND	GND	GND

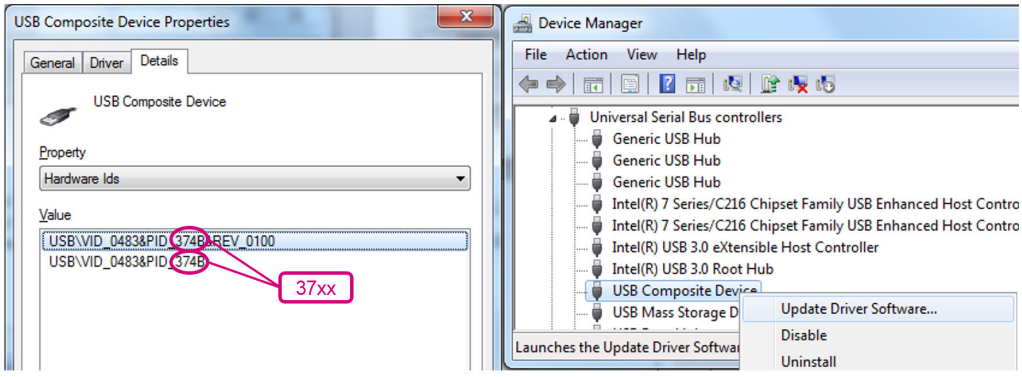
7.3.2 Drivers

Before connecting the STM32U575I-EV Evaluation board to a Windows PC via USB, the user must install a driver for the STLINK-V3E (not required for Windows 10). It is available on the *www.st.com* website.

In case the STM32U575I-EV Evaluation board is connected to the PC before the driver is installed, some STM32U575I-EV Evaluation board interfaces might be declared as *Unknown* in the PC device manager. In this case, the user must install or update the driver files, and update the driver of the connected device from the device manager as shown in Figure 8.

Note: Prefer using the USB Composite Device to handle a full recovery.

Figure 8. USB composite device



Note: 37xx:

- *374E for STLINK-V3E without bridge functions*
- *374F for STLINK-V3E with bridge functions*

7.3.3 STLINK-V3E firmware upgrade

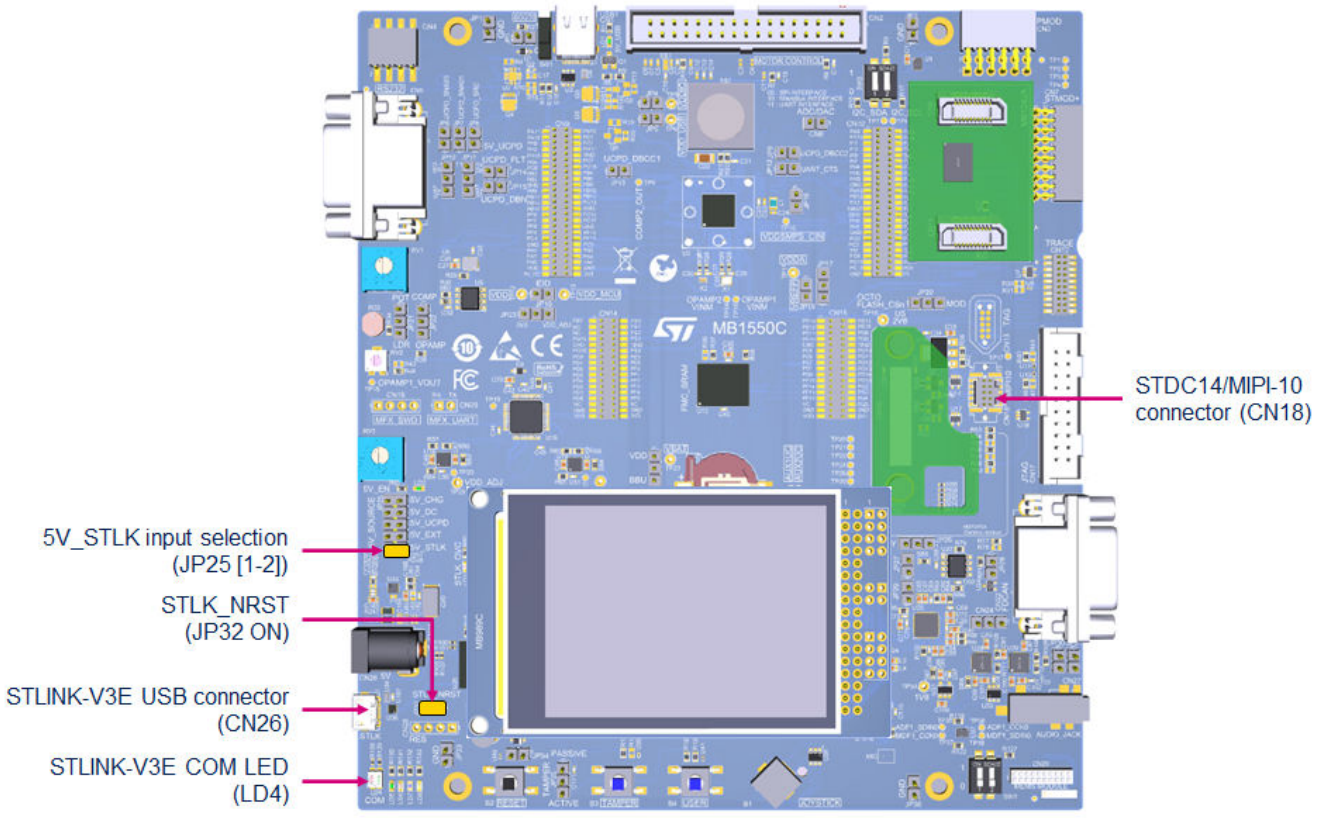
The STLINK-V3E embeds a firmware upgrade mechanism for in-place upgrades through the USB port. As the firmware might evolve during the lifetime of the STLINK-V3E product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the STM32U575I-EV Evaluation board and periodically, to stay up-to-date with the latest firmware version.

7.3.4 Using an external debugging tool to program and debug the on-board STM32

There are two basic ways to support an external debug tool:

1. Keep the embedded STLINK-V3E running. Power on the STLINK-V3E at first until the red LED COM lights. Then connect the external debugging tool through the STDC14/MIPI10 debug connector (CN18).
2. Set the embedded STLINK-V3E in the high-impedance state: When setting the STLK_NRST JP32 jumper JP32 is ON, the embedded STLINK-V3E is in the reset state and all GPIOs are set in high impedance. Then the user can connect the external debugging tool through the STDC14/MIPI10 debug connector (CN18).

Figure 9. Connecting an external debugging tool to program the onboard STM32U5



7.4 STDC14/MIPI10 connector

7.4.1 Description

The 5x2-pin 1.27 mm pitch header connector (CN18) compatible with STDC14 can output JTAG signals used for debugging.

The CN18 footprint supports the STDC14 interface and also the MIPI10 interface. By default, only a MIPI10 connector is present.

Table 6 describes the hardware configuration for the STDC14 function.

Table 6. Hardware I/O configuration for the STDC14 connector (CN18)

I/O	Solder bridge	Setting(1)	Comment
PA9	-	-	PA9 is used as USART1_TX, it is connected to T_VCP_RX.
PA10	-	-	PA10 is used as USART1_RX, it is connected to T_VCP_TX.
PA13	-	**-**	**PA13 is connected to JTAG JTMS or SWD SWDIO.**
PA14	-	**-**	**PA14 is connected to JTAG JTCK or SWD SWCLK.**
PA15	SB15	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is NOT connected to JTAG. PA15 can be used for UCPB.
PB3	SB114	**ON**	**PB3 is connected to JTAG JTDO or SWD SWO.**
		OFF	PB3 is NOT connected to JTAG or SWD. PB3 can be used for audio MEMS
NRST		**ON**	**NRST is used to reset the target.**

1. *The default configuration is in bold.*

Figure 10 shows the STDC14 connector (CN18) pinout.

Figure 10. STDC14 connector (CN18) pinout

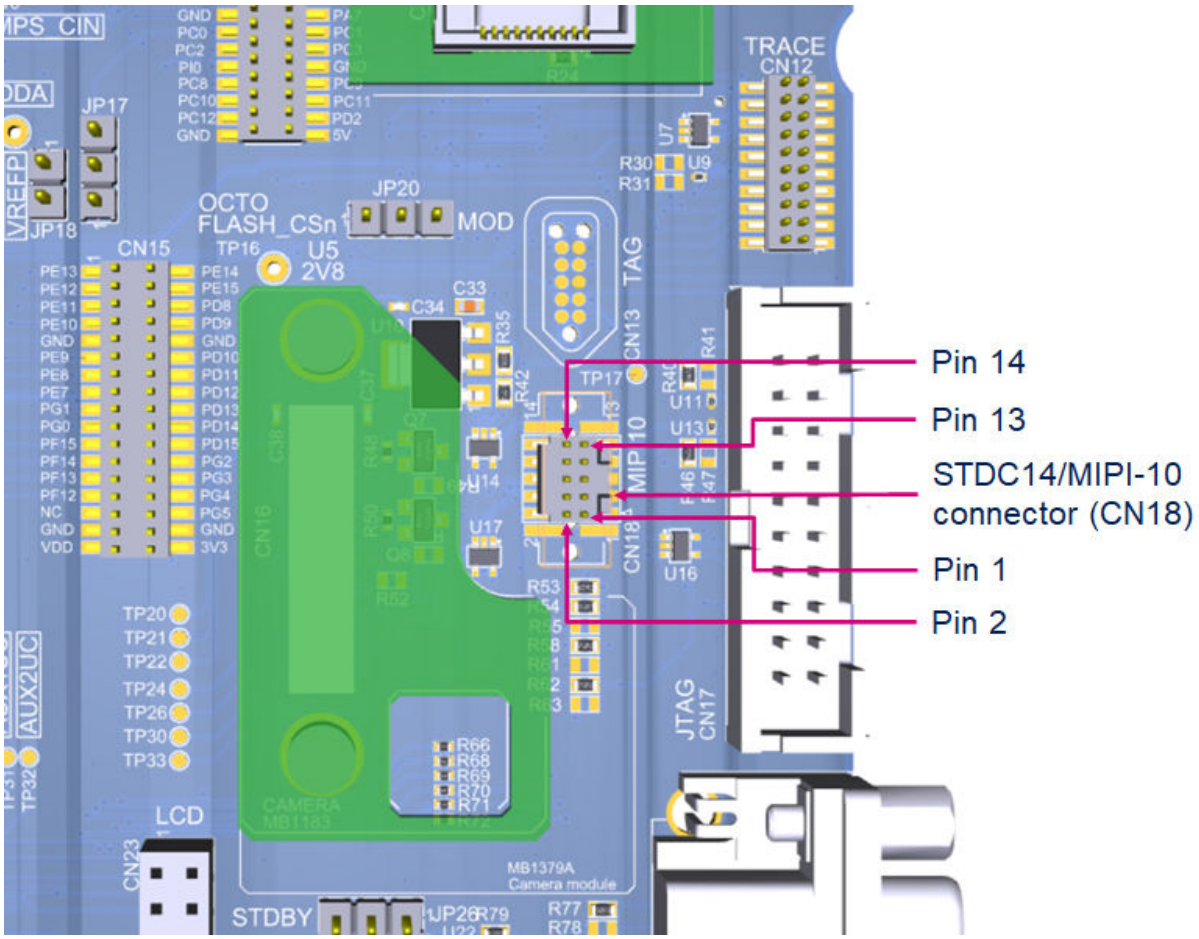


Table 7 describes the STDC14/MIPI10 connector pinout compatible with both STDC14 and MIPI10 interfaces.

Table 7. STDC14/MIPI10 debug connector (CN18) pinout

MIPI10 pin	STDC14 pin	STM32 pin	Board function
-	1	-	Reserved
-	2	-	Reserved
1	3	VDD	Target VDD
2	4	PA13	JTMS_SWDIO: Target SWDIO using SWD protocol or target JTMS using JTAG protocol
3	5	GND	Ground
4	6	PA14	JTCK_SWCLK: Target SWCLK using SWD protocol or target JTCK using JTAG protocol
5	7	GND	Ground
6	8	PB3	JTDO_SWO: Target SWO using SWD protocol or target JTDO using JTAG protocol
7	9	-	NC
8	10	PA15	JTDI: Not used by SWD protocol, target JTDI using JTAG protocol, only for external tools
9	11	-	GNDDetect: GND detection for plug indicator, used on SWD and JTAG neither
10	12	NRST	NRST: Target NRST using SWD protocol or target JTMS using JTAG protocol
-	13	PA10	T_VCP_RX: Target Rx used for VCP and connected to STLK_VCP_TX (UART supporting the bootloader)
-	14	PA9	T_VCP_TX: Target Tx used for VCP and connected to STLK_VCP_RX (UART supporting the bootloader)

Two level shifters are used on the VCP and SWD interfaces to offer a debug capability with MCU powered by 1V8. A level shifter is used for the signal from target MCU (1V8) to STLINK-V3E (3V3).

1. U27 used for T_VCP_TX/STLK_VCP_RX signal
2. U30 used for T_SWDIO and T_SWO signal

7.4.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the STDC14 features:

- By default, only a MIPI10 connector is present on the CN18 footprint.
- The STDC14 function is mainly limited to the SWD function. The TDI and TDO functions are optional.
- The STDC14 function JTDI cannot be operated simultaneously with the UCPD function.
- The STDC14 function JTDO/SWO cannot be operated simultaneously with the audio MEMS function.

7.5 TAG footprint

7.5.1 Description

The CN13 footprint can also output a debug interface compatible with the TAG probe TC2050-IDC-NL.

Table 8 describes the hardware configuration for the TAG function.

Table 8. Hardware I/O configuration for the TAG connector (CN13)

I/O	Solder bridge	Setting(1)	Comment
PA13	-	**-**	**PA13 is connected to JTAG JTMS or SWD SWDIO.**
PA14	-	**-**	**PA14 is connected to JTAG JTCK or SWD SWCLK.**
PA15	SB15	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is not connected to JTAG. PA15 can be used for UCPB.
PB3	SB114	**ON**	**PB3 is connected to JTAG JTDO or SWD SWO.**
		OFF	PB3 is not connected to JTAG or SWD. PB3 can be used for audio MEMS.
PB4	SB32	**ON**	**PB4 can be used for the JTAG TRSTN.**
		OFF	PB4 is not connected to JTAG. PB4 can be used for audio MEMS, comparator, or STMod+
NRST	-	**ON**	**NRST is used to reset the target.**

1. *The default configuration is shown in bold.*

Figure 11 shows the TAG connector pinout.

Figure 11. TAG connector (CN13) pinout

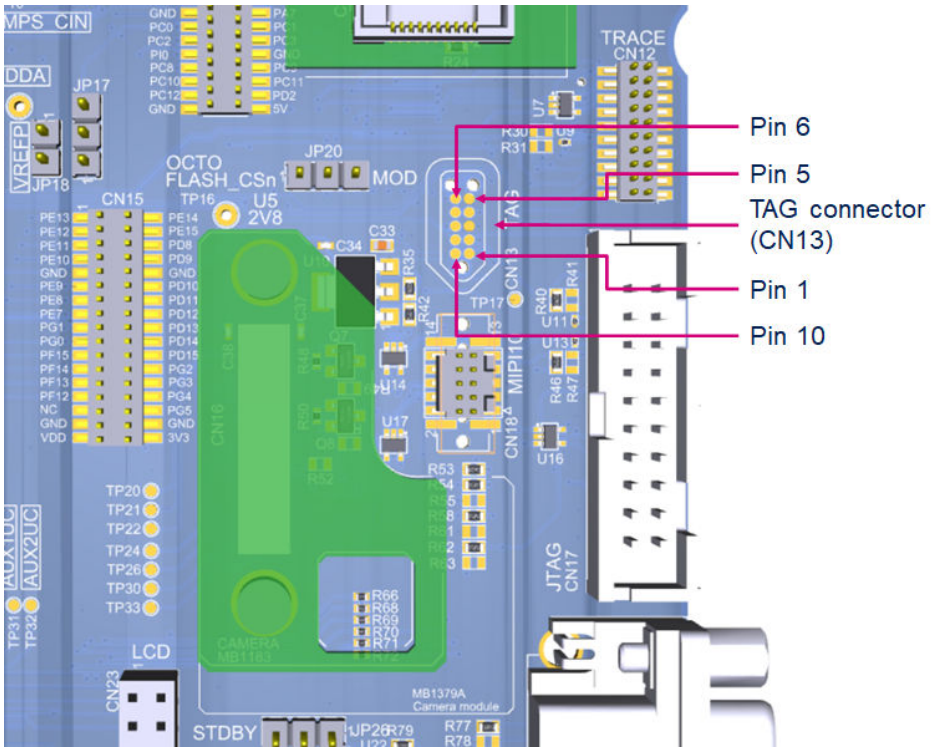


Table 9 describes the TAG connector (CN13) pinout.

Table 9. TAG connector (CN13) pinout

Connector pin number	STM32 pin	Board function
1	VDD	Power
2	PA13	JTMS_SWDIO: Target SWDIO using SWD protocol or target JTMS using JTAG protocol
3	GND	Power
4	PA14	JTCK_SWCLK: Target SWCLK using SWD protocol or target JTCK using JTAG protocol
5	GND	Power
6	PB3	JTDO_SWO: Target SWO using SWD protocol or target JTDO using JTAG protocol
7	-	NC
8	PA15	JTDI: Not used by SWD protocol, target JTDI using JTAG protocol, only for external tools
9	PB4	JTRSTN: JTAG RESET protocol
10	NRST	NRST: Target NRST using SWD protocol or target JTMS using JTAG protocol

7.5.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the TAG features:

- The TAG function is mainly limited to the SWD function. The TDI and TDO functions are optional.
- The TAG TRSTN function cannot be operated simultaneously with the comparator function.
- The TAG TRSTN function cannot be operated simultaneously with the STMod+ function.
- The TAG JTDI function cannot be operated simultaneously with the UCPD function.
- The TAG JTDO/SWO function cannot be operated simultaneously with the audio MEMS function.

7.6 ETM trace

7.6.1 Description

The header 10x2-pin 1.27 mm pitch header connector (CN12) can output trace signals used to debug.
Table 10 describes the hardware configuration for the TRACE function.

Table 10. Hardware I/O configuration for the TRACE connector (CN12)

I/O	Solder bridge	Setting[1]	Comment
PC9	SB77	**ON**	**PC9 can be used for the TRACE function TRACE D0.**
		OFF	PC9 is not connected to TRACE. PC9 can be used for SDIO.
PC10	SB81	**ON**	**PC10 can be used for the TRACE function TRACE D1.**
		OFF	PC10 is not connected to TRACE. PC10 can be used for SDIO.
PE5	R194	**ON**	**PE5 can be used for the TRACE function TRACE D2.**
		OFF	PE5 is not connected to TRACE. No other multiplexing
PC12	SB92	**ON**	**PC12 can be used for the TRACE function TRACE D3.**
		OFF	PC12 is not connected to TRACE. PC12 can be used for SDIO or STMod+.
PE2	R184	**ON**	**PE2 can be used for the trace function TRACE CLK.**
		OFF	PE2 is not connected to TRACE. No other multiplexing
PA13	-	**-**	**PA13 is connected to JTAG JTMS or SWD SWDIO.**
PA14	-	**-**	**PA14 is connected to JTAG JTCK or SWD SWCLK.**
PA15	SB15	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is not connected to JTAG. PA15 can be used for UCPB.
PB3	SB114	**ON**	**PB3 is connected to JTAG JTDO or SWD SWO.**
		OFF	PB3 is not connected to JTAG or SWD. PB3 can be used for audio MEMS
NRST	-	**ON**	**NRST is used to reset the target.**

1. *The default configuration is shown in bold.*

Figure 12 shows the TRACE connector (CN12) pinout.

Figure 12. TRACE connector (CN12) pinout

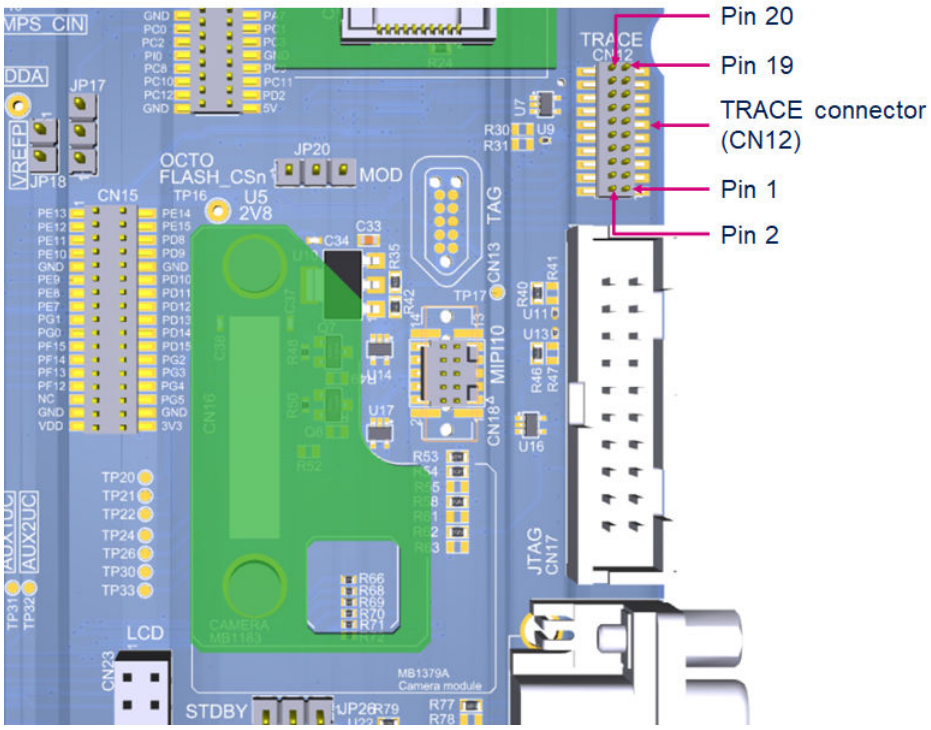


Table 11 describes the TRACE connector pinout.

Table 11. TRACE connector (CN12) pinout

Connector pin number	STM32 pin	Board function
1	VDD	Power
2	PA13	JTMS_SWDIO: Target SWDIO using SWD protocol or target JTMS using JTAG protocol
3	GND	Power
4	PA14	JTCK_SWCLK: Target SWCLK using SWD protocol or target JTCK using JTAG protocol
5	GND	Power
6	PB3	JTDO_SWO: Target SWO using SWD protocol or target JTDO using JTAG protocol
7	-	NC
8	PA15	JTDI: Not used by SWD protocol, target JTDI using JTAG protocol, only for external tools
9	GND	Power
10	NRST	NRST: Target NRST using SWD protocol or target JTMS using JTAG protocol
11	GND	Power
12	PE2	TRACE_CLK
13	GND	Power
14	PC9	TRACE_D0
15	GND	Power
16	PC10	TRACE_D1
17	GND	Power
18	PE5	TRACE_D2
19	GND	Power
20	PC12	TRACE_D3

7.6.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the TRACE features:

- The TRACE D0/D1/D3 function cannot be operated simultaneously with the SD card function.
- The TRACE D3 function cannot be operated simultaneously with the STMod+ (SPI) function.
- The TRACE JTDI function cannot be operated simultaneously with the UCPD function.
- The TRACE JTDO/SWO function cannot be operated simultaneously with the audio MEMS function.
- The TRACE JTRSTN function cannot be operated simultaneously with the COMP2 interface.

7.7 JTAG connector

7.7.1 Description

The 10x2-pin 2.54 mm pitch header connector (CN17) can output JTAG signals used to debug.

Table 12 describes the hardware configuration for the JTAG function.

Table 12. Hardware I/O configuration for the JTAG function on the CN17 connector

I/O	Solder bridge	Setting[1]	Comment
PA13	-	**-**	**PA13 is connected to JTAG JTMS or SWD SWDIO.**
PA14	-	**-**	**PA14 is connected to JTAG JTCK or SWD SWCLK.**
PA15	SB15	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is NOT connected to JTAG. PA15 can be used for UCPB.
PB3	SB114	**ON**	**PB3 is connected to JTAG JTDO or SWD SWO.**
		OFF	PB3 is NOT connected to JTAG or SWD. PB3 can be used for audio MEMS
PB4	SB32	**ON**	**PB4 can be used for the JTAG TRSTN**
		OFF	PB4 is NOT connected to JTAG. PB4 can be used for audio MEMS, comparator, or STMod+.
NRST	-	**ON**	**NRST is used to reset the target.**

1. *The default configuration is shown in bold.*

Figure 13 shows the JTAG connector (CN17) pinout.

Figure 13. JTAG connector (CN17) pinout

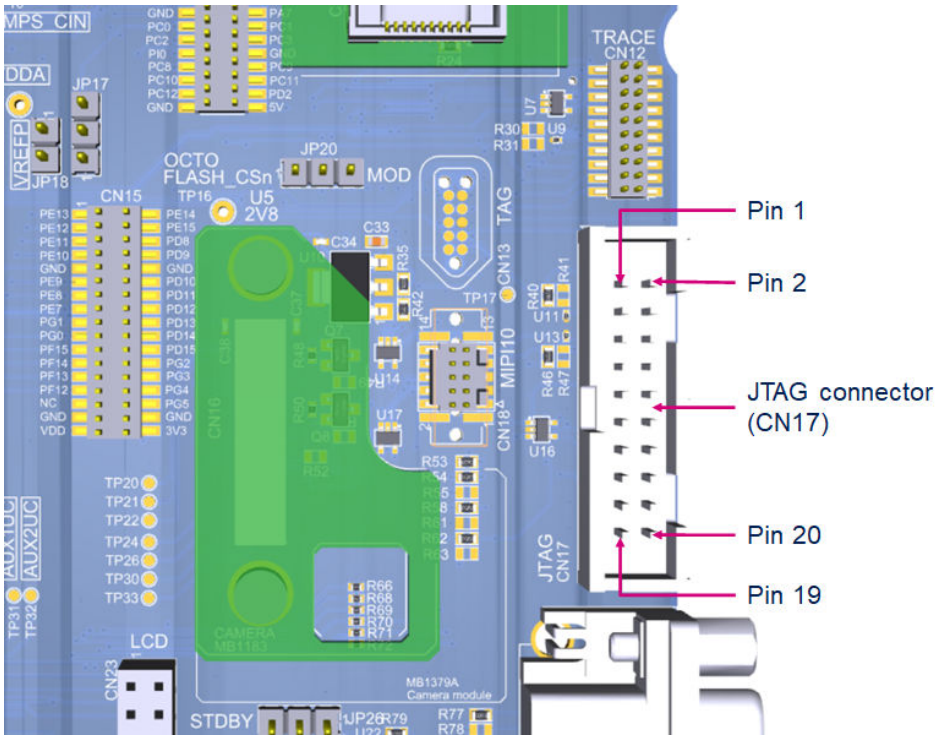


Table 13. JTAG connector (CN17) pinout describes the JTAG connector (CN17) pinout.

Table 13. JTAG connector (CN17) pinout

Connector pin number	STM32 pin	Board function
1	VDD	Power
2	VDD	Power
3	PB4	JTRSTN: JTAG RESET protocol
4	GND	Power
5	PA15	JTDI: Not used by SWD protocol, target JTDI using JTAG protocol, only for external tools
6	GND	Power
7	PA13	JTMS_SWDIO: Target SWDIO using SWD protocol or target JTMS using JTAG protocol
8	GND	Power
9	PA14	JTCK_SWCLK: Target SWCLK using SWD protocol or target JTCK using JTAG protocol
10	GND	Power
11	-	-
12	GND	Power
13	PB3	JTDO_SWO: Target SWO using SWD protocol or target JTDO using JTAG protocol
14	GND	Power
15	NRST	NRST: Target NRST using SWD protocol or target JTMS using JTAG protocol
16	GND	Power
17	-	TRGIN
18	GND	Power
19	-	TRGOUT
20	GND	Power

7.7.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the JTAG features:

- The JTAG function is mainly limited to the SWD function. The TDI and TDO functions are optional.
- The JTAG TRSTN function cannot be operated simultaneously with the comparator function.
- The JTAG TRSTN function cannot be operated simultaneously with the STMod+ function.
- The JTAG TRSTN function cannot be operated simultaneously with the audio MEMS function.
- The JTAG JTDI function cannot be operated simultaneously with the UCPD function.

7.8 Power supply

7.8.1 5 V power supply general view

The STM32U575I-EV Evaluation board is designed to be powered from a 5 V DC power source. One of the following five 5 V DC power inputs can be used, upon an appropriate board configuration:

- 5V_STLK from the Micro-B USB receptacle (CN26) of STLINK-V3E (default)
- 5V_EXT from the power jack marked 5V (CN25) on the board. The positive pole is on the center pin as illustrated in Figure 16.
- 5V_UCPD from the USB Type-C® receptacle (CN1) of the USB user interface
- 5V_DC from pin 49 of the extension connector (CN9) for the custom daughterboard
- 5V_CHG from the Micro-B USB receptacle (CN26) of STLINK-V3E, in case of a wall charger (no enumeration)

No external power supply is provided with the board.

When 5V_EXT or 5V_DC is used to power the board, it must comply with the standard EN 60950-1:2006+A11/2009+A1/2010+A12/2011+A2/2013, EN 62368-1 (2014+A11/2017). It must also be a safety extralow voltage (SELV/ES1) with limited power capability (LPS/ES2).

LD2 green LED turns on when the voltage on the power line marked as 5V is present. All supply lines required for the operation of the components on STM32U575I-EV are derived from that 5V line.

5 V/500 mA is the standard to power the STM32U575I-EV Evaluation board.

Table 14 describes the 5 V power supply capabilities.

Table 14. Power source capabilities

Input power name	Connector pins	Voltage range	Max. current	Limitation
5V_STLK	CN26 pin 1 JP25 [1-2]	4.75 to 5.25 V	500 mA	The maximum current depends on the USB enumeration: • 100 mA without enumeration • 500 mA with correct enumeration
5V_EXT	C25 pin 1 JP25 [3-4]		-	The maximum current depends on the power source.
5V_UCPD	CN1 JP25 [5-6]		1 A	The maximum current depends on the USB Type-C® host used to power the STM32U575I-EV board.
5V_DC	CN9 pin 49 JP25 [7-8]		-	The maximum current depends on the power source.
5V_CHG	CN26 pin 1 JP25 [9-10]		-	The maximum current depends on the USB wall charger used to power the board (no enumeration, no current protection).

7.8.2 5V_STLK power source

5V_STLK is a DC power with limitation from the STLINK-V3E USB connector (USB type Micro-B connector of STLINK-V3E). In this case, the JP25 jumper must be on pin [1-2] to select the 5V_STLK power source. This is the default setting. If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the T_PWR_EN signal, from the STLINK-V3E MCU (U26). This pin is connected to the USB power switch (U20), which powers the board. This power switch features also a 500 mA current limitation to protect the PC in case of an onboard short-circuit.

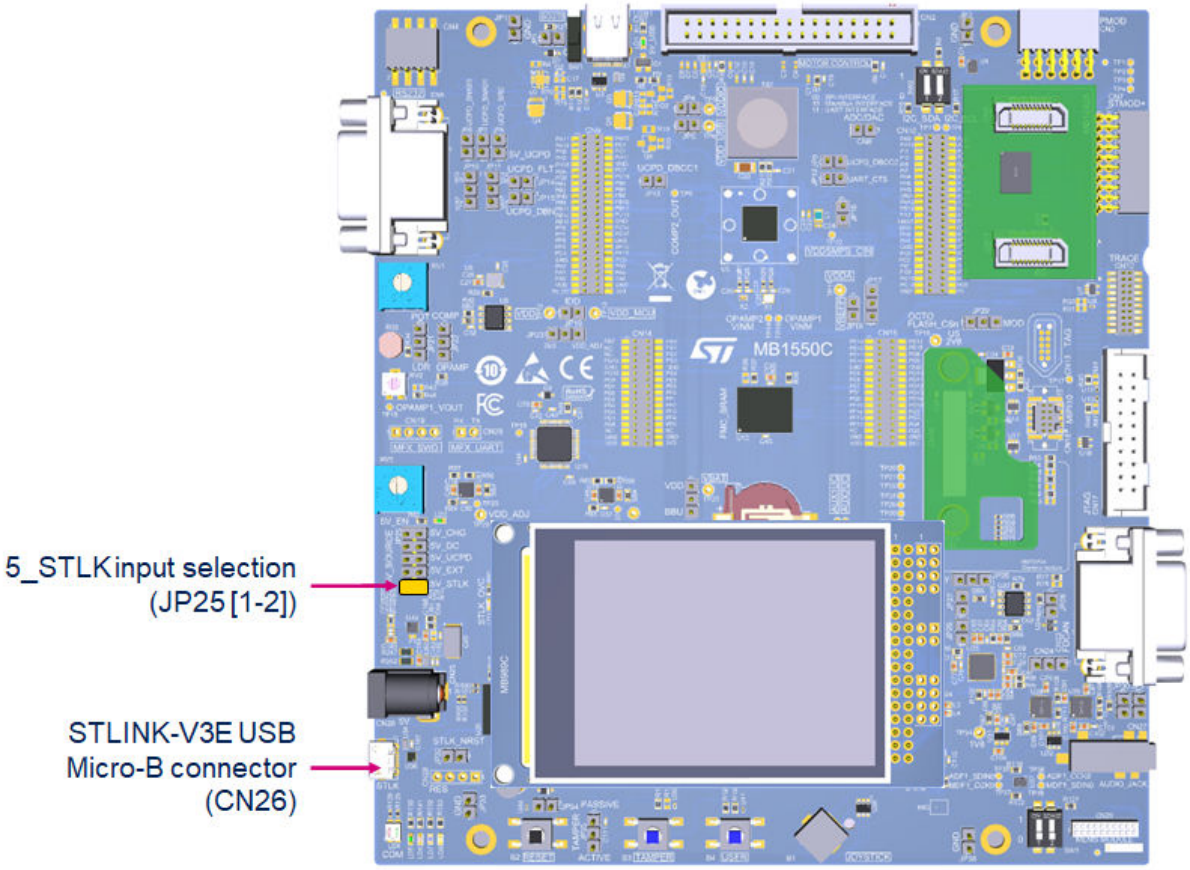
The STM32U575I-EV board with its shield can be powered from the STLINK-V3E USB connector (CN26), but only the STLINK-V3E circuit has the power before USB enumeration, as the host PC only provides 100 mA to the board at that time. During the USB enumeration, the STM32U575I-EV board asks for 500 mA power to the host PC.

If the host can provide the required power, the enumeration finishes with a *SetConfiguration* command. Then, the power switch is turned ON, the LD2 green LED turns ON. Thus, the STM32U575I-EV board with its shield can consume 500 mA current, but not more.

If the host cannot provide the requested current, the enumeration fails. Therefore, the power switch remains OFF and the MCU part including the extension board is not powered. As a consequence, the 5V LD2 green LED remains turned OFF. In this case, it is mandatory to use an external power supply.

The 5V_STLK power source configuration for the JP25 jumper is described in Figure 14.

Figure 14. JP25 [1-2]: 5V_STLK power source



7.8.3 5V_EXT power source

5V_EXT is the DC power coming from the power jack (CN25). In this case, the JP25 jumper must be on pin [3-4] to select the 5V_EXT power source. The positive pole is on the center pin as illustrated in Figure 15.

The 5V_EXT power source configuration for the JP25 jumper is described in Figure 16.

Figure 15. JP25 [3-4]: 5V_EXT power source

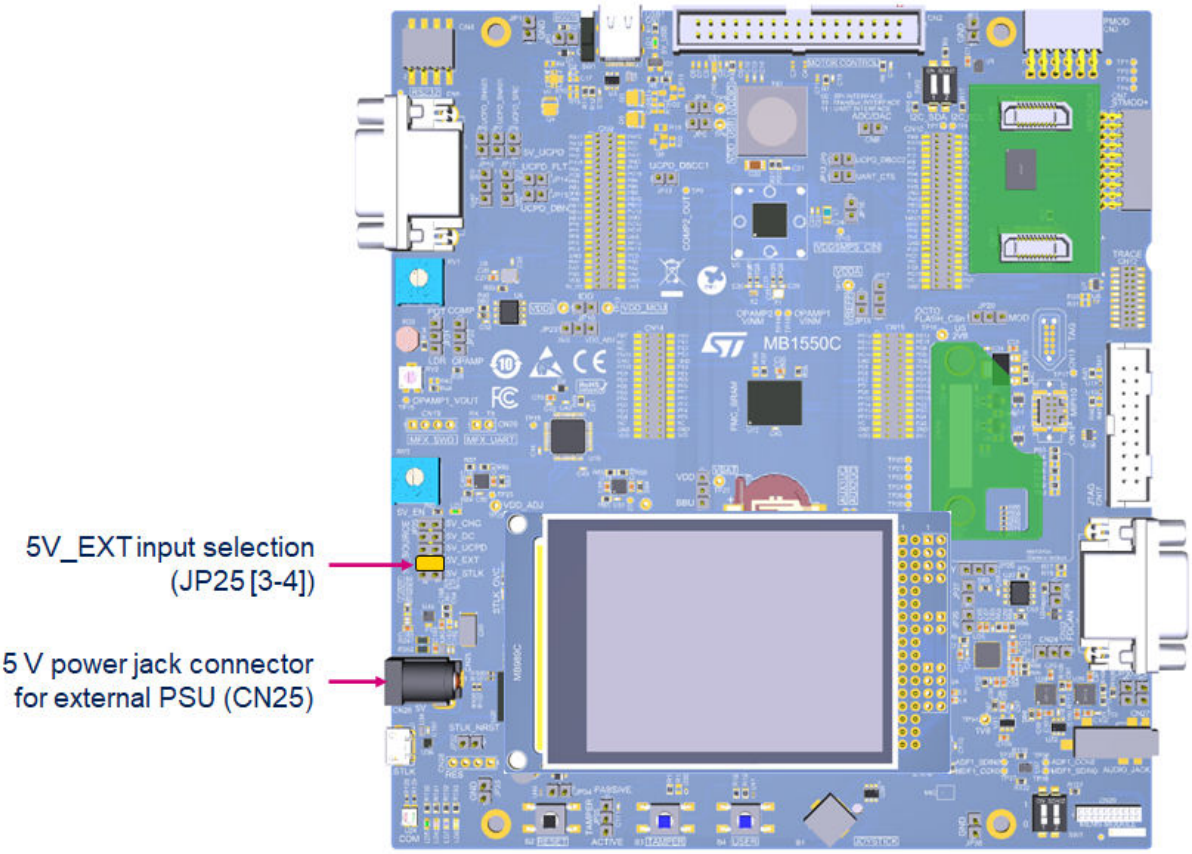
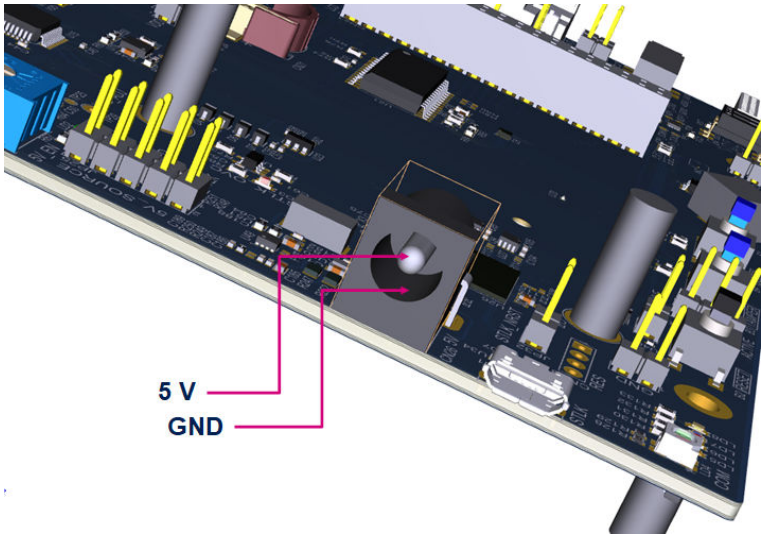


Figure 16. 5 V power jack connector (CN25) for external PSU

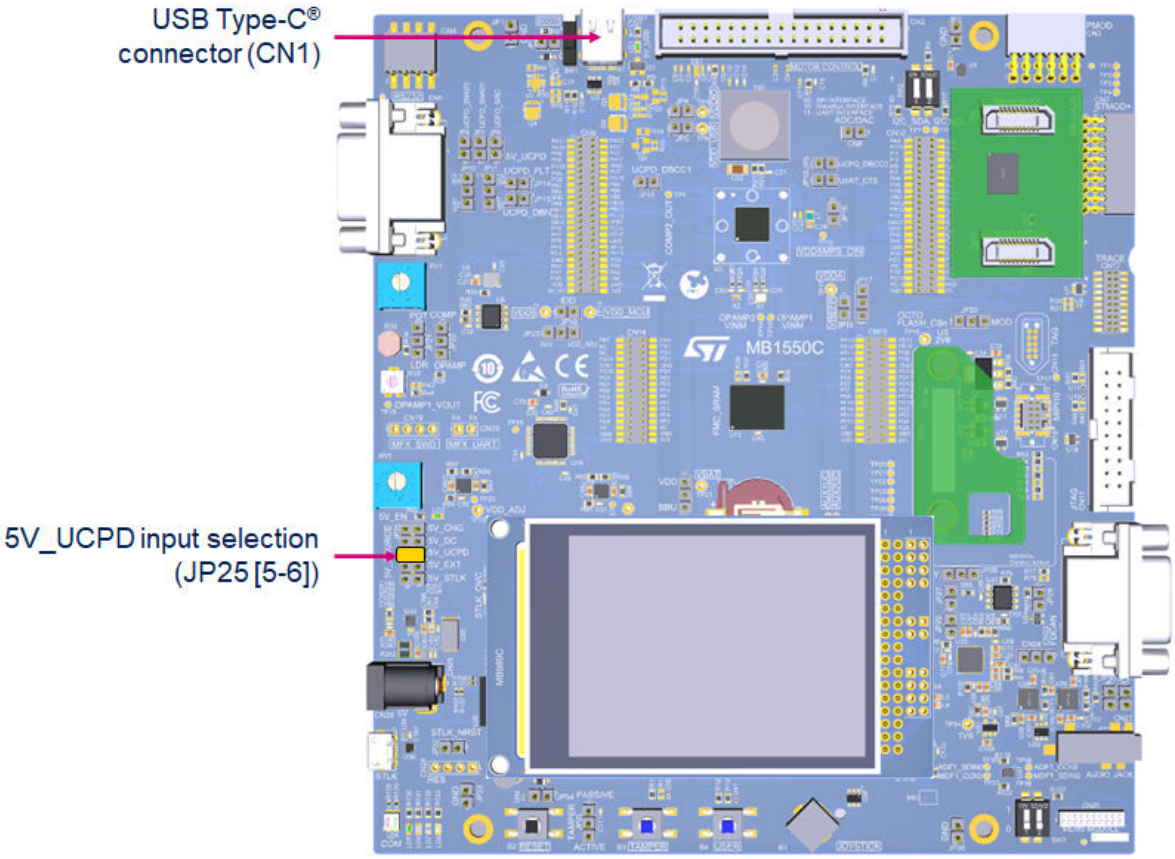


7.8.4 5V_UCPD power source

5V_UCPD is the DC power supply connected to the user USB Type-C® connector (CN1). In this case, the JP25 jumper must be set on [5-6] to select the 5V_UCPD power source.

The 5V_UCPD power source configuration for the JP25 jumper is described in Figure 17.

Figure 17. JP25 [5-6]: 5V_UCPD power source

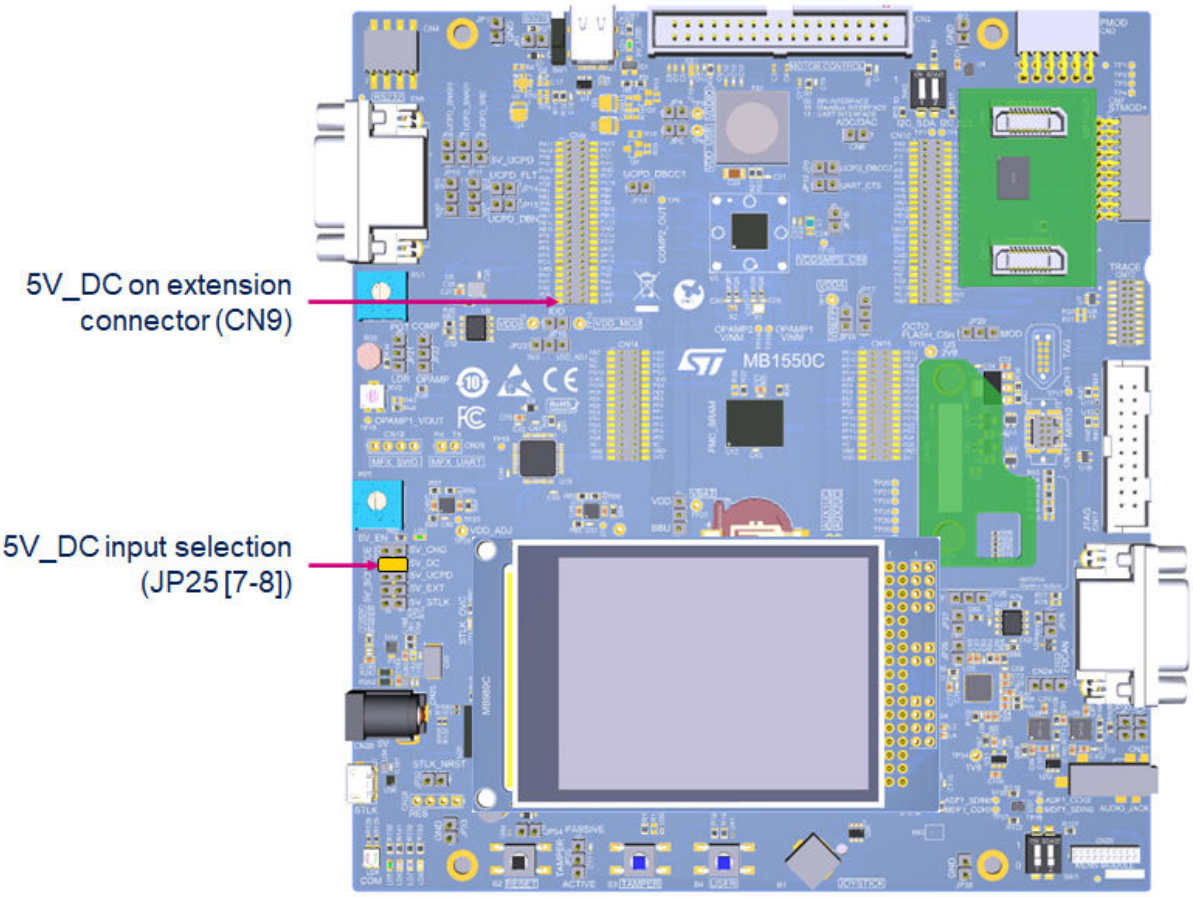


7.8.5 5V_DC power source

5V_DC is the DC power coming from the external 5V DC power on the extension connector (CN9 pin 49). In this case, the JP25 jumper must be on pin [7-8] to select the 5V_DC power source.

The 5V_DC power source configuration for the JP25 jumper is described in Figure 18.

Figure 18. JP25 [7-8]: 5V_DC power source

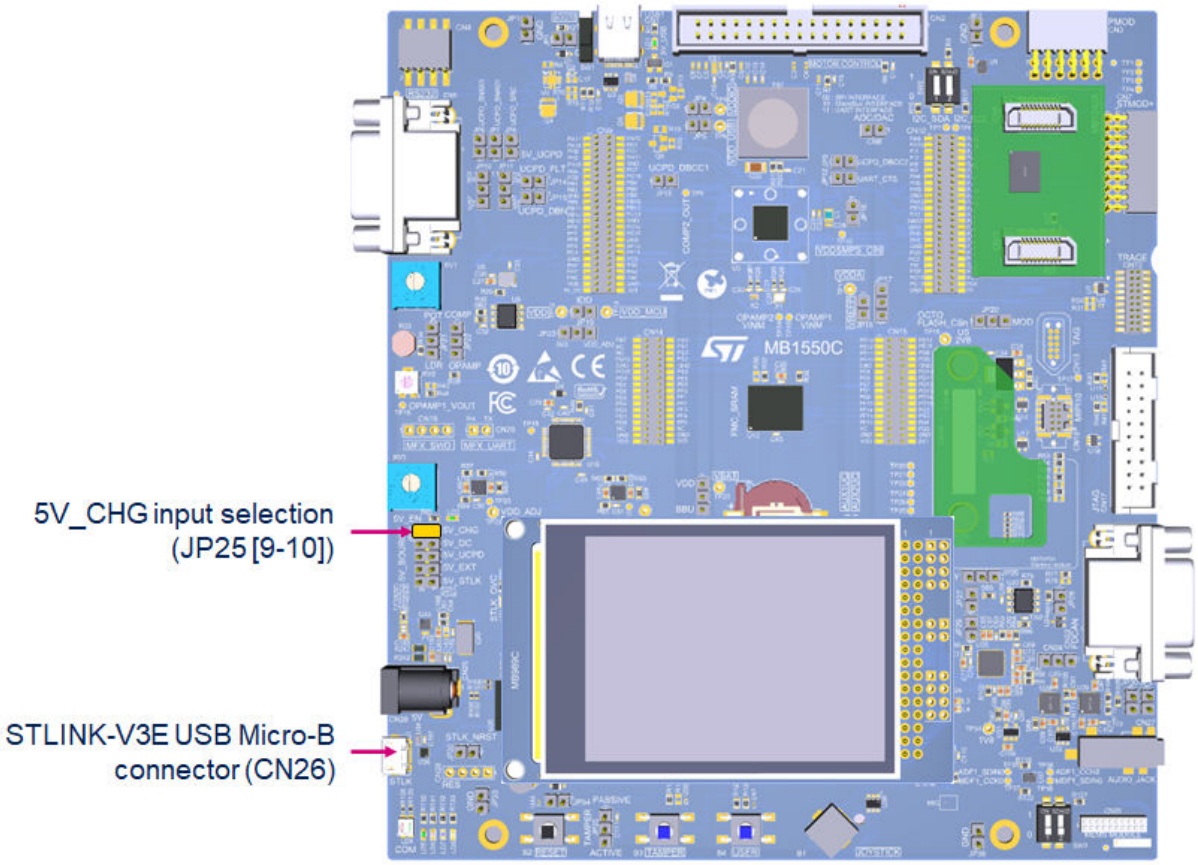


7.8.6 5V_CHG power source

5V_CHG is the DC power charger connected to the USB STLINK-V3E connector (CN26). In this case, the JP25 jumper must be set on [9-10] to select the 5V_CHG power source. If the STM32U575I-EV board is powered by an external USB charger, then the debug is not available. If a computer is connected instead of the charger, the current limitation is no longer effective. In this case, the computer might be damaged. To avoid this risk, it is recommended to select the 5V_STLK mode.

The 5V_CHG power source configuration for the JP25 jumper is described in Figure 19.

Figure 19. JP25 [9-10]: 5V_CHG power source



Note: With this JP25 configuration: 5V_CHG, the USB_PWR protection is bypassed. Never use this configuration with a computer connected instead of the charger, because the USB_PWR_protection is bypassed. If the board consumption is higher than 500 mA, this can damage the computer.

Caution: In case the maximum current consumption of the STM32U575I-EV board with its extension boards exceeds 500 mA, it is recommended to power the STM32U575I-EV board using an external power supply connected to 5V_EXT or 5V_DC.

7.8.7 Programing/debugging when the power supply is not from STLINK-V3E (5V_STLK)

5V_EXT, 5V_DC, or 5V_UCPD can be used as an external power supply in case the current consumption of the STM32U575I-EV with expansion boards exceeds the allowed current on USB. In such a condition, it is still possible to use USB for communication for programming or debugging only.

In this case, it is mandatory to power the board first using 5V_EXT, 5V_DC or 5V_UCPD then connect the STLINK-V3E USB cable to the PC. Proceeding this way, the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect the JP25 jumper according to the external 5 V power source selected.
2. Connect the external power source selected.
3. Power on the external power source.
4. Check that the 5 V green LED (LD2) is turned ON.
5. Connect the PC to the STLINK-V3E USB connector (CN26).

If this sequence is not respected, the board might be powered by V_{BUS} first from STLINK-V3E, and the following risks might be encountered:

- If the board needs more than 500 mA current, the PC might be damaged or limit the current. As a consequence, the board is not powered correctly.
- 500 mA is requested at enumeration. So, there is a risk that the request is rejected and enumeration does not succeed if the PC does not provide such a current. Consequently, the board is not powered (LED LD2 remains OFF).

7.8.8 Power supply output

5V: When the STM32U575I-EV board is powered by STLINK-V3E USB, 5V_EXT, or 5V_DC, the 5 V (CN10 pin 50) can be used as an output power supply for an extension board plugged into CN10. In this case, the maximum current of the power source specified in Table 14 must be respected.

3V3: CN9 pin 50, CN14 pin 34, or CN15 pin 34 can also be used as power supply output. The current is limited by the 1.3 A maximum current capability of the regulator (U19) provided to the STM32U575I-EV board and its shield.

7.8.9 Internal power supply

For all general information concerning design recommendations for STM32U5 with INTERNAL SMPS, and design guide for ultra-low-power applications with performance, refer to *Getting started with STM32U5 MCU hardware development* (AN5373) at the *www.st.com* website.

3V3

Regardless of the 5V power source, the U19 LDO is used to deliver a fixed 3.3 V power supply, with a current capability of 1.3 A. This power source of 3.3 V is shared between the STM32U575I-EV and its expansion boards.

VDD_ADJ

Regardless of the 5 V power source, the U18 LDO is used to deliver an adjusted power voltage, with a range of 1.7 to 3.6 V, and a current capability of 1.3 A. This voltage is tuned, thanks to the RV3 potentiometer. This adjustable voltage must be reserved for MCU debugging capability. Be careful to set and select the features compatible with this adjustable voltage range before updating the board accordingly.

Caution: The power-on sequence is not respected when using VDD_ADJ below 3.3 V, refer to the application note *Getting started with STM32U5 MCU hardware development* (AN5373) and the STM32U5xx product datasheets for low-voltage power sequencing.

2V8

Regardless of the 5 V power source, the U10 LDO is used to deliver a fixed 2.8 V voltage, with a current capability of 800 mA. This voltage source is mainly reserved for the camera daughterboard. This one is not targeted to supply the MCU. To drive the MCU in low voltage, use the VDD_ADJ supply voltage.

1V8

Regardless of the 5 V power source, the U31 LDO is used to deliver a fixed 1.8 V voltage, with a current capability of 150 mA. This voltage source is mainly reserved for the low-power audio codec. This one is not targeted to supply the MCU. To drive the MCU in low voltage, use the VDD_ADJ supply voltage.

Table 15 details the LDO and associated hardware solder bridge configuration.

Table 15. LDO and associated hardware solder bridge configuration

I/O	Solder bridge	Definition	Setting[1]	Comment
3V3	SB4	LDO output for 3V3	**ON**	**U19 can provide the main 3V3.**
			OFF	U19 output disconnected
VDD_ADJ	SB3	LDO output for VDD_ADJ	**ON**	**U18 can provide the main VDD_ADJ: 1V7 to 3V6.**
			OFF	U18 output disconnected
2V8	SB104	LDO output for camera daughterboard	**ON**	**U10 can provide 2.8 V to the camera daughterboard.**
			OFF	U10 output disconnected, no 2.8 V for camera daughterboard
1V8	SB7	LDO output for audio codec	**ON**	**The LDO is the audio 1.8 V source.**
			OFF	U31 output disconnected, no internal audio 1.8 V source

1. *The default configuration is in bold.*

7.8.10 VDD_MCU IDD measurement

The labeled IDD JP19 jumper can measure the consumption of the STM32 microcontroller replacing the jumper by an ammeter or a current measurement tool.

- Jumper ON: The STM32 microcontroller is powered (default).
- Jumper OFF: an ammeter or an external 3V3 power source must be connected to the power and measure the STM32 microcontroller consumption.

The IDD jumper can measure the current for both 3V3 and 1V8 MCU voltage ranges.

For specific consumption measurement by external tools like STM32CubeMonitor-Power (STM32CubeMonPwr) or ULPBench probe, where only VDD_MCU is externally powered (meaning no STLINK, no 5V, no VDD, only JP19 pin 2 powered by 3V3 or 1V8), it is recommended to configure the STM32U575I-EV Evaluation board to avoid leakage currents from I/Os connected to unpowered components. This configuration can be used to ensure that there is no return consumption from other power sources such as VDD_MCU.

For the software configuration, all I/Os must be set correctly according to the Cube power consumption example.

From the hardware point of view, it is recommended to disconnect the signal RSTN from the unpowered components.

To measure STM32U575AII6Q consumption with this test bench configuration, the board configuration must be:

- Memory module MB1242 removed to avoid an average leakage consumption of around 750 µA.
- R211 0-ohm resistor removed on the NRST signal on the embedded Octo-SPI flash memory (U47) to avoid an average leakage consumption of around 180 µA.
- LCD and camera modules removed to avoid an average leakage consumption of around 2 µA.
- D3 removed on the U15 MFX_NRST signal and R69 on the STLINK MCU (U26) to avoid a leakage consumption of around 0.7 µA.

Table 16 details the MCU power supply configuration and the associated hardware configuration.

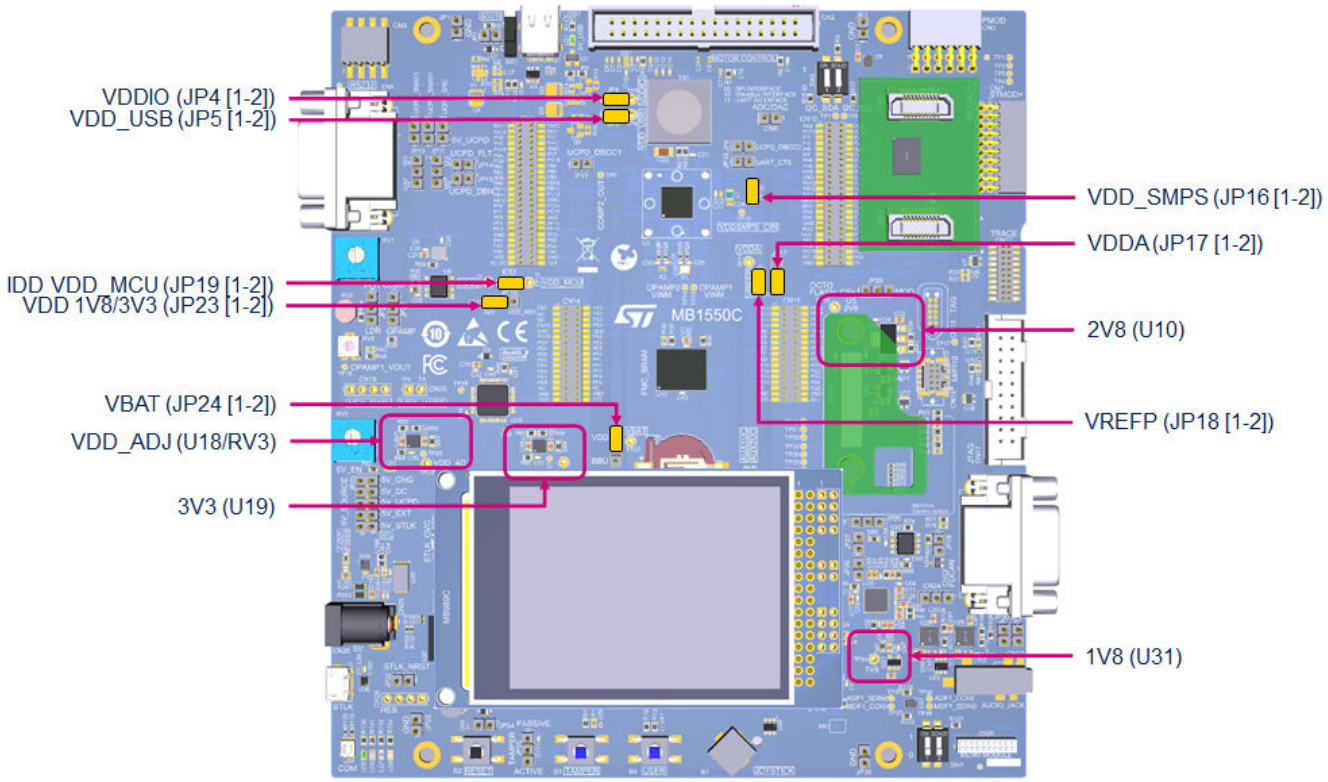
Table 16. Hardware configuration for the MCU power supply voltage

Jumper	Definition	Setting[1]	Comment
JP23	VDD source selection Range 1.7 V < VDD < 3.6 V	**JP23[1-2]**	**The VDD source is fixed at 3.3 V.**
		JP23[2-3]	The VDD source is VDD_ADJ (1.7 V to 3.6 V).
JP19	VDD_MCU power measurement selection: IDD Range 1.7 V < VDD_MCU <3.6 V	**JP19 ON**	**VDD_MCU is connected to VDD.**
		JP19 OFF	Use an ammeter to measure the MCU power consumption, or connect an external 3V3 or 1V8 external source on pin 2 to supply the MCU (STLINK-PWR tools with the STM32CubeMonitor-Power or ULPBench probe as an example).
JP4	VDDIO source selection for PG [2-15] Range 1.7 V < VDDIO < 3.6 V	**JP4 ON**	**VDDIO source is VDD_MCU.**
		JP4 OFF	VDDIO is not supplied or open for debugging or current measurement
JP24	VBAT source selection Range 1.7 V < VBAT < 3.6 V	**JP24[1-2]**	**VBAT source is VDD.**
		JP24[2-3]	The VBAT source is the external battery.
JP17	VDDA source selection Range 1.7 V < VDDA < 3.6 V	**JP17[1-2]**	**VDDA source is VDD_MCU.**
		JP17[2-3]	The VDDA source is fixed at 3.3 V.
JP18	VREFP source selection Range 1.7 V < VREFP < 3.6 V	**JP18 ON**	**VREFP source is VDDA.**
		JP18 OFF	VREFP is not supplied or open for debugging or current measurement
JP5	VDD_USB source selection Range 3.0 V < VDD_USB < 3.6 V	**JP5 ON**	**VDD_USB source is 3.3 V.**
		JP5 OFF	The USB feature is not supplied or open for debugging or current measurement
JP16	VDD_SMPS source selection Range 1.7 V < VDDSMPS < 3.6 V	**JP16 ON**	**VDD_SMPS source is VDD_MCU.**
		JP16 OFF	VDD_SMPS is not supplied or open for debugging or current measurement.

1. *The default configuration is in bold.*

Figure 20 describes the MCU power-supplied position on the STM32U575I-EV board.

Figure 20. Jumpers and solder bridges for power sources



7.9 Clock references

Two clock references are available on the STM32U575I-EV for the STM32U575AII6Q target microcontroller.

- 32.768 kHz crystal X2, for LSE embedded RTC
- 16 MHz crystal X1, for HSE clock generator.

The main clock can also be generated using an internal RC oscillator.

Table 17 describes the hardware configuration for the LSE 32.768 kHz.

Table 17. Hardware I/O configuration for the 32.768 kHz

I/O	Solder bridge	Setting(1)	Comment
PC14	SB87	**OFF**	**X2 is used as a clock reference with the connected R27.** **PC14 OSC32_IN terminal is not routed to the extension connector (CN9).**
		ON	PC14 OSC32_IN is routed to the extension connector (CN9). R27 must be removed from the X2 crystal circuit so as not to disturb the clock reference, clock source from the daughterboard, or PC14 IO function.
PC15	SB86	**OFF**	**X2 is used as a clock reference with the connected R28.** **PC15 OSC32_OUT terminal is not routed to the extension connector (CN9).**
		ON	PC15 OSC32_OUT is routed to the extension connector (CN9). R28 must be removed from the X2 crystal circuit so as not to disturb the clock reference, clock source from the daughterboard, or PC15 IO function.

1. *The default configuration is shown in bold.*

Refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867) with the following characteristics: 32.768 kHz, 9 pF, 20 ppm.

Table 18 describes the hardware configuration for the 16 MHz HSE clock.

Table 18. Hardware I/O configuration for the 16 MHz HSE clock

I/O	Solder bridge	Setting(1)	Comment
PH0	SB89	**OFF**	**X1 can be used as a clock reference with the connected R25.** **PH0 OSC_IN terminal is not routed to the extension connector (CN10). SB90 for MCO must be open.**
		ON	PH0 OSC_IN is routed to the extension connector (CN10). R25 and SB90 must be removed so as not to disturb the clock reference, clock source on the daughterboard, or PH0 IO function.
	SB90	**OFF**	**PH0 OSC_IN terminal is not connected to the STLINK-V3 MCO clock reference.**
		ON	PH0 OSC_IN is connected to the ST-LINK MCO clock reference. R25 and SB89 must be removed so as not to disturb the MCO clock reference.
PH1	SB88	**OFF**	**X1 can be used as a clock reference with the connected R26.** **The PH1 OSC_OUT terminal is not routed to the extension connector (CN10).**
		ON	PH1 OSC_OUT is routed to the extension connector (CN10). R26 must be removed, in order not to disturb clock reference, clock source on the daughterboard, or PH1 IO function.

1. *The default configuration is shown in bold.*

7.10 Reset sources

The reset signal of the STM32U575AII6Q on the STM32U575I-EV Evaluation board is active at a low level.

Sources of reset are:

- The black RESET button (B2)
- The JTAG connector (CN17), the TRACE connector (CN12), the STDC14 connector (CN18), and the TAG connector (CN13, reset from debug tools)
- Through the extension connector (CN10 pin 27, reset from daughterboard)
- The embedded STLINK-V3E MCU (U26)
- The optional external RS-232 interface (JP34 OFF)

7.11 RSS/bootloader

7.11.1 Description

The bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the flash memory by using USART, I^2C, SPI, CAN FD, or USB FS in device mode through the DFU (device firmware upgrade). The bootloader is available on all devices. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

The root secure services (RSS) are embedded in a flash area named the secure information block, programmed during ST production. For example, it enables secure firmware installation (SFI) thanks to the RSS extension firmware (RSSe SFI). This feature allows customers to protect the confidentiality of the firmware to be provisioned into the STM32 when production is subcontracted to an untrusted third-party. The root secure services are available on all devices, after enabling the TrustZone® through the TZEN option bit.

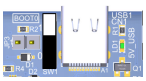
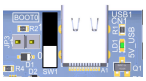
The bootloader version can be identified by reading the bootloader ID at the address `0x0BF97FFE`.

7.11.2 Boot from RSS

The BOOT0 value might come from the PH3_BOOT0 pin, connected to the boot switch (SW1), or from an option bit depending on the value of a user option bit.

Table 19 describes the hardware configuration of the switch (SW1) for the Boot mode.

Table 19. Boot selection switch (SW1)

I/O	Switch	Setting[1]	Comment
PH3	SW1	**BOOT0 = 0 (SW1 down)** 	**The BOOT0 line is tied LOW. STM32U575AII6Q boot address defined by the user option bytes NSBOOTADD0 or SECBOOTADD0 according to the TrustZone® setting.**
		BOOT0 = 1 (SW1 up) 	The BOOT0 line is tied HIGH. STM32U575AII6Q boot address defined by the user option bytes NSBOOTADD1 or RSS according to the TrustZone® setting.

1. *The default configuration is shown in bold.*

An external equipment connected to the RS-232 connector (CN6 pin 6) can also drive the BOOT0 line. In this case, the jumper JP3 must be ON.

7.12 Audio

7.12.1 Description

A low-power stereo codec with a headphone amplifier is connected to the SAI interface of STM32U575AII6Q, which supports the TDM feature of the SAI port. The TDM feature offers STM32U575AII6Q the capability to stream stereo audio channels.

There is also one digital microphone on the STM32U575I-EV Evaluation board, which offers the possibility to connect a MEMS extension daughterboard.

7.12.2 Operating voltage

The microphone is supplied by VDD and compatible with the VDD_MCU voltage range from 1.71 to 3.6 V. The audio codec has two supplies:

- VDD_CODEC connected to VDD compatible with VDD_MCU low voltage 1.71 V but limited to a maximum of 3.47 V according to the audio codec datasheet
- 1V8_CODEC dedicated 1.8 V source provided by U31

7.12.3 Audio codec interface

The audio codec interface is the MCU SAI1 and the I2C2 interface.

The audio codec I^2C frequency is limited to 100 kHz. The base I^2C-bus address is `0x94` (`0b 1001.010x`).

Table 20 describes the hardware configuration for the audio codec interface SAI and I^2C.

Table 20. Hardware I/O configuration for the audio codec interface SAI and I^2C

I/O	Hardware	Setting[1]	Configuration
PF6	R153	**ON**	**PF6 is used as SAI1_SDIN_B to interface the audio codec.** No other multiplexing
PF7	R154	**ON**	**PF7 is used as SAI1_MCLK_B to interface the audio codec.** No other multiplexing
PF8	R157	**ON**	**PF8 is used as SAI1_SCK_B to interface the audio codec.** No other multiplexing
PF9	SB62	**ON**	**PF9 is used as SAI1_FS_B to interface the audio codec.**
		OFF	PF9 is not used for the audio codec. It can be used for motor control.
PD6	R206	**ON**	**PD6 is used as SAI1_SDOUT_A to interface the audio codec.** No other multiplexing
PB10	SB46	**ON**	**PB10 is used as I2C_SCL to interface the audio codec and it is shared with MFX, UCPD, touch panel, Ext_I2C, EEPROM, 3D accelerometer, 3D gyroscope, camera, and STMod+.**
PB11	SB49	**ON**	**PB11 is used as I2C_SDA to interface the audio codec and it is shared with MFX, UCPD, touch panel, Ext_I2C, EEPROM, 3D accelerometer, 3D gyroscope, camera, and STMod+.**

1. *The default configuration is shown in bold.*

7.12.4 Digital microphones

U48 on the STM32U575I-EV Evaluation board is an ST MEMS digital omnidirectional microphone providing PDM (pulse density modulation) outputs. The data output of the microphone is connected to the ADF1 interface of STM32U575AII6Q. The programmable clock directly generated by STM32U575AII6Q drives the microphone.

Table 21 and Table 22 describe the hardware configuration for the MEMS ADF1 interface.

Table 21. Hardware I/O configuration for the ADF1 interface

I/O	Solder bridge	Setting(1)	Configuration
PB3	SB115	**ON**	**PB3 is used as ADF1_CCK0 to interface the audio MEMS**
		OFF	PB3 is not used for the audio MEMS. It can be used for JTAG JTDO/SWO
PB4	SB26	**ON**	**PB4 is used as ADF1_SDIN0 to interface the audio MEMS.**
		OFF	PB4 is not used for the audio MEMS. It can be used for JTAG JTRSTN, comparator, or STMod+

1. *The default configuration is shown in bold.*

Table 22. SW3 configuration for the ADF-MEMS interface

Switch	Setting(1)	Configuration
SW3-1	**OFF**	**ADF1_CCK0 and ADF SDIN0 interface the audio MEMS (U48)**
	ON	ADF1_CCK0 and ADF SDIN0 interface the audio MEMS daughterboard on CN29
SW3-2	**OFF**	**MDF1_CCK0 and MDF SDIN0 interface the audio MEMS daughterboard on CN29**
		If SW3-1 is also ON at the same time, MDF1 and AD1 are connected for debugging purposes.
	ON	N/A

1. *The default configuration is shown in bold.*

7.12.5 Headphones outputs

The STM32U575I-EV Evaluation board can drive stereo headphones. The STM32U575AII6Q sends up the stereo audio channels, via its SAI1 TDM port, to the codec device. The codec device converts the digital audio stream to stereo analog signals. It then boosts them for the direct drive of headphones connected to the 3.5 mm stereo jack receptacle (CN27) on the board.

An I^2C bus sets the audio codec. The address is a 7-bit address, with an additional bit to read or write (HIGH to read, LOW to write). The AD0 pin connected to GND gives the least significant bit of the address. The address of the audio codec is `0b1001010x`. The hexadecimal code is `0x94` to write, and `0x95` to read.

Caution: The audio codec I^2C interface is compatible with the I^2C clock at 100 kHz only.

7.12.6 Audio jack connector

Figure 21 shows the CN27 audio jack connector.

Figure 21. Audio jack connector (CN27)

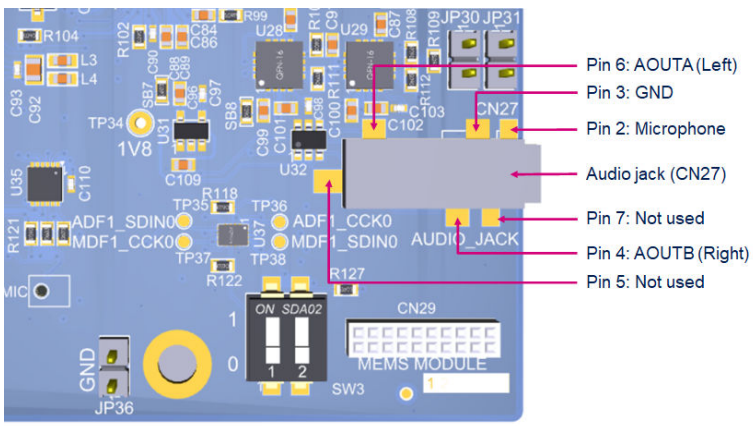


Table 23 describes the audio jack connector (CN27) pinout.

Table 23. Audio jack connector (CN27) pinout

Connector pin number	Audio codec pin	Board function
2	MICIN1	MIC_IN: Microphone input
3	GND	Power
4	AOUTB (RIGHT)	AOUTB analog audio output B-channel: loudspeaker right side
5	N/A	N/A
6	AOUTA (LEFT)	AOUTA analog audio output A-channel: loudspeaker left side
7	N/A	N/A

7.12.7 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the AUDIO features:

The audio codec (SAI1_FS_B) cannot be operated simultaneously with motor control.

The MEMS on ADF1 cannot be operated simultaneously with the ADF1 EXT MEMS daughterboard connector (CN29).

The MEMS on ADF1 cannot be operated simultaneously with the full JTAG.

The MEMS on ADF1 cannot be operated simultaneously with the STMod+ SPI_MISO2 interface.

The MEMS on ADF1 cannot be operated simultaneously with the comparator1 input.

7.13 USB Type-C® FS port

7.13.1 Description

The STM32U575I-EV Evaluation board supports USB full-speed (FS) communication. The USB connector (CN1) is a USB Type-C® connector.

The STM32U575I-EV Evaluation board supports USB Type-C® Sink and Source modes.

An LD1 green LED lights up when V_{BUS} is powered by a USB Host when the STM32U575I-EV Evaluation board works as a USB Device, or when STM32U575AII6Q provides the 5 V USB to external devices.

7.13.2 Operating voltage

The STM32U575I-EV Evaluation board supports 5 V USB voltage, from 4.75 to 5.25 V.

MCU VDD_USB only supports the 3.3 V voltage.

7.13.3 USB FS device

When a USB host connection to the USB Type-C® connector (CN1) of the STM32U575I-EV Evaluation board is detected, the STM32U575I-EV Evaluation board starts behaving as a USB device. Depending on the powering capability of the USB host, the board can take power from the V_{BUS} terminal of CN1. In the board schematic diagrams, the corresponding power voltage line is called 5V_UCPD.

Section 7.8 provides information on how to use the powering option.

Table 24 describes the hardware configuration for the USB interface.

Table 24. Hardware I/O configuration for the USB interface

I/O	Hardware	Setting(1)	Configuration
PA11	R139	**OFF**	**PA11 used as USB_FS_N diff pair interface**
		ON	PA11 connected in parallel to the extension connector (CN9) USB interface can be disturbed.

I/O	Hardware	Setting(1)	Configuration
PA12	R140	**OFF**	**PA12 used as USB_FS_P diff pair interface**
		ON	PA12 connected in parallel to the extension connector (CN9) USB interface can be disturbed.

1. *The default configuration is in bold.*

7.13.4 UCPD

USB Type-C® introduces the USB Power Delivery feature. STM32U575I-EV Evaluation board supports the dead battery, the SINK mode, and the SOURCE mode. The fast role swap (FRS) is optional.

In addition to the DP/DM I/Os directly connected to the USB Type-C® connector, some I/Os are also used for UCPD configuration: Configuration Channel (CCx), VBUS-SENSE, IBUS_SENSE, I²C interface, and UCPD_FAULT (FLT) feature.

To protect STM32U575I-EV from USB overvoltage, a USB Type-C® PPS-compliant port protection IC is used, compliant with IEC6100-4-2 level 4.

- Configuration Channel I/O: UCPD_CCx: These signals are connected to the associated CCx line of the USB Type-C® connector through the ST USB port protection. These lines are used for the configuration channel lines (CCx) to select the USB Type-C® current mode. STM32U575I-EV supports SINK and source current modes.
- Dead battery: UCPD_DBn: The port protection internally manages the dead battery function and its associated resistors link to the UCPD feature. No I/O or external resistors are necessary for this function.
- V_{BUS} fault detection: UCPD_FLT: This signal is provided by the STM USB port protection. It is used as a fault reporting to the MCU after a bad V_{BUS} level detection. By design, RSENSE set the STM32U575I-EV V_{BUS} protection to 6 V maximum.
- An I²C bus drives the port protection component. The base I²C-bus address is `0x68` (`0b0110100x`).

Table 25 describes the hardware configuration for the UCPD interface.

Table 25. Hardware I/O configuration for the UCPD feature

I/O	Hardware	Setting(1)	Configuration
PA15	SB19	**ON**	**PA15 is used as UCPD_CC1 and connected to the USB Type-C® port protection and cannot be used as JTAG.**
		OFF	PA15 is not connected to the USB Type-C® port protection and can be used for JTAG (T_JTDI)
PB15	SB52	**ON**	**PB15 is used as UCPD_CC2 and connected to the USB Type-C® port protection and cannot be used as UCPD_CC2.**
		OFF	PB15 is not connected to the USB Type-C® port protection. No other multiplexing
PA5	SB75	**ON**	**PA5 is used as VBUS_SENSE.**
		OFF	PA5 is not used for UCPD and can be used on STMod+.
PB8	JP14	**ON**	**IO UCPD_FLT is connected to the USB Type-C® port protection and used as overvoltage fault reporting to MCU.**
		OFF	PB8 is not used for UCPD_FLT and can be used as FDCAN or for external MEMS.
PA0	SB72	**ON**	**ADC on PA0 is used for IBUS_SENSE.**
		OFF	PA0 is not used for IBUS_SENSE and can be used for OPAMP, STMod+, or motor control.
PG8	SB11	ON	Port protection supplied by PG8 I/O
		OFF	**Port protection supplied by VDD through SB10**

I/O	Hardware	Setting[1]	Configuration
PB10	SB46	**ON**	**PB10 is used as I2C_SCL to interface the port protection and is shared with MFX, touch panel, Ext_I2C, EEPROM, 3D accelerometer, 3D gyroscope, camera, and STMod+.**
PB11	SB49	**ON**	**PB11 is used as I2C_SDA to interface the port protection and is shared with MFX, touch panel, Ext_I2C, EEPROM, 3D accelerometer, 3D gyroscope, camera, and STMod+.**
PB5[2]	JP13	ON	UCPD_DBCC1 is connected to GND for the UCPD DB function through the STM32
		OFF	**MCU UCPD_DBCC1 is not connected to GND and can be used for the comparator or STMod+.**
PB14[2]	JP9	ON	UCPD_DBCC2 is connected to GND for the UCPD DB function through the STM32.
		OFF	**MCU UCPD_DBCC2 is not connected to GND and can be used for TSC function.**

1. *The default configuration is in bold.*
2. *The UCPD DBn function is done by the port protection. The use of PB5 and PB14 for the DBn function is only for development purposes.*

7.13.5 USB Type-C® connector

Figure 22 shows the pinout of the USB Type-C® connector (CN1).

Figure 22. USB Type-C® connector (CN1) pinout

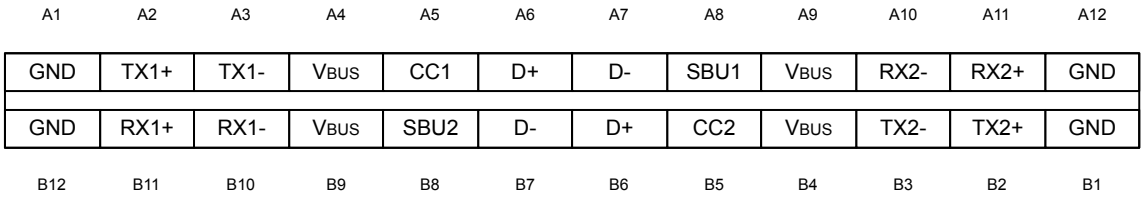


Table 26 describes the pinout of the CN1 USB Type-C® connector.

Table 26. USB Type-C® connector (CN1) pinout

Connector pin number	STM32 pin	Board function
A1	-	Power GND
A2	-	TX1+ (not used)
A3	-	TX1- (not used)
A4	-	VBUSc: 5V V_{BUS} before protection
A5	PA15	CC1: configuration channel 1
A6	PA12	D+: USB data interface differential pair P
A7	PA11	D-: USB data interface differential pair N
A8	--	SBU1 (not used)
A9	-	VBUSc: 5V V_{BUS} before protection
A10	-	RX2- (not used)
A11	-	RX2+ (not used)
A12	-	Power GND

Connector pin number	STM32 pin	Board function
B1	-	Power GND
B2	-	TX2+ (not used)
B3	-	TX2- (not used)
B4	-	VBUSc: 5V V_{BUS} before protection
B5	PB15	CC2: configuration channel 2
B6	PA12	D+: USB data interface differential pair P
B7	PA11	D-: USB data interface differential pair N
B8	-	SBU2 (not used)
B9	-	VBUSc: 5V V_{BUS} before protection
B10	-	RX1- (not used)
B11	-	RX1+ (not used)
B12	-	Power GND

7.13.6 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the USB features:

- The USB UCPD_CC1 cannot be operated simultaneously with the full JTAG.
- The USB UCPD_DBCC1 cannot be operated simultaneously with the comparator.
- The USB UCPD_DBCC2 cannot be operated simultaneously with the STMod+ (SPI).
- The USB UCPD VBUS_VSENSE cannot be operated simultaneously with the STMod+ (PWM).
- The USB UCPD IBUS_VSENSE cannot be operated simultaneously with the OPAMP, STMod+ (ADC), and motor control.
- The USB UCPD_FLT cannot be operated simultaneously with the CAN-FD feature.
- The USB UCPD_FLT cannot be operated simultaneously with MDF1_CCK0 for external MEMS.

7.14 RS-232 port

7.14.1 RS-232 port

The STM32U575I-EV Evaluation board offers one RS-232 communication port. The RS-232 communication port uses the DB9 male connector (CN6).

7.14.2 Operating voltage

The RS-232 transceiver (U43) is supplied by the fixed 3V3 power voltage. To support the MCU 1V8 I/O configuration, the level shifter (U45) is used for the MCU output I/O to reach the transceiver voltage input high level (VIH).

In this configuration, the RS-232 interface is fully compatible with the MCU voltage range from 1.71 to 3.6 V.

7.14.3 RS-232 interface

The RS-232 interface is connected to MCU LPUART1. It can be used in 2-wire mode (Rx and Tx) or 4-wire mode (Rx, Tx, RTS, and CTS).

Table 27 describes the hardware configuration for the RS-232 interface.

Table 27. Hardware I/O configuration for the RS-232 interface

I/O	Hardware	Setting[1]	Configuration
PG7	JP10	**[1-2]**	**PG7 LPUART1_TX is NOT connected to the RS-232 transceiver** **PG7 is used as LPBAM_I2C or UCPD_FRSCC2**
		[2-3]	PG7 LPUART1_TX is connected to the RS-232 transceiver.
PG8	JP11	**[1-2]**	**PG8 LPUART1_RX is NOT connected to the RS-232 transceiver** **PG8 is used as LPBAM_I2C or UCPD_PWR**
		[2-3]	PG8 LPUART1_RX is connected to the RS-232 transceiver.
PB13	JP12	**OFF**	**PB13: LPUART1_CTS is not connected to the RS-232 transceiver. PB13 can be used for TSC.**
		ON	PB13: LPUART1_CTS is connected to the RS-232 transceiver
PG6	SB38	OFF	PG6: LPUART1_RTS is not connected to the RS-232 transceiver. PG6 can be used for UCPD_FRSCC1
		ON	**PG6: LPUART1_RTS is connected to the RS-232 transceiver**

1. *The default configuration is in bold.*

Figure 23 shows the RS-232 connector (CN6) pinout.

Figure 23. RS-232 connector (CN6) pinout

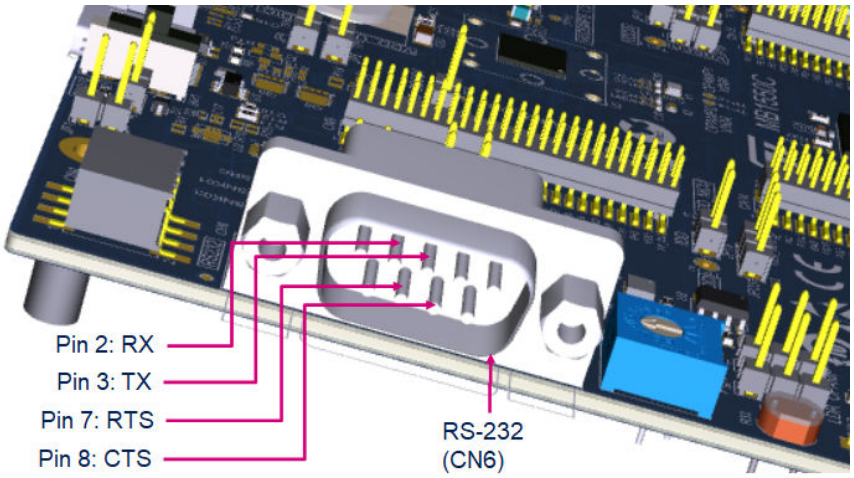


Table 28 describes the RS-232 connector (CN6) pinout.

Table 28. RS-232 connector (CN6) pinout

Connector pin number	STM32 pin	Board function
1	NC	NC
2	PG8	RXD/UART_RX from MCU
3	PG7	TXD/UART_TX from MCU
4	NC	NC
5	GND	GND
6	PH3_BOOT0	DSR/Used as external input for BOOT0 pin driving
7	PG6	RTS/UART_RTS from MCU
8	PB13	CTS/UART_CTS from MCU
9	NC	NC

7.14.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the RS-232 features:

- The RS-232 RX/TX cannot be operated simultaneously with the UCPD_PWR interface.
- The RS-232 RX/TX cannot be operated simultaneously with the optional I2C3 LPBAM interface.
- The RS-232 CTS cannot be operated simultaneously with the TSC feature.

7.15 microSD™ card

7.15.1 Description

The slot for the microSD™ card (CN30) is routed to the STM32U575AII6Q SDIO port. This interface is compliant with SD memory card specification version 6.0: SDR104 SDMMC_CK speed limited to the maximum allowed I/O speed. UHS-II mode is not supported. The microSD™ card interface is on the bottom side of the board.

7.15.2 Operating voltage

The SD card interface is only compatible with the 3.3 V voltage range, from 2.7 to 3.6 V.

The SD card interface does not support the MCU low voltage 1.8 V range.

7.15.3 SD card interface

The SD card interface is used in four data lines D [3:0], one clock, one command line, and a card detection signal. Table 29 describes the hardware configuration for the SDIO interface.

Table 29. Hardware I/O configuration for the SDIO interface

I/O	Hardware	Setting(1)	Configuration
PI0	SB74	**ON**	**PI0 is connected to SDCARD DETECT** No other multiplexing
PC8	SB84	**ON**	**PC8 is connected to SDCARD SDIO1_D0**
		OFF	PC8 is not connected to SDCARD SDIO1_D0 PC8 can be used for motor control
PC9	SB83	**ON**	**PC9 is connected to SDCARD SDIO1_D1**
		OFF	PC9 is not connected to SDCARD SDIO1_D1 PC9 can be used for TRACE ETM
PC10	SB85	**ON**	**PC10 is connected to SDCARD SDIO1_D2**
		OFF	PC10 is not connected to SDCARD SDIO1_D2 PC10 can be used for TRACE ETM
PC11	R168	**ON**	**PC11 is connected to SDCARD SDIO1_D3** No other multiplexing
PC12	SB91	**ON**	**PC12 is connected to SDCARD SDIO1_CLK**
		OFF	PC12 is not connected to SD card SDIO1_CLK PC12 can be used for Trace ETM or STMod+
PD2	R171	**ON**	**PD2 is connected to SD card SDIO1_CMD** No other multiplexing

1. *The default configuration is in bold.*

Figure 24 shows the SD card connector (CN30) pinout.

Figure 24. SD card connector (CN30) pinout

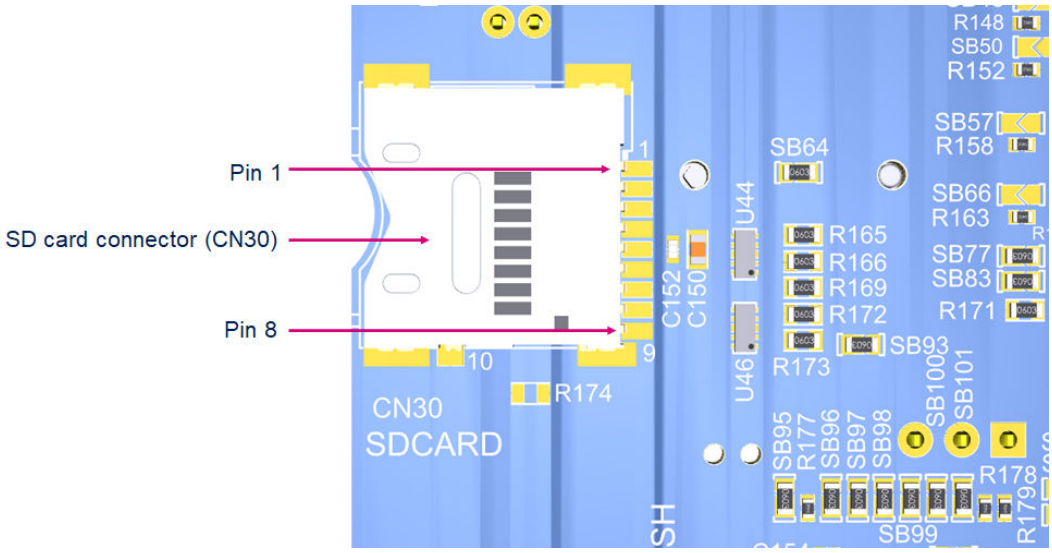


Table 30 describes the SD card connector (CN30) pinout.

Table 30. SD card connector (CN30) pinout

Connector pin number	STM32 pin	Board function
1	PC10	SDIO1_D2: SDCARD DATA 2
2	PC11	SDIO1_D3: SDCARD DATA 3
3	PD2	SDIO1_CMD: SDCARD COMMANDE line
4	VDD	VDD_SDCARD
5	PC12	SDIO1_CLK: SDCARD CLOCK line
6	-	GND
7	PC8	SDIO1_D0: SDCARD DATA 0
8	PC9	SDIO1_D1: SDCARD DATA 1
9	GND	GND for detection pin of card insertion
10	PI0	SDCARD_DETECT active LOW

7.15.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the SD card features

- The microSD™ card D0 cannot be operated simultaneously with the motor-control function.
- The microSD™ card D1/D2/CLK cannot be operated simultaneously with the trace function.
- The microSD™ card CLK cannot be operated simultaneously with the STMod+ SPI function.

7.16 CAN FD

7.16.1 Description

The STM32U575I-EV Evaluation board supports one CAN FD compliant with ISO-11898-1 version 2.0 parts A and B. The DB9 male connector (CN22) is available as a CAN-FD interface.

7.16.2 Operating voltage

A 3.3 V CAN transceiver is fitted between the CN22 connector and the CAN-FD controller port of STM32U575AII6Q.

In this configuration, the CAN-FD interface is compatible with the MCU voltage range, from 1.8 to 3.6 V (Low voltage 1.71 V does not fit with the CAN transceiver specification).

7.16.3 CAN-FD interface

The JP26 jumper allows selecting one among the high-speed, standby, and slope-control modes of the CAN transceiver.

The JP28 jumper can fit a CAN termination resistor (R81). The JP27 and JP29 are used to connect the CAN transceiver to STM32U575AII6Q. This helps to select the multiplexing for the CAN-FD I/O, which is shared with other interfaces.

Table 31 describes the hardware configuration for the CAN-FD interface.

Table 31. Hardware I/O configuration for the CAN-FD interface

I/O	Jumper	Setting[1]	Configuration
-	JP26	**JP26[1-2]**	**The CAN transceiver operates in high-speed mode.**
		JP26[2-3]	The CAN transceiver is in standby mode.
-	JP28	**ON**	**Termination resistor fitted on the CAN physical link**
		OFF	No termination resistor on the CAN physical link
PB8	JP29	ON	PB8 is used from the STM32U575AII6Q terminal as CAN_RX.
		OFF	**PB8 is not used for the CAN transceiver.** **PB8 can be used for UCPD or Ext-MEMS.**
PB9	JP27	ON	PB9 is used from the STM32U575AII6Q terminal as CAN_TX.
		OFF	**PB9 is not used for the CAN transceiver.** **PB9 can be used for UCPD.**

1. *The default configuration is shown in bold.*

Figure 25 shows the CAN-FD connector (CN22) pinout.

Figure 25. CAN-FD connector (CN22) pinout

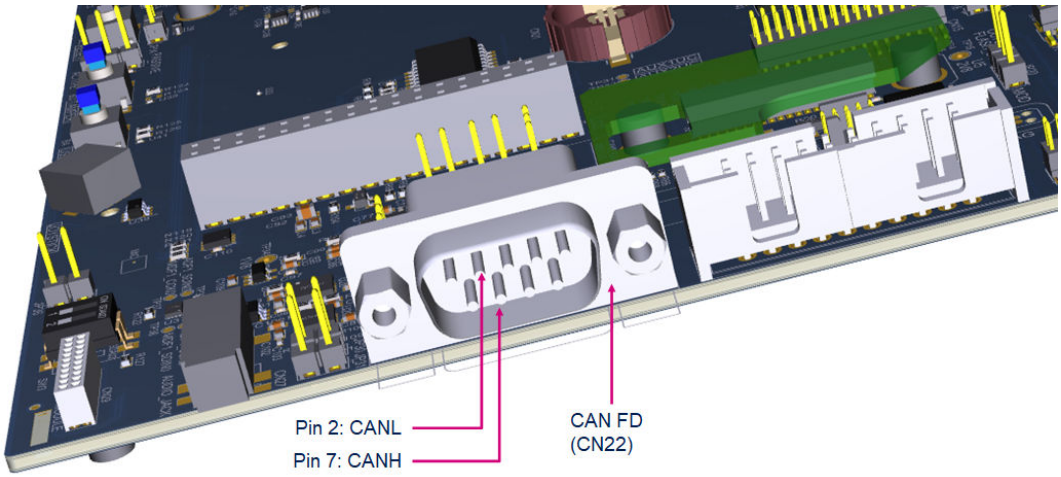


Table 32 describes the CAN-FD connector (CN22) pinout.

Table 32. CAN-FD connector pinout (CN22) to the transceiver

Connector pin number	U22 transceiver	Board function
1	-	NC
2	CANL	CANL
3	GND	GND
4	-	NC
5	-	NC
6	GND	GND
7	CANH	CANH
8	-	NC
9	-	NC

7.16.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the CAN-FD features:

- The CAN FD Tx and Rx cannot be operated simultaneously with the UCPD interface.
- The CAN FD Rx cannot be operated simultaneously with the EXT-MEMS MDF1.

7.17 Smartcard

7.17.1 Description

The STM32U575I-EV Evaluation board supports one smartcard interface. The smartcard connector (CN31) is used as a card reader. The smartcard interface is on the bottom side of the board.

7.17.2 Operating voltage

The smartcard interface is only compatible with the 2.7 to 3.6 V MCU voltage range. The smartcard interface does not support the 1.8 V low-power MCU.

7.17.3 Smartcard interface

A smartcard interface is used between the card reader connector (CN31) and the smartcard controller port of STM32U575AII6Q.

Table 33 describes the hardware configuration for the smartcard interface.

Table 33. Hardware I/O configuration for the smartcard interface

I/O	Solder bridge	Setting(1)	Configuration
PC4	SB116	**ON**	**PC4 is connected to the smartcard interface as SMARTCARD_IO**
		OFF	PC4 is not connected to the smartcard interface PC4 can be used for LCD
PB12	SB42	**ON**	**PB12 is connected to the smartcard interface as SMARTCARD_CLK**
		OFF	PB12 is not connected to the smartcard interface PB12 can be used for OCTOPSI_CLKN or motor control
MFX_IO6	-	-	**MFX_IO6 used as SMARTCARD_OFF** No other multiplexing
MFX_IO7	-	-	**MFX_IO7 used as SMARTCARD_RST** No other multiplexing
MFX_IO9	-	-	**MFX_IO9 used as SMARTCARD_CMDVCC** No other multiplexing
MFX_IO10	-	-	**MFX_IO10 used as SMARTCARD_3/5V** No other multiplexing

1. *The default configuration is shown in bold.*

Figure 26 shows the smartcard connector (CN31) pinout.

Figure 26. Smartcard connector (CN31) pinout

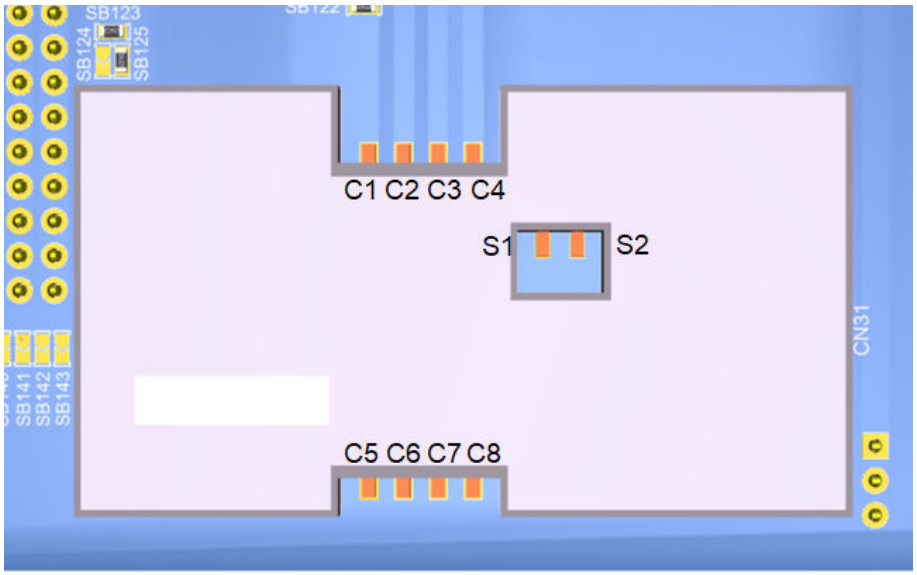


Table 34 describes the smartcard interface (U31) and CN31 connector pinout.

Table 34. Smartcard interface (U31) and CN31 connector pinout

Pin	U21 transceiver	Board function
C1	17 VCC	Smartcard power supply
C2	16 RST	Smartcard reset
C3	15 CLK	Smartcard clock
C4	13 AUX1	Smartcard auxiliary I/O 1
C5	14 GND	GND
C6	-	NC
C7	11 I/O	Smartcard I/O
C8	12 AUX2	Smartcard auxiliary I/O 2
S1	GND	GND: used for smartcard detection
S2	9 PRESN	Smartcard detection active low level

7.17.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the smartcard features:

- The smartcard USART3_TX cannot be operated simultaneously with the LCD with the TE feature.
- The smartcard USART3_CK cannot be operated simultaneously with the Octo-SPI with CLKN (1.8 V configuration).
- The smartcard USART3_CK cannot be operated simultaneously with the motor control.

7.18 User LEDs

7.18.1 Description

Four general-purpose colored LEDs (LD5, LD6, LD7, and LD8) are available as light indicators. Each LED is in a light-emitting state when a low level is applied to the corresponding I/O ports.

The LD5 green and LD6 red user LEDs are directly connected to STM32U575AII6Q.

The LD7 blue and LD8 yellow user LEDs are connected to the I/O expander.

7.18.2 Operating voltage

As the I/O low-level drives the LEDs, they are compatible with VDD_MCU 1.8 V. The voltage isolation is done with an NPN transistor.

7.18.3 LED interface

Table 35 describes the hardware configuration for the LED interface.

Table 35. Hardware I/O configuration for the LED interface

I/O	Hardware	Setting[1]	Configuration
PB7	-	**-**	**PB7 is connected to the active-low green LED (LD5).** No other multiplexing
PH7	-	**-**	**PH7 is connected to the active-low red LED (LD6).** No other multiplexing
MFX_IO11	-	-	**MFX_IO11 is connected to the active-low blue LED (LD7).** No other multiplexing
MFX_IO13	-	-	**MFX_IO13 is connected to the active-low yellow LED (LD8).** No other multiplexing

1. *The default configuration is shown in bold.*

7.19 Physical input devices: buttons

7.19.1 Description

The STM32U575I-EV Evaluation board provides several input devices for physical human control. These are:

- Four-way joystick controller with a selection key (B1)
- Reset button (B2)
- Tamper button (B3)
- User button (B4)

7.19.2 Operating voltage

The input devices for physical human control are connected to VDD or are referenced to GND. So, input devices are compatible with VDD_MCU voltage range from 1.71 to 3.6 V.

7.19.3 Physical input I/O interface

Table 36 describes the hardware configuration for the physical user interface.

Table 36. Hardware I/O configuration for the physical user interface

I/O	Hardware	Setting(1)	Configuration
PA1	SB78/JP35	**[1-2]**	**PA1 is connected to the B3 tamper key button as a passive tamper function (active HIGH).**
		[2-3]	PA1 is connected to the PC13 tamper I/O as an active tamper function
		OFF	PA1 is NOT connected to the tamper key. PA1 can be used for STMod+ or motor control.
PC13	JP35	[1-2]	**PC13 is connected to the B4 user button (active HIGH)**
		[2-3]	**PC13 is connected to the PA13 tamper key as an active tamper function.** B4 is always connected to PC13 through R125. R125 is OFF to isolate B4 from PC13.
NRST	-	**-**	**Reset button source (active LOW)**
MFX_IO0	-	**-**	**JOY_SEL: Joystick selection connected to B1 pin 2**
MFX_IO1	-	**-**	**JOY_DOWN: Joystick down direction connected to B1 pin 3**
MFX_IO2	-	**-**	**JOY_LEFT: Joystick left direction connected to B1 pin 1**
MFX_IO3	-	**-**	**JOY_RIGHT: Joystick right direction connected to B1 pin6**
MFX_IO4	-	**-**	**JOY_UP: Joystick up direction connected to B1 pin4**

1. *The default configuration is shown in bold.*

7.19.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the physical interface features:

- The passive tamper key function cannot be operated simultaneously with the active tamper, the STMOD+_INT or the motor-control functions. The user button function cannot be operated simultaneously with the active tamper function.

7.20 Operational amplifiers and comparator

7.20.1 Description

The STM32U575I-EV Evaluation board offers the possibility to test the internal operational amplifiers and comparators according to:

- 10 kΩ potentiometer (RV1)
- LDR light-dependent resistor (R33)

Potentiometer and light-dependent resistor can be mutually and exclusively routed to the PB4 (Comp) or PA0 (OpAmp) port of STM32U575AII6Q.

7.20.2 Operating voltage

The operational amplifiers and comparator are connected to VDD or are referenced to GND. So, the operational amplifiers and comparator are compatible with the VDD_MCU voltage range from 1.71 to 3.6 V.

7.20.3 Operational amplifiers

STM32U575AII6Q provides two onboard operational amplifiers. One of which, OpAmp1, is made accessible on STM32U575I-EV. OpAmp1 has its inputs and its output routed to I/O ports.

Table 37 describes the hardware configuration for the operational amplifier interface.

Table 37. Hardware I/O configuration for the operational amplifier interface

I/O	Hardware	Setting[1]	Configuration
PA0	SB68	**ON**	**PA0 is used as OPAMP1_INP and connected to JP122 pin 3**
		OFF	PA0 is not used as OpAmp. PA0 can be used for STMod+, UCPD, or motor control.
OPAMP1_INM	_	-	**OPAMP1_INM dedicated pin is used as OPAMP1_INM and connected to R44/RV2.**
PA3	SB53	ON	PA3 is used as OPAMP1_VOUT and connected to TP18.
		OFF	**PA3 is not used as OpAmp.** **PA3 can be used for Octo-SPI or motor control.**

1. *The default configuration is shown in bold.*

The noninverting input PA0 is accessible on JP22 jumper header pin 3. On top of the possibility of routing, either from the potentiometer or LDR to PA0, an external source can also be connected to it, using the JP22 terminal 3.

The PA3 output of the operational amplifier can be accessed on the TP18 test point. Refer to the schematic of the STM32U575I-EV Evaluation board.

The ratio of the variable resistor RV2 and the resistor R44 determines the gain of OpAmp1, as shown in the following equation:

$$Gain = 1 + \left(\frac{RV2}{R44}\right)$$

With the RV2 ranging from 0 to 10 kΩ and the R44 being 1 kΩ, the gain can vary from 1 to 11.

The R39 resistor in series on PA0 is beneficial for reducing the output offset.

Table 38 describes the jumper configuration to enable the LDR or the potentiometer to the OpAmp1 function.

Table 38. Jumper configuration to enable the LDR or the potentiometer to the OpAmp1 function

Hardware	Setting[1]	Configuration
JP21/JP22	JP21[1-2]/ JP22[2-3]	The potentiometer is routed to the OPAMP1_INP PA0 pin of STM32U575AII6Q.
	JP21[2-3]/ JP22[2-3]	**LDR is routed to the OPAMP1_INP PA0 pin of STM32U575AII6Q.**

1. *The default configuration is shown in bold.*

7.20.4 Comparator

STM32U575AII6Q provides two onboard comparators. One of which, Comp2, is made accessible on the STM32U575I-EV Evaluation board. Comp2 has its noninverting input and its output.

Table 39 describes the hardware configuration for the comparator interface.

Table 39. Hardware I/O configuration for the comparator interface

I/O	Hardware	Setting(1)	Configuration
PB4	SB40	**ON**	**PB4 is used as COMP2_INP and connected to JP22 pin1**
		OFF	PB4 is NOT used as COMP PB4 can be used for audio MEMS, JTAG, or STMod+
PB5	SB39	**ON**	**PB5 is used as COMP2_OUT and connected to TP9**
		OFF	PB5 is NOT used as COMP PB5 can be used for USB or STMod+

1. *The default configuration is shown in bold.*

The input is accessible on pin 1 of the JP22 jumper header. On top of the possibility of routing either from the potentiometer or LDR to PB4, an external source can also be connected to it, using the JP22 terminal 1.

The PB5 output of the comparator can be accessed on test point TP9. Refer to the schematic of the STM32U575I-EV Evaluation board.

Table 40 describes the jumper configuration to enable the LDR or the potentiometer to Comp2 function.

Table 40. Jumper configuration to enable the LDR or the potentiometer to Comp2 function

Hardware	Setting(1)	Configuration
JP21/JP22	JP21[1-2]/ JP22[1-2]	Potentiometer RV1 is routed to pin PB4 of STM32U575AII6Q.
	JP21[2-3]/ JP22[1-2]	**LDR is routed to pin PB4 of STM32U575AII6Q.**

1. *The default configuration is shown in bold.*

7.20.5 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the physical interface features:

- OPAMP1_VOUT cannot be operated simultaneously with the OCTOSPI_CLK, or the motor-control functions.
- OPAMP1_INP cannot be operated simultaneously with the STMOD+_ADC, the UCPD IBUS-SENSE, or the motor control functions.
- COMP cannot be operated simultaneously with the audio MEMS ADF1, the JTAG JRSTN, the STMod+ SPI3_MISO2/MOSI2, and the MCU UCPD_DBCC1 functions.

7.21 Analog I/Os, VREF

7.21.1 Description

The STM32U575I-EV Evaluation board provides onboard analog-to-digital ADC and digital-to-analog DAC converters. The port PA4 can be configured to operate either as ADC input or as DAC output. PA4 is routed to the two-way header (CN8) allowing it to fetch signals to or from PA4 or to ground it setting CN8 ON.

7.21.2 ADC/DAC I/O interface

The parameters of the ADC input low-pass filter formed with R143 and C117 can be modified by replacing these components according to application requirements.

Similarly, the parameters of the DAC output low-pass filter formed with R144 and C117 can be modified by replacing these components according to application requirements.

The VREFP terminal of STM32U575AII6Q is used as the reference voltage for both ADC and DAC. By default, it is routed to VDDA by setting the JP18 two-way jumper ON. This jumper can be removed and an external voltage applied to JP18 terminal 2 for specific purposes.

Table 41 describes the hardware configuration for the ADC/DAC interface.

Table 41. ADC/DAC interface and connector (CN8) pinout

I/O	Hardware	Setting[1]	Configuration
PA4	SB16	**ON**	**PA4 is used as an ADC/DAC and connected to CN8 pin 1**
		OFF	PA4 is not used as an ADC/DAC PA4 can be used for STMod+ or motor control
VREFP	JP18	**ON**	**VDDA on VREFP used as ADC/DAC power supply reference**
		OFF	ADC/DAC not powered. External power supply reference can be applied to JP18 pin 2

1. *The default configuration is shown in bold.*

Table 42 describes the jumper configuration for the ADC/DAC interface.

Table 42. ADC/DAC interface and connector (CN8) pinout

Connector pin number	STM32 pin	Board function
1	PA4	ADC/DAC for test purpose
2	GND	GND reference

7.21.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the ADC/DAC features:

- ADC/DAC cannot be operated simultaneously with the STMod+ SPI_NSS function.
- ADC/DAC cannot be operated simultaneously with the motor-control function.

7.22 SRAM device

7.22.1 Description

A 16-Mbit static RAM (16-bit word SRAM) is fitted on the STM32U575I-EV Evaluation board in the U12 position.

7.22.2 Operating voltage

The SRAM is only functional in the voltage range from 2.4 to 3.6 V, according to the SRAM datasheet. This SRAM does not support the 1.8 V MCU low voltage.

7.22.3 SRAM interface

The STM32U575I-EV Evaluation board and the FMC addressing capabilities handle hosting SRAM devices up to 32 Mbytes. This is the reason why the schematic of the STM32U575I-EV Evaluation board mentions several SRAM devices, but by default, the STM32U575I-EV Evaluation board is assembled with a 16-Mbit SRAM.

The SRAM device is attached to the 16-bit data bus and accessed with FMC. The base address is `0x6000 0000`, corresponding to NOR/SRAM1 bank1. The SRAM device is selected with the FMC_NE1 chip select. FMC_NBL0 and FMC_NBL1 signals allow selecting 8-bit and 16-bit data word operating modes.

Table 43 describes the hardware configuration for the SRAM interface.

Table 43. **Hardware I/O configuration for the SRAM interface**

I/O	Hardware	Setting[1]	Configuration
PD7	R202	**ON**	**PD7 is used as FMC_NE1 and connected to SRAM**
PD5	R210	**ON**	**PD5 is used as FMC_NWE and connected to SRAM and LCD**
PD4	R216	**ON**	**PD4 is used as FMC_NOE and connected to SRAM and LCD**
PE0	R176	**ON**	**PE0 is used as FMC_NBL0 and connected to SRAM**
PE1	R181	**ON**	**PD4 is used as FMC_NBL1 and connected to SRAM**
PD14	R207	**ON**	**PD14 is used as FMC_D0 and connected to SRAM and LCD**
PD15	R213	**ON**	**PD15 is used as FMC_D1 and connected to SRAM and LCD**
PD0	R228	**ON**	**PD0 is used as FMC_D2 and connected to SRAM and LCD**
PD1	R224	**ON**	**PD1 is used as FMC_D3 and connected to SRAM and LCD**
PE7	R200	**ON**	**PE7 is used as FMC_D4 and connected to SRAM and LCD**
PE8	R197	**ON**	**PE8 is used as FMC_D5 and connected to SRAM and LCD**
PE9	R193	**ON**	**PE9 is used as FMC_D6 and connected to SRAM and LCD**
PE10	R188	**ON**	**PE10 is used as FMC_D7 and connected to SRAM and LCD**
PE11	R185	**ON**	**PE11 is used as FMC_D8 and connected to SRAM and LCD**
PE12	R182	**ON**	**PE12 is used as FMC_D9 and connected to SRAM and LCD**
PE13	R180	**ON**	**PE13 is used as FMC_D10 and connected to SRAM and LCD**
PE14	R175	**ON**	**PE14 is used as FMC_D11 and connected to SRAM and LCD**
PE15	R183	**ON**	**PE15 is used as FMC_D12 and connected to SRAM and LCD**
PD8	R186	**ON**	**PD8 is used as FMC_D13 and connected to SRAM and LCD**
PD9	R190	**ON**	**PD9 is used as FMC_D14 and connected to SRAM and LCD**
PD10	R192	**ON**	**PD10 is used as FMC_D15 and connected to SRAM and LCD**
PF0	R205	**ON**	**PF0 is used as FMC_A0 and connected to SRAM**
PF1	R208	**ON**	**PF1 is used as FMC_A1 and connected to SRAM**
PF2	R214	**ON**	**PF2 is used as FMC_A2 and connected to SRAM**
PF3	R218	**ON**	**PF3 is used as FMC_A3 and connected to SRAM**
PF4	R223	**ON**	**PF4 is used as FMC_A4 and connected to SRAM**
PF5	R227	**ON**	**PF5 is used as FMC_A5 and connected to SRAM**
PF12	R225	**ON**	**PF12 is used as FMC_A6 and connected to SRAM**
PF13	R221	**ON**	**PF13 is used as FMC_A7 and connected to SRAM**
PF14	R219	**ON**	**PF14 is used as FMC_A8 and connected to SRAM**
PF15	R215	**ON**	**PF15 is used as FMC_A9 and connected to SRAM**
PG0	R209	**ON**	**PG0 is used as FMC_A10 and connected to SRAM**
PG1	R203	**ON**	**PG1 is used as FMC_A11 and connected to SRAM**
PG2	R217	**ON**	**PG2 is used as FMC_A12 and connected to SRAM**
PG3	R222	**ON**	**PG3 is used as FMC_A13 and connected to SRAM**
PG4	R226	**ON**	**PG4 is used as FMC_A14 and connected to SRAM**
PG5	R229	**ON**	**PG5 is used as FMC_A15 and connected to SRAM**
PD11	R196	**ON**	**PD11 is used as FMC_A16 and connected to SRAM**
PD12	R199	**ON**	**PD12 is used as FMC_A17 and connected to SRAM**
PD13	R204	**ON**	**PD13 is used as FMC_A18 and connected to SRAM**

I/O	Hardware	Setting[1]	Configuration
PE3	R189	**ON**	**PE3 is used as FMC_A19 and connected to SRAM**
PE4	R191	ON	PE4 is used as FMC_A20 and connected to SRAM
		OFF	**PE4 is not used as FMC_A20.** **PE4 can be used for audio MEMS**

1. *The default configuration is shown in bold.*

7.22.4 I/O restriction to other features

By default, only a 16-Mbit SRAM is present on the STM32U575I-EV Evaluation board. An update of the SRAM (footprint compatible) is possible to increase the memory up to 32 Mbits (21 address lines). The FMC interface is shared with the LCD.

7.23 Octo-SPI2 flash memory device

7.23.1 Description

A 512-Mbit Octo-SPI flash memory device is fitted on the STM32U575I-EV Evaluation board in the U47 position, on the bottom side of the PCB. This is used to evaluate the STM32U575AII6Q Octo-SPI2 interface.

The Octo-SPI flash memory can operate in both single (STR) and double (DTR) transfer rate modes.

7.23.2 Operating voltage

The voltage of the Octo-SPI flash memory device is in the range of 2.7 to 3.6 V. The Octo-SPI memory does not support the 1.8 V MCU low voltage.

7.23.3 Octo-SPI2 flash I/O interface

Table 44 describes the hardware configuration for the Octo-SPI2 interface.

Table 44. Hardware I/O configuration for the Octo-SPI2 flash interface

I/O	Hardware	Setting[1]	Configuration
PI5	SB112 JP20[1-2]	**ON**	**PI5 is connected to Octo-SPI2 FLASH as NCS**
		OFF	PI5 is NOT connected to Octo-SPI2 FLASH PI5 can be used for camera
PH6	R179	**ON**	**PH6 is connected to Octo-SPI2 FLASH as CLK**
		OFF	No other multiplexing
PH4	R178	**ON**	**PH4 is connected to Octo-SPI2 FLASH as DQS**
		OFF	No other multiplexing
PI3	SB98	**ON**	**PI3 is connected to Octo-SPI2 FLASH as IO0**
		OFF	PI3 is NOT connected to Octo-SPI2 FLASH PI3 can be used for camera
PI2	SB101	**ON**	**PI2 is connected to Octo-SPI2 FLASH as IO1**
		OFF	PI2 is NOT connected to Octo-SPI2 FLASH PI2 can be used for camera
PI1	R177	**ON**	**PI1 is connected to Octo-SPI2 FLASH as IO2**
		OFF	No other multiplexing
PH8	SB96	**ON**	**PH8 is connected to Octo-SPI2 FLASH as IO3**
		OFF	PH8 is NOT connected to Octo-SPI2 FLASH PH8 can be used for camera
PH9	SB95	**ON**	**PH9 is connected to Octo-SPI2 FLASH as IO4**
		OFF	PH9 is NOT connected to Octo-SPI2 FLASH PH9 can be used for camera
PH10	SB97	**ON**	**PH10 is connected to Octo-SPI2 FLASH as IO5**
		OFF	PH10 is NOT connected to Octo-SPI2 FLASH PH10 can be used for camera
PH11	SB99	**ON**	**PH11 is connected to Octo-SPI2 FLASH as IO6**
		OFF	PH11 is NOT connected to Octo-SPI2 FLASH PH11 can be used for camera
PH12	SB100	**ON**	**PH12 is connected to Octo-SPI2 FLASH as IO7**
		OFF	PH12 is NOT connected to Octo-SPI2 FLASH PH12 can be used for camera
NRST	R211	**ON**	**NRST is connected to octo-SPI2 FLASH RESETN pin**

1. *The default configuration is shown in bold.*

7.23.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the Octo-SPI2 flash features:

- The Octo-SPI flash function cannot be operated simultaneously with the camera daughterboard. There is no older bridge for the camera interface. It is recommended to remove the camera daughterboard to use the Octo-SPI2 flash device.

7.24 Octo-SPI1

7.24.1 Description

The STM32U575I-EV Evaluation board embeds the possibility of evaluating more Octo-SPI memory devices. Two 2x10-pin high-speed socket connectors are available to support the MB1242 ST memory daughterboard. One MB1242 with Octo-SPI PSRAM memory is included on the STM32U575I-EV Evaluation board.

7.24.2 Operating voltage

Depending on the MB1242 daughterboard and Octo-SPI memory used, the Octo-SPI1 interface is compatible with the VDD_MCU voltage range from 1.71 to 3.6 V.

7.24.3 Octo-SPI1 I/O interface

Table 45 describes the hardware configuration for the Octo-SPI1 interface of the external MB1242 daughterboard.

Table 45. Hardware I/O configuration for the Octo-SPI1 interface for the external MB1242 daughterboard

I/O	Hardware	Setting[1]	Configuration
PA2	R151	**ON**	**PA2 is connected to Octo-SPI1 as chip select (active low) mainly for the Octo-SPI PSRAM configuration.**
		OFF	PA2 is NOT connected to Octo-SPI1. PA2 can be used for motor control.
PI5	SB112 JP20[2-3]	**ON**	**PI5 is connected to Octo-SPI1 as chip select (active low) mainly for Octo-SPI flash configuration.**
		OFF	PI5 is NOT connected to Octo-SPI1 flash memory. PI5 can be used for the camera.
PA3	R150	**ON**	**PA3 is connected to Octo-SPI1 as CLK_P.**
		OFF	PA3 is NOT connected to Octo-SPI. PA3 can be used for OpAmp or motor control.
PB12	SB47	ON	PB12 is connected to Octo-SPI1 as CLK_N.
		OFF	**PB12 is NOT connected to Octo-SPI1** **PB12 can be used for smartcard** or motor control
PB2	R148	**ON**	**PB2 is connected to Octo-SPI1 as DQS**
		OFF	PB2 is NOT connected to Octo-SPI1. PB2 can be used for motor control.
PB1	R155	**ON**	**PB1 is connected to Octo-SPI1 as IO0.**
		OFF	PB1 is NOT connected to Octo-SPI1. PB1 can be used for motor control.
PB0	R152	**ON**	**PB0 is connected to Octo-SPI1 as IO1.**
		OFF	PB0 is NOT connected to Octo-SPI1. PB0 can be used for motor control.
PA7	R159	**ON**	**PA7 is connected to Octo-SPI1 as IO2.**
		OFF	PA7 is NOT connected to Octo-SPI1. PA7 can be used for motor control.
PA6	R158	**ON**	**PA6 is connected to Octo-SPI1 as IO3**
		OFF	PA6 is NOT connected to Octo-SPI1. PA6 can be used for motor control.
PC1	R163	**ON**	**PC1 is connected to Octo-SPI1 as IO4.**

I/O	Hardware	Setting[1]	Configuration
PC1	R163	OFF	PC1 is NOT connected to Octo-SPI1. PC1 can be used for motor control.
PC2	R162	**ON**	**PC2 is connected to Octo-SPI1 as IO5.**
		OFF	PC2 is NOT connected to Octo-SPI1. PC2 can be used for motor control.
PC3	R164	**ON**	**PC3 is connected to Octo-SPI1 as IO6.**
		OFF	PC3 is NOT connected to Octo-SPI1. PC3 can be used for motor control.
PC0	R160	**ON**	**PC0 is connected to Octo-SPI1 as IO7.**
		OFF	PC0 is NOT connected to Octo-SPI1. PC0 can be used for motor control.
NRST	SB64	**ON**	**NRST is connected to the Octo-SPI1 RESETN pin.**

1. *The default configuration is shown in bold.*

To support the MB1242 Octo-SPI memory daughterboard, two high-speed socket connectors are used. Figure 27 shows the Octo-SPI connector (CN5/CN11) pinout.

Figure 27. Octo-SPI connector (CN5/CN11) pinout

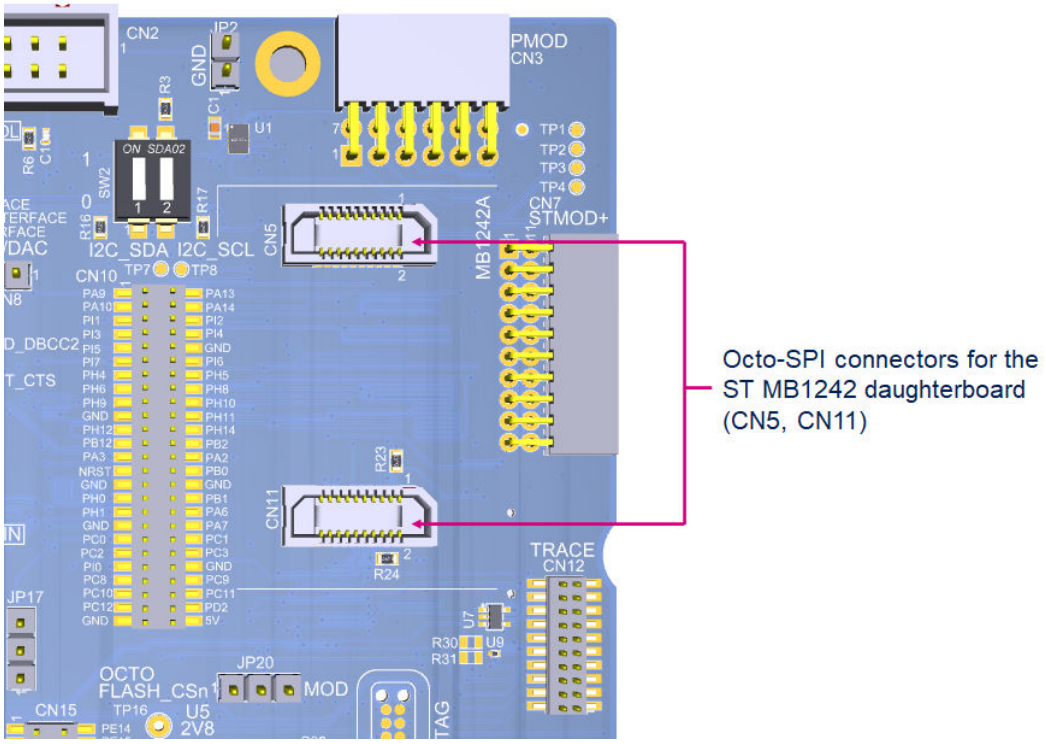


Table 46 describes the Octo-SPI connector (CN11) pinout

Table 46. Octo-SPI connector (CN11) pinout

Connector pin number	STM32 pin	Board function
1	PI5	Octo-SPI chip select interface low level. mainly for Octo-SPI flash memory configuration. This signal is connected to a 10K pull-up on board (R23).
2	VDD	Power VDD
3	PB1	OCTOPSI_1 interface data0
4	VDD	Power VDD
5	PB0	OCTOPSI_1 interface data1
6	PA2	Octo-SPI chip select interface low level. mainly for Octo-SPI PSRAM device configuration. This signal is connected to a 10K pull-up on board (R24).
7	PA7	OCTOPSI_1 interface data2
8	PC1	OCTOPSI_1 interface data4
9	PA6	OCTOPSI_1 interface data3
10	PC2	OCTOPSI_1 interface data5
11	PB2	OCTOPSI_1 data strobe signal
12	PC3	OCTOPSI_1 interface data6
13	GND	Power GND
14	PC0	OCTOPSI_1 interface data7
15	PB12	OCTOPSI_1_CLK_N: For a memory with differential clock
16	NRST	OCTOPSI_1 reset function
17	PA3	OCTOPSI_1_CLK_P clock for single or differential clock
18	GND	Power GND
19	GND	Power GND
20	GND	Power GND

Table 47 describes the Octo-SPI connector (CN5) pinout

Table 47. Octo-SPI connector (CN5) pinout

Connector pin number	STM32 pin	Board function
1	VDD	Power VDD
2	VDD	Power VDD
3	VDD	Power VDD
4	VDD	Power VDD
5	NC	-
6	NC	-
7	NC	-
8	NC	-
9	NC	-
10	NC	-
11	NC	-
12	NC	-
13	RFU2	Reserved for future use 2
14	RFU1	Reserved for future use 1
15	RSTOUTn	Optional reset output from MB1242 daughterboard
16	INTn	Optional interruption output from MB1242 daughterboard
17	GND	Power GND
18	GND	Power GND
19	GND	Power GND
20	GND	Power GND

7.24.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the Octo-SPI1 interface:

- The Octo-SPI1 function cannot be operated simultaneously with the motor-control function.
- The Octo-SPI1 CLK function cannot be operated simultaneously with the OpAmp function.
- The Octo-SPI1 CLKN function cannot be operated simultaneously with Smartcard_CLK and motor control.

7.25 EEPROM

7.25.1 Description

The 128-Kbit I^2C-bus EEPROM device is fitted on the STM32U575I-EV Evaluation board in the U8 position. It is accessed with STM32U575AII6Q I^2C-bus lines I2C_SCL and I2C_SDA. EEPROM write protection is possible when the SB2 solder bridge is OFF. SB2 is ON by default and writing into the EEPROM is enabled.

7.25.2 Operating voltage

The EEPROM device operating voltage is fully compatible with the 1.71 to 3.6 V MCU voltage range.

7.25.3 EEPROM I/O interface

The EEPROM I²C interface supports all the I²C-bus modes with speeds up to 1 MHz. The I²C-bus base address is `0xA0` (`0b1010000x`).

Table 48 describes the hardware configuration for the EEPROM interface.

Table 48. Hardware I/O configuration for the EEPROM interface

I/O	Hardware	Setting(1)	Configuration
PG8	JP11	**[1-2]**	**PG8 is used as I2C3_SDA to interface the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector.**
		[2-3]	PG8 is used as RS-232 or STMod+ USART.
PG7	JP10	**[1-2]**	**PG7 is used as I2C3_SCL to interface the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector.**
		[2-3]	PG8 is used as RS-232 or STMod+ USART.
PB11	SB14	ON	PB11 is used as I2C2_SDA to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensor like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector (SB49 ON).
		OFF	**PB11 is not used as I²C for the sensor, the EEPROM, and the external I²C connector.**
PB10	SB13	ON	PB10 is used as I2C2_SCL to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensor like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector (SB46 ON).
		OFF	**PB10 is not used as I²C for the sensor, the EEPROM, and the external I²C connector.**

1. *The default configuration is shown in bold.*

7.26 EXT_I2C connector

7.26.1 Description

The EXT_I2C connector (CN4) can be connected to the I²C-bus daughterboard. MFX_GPIO8 of MFX MCU provides EXT_RESET.

7.26.2 Operating voltage

CN4 pin 4 is connected to VDD. Therefore, the external daughterboard must be compliant with the MCU normal-voltage range from 2.7 to 3.3 V, or low-voltage range from 1.7 to 3.3 V.

7.26.3 EXT_I2C I/O interface

The EXT_I2C connector can accept a daughterboard that can have a different I²C base address. Be careful not to use a daughterboard with an I²C base address already used in the STM32U575I-EV Evaluation board to avoid I²C conflict.

Table 49 describes the hardware configuration for the EXT_I2C connector.

Table 49. Hardware I/O configuration for the EXT_I2C connector

I/O	Hardware	Setting[1]	Configuration
PG8	JP11	**[1-2]**	**PG8 is used as I2C3_SDA to interface the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector**
		[2-3]	PG8 is used as RS-232 or STMod+ USART
PG7	JP10	**[1-2]**	**PG7 is used as I2C3_SCL to interface the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector**
		[2-3]	PG8 is used as RS-232 or STMod+ USART
PB11	SB14	ON	PB11 is used as I2C2_SDA to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensor like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector (SB49 0N)
		OFF	**PB11 is not used as I²C for the sensor, the EEPROM, and the external I²C connector**
PB10	SB13	ON	PB10 is used as I2C2_SCL to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensor like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector (SB46 ON)
		OFF	**PB10 is not used as I²C for the sensor, the EEPROM, and the external I²C connector**

1. *The default configuration is shown in bold.*

Figure 28 shows the EXT_I2C connector (CN4) pinout

Figure 28. EXT_I2C connector (CN4) pinout front view

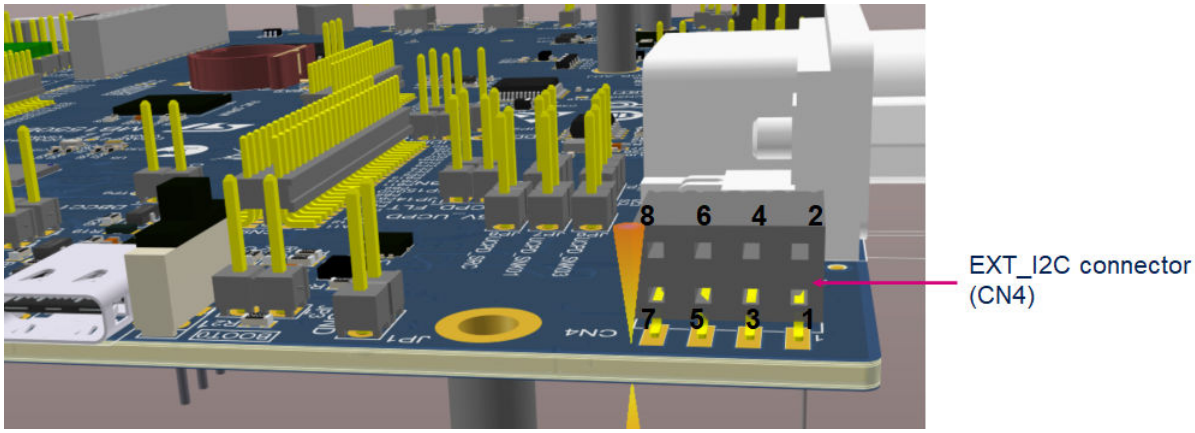


Table 50. **EXT_I2C connector (CN4) pinout**

Connector pin number	STM32 pin	Board function
1	-	-
2	GND	Power GND
3	-	-
4	VDD	Power VDD
5	MFX_IO8	External reset command from MFX
6	PG7/PB10	I^2C SCL clock signal
7	-	-
8	PG8/PB11	I^2C SDA data signal

7.27 Touchkey button

7.27.1 Description

The STM32U575I-EV Evaluation board supports a touchkey button based on either RC charging or charge transfer technique. This one is enabled by default.

7.27.2 Touchkey button I/O interface

The touchkey button is connected to one of the TSC ports of STM32U575AII6Q with the related charge capacitor.

An active shield is designed in layer 2 of the main PCB, under the button footprint. It helps reduce disturbances from other circuits to avoid false touch detections.

The active shield is connected to another TSC interface of STM32U575AII6Q through the R21 serial resistor. The related charge capacitor is connected to the same TSC interface.

The solder bridge and jumper configuration related to the touchkey function enables or disables its operation. However, most of them serve to optimize the touchkey performance, by isolating copper tracks to avoid disturbances due to their antenna effect.

For more information about the TSC interface and the tuning explanation for this interface, refer to the application note *Getting started with touch sensing control on STM32 microcontrollers* (AN5105) and the STM32U5xx product datasheets.

Table 51 describes the hardware configuration for the touchkey button interface.

Table 51. Hardware I/O configuration for the touchkey button interface

I/O	Hardware	Setting[1]	Configuration
PC6	SB24/SB29	**OFF**	**PC6 is directly connected to the touchkey button.**
		ON	PC6 can be used for the extension I/O connector or motor control. In this case, the touchkey layout is not optimized and the touchkey button might not be functional.
PC7	SB25/SB30	**OFF**	**PC7 is directly connected to TKEY_CS.**
		ON	PC7 can be used for the extension I/O connector or motor control. In this case, the touchkey layout is not optimized and the touchkey button might not be functional.
PB13	JP12/SB34	**OFF/OFF**	**PB13 is directly connected to the SHIELD touchkey button.**
		ON/ON	PB13 can be used for the extension I/O connector, RS-232, or STMod+. In this case, the touchkey layout is not optimized and the touchkey button might not be functional.
PB14	JP9/SB23	**OFF/OFF**	**PB14 is directly connected to SHIELD_CS.**
		ON/ON	PB14 can be used for the extension I/O connector or UCPD. In this case, the touchkey layout is not optimized and the touchkey button might not be functional.

1. *The default configuration is shown in bold.*

7.27.3 I/O restriction to other features

Caution: Due to the sharing of some I/Oss of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the touchkey button feature:

- The touchkey button cannot be operated simultaneously with the motor-control function.
- The touchkey button cannot be operated simultaneously with the RS-232 4-wire interface LPUART1_CTS.
- The touchkey button cannot be operated simultaneously with the STMOD+_LPUART1_CTS.
- The touchkey button cannot be operated simultaneously with the MCU UCPD_DBCC2.

7.28 MFX MCU

7.28.1 Description

The multifunction expander MFX MCU is used as a GPIO expander and is fitted on the STM32U575I-EV Evaluation board in the U15 position.

7.28.2 Operating voltage

The MFX MCU is connected to VDD and is fully compatible with the 1.71 to 3.6 V MCU voltage range.

7.28.3 MFX I/O-expander

The MFX circuit on the STM32U575I-EV Evaluation board acts as an I/O-expander. The communication interface between MFX and STM32U575AII6Q is an I^2C bus, with a wake-up pin and an interrupt pin.

Table 52 describes the hardware configuration for the MFX interface.

Table 52. Hardware I/O configuration for the MFX interface

I/O	Hardware	Setting[1]	Configuration
PC5	SB70	**ON**	**PC5 is connected to MFX as MFX_IRQ_OUT.** No other multiplexing
PF11	SB60	**ON**	**PF11 is connected to MFX as MFX_WAKEUP.** No other multiplexing
NRST	-	**ON**	**MCU NRST direct connection.**
PB11	SB49	**ON**	**PB11 is used as I2C2_SDA to interface the audio codec, the MFX, the UCPD, the CTP, the camera, STMod+, and optionally the sensor like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector (SB49 0N).**
PB10	SB46	**ON**	**PB10 is used as I2C2_SCL to interface the audio codec, the MFX, the UCPD, the CTP, the camera, the STMod+, and optionally the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector (SB46 ON).**

1. *The default configuration is shown in bold.*

Table 53 describes the hardware I/O driven by the MFX.

Table 53. Hardware I/O driven by the MFX

I/O	Hardware	Setting	Configuration
18	GPIO0	JOY_SEL	B1 joystick selection
19	GPIO1	JOY_DOWN	B1 joystick down direction
20	GPIO2	JOY_LEFT	B1 joystick left direction
39	GPIO3	JOY_RIGHT	B1 joystick right direction
40	GPIO4	JOY_UP	B1 joystick up direction
15	GPIO5	MEMS_LED	CN29 LED for external audio module
16	GPIO6	SMARTCARD_OFF	U21 smartcard OFF
17	GPIO7	SMARTCARD_RST	U21 smartcard RESET
29	GPIO8	EXT_RESET	CN4 external I²C module RESET
30	GPIO9	SMARTCARD_CMDVCC	U21 smartcard VCC cmd
31	GPIO10	SMARTCARD_3V/5V	U21 smartcard 3 V 5 V selection
32	GPIO11	LED_BLUE	Blue LED (LD7)
33	GPIO12	LCD_RESET	CN23 LCD reset
26	GPIO13	LED_YELLOW	Yellow LED (LD8)
27	GPIO14	STMOD+_RST	CN7 STMod+ reset, CN3 PMOD_RST
28	GPIO15	AUDIO_RSTN	U25 audio reset

7.29 TFT LCD

7.29.1 Description

The 34-pin 2.54 mm pitch female connector (CN23) is designed to connect the MB989 TFT LCD daughterboard supporting the FMC interface to the MB1550 main board. The LCD daughterboard is composed of the TFT LCD daughterboard supporting a resolution of 240 x 320 dots 262K colors and a touch-panel feature driven by MFX in U15 position.

7.29.2 Operating voltage

The design of the MB989 LCD daughterboard is compatible with a voltage range from 1.65 to 3.3 V. So, the LCD is fully compatible with the 1.8 V MCU low voltage.

7.29.3 LCD interface

Table 54 describes the hardware configuration for the LCD and CTP interface.

Table 54. Hardware I/O configuration for the LCD and CTP interface

I/O	Hardware	Setting(1)	Configuration(2)
PG12	R187	**ON**	**PG12 is used as FMC_NE4_LCD_CSn and connected to LCD**
PD5	R210	**ON**	**PD5 is used as FMC_NWE and connected to SRAM and LCD**
PD4	R216	**ON**	**PD4 is used as FMC_NOE and connected to SRAM and LCD**
PE6	R198	**ON**	**PE6 is used as FMC_A22_LCD_RS and connected to LCD**
PD14	R207	**ON**	**PD14 is used as FMC_D0 and connected to SRAM and LCD**
PD15	R213	**ON**	**PD15 is used as FMC_D1 and connected to SRAM and LCD**
PD0	R228	**ON**	**PD0 is used as FMC_D2 and connected to SRAM and LCD**
PD1	R224	**ON**	**PD1 is used as FMC_D3 and connected to SRAM and LCD**
PE7	R200	**ON**	**PE7 is used as FMC_D4 and connected to SRAM and LCD**
PE8	R197	**ON**	**PE8 is used as FMC_D5 and connected to SRAM and LCD**
PE9	R193	**ON**	**PE9 is used as FMC_D6 and connected to SRAM and LCD**
PE10	R188	**ON**	**PE10 is used as FMC_D7 and connected to SRAM and LCD**
PE11	R185	**ON**	**PE11 is used as FMC_D8 and connected to SRAM and LCD**
PE12	R182	**ON**	**PE12 is used as FMC_D9 and connected to SRAM and LCD**
PE13	R180	**ON**	**PE13 is used as FMC_D10 and connected to SRAM and LCD**
PE14	R175	**ON**	**PE14 is used as FMC_D11 and connected to SRAM and LCD**
PE15	R183	**ON**	**PE15 is used as FMC_D12 and connected to SRAM and LCD**
PD8	R186	**ON**	**PD8 is used as FMC_D13 and connected to SRAM and LCD**
PD9	R190	**ON**	**PD9 is used as FMC_D14 and connected to SRAM and LCD**
PD10	R192	**ON**	**PD10 is used as FMC_D15 and connected to SRAM and LCD**
PA8	-	**ON**	**PA8 is used as LCD_BL_CTRL.**
NRST	R120	**ON**	**MCU NRST direct connection to the CTP driver.**
PG15	SB35	**ON**	**PG15 is used as LCD_CTP_INT for the CTP driver.**
PB11	SB49	**ON**	**PB11 is used as I2C2_SDA to interface the audio codec, MFX, UCPD, CTP, camera, STMod+, and optional sensors like the 3D accelerometer and the 3G gyroscope, but also the I^2C EEPROM and the external I^2C connector**

I/O	Hardware	Setting[1]	Configuration[2]
PB10	SB46	**ON**	**PB10 is used as I2C2_SCL to interface the audio codec, MFX, UCPD, CTP, camera, STMod+, and optional sensors like the 3D accelerometer and the 3G gyroscope, but also the I^2C EEPROM and the external I^2C connector**
MFX-IO12	-	**ON**	**MFX_IO12 is used as LCD_RESET and connected to LCD.**
TSC_XP	SB129	**OFF**	**TSC_XP is not managed by an external CTP driver but can be managed by MFX according to SB configuration.**
		ON	TSC_XP is managed by an external CTP driver.
	SB136	OFF	TSC_XP is not managed by MFX but can be managed by the CTP driver according to SB configuration.
		ON	**TSC_XP is managed by MFX.**
TSC_XN	SB131	**OFF**	**TSC_XN is not managed by an external CTP driver but can be managed by MFX according to SB configuration.**
		ON	TSC_XN is managed by an external CTP driver
	SB142	OFF	TSC_XN is not managed by MFX but can be managed by the CTP driver according to SB configuration.
		ON	**TSC_XN is managed by MFX.**
TSC_YP	SB130	**OFF**	**TSC_YP is not managed by an external CTP driver but can be managed by MFX according to SB configuration.**
		ON	TSC_YP is managed by an external CTP driver
	SB139	OFF	TSC_YP is not managed by MFX but can be managed by the CTP driver according to SB configuration
		ON	**TSC_YP is managed by MFX.**
TSC_YN	SB132	**OFF**	**TSC_YN is not managed by an external CTP driver but can be managed by MFX according to SB configuration**
		ON	TSC_YN is managed by an external CTP driver
	SB140	OFF	TSC_YN is not managed by MFX but can be managed by the CTP driver according to SB configuration
		ON	**TSC_YN is managed by MFX**

1. *The default configuration is shown in bold.*
2. *For information: Because the CTP driver is obsolete, signals are managed by MFX.*

Figure 29 shows the LCD connector (CN23) pinout.

Figure 29. LCD connector (CN23) pinout

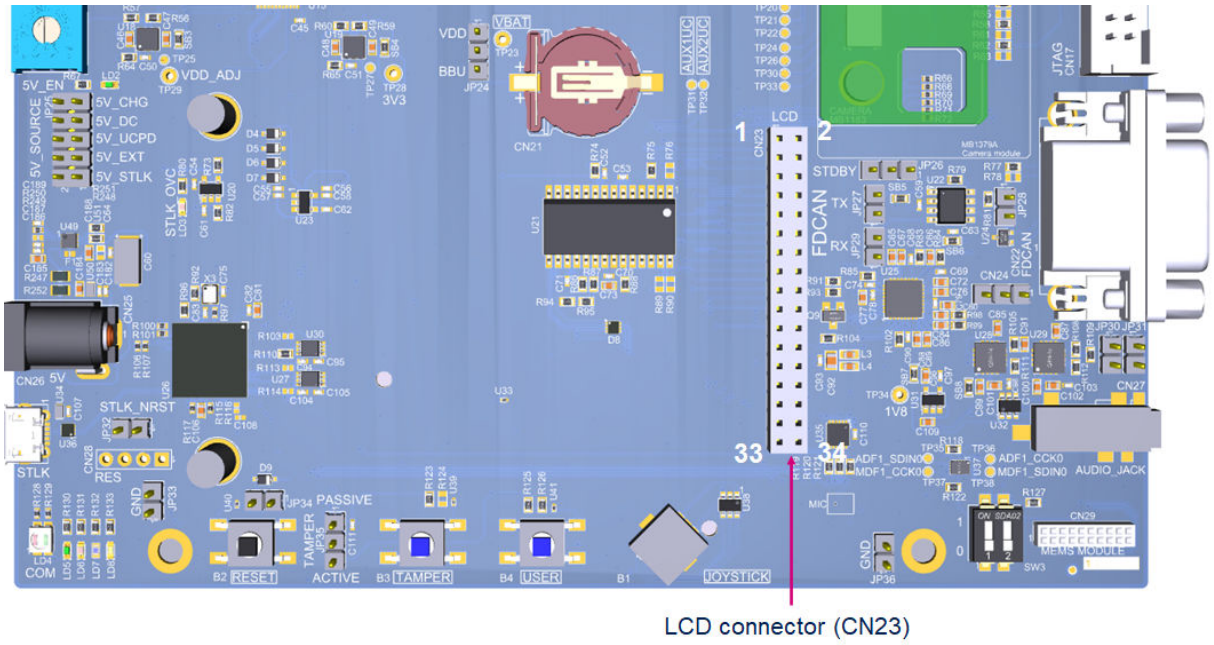


Table 55 describes the LCD connector (CN23) pinout

Table 55. LCD connector (CN23) pinout

Connector pin number	STM32 pin	Board function
1	PG12	FMC_NE4_LCD_CSn: Chip select function (active low)
2	PE6	FMC_A22_LCD_RS: Register-select signal
3	PD5	FMC_NWE: Write enable signal active high
4	PD4	FMC_NOE: Read enable signal active low
5	MFX_IO12	LCD_RESET: LCD reset
6	PD14	D0: FMC data bus interface data_0
7	PD15	D1: FMC data bus interface data_1
8	PD0	D2: FMC data bus interface data_2
9	PD1	D3: FMC data bus interface data_3
10	PE7	D4: FMC data bus interface data_4
11	PE8	D5: FMC data bus interface data_5
12	PE9	D6: FMC data bus interface data_6
13	PE10	D7: FMC data bus interface data_7
14	PE11	D8: FMC data bus interface data_8
15	PE12	D9: FMC data bus interface data_9
16	PE13	D10: FMC data bus interface data_10
17	PE14	D11: FMC data bus interface data_11
18	PE15	D12: FMC data bus interface data_12
19	PD8	D13: FMC data bus interface data_13
20	PD9	D14: FMC data bus interface data_14
21	PD10	D15: FMC data bus interface data_15
22	-	BLGND: Dedicated GND for backlight
23	PA8	BL_CTRL: Backlight control ON/OFF
24	VDD	VDD_LCD power supply for IO interface
25	VDD	VCI power supply for the analog part
26	GND	Power GND
27	GND	Power GND
28	-	VDD_BL: Dedicated power voltage for backlight
29	-	SDO SPI interface output not used
30	-	SDI SPI interface input not used fixed to GND
31	MFX_XP/GPO0	Touch-panel control signal TSC_XN/XL
32	MFX_XN/GPO1	Touch-panel control signal TSC_XP/XR
33	MFX_YP/GPO2	Touch-panel control signal TSC_YN/YD
34	MFX_YN/GPO3	Touch-panel control signal TSC_YP/YU

7.29.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the LCD feature:

- The FMC interface is shared with SRAM.

7.30 Camera

7.30.1 Description

The 40-pin 1.00 mm pitch female connector (CN16) is designed to connect the MB1379 CMOS camera daughterboard supporting the DCMI interface.

The CMOS camera daughterboard is composed of the QSXGA 5-Mpixel CMOS camera with a dedicated 24 MHz crystal.

7.30.2 Operating voltage

The MB1379 CMOS camera requests a 2.8 V supply for the analog part and I/Os compatible with 1.8 to 2.8 V voltage. For DCMI signals from the camera to the MCU, a 2.8 V I/O level is considered enough to show a HIGH state for a 3.3 V I/O.

For the signal from the MCU to the camera, meaning the I^2C interface, two MOSFETs are used on this interface to drive the I^2C camera between 3.3 and 2.8 V.

7.30.3 Camera interface

The camera daughterboard cannot be operated simultaneously with the Octo-SPI2 flash memory. To use the camera daughterboard, keep Octo-SPI2 flash memory unselected (PI5 chip-select HIGH) or removed JP20 from Octo-SPI2 flash chip select signal (R195 external pull-up resistor keeps Octo-SPI2 CS flash memory signal HIGH). To have a clear bus interface, remove the Octo-SPI2 flash memory solder bridge. Refer to Section 7.23: Octo-SPI2 flash memory device for further details.

Table 56 describes the hardware configuration for the camera interface.

Table 56. Hardware I/O configuration for the camera interface

I/O	Hardware	Setting[1]	Configuration
PG10	SB103	**ON**	**PG10 is used as CAMERA PLUG (detection of the camera daughterboard presence).**
		OFF	PG10 can be used for STMod+.
PI2	-	**ON**	**PI2 is used as CAMERA RSTI (reset of the camera daughterboard).**
PI3	-	**ON**	**PI3 is used as CAMERA XSDN (external CLOCK for the camera daughterboard). It is not used inside this camera daughterboard, which has an internal 24 MHz crystal.**
PH9	-	**ON**	**PH9 is used as DCMI_D0 of the camera daughterboard.**
PH10	-	**ON**	**PH10 is used as the DCMI_D1 of the camera daughterboard.**
PH11	-	**ON**	**PH11 is used as the DCMI_D2 of the camera daughterboard.**
PH12	-	**ON**	**PH12 is used as the DCMI_D3 of the camera daughterboard.**
PH14	-	**ON**	**PH14 is used as the DCMI_D4 of the camera daughterboard.**
PI4	-	**ON**	**PI4 is used as DCMI_D5 of the camera daughterboard.**
PI6	-	**ON**	**PI6 is used as DCMI_D6 of the camera daughterboard.**
PI7	-	**ON**	**PI7 is used as DCMI_D7 of the camera daughterboard.**
PH8	-	**ON**	**PH8 is used as DCMI_HSYNC of the camera daughterboard.**
PI5	-	**ON**	**PI5 is used as DCMI_VSYNC of the camera daughterboard.**
PH5	R145	**ON**	**PH5 is used as DCMI_PIXCLK of the camera daughterboard.**
PB11	-	**ON**	**PB11 is used as I2C2_SDA to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensors like the 3D accelerometer and the 3G gyroscope, but also the I^2C EEPROM and the external I^2C connector**
PB10	-	**ON**	**PB10 is used as I2C2_SCL to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensors like the 3D accelerometer and the 3G gyroscope, but also the I^2C EEPROM and the external I^2C connector**

1. *The default configuration is shown in bold.*

Figure 30 shows the camera connector (CN16) pinout.

Figure 30. Camera connector (CN16) pinout

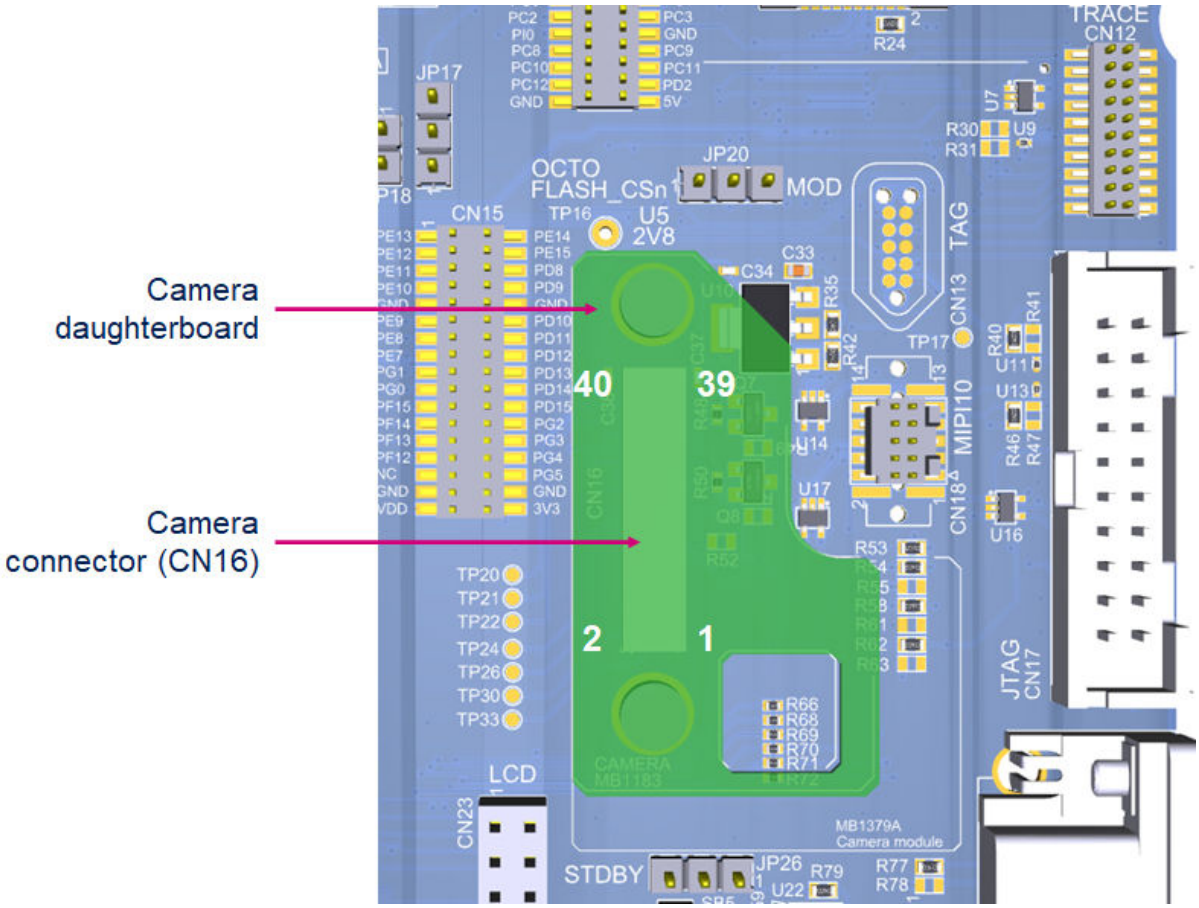


Table 57 describes the camera daughterboard connector (CN16) pinout

Table 57. **Camera connector (CN16) pinout**

Connector pin number	STM32 pin	Board function
1	-	Not used
2	-	Not used
3	GND	Power GND
4	GND	Power GND
5	-	Not used
6	-	Not used
7	GND	Power GND
8	GND	Power GND
9	-	Not used
10	-	Not used
11	GND	Power GND
12	GND	Power GND
13	PB10	I2C_SCL_CAMERA
14	PB11	I2C_SDA_CAMERA
15	PG10	CAMERA_PLUG
16	GND	Power GND
17	PI2	CAMERA_RSTI
18	-	Not used
19	PI3	CAMERA_XSDN
20	-	Not used
21	GND	Power GND
22	GND	Power GND
23	PH9	DCMI_D0
24	PH10	DCMI_D1
25	PH11	DCMI_D2
26	PH12	DCMI_D3
27	PH14	DCMI_D4
28	PI4	DCMI_D5
29	PI6	DCMI_D6
30	PI7	DCMI_D7
31	PH8	DCMI_HSYNC
32	PI5	DCMI_VSYNC
33	PH5	DCMI_PIXCLK
34	-	Not used
35	-	Not used
36	-	Not used
37	GND	Power GND
38	GND	Power GND
39	-	Power 2V8
40	-	Power 2V8

7.30.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the camera feature:

- The camera function cannot be operated simultaneously with the Octo-SPI2 flash memory.

7.31 Pmod™ connector

7.31.1 Description

The standard 12-pin Pmod™ connector (CN3) is available on the STM32U575I-EV Evaluation board to support low frequency, low I/O pin count peripheral daughterboards. The Pmod™ interface, which is implemented in the STM32U575I-EV Evaluation board, is compatible with the Pmod™ type 2A and 4A I/O signal assignment convention.

7.31.2 Operating voltage

The Pmod™ connector is directly supplied by VDD.

VDD must be set to 3.3 V to be I/O compatible with the Pmod™ connector.

7.31.3 Pmod™ I/O interface

The Pmod™ connector supports several interface configurations:

- SPI interface: NSS, MOSI, MISO, and SCK
- UART interface: Tx, Rx, CTS, and RTS
- mikroBUS™ interface: NSS, Tx, Rx, and SCK

To support the selection of SPI or UART function connections on Pmod™, a quad-SPDT switch is added to the board. This switch is controlled manually.

Table 58 describes the SW2 configuration to select the Pmod™ interface.

Table 58. SW2 configuration for Pmod™ interface

Hardware SW2 [2-1][1]	Interface
00	SPI interface selected
01	mikroBUS™ interface selected
10	Not used
11	**UART interface selected**

1. *The default configuration is in bold.*

Table 59 describes the hardware configuration for the Pmod™ interface.

Table 59. Hardware I/O configuration for the Pmod™ interface

I/O	Hardware	Setting(1)	Configuration
PA4	SB18	**ON**	**PA4 is used as SPI_NSS on Pmod™ and shared with STMod+ and ADC/ DAC.**
		OFF	PA4 is not used as SPI_NSS on Pmod™. PA4 can be used for motor control or ADC/DAC.
PC12	SB94	**ON**	**PC12 is used as SPI3_MOSI on Pmod™ and shared with STMod+, trace, and SD card.**
		OFF	PC12 is not used as SPI3_MOSI on Pmod™. PC12 can be used for the SD card or trace.
PG10	SB102	**ON**	**PG10 is used as SPI3_MISO on Pmod™ and shared with STMod+ and the camera.**
		OFF	PG10 is not used as SPI3_MISO on Pmod™. PG10 can be used for the camera.
PG9	SB108	**ON**	**PG9 is used as SPI3_SCK on Pmod™ and shared with STMod+.**
		OFF	PG9 is not used as SPI3_SCK on Pmod™ PG9 can be used for motor control
PB13	JP12	ON	PB13 is used as LPUART1_CTS on Pmod™ and shared with STMod+ and RS-232.
		OFF	**PB13 is not used as LPUART1_CTS on Pmod™.** **PB13 can be used for touchkey.**
PG7	JP10	[2-3]	PG7 is used as LPUART1_TX on Pmod™ and shared with STMod+ and RS-232.
		[1-2]	**PG7 is not used as LPUART1_TX on Pmod™.** **PG7 can be used for I^2C SENSOR or UCPD.**
PG8	JP11	[2-3]	**PG8 is used as LPUART1_RX on Pmod™ and shared with STMod+ and RS-232.**
		[1-2]	PG8 is not used as LPUART1_RX on Pmod™. PG8 can be used for UCPD or I2C3 backup.
PG6	SB38	**ON**	**PG6 is used as LPUART1_RTS on Pmod™ and shared with STMod+ and RS-232**
		OFF	PG6 is not used as LPUART1_RX on Pmod™. PG6 can be used for UCPD.
PA1	SB71/R135	**ON/ON**	**PA1 is used as PMOD_INT on Pmod™ and shared with STMod+ and TAMPER_KEY.**
		OFF/OFF	PA1 is not used as PMOD_INT on Pmod™. PA1 can be used for tamper key or motor control.
MFX_IO14	R134	**ON**	**MFX_IO14 is used as PMOD_RST on Pmod™ and shared with STMod+.**

1. *The default configuration is shown in bold.*

Figure 31 shows the Pmod™ connector (CN3) pinout.

Figure 31. Pmod™ connector (CN3) pinout

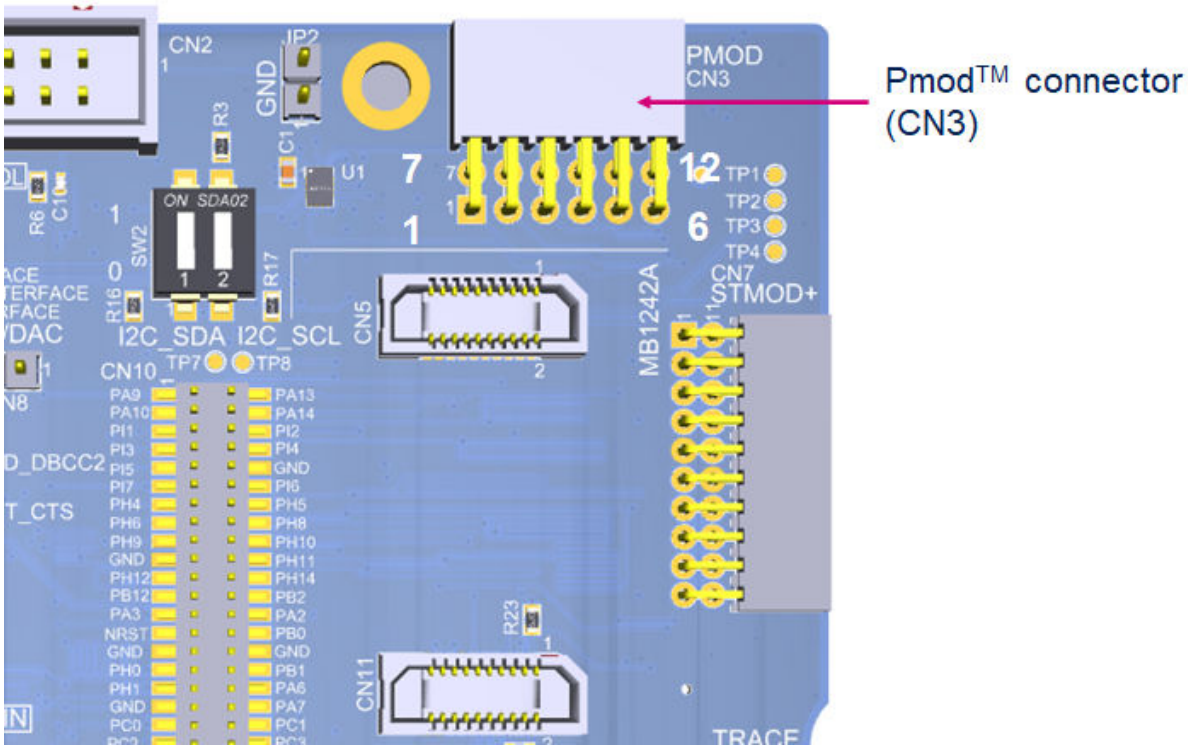


Table 60 describes the Pmod™ connector (CN3) pinout

Table 60. Pmod™ connector (CN3) pinout

Connector pin number	STM32 pin	Board function
1	PA4/PB13	SPI_NSS/LPUART1_CTS
2	PC12/PG7	SPI3_MOSI/UART_TX
3	PG10/PG8	SPI3_MISO/UART_RX
4	PG9/PG6	SPI3_SCK/LPUART1_RTS
5	GND	Power GND
6	VDD	Power VDD
7	PA1	PMOD_INT
8	MFX_IO14	PMOD_RST
9	NC	NC
10	NC	NC
11	GND	Power GND
12	VDD	Power VDD

7.31.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the Pmod™ feature:

- Pmod™ cannot be operated simultaneously with the STMod+ function.
- Pmod™ cannot be operated simultaneously with the UCPD function.
- Pmod™ cannot be operated simultaneously with the ADC/DAC function.
- Pmod™ cannot be operated simultaneously with the motor-control function.
- Pmod™ cannot be operated simultaneously with the TRACE function.
- Pmod™ cannot be operated simultaneously with the SDIO function.
- Pmod™ cannot be operated simultaneously with the tamper-key function.
- Pmod™ cannot be operated simultaneously with the RS-232 function.
- Pmod™ cannot be operated simultaneously with the optional I2C3 function.

7.32 STMod+ connector

7.32.1 Description

The standard 20-pin STMod+ connector (CN7) is available on the STM32U575I-EV Evaluation board to support flexibility in small form factor applications. The STMod+ expansion connector supports the MB1280 fan-out expansion board for Wi-Fi®, Grove, and mikroBUS™ compatible connectors.

For more detailed information about the MB1280 fan-out expansion board, refer to the user manual *STMod+ fan-out expansion board for STM32 Discovery kits and Evaluation boards* (UM2695).

7.32.2 Operating voltage

The STMod+ connector is directly supplied by 5 V. The STM32U575I-EV Evaluation boardI/O level can be set according to the 3.3 V STMod+ connector. The fan-out board also embeds a 3.3 V regulator and I^2C level shifters. For more detailed information, refer to the STMicroelectronics fan-out board user manual and relevant datasheets of associated daughterboards.

7.32.3 STMod+ I/O interface

The STMod+ connector supports several interface configurations:

- SPI interface: NSS, MOSI, MISO, SCK
- UART interface: Tx, Rx, CTS, RTS
- mikroBUS™ interface: NSS, Tx, Rx, SCK
- But also I^2C, one ADC, one PWM, and some more I/Os

To support the selection of SPI or UART function connections on STMod+, a quad-SPDT switch is added to the board. This switch is controlled manually.

Table 61 describes the SW2 configuration to select the STMod+ interface.

Table 61. SW2 configuration for STMod+ interface

Hardware SW2 [2-1][1]	Interface
00	SPI interface selected
01	mikroBUS™ interface selected
10	Not used
11	**UART interface selected**

1. *The default configuration is in bold.*

Table 62 describes the hardware configuration for the STMod+ interface.

Table 62. Hardware I/O configuration for the STMod+ interface

I/O	Hardware	Setting(1)	Configuration
PA4	SB18	**ON**	**PA4 is used as SPI_NSS on STMod+ and shared with Pmod™ and ADC/DAC.**
		OFF	PA4 is not used as SPI_NSS on STMod+. PA4 can be used for motor control or ADC/DAC
PC12	SB94	**ON**	**PC12 is used as SPI3_MOSI on STMod+ and shared with Pmod™ and TRACE and SD-Card.**
		OFF	PC12 is not used as SPI3_MOSI on STMod+. PC12 can be used for SD-Card or TRACE.
PG10	SB102	**ON**	**PG10 is used as SPI3_MISO on STMod+ and shared with Pmod™ and camera.**
		OFF	PG10 is not used as SPI3_MISO on STMod+. PG10 can be used for a camera.
PG9	SB108	**ON**	**PG9 is used as SPI3_SCK on STMod+ and shared with Pmod™.**
		OFF	PG9 is not used as SPI3_SCK on STMod+. PG9 can be used for motor control.
PB13	JP12	ON	PB13 is used as LPUART1_CTS on STMod+ and shared with Pmod™ and RS-232.
		OFF	**PB13 is not used as LPUART1_CTS on STMod+.** **PB13 can be used for touchkey.**
PG7	JP10	[2-3]	PG7 is used as LPUART1_TX on STMod+ and shared with Pmod™ and RS-232.
		[1-2]	**PG7 is not used as LPUART1_TX on STMod+.** **PG7 can be used for I²C for SENSOR or UCPD.**
PG8	JP11	[2-3]	PG8 is used as LPUART1_RX on STMod+ and shared with Pmod™ and RS-232.
		[1-2]	**PG8 is not used as LPUART1_RX on STMod+.** **PG8 can be used for UCPD or I2C3 backup.**
PG6	SB38	**ON**	**PG6 is used as LPUART1_RTS on STMod+ and shared with Pmod™ and RS-232.**
		OFF	PG6 is not used as LPUART1_RX on STMod+. PG6 can be used for UCPD.
PB5	SB36	**ON**	**PB5 is used as SPI3_MOSI2 on STMod+.**
		OFF	PB5 is not used as SPI3_MOSI2 on STMod+. PB5 can be used for USB or COMP.
PB4	SB37	**ON**	**PB4 is used as SPI3_MISO2 on STMod+.**
		OFF	PB4 is not used as SPI3_MISO2 on STMod+. PB4 can be used for ADF1_SDIN0, JTAG, or COMP.
PB11	SB49	**ON**	**PB11 is used as I2C2_SDA to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector.**
PB10	SB46	**ON**	**PB10 is used as I2C2_SCL to interface the audio codec, MFX, UCPD, CTP, the camera, STMod+, and optionally the sensors like the 3D accelerometer and the 3G gyroscope, but also the I²C EEPROM and the external I²C connector.**
PA1	SB71/R135	**ON/ON**	**PA1 is used as PMOD_INT on STMod+ and shared with Pmod™ and TAMPER_KEY**
		OFF/OFF	PA1 is not used as STMOD+_INT on STMod+.

I/O	Hardware	Setting[1]	Configuration
PA1	SB71/R135		PA1 can be used for TAMPER_KEY or motor control.
MFX_IO14	R134	**ON**	**MFX_IO14 is used as STMOD+_RST on STMod+ and shared with Pmod™.**
PA0	SB79	**ON**	**PA0 is used as an ADC on STMod+.**
		OFF	PA0 is not used as an ADC on STMod+. PA0 can be used for OpAmp or motor control.
PA5	SB82	**ON**	**PA5 is used as PWM on STMod+.**
		OFF	PA5 is not used as PWM on STMod+. PA5 can be used for VBUS_SENSE.
PE4	SB105	**ON**	**PE4 is used as MDF1_SDIN3 on STMod+ shared with onboard MEMS.**
		OFF	PE4 is not used as MDF1_SDIN3 on STMod+. PE4 can be used for SRAM-A20.
PF10	SB55	**ON**	**PF10 is used as MDF1_CCK1 on STMod+ shared with onboard MEMS.**
		OFF	PF10 is not used as MDF1_CCK1 on STMod+. PF10 can be used for motor control.
PB6	SB41	**ON**	**PB6 is used as MDF1_SDIN5 on STMod+ shared with onboard MEMS.**
		OFF	PB6 is not used as MDF1_SDIN5 on STMod+. PB6 can be used for motor control.

1. *The default configuration is shown in bold.*

Figure 32 shows the STMod+ connector (CN7) pinout.

Figure 32. STMod+ connector (CN7) pinout

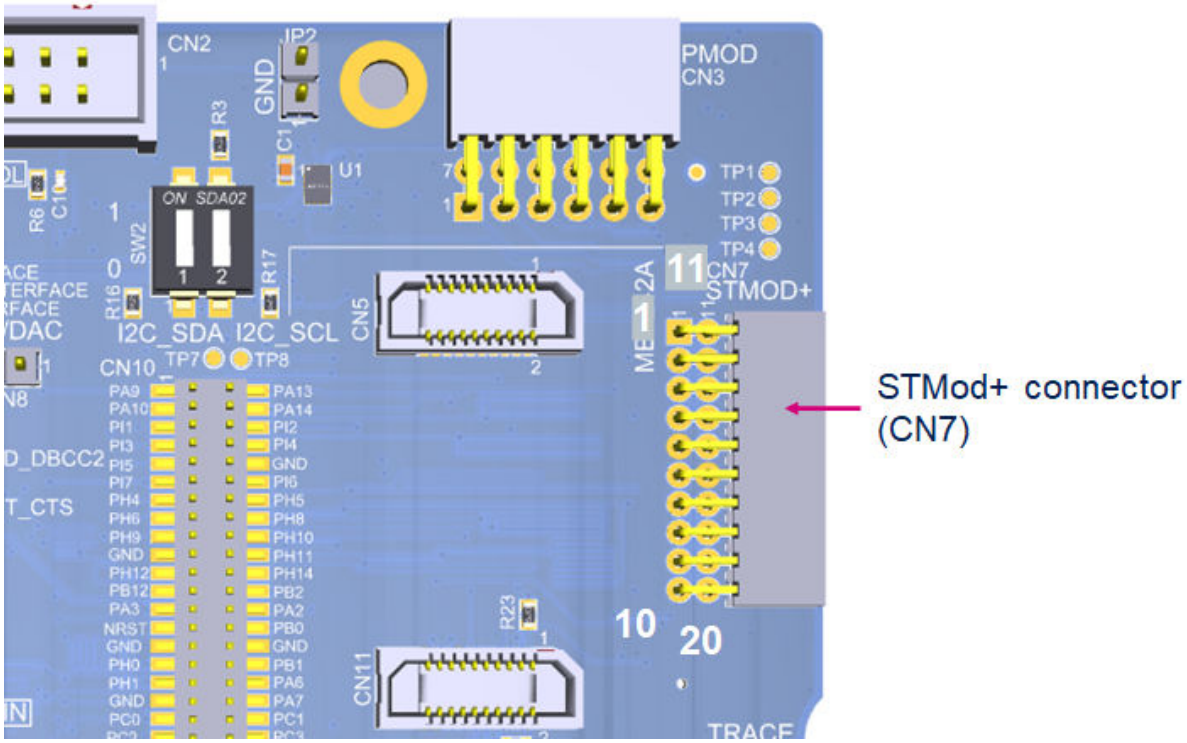


Table 63 describes the STMod+ connector (CN7) pinout.

Table 63. STMod+ connector (CN7) pinout

Connector pin number	STM32 pin	Board function
1	PA4/PB13	SPI_NSS/LPUART1_CTS
2	PC12/PG7	SPI3_MOSI/UART_TX
3	PG10/PG8	SPI3_MISO/UART_RX
4	PG9/PG6	SPI3_SCK/LPUART1_RTS
5	GND	Power GND
6	-	Power 5V
7	PB10	I2C_SCL
8	PB5	SPI3_MOSI2
9	PB4	SPI3_MISO2
10	PB11	I2C_SDA
11	PA1	STMOD+_INT
12	MFX_IO14	STMOD+_RST
13	PA0	STMOD+_ADC
14	PA5	STMOD+_PWM
15	-	5V
16	-	GND
17	PE4	MDF1_SDIN3
18	PF10	MDF1_CCK1
19	PB6	MDF1_SDIN5
20	PF10	MDF1_CCK1

7.32.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the STMod+ feature:

- STMod+ cannot be operated simultaneously with the Pmod™ function.
- STMod+ cannot be operated simultaneously with the UCPD function.
- STMod+ cannot be operated simultaneously with the ADC/DAC function.
- STMod+ cannot be operated simultaneously with the motor-control function.
- STMod+ cannot be operated simultaneously with the TRACE function.
- STMod+ cannot be operated simultaneously with the SDIO function.
- STMod+ cannot be operated simultaneously with the tamper-key function.
- STMod+ cannot be operated simultaneously with the RS-232 function.
- STMod+ cannot be operated simultaneously with the optional I2C3 function.
- STMod+ cannot be operated simultaneously with the OpAmp function.

7.33 Motor control

7.33.1 Description

The CN2 connector is designed to receive a motor-control (MC) daughterboard.

7.33.2 Motor-control I/O interface

The motor-control I/O interface is not connected by default, because it is too high I/O consuming.

Table 64 describes the assignment of the motor-control interface and the I/O function associated with STM32U575AII6Q.

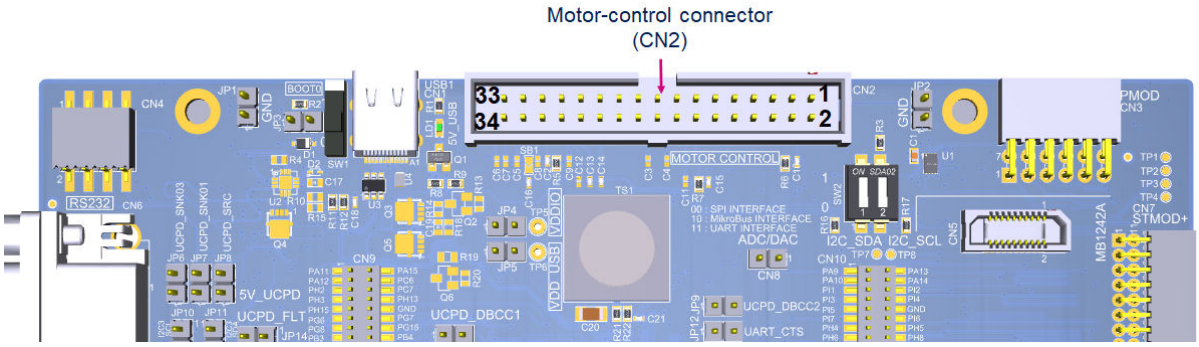
Table 64. Motor-control terminal and I/O function assignment

Motor-control connector (CN2)		STM32U575AII6Q microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modification for enabling motor control
1	Emergency stop	PB6	TIM8_BKIN2	-	Close SB43 Remove SB41 (MDF1_SDIN5)
2	GND	-	GND	-	-
3	PWM_1H	PC6	TIM8_CH1	-	Close SB29 TKEY always connected with serial resistor R21 (10K)
4	GND	-	GND	-	-
5	PWM_1L	PA7	TIM8_CH1N	-	Close SB61 Remove R159 (Octo-SPI)
6	GND	-	GND	-	-
7	PWM_2H	PC7	TIM8_CH2	-	Close SB30 TKEY_CS always connected with capacitor to GND
8	GND	-	GND	-	-
9	PWM_2L	PB0	TIM8_CH2N	-	Close SB50 Remove R152 (Octo-SPI)
10	GND	-	GND	-	-
11	PWM_3H	PC8	TIM8_CH3	-	Close SB80 Open SB84 (SDIO)
12	GND	-	GND	-	-
13	PWM_3L	PB1	TIM8_CH3N	-	Close SB54 Remove R155 (Octo-SPI)
14	Bus voltage	PA4	ADC1_IN9	-	Close SB17 Open SB18 STMod+ or no daughterboard Open SB16 or no ADC/DAC on CN8
15	PhaseA current+	PC0	ADC1_IN1	-	Close SB63 Remove R160 (Octo-SPI)
16	PhaseA current-	-	GND	-	-
17	PhaseB current+	PC1	ADC1_IN2	-	Close SB66 Remove R163 (Octo-SPI)
18	PhaseB current-	-	GND	-	-
19	PhaseC current+	PC2	ADC1_IN3	-	Close SB73 Remove R162 (Octo-SPI)

Motor-control connector (CN2)		STM32U575AII6Q microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modification for enabling motor control
20	PhaseC current-	-	GND	-	-
21	ICL shut out	PG9	GPIO	-	Close SB107 Open SB108 STMod+ or no daughterboard
22	GND	-	GND	-	-
23	Dissipative Brake	PB2	GPIO	-	Close SB45 Remove R148 (Octo-SPI)
24	PFC ind. curr.	PC3	ADC1_IN4	-	Close SB69 Remove R164 (Octo-SPI)
25	5V	-	5 V	-	-
26	MC Temp.	PA3	ADC1_IN8	-	Close SB51 Removed R150 (Octo-SPI) Open SB53 OpAmp
27	PFC sync	PF9	TIM15_CH1	TIM15_CH1	Close SB59 Open SB62 audio SAI
28	3V3	-	3.3 V	-	-
29	PFC PWM	PF10	TIM15_CH2	-	Close SB58 Open SB55 MDF1_CCK1
30	PFC shut down	PB12	TIM15_BKIN	-	Close SB44 Open SB42 smartcard Open SB47 (Octo-SPI)
31	Encoder A	PA0	TIM2_CH1	ADC12_IN5	Close SB65 Open SB68 OpAmp Open SB79 STMod+ Open SB72 UCPD
32	PFC Vac	PA6	ADC1_IN11	-	Close SB57 Remove R158 (Octo-SPI)
33	Encoder B	PA1	TIM2_CH2	ADC12_IN6	Close SB67 Open SB78 TAMPER KEY Open SB71 STMod+
34	Encoder index	PA2	TIM2_CH3	ADC12_IN7	Close SB48 Removed R151 (Octo-SPI)

Figure 33 shows the motor-control connector (CN2) pinout.

Figure 33. Motor-control connector (CN2) pinout



7.33.3 I/O restriction to other features

Caution: Due to the sharing of some I/Oss of STM32U575AII6Q by multiple peripherals, the following limitations apply in using the motor-control feature:

- The motor control cannot be operated simultaneously with the touchkey button function.
- The motor control cannot be operated simultaneously with the Octo-SPI function.
- The motor control cannot be operated simultaneously with the STMod+ function.
- The motor control cannot be operated simultaneously with the SDIO function.
- The motor control cannot be operated simultaneously with the ADC/DAC function.
- The motor control cannot be operated simultaneously with the OpAmp function.
- The motor control cannot be operated simultaneously with the audio function.
- The motor control cannot be operated simultaneously with the smartcard function.
- The motor control cannot be operated simultaneously with the tamper key function.

7.34 Extension connectors (CN9, CN10, CN14, and CN15)

7.34.1 Description

The headers (CN9, CN10, CN14, and CN15) complement each other to give access to all GPIOs of the STM32U575AII6Q microcontroller. In addition to GPIOs, the following signals and power supply lines are also routed on these connectors:

- GND
- 5V
- 3V3
- 5V_DC
- VDD
- RESETn
- Clock terminals PC14-OSC32_IN, PC15-OSC32_OUT, PH0-OSC_IN, and PH1-OSC_OUT

CN9 and CN10 are two-row headers of 25 pins, with a 1.27 mm pitch.

CN14 and CN15 are two-row headers of 17 pins, with a 1.27 mm pitch, mainly used for FMC interface access.

Figure 34 shows the connector (CN9 and CN10) pinout.

Figure 34. Connector (CN9 and CN10) pinout

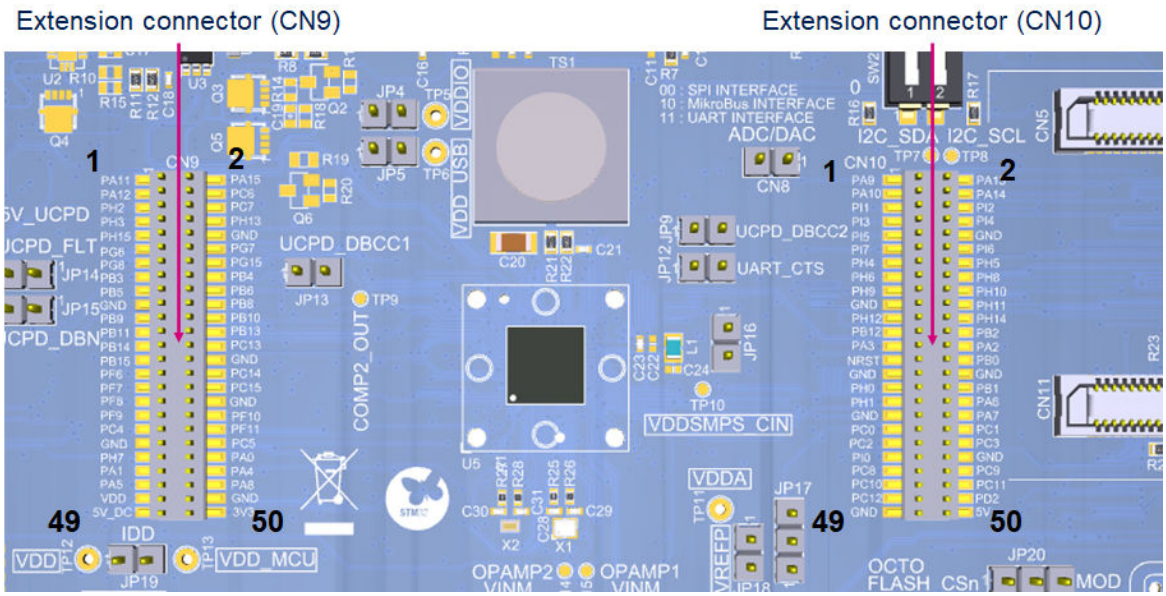


Table 65 describes the connector (CN9) pinout.

Table 65. Connector (CN9) pinout

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
1	PA11	USB_FS_N	-
2	PA15	UCPD_CC1, JTDI	-
3	PA12	USB_FS_P	-
4	PC6	TKEY	MC
5	PH2	UCPD_SOURCE_EN	-
6	PC7	TKEY_CS	MC
7	PH3	BOOT0	-
8	PH13	UCPD_DISCHARGE	-
9	PH15	GYRO_ACC_INT	-
10	GND	POWER GND	-
11	PG6	UART_RTS	UCPD_FRSCC1
12	PG7	I2C3_SCL (LPBAM)	UART_TX, UCPD_FRSCC2
13	PG8	I2C3_SDA (LPBAM)	UART_RX, UCPD_PWR
14	PG15	LCD_CTP_INT	-
15	PB3	ADF1_CCK0, JTDO_SWO	-
16	PB4	ADF1_SDIN0, JTRSTN, COMP2_INP, SPI3_MISO2	-
17	PB5	COMP2_OUT, SPI3_MOSI2	USB_DBCC1
18	PB6	MDF1_SDIN5	MC
19	GND	POWER GND	-

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
20	PB8	UCPD_FLT, MDF1_CCK0	FDCAN_RX
21	PB9	UCPD_DBn	FDCAN_TX
22	PB10	I2C2_SCL	-
23	PB11	I2C2_SDA	-
24	PB13	SHIELD	UART_CTS
25	PB14	SHIELD_CS	USB_DBCC2
26	PC13	USER BUTTON	ACTIVE TAMPER
27	PB15	UCPD_CC2	-
28	GND	POWER GND	-
29	PF6	SAI1_SD_B	-
30	PC14	OSC32-IN	-
31	PF7	SAI1_MCLK_B	-
32	PC15	OSC32_OUT	-
33	PF8	SAI1_SCK_B	-
34	GND	POWER GND	-
35	PF9	SAI1_FS_B	MC
36	PF10	MDF1_CCK1	MC
37	PC4	SMARTCARD_IO	LCD_TE
38	PF11	MFX_WAKEUP	-
39	GND	POWER GND	-
40	PC5	MFX_IRQ_OUT	-
41	PH7	LED_RED	-
42	PA0	OPAMP1_INP, STMOD+_ADC, IBUS-SENSE	MC
43	PA1	STMOD+_INT, TAMPER_KEY	MC
44	PA4	SPI_NSS, ADC_DAC	MC
45	PA5	VBUS_SENSE, STMOD+_PWM	-
46	PA8	LCD_BL_CTRL	-
47	VDD	POWER	-
48	GND	POWER GND	-
49	5V_DC	POWER 5 V	-
50	3V3	POWER 3.3 V	-

1. *Exclusive when several are connected by default.*
2. *Meaning this requires a board update to activate it.*

Table 66 describes the connector (CN10) pinout.

Table 66. Connector (CN10) pinout

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
1	PA9	UART T_VCP_TX	-
2	PA13	SWDIO, JTMS	-
3	PA10	UART T_VCP_RX	-

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
4	PA14	SWCLK, JTCK	-
5	PI1	OCTOSPI2_IO2	-
6	PI2	OCTOSPI2_IO1, CAMERA_RSTI	-
7	PI3	OCTOSPI2_IO0, CAMERA_XSDN	-
8	PI4	DCMI_D5	-
9	PI5	OCTOSPI2_NCS, DCMI_VSYNC	-
10	GND	POWER GND	-
11	PI7	DCMI_D7	-
12	PI6	DCMI_D6	-
13	PH4	OCTOSPI2_DQS	-
14	PH5	DCMI_PIXCLK	-
15	PH6	OCTOSPI2_CLK	-
16	PH8	OCTOSPI2_IO3, DCMI_HSYNC	-
17	PH9	OCTOSPI2_IO4, DCMI_D0	-
18	PH10	OCTOSPI2_IO5, DCMI_D1	-
19	GND	POWER GND	-
20	PH11	OCTOSPI2_IO6, DCMI_D2	-
21	PH12	OCTOSPI2_IO7, DCMI_D3	-
22	PH14	DCMI_D4	-
23	PB12	SMARTCARD_CLK	OCTOSPI1_CLK_N, MC
24	PB2	OCTOSPI1_DQS	MC
25	PA3	OCTOSPI1_CLK_P	OPAMP1_VOUT, MC
26	PA2	OCTOSPI1_NCS	MC
27	NRST	RESET	-
28	PB0	OCTOSPI1_IO1	MC
29	GND	POWER GND	-
30	GND	POWER GND	-
31	PH0	OSC-IN	-
32	PB1	OCTOSPI1_IO0	MC
33	PH1	OSC_OUT	-
34	PA6	OCTOSPI1_IO3	MC
35	GND	POWER GND	-
36	PA7	OCTOSPI1_IO2	MC
37	PC0	OCTOSPI1_IO7	MC
38	PC1	OCTOSPI1_IO4	MC
39	PC2	OCTOSPI1_IO5	MC
40	PC3	OCTOSPI1_IO6	MC
41	PI0	SDCARD_DETECT	-
42	GND	POWER GND	-
43	PC8	SDIO_D0	MC
44	PC9	SDIO_D1, TRACE_D0	-

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
45	PC10	SDIO_D2, TRACE_D1	-
46	PC11	SDIO1_D3	-
47	PC12	SDIO1_CLK, SPI3_MOSI, TRACE_D3	-
48	PD2	SDIO1_CMD	-
49	GND	POWER GND	-
50	5V	POWER 5 V	-

1. *Exclusive when several are connected by default.*
2. *Meaning this requires a board update to activate it.*

Figure 35 shows the connector (CN14 and CN15) pinout.

Figure 35. Connector (CN14 and CN15) pinout

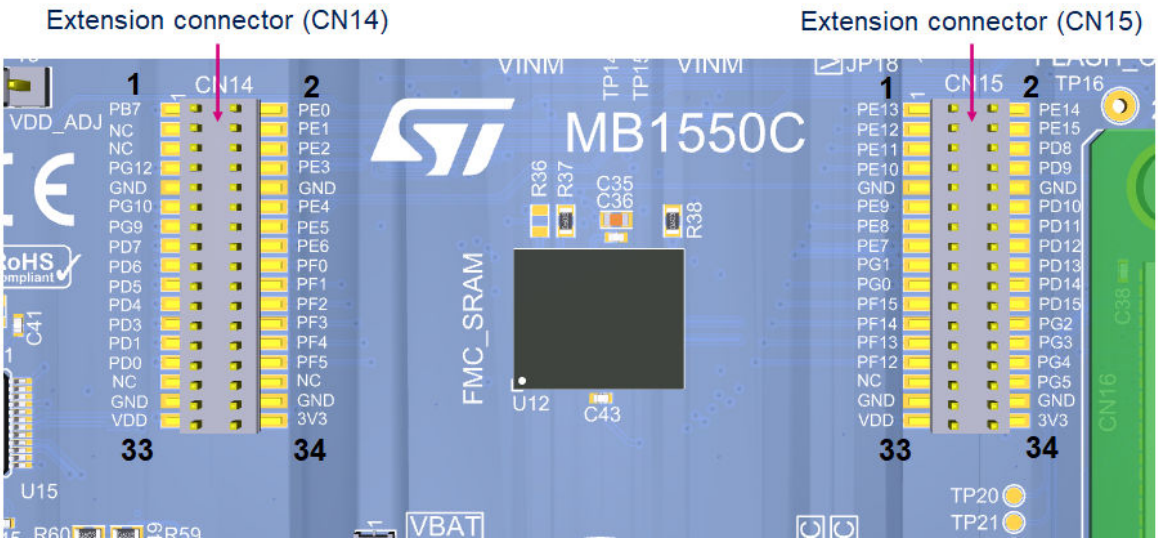


Table 67 describes the connector (CN14) pinout.

Table 67. Connector (CN14) pinout

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
1	PB7	LED_GREEN	-
2	PE0	FMC_NBL0	-
3	NC	NC	-
4	PE1	FMC_NBL1	-
5	NC	NC	-
6	PE2	TRACE_CLK	-
7	PG12	FMC_NE4_LCD_CSN	-
8	PE3	FMC_A19	-
9	GND	POWER GND	-
10	GND	POWER GND	-
11	PG10	CAMERA_PLUG, SPI3_MISO	-

Connector pin number	STM32 pin	Default board function(1)	Optional board function(2)
12	PE4	MDF1_SDIN3	FMC_A20
13	PG9	SPI3_SCK	MC
14	PE5	TRACE_D2	-
15	PD7	FMC_NE1	-
16	PE6	FMC_A22_LCD_RS	-
17	PD6	SAI1_SD_A	-
18	PF0	FMC_A0	-
19	PD5	FMC_NWE	-
20	PF1	FMC_A1	-
21	PD4	FMC_NOE	-
22	PF2	FMC_A2	-
23	PD3	MDF1_SDIN0	-
24	PF3	FMC_A3	-
25	PD1	FMC_D3	-
26	PF4	FMC_A4	-
27	PD0	FMC_D2	-
28	PF5	FMC_A5	-
29	NC	NC	-
30	NC	NC	-
31	GND	POWER GND	-
32	GND	POWER GND	-
33	VDD	POWER VDD	-
34	3V3	POWER 3.3 V	-

1. *Exclusive when several are connected by default.*
2. *Meaning this requires a board update to activate it.*

Table 68 describes the connector (CN15) pinout.

Table 68. Connector (CN15) pinout

Connector pin number	STM32 pin	Board function
1	PE13	FMC_D10
2	PE14	FMC_D11
3	PE12	FMC_D9
4	PE15	FMC_D12
5	PE11	FMC_D8
6	PD8	FMC_D13
7	PE10	FMC_D7
8	PD9	FMC_D14
9	GND	POWER GND
10	GND	POWER GND
11	PE9	FMC_D6

Connector pin number	STM32 pin	Board function
12	PD10	FMC_D15
13	PE8	FMC_D5
14	PD11	FMC_A16
15	PE7	FMC_D4
16	PD12	FMC_A17
17	PG1	FMC_A11
18	PD13	FMC_A18
19	PG0	FMC_A10
20	PD14	FMC_D0
21	PF15	FMC_A9
22	PD15	FMC_D1
23	PF14	FMC_A8
24	PG2	FMC_A12
25	PF13	FMC_A7
26	PG3	FMC_A13
27	PF12	FMC_A6
28	PG4	FMC_A14
29	NC	NC
30	PG5	FMC_A15
31	GND	POWER GND
32	GND	POWER GND
33	VDD	POWER VDD
34	3V3	POWER 3V3

8 STM32U575I-EV product information

8.1 Product marking

The stickers located on the top or bottom side of all PCBs provide product information:

- First sticker: product order code and product identification, generally placed on the main board featuring the target device.
  Example:

  Product order code
  Product identification

- Second sticker: board reference with revision and serial number, available on each PCB.
  Example:

  MBxxxx-Variant-yzz
  syywwxxxxx

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: *"MBxxxx-Variant-yzz"*, where *"MBxxxx"* is the board reference, *"Variant"* (optional) identifies the mounting variant when several exist, *"y"* is the PCB revision, and *"zz"* is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Parts marked as *"ES"* or *"E"* are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

"ES" or *"E"* marking examples of location:

- On the targeted STM32 that is soldered on the board (for an illustration of STM32 marking, refer to the STM32 datasheet *Package information* paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck, or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a *"U"* marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers might need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

8.2 STM32U575I-EV product history

Table 69. Product history

Order code	Product identification	Product details	Product change description	Product limitations
STM32U575I-EV	VA32U575I$AT1	MCU: • STM32U575AII6Q silicon revision "X"	Initial revision	No limitation
		MCU errata sheet: • *STM32U575xx and STM32U585xx device errata* (ES0499)		
		Board: • MB1550-U575AIQ-C02 (main board) • MB989-P-C01 (LCD daughterboard) • MB1242-APS6408L-B01 (Octo-SPI memory daughterboard) • MB1379-2V8-A05 (camera daughterboard)		
	VA32U575I$AT2	MCU: • STM32U575AII6Q silicon revision "X"	Packaging: plastic blister replaced by a carton box	No limitation
		MCU errata sheet: • *STM32U575xx and STM32U585xx device errata* (ES0499)		
		Board: • MB1550-U575AIQ-C02 (main board) • MB989-P-C01 (LCD daughterboard) • MB1242-APS6408L-B01 (Octo-SPI memory daughterboard) • MB1379-2V8-A05 (camera daughterboard)		
	VA32U575I$AT3	MCU: • STM32U575AII6Q silicon revision "W"	• MCU silicon revision changed • Main board revision changed • LCD daughterboard revision changed	No limitation
		MCU errata sheet: • *STM32U575xx and STM32U585xx device errata* (ES0499)		
		Board: • MB1550-U575AIQ-C03 (main board) • MB989-P-C02 (LCD daughterboard) • MB1242-APS6408L-B01 (Octo-SPI memory daughterboard) • MB1379-2V8-A05 (camera daughterboard)		

8.3 Board revision history

Table 70. **Board revision history**

Board reference	Board variant and revision	Board change description	Board limitations
MB1550 (main board)	U575AIQ-C02	Initial revision	No limitation
	U575AIQ-C03	• C30 and C31 capacitors updated from 1.8 to 6.8 pF • Several part references updated due to obsolescence, such as LEDs. Refer to the bill of materials for details.	No limitation
MB989 (LCD daughterboard)	P-C01	Initial revision	No limitation
	P-C02	Several part references updated due to obsolescence, such as capacitors. Refer to the bill of materials for details.	No limitation
MB1242 (Octo-SPI memory daughterboard)	APS6408L-B01	Initial revision	No limitation
MB1379 (camera daughterboard)	2V8-A02	Initial revision	The I/O selected for camera detection is shared with an I/O for STMod+ on MB1550. The use of a direct 0-ohm resistor for pull-down (on pin 16) is not recommended as in case of an I/O setting issue, the board is in short circuit, and this can crash the I/O port.
	2V8-A04	The R7 resistor is updated from 0 to 1 kΩ.	When a main board is used via B-CAMS-OMV, the reset signal is pulled by an MB1379 R3 10-kΩ resistor.
	2V8-A05	The R3 resistor is removed and the R4 resistor is updated to 100 Ω.	No limitation

9 Federal Communications Commission (FCC) and ISED Canada Compliance Statements

9.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Responsible party (in the USA)

Francesco Doddo
STMicroelectronics, Inc.
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USA
Telephone: +1 781-472-9634

9.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada: CAN ICES-3 (A) / NMB-3 (A).

10 CE conformity

10.1 Warning

EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

Revision history

Table 71. **Document revision history**

Date	Revision	Changes
22-Sep-2021	1	Initial release.
24-May-2024	2	Updated STM32U575I-EV product information with added Product history and Board revision history tables.

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