UM2697

User manual

SPC58NH-DISP discovery board

Introduction

The SPC58NH-DISP discovery board is a standalone hardware platform to evaluate and develop applications with the SPC58NH92C5, packaged in a FPBGA386 microcontroller at budget price.

This document provides information about the hardware architecture and how to configure the jumpers to enable specific functions.

1 SPC58NH-DISP discovery board

The SPC58NH-DISP discovery board is based on the microcontroller SPC58NH92C5, a high performance e200z4d triple core 32-bit Power Architecture technology CPU, 200 MHz core frequency with 10496 KB on chip Flash (10240 KB code Flash + 256 KB data Flash) in an FPBGA386 package.

The several peripherals such as DSPI, LIN (LIN and UART), FlexRay, CAN-FD, two independent ethernet ports (10/100 Mbps and 1 Gbps), make the SPC58NH-DISP an excellent starter kit for the SW designer to quickly evaluate the microcontroller as well as to develop and to debug applications.

Free ready-to-run application firmware examples are available inside SPC5Studio web page (http//:www.st.com/spc5studio) to quickly support evaluation and development.

The PCB, the components and all HW parts assembled in this board meet the requirements of the applicable RoHS directives.

1.1 Interfaces and connectors

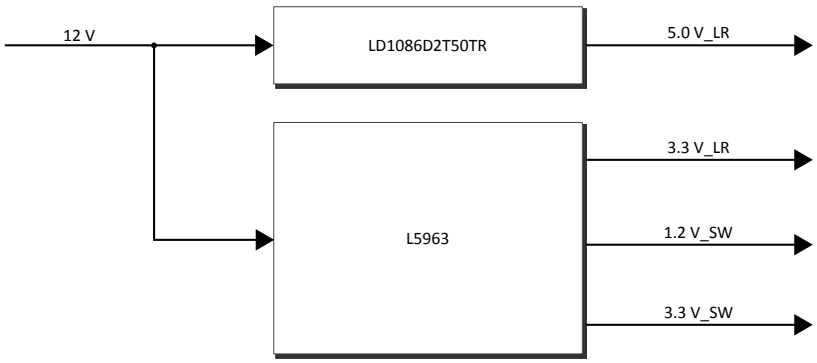
- 1 ethernet port 10/100 Mbps
- 1 ethernet port 1 Gbps
- eMMC
- SD card reader
- HyperFlash and HyperRam
- 3 CAN FD ports with transceiver DB9 connector
- 12 CAN port (GPIO level, 2 connectors)
- 4 x I²C connector
- 1 LIN and 1 K-Line with transceivers
- 2 FlexRay channels (a single transceiver is shared with jumpers)
- 2 UART channels with a DB9 and connector 4x0.1”
- USB to UART (with opto-coupler option)
- 1xST33xx connector
- JTAG (header 2x7 0.1” pin)
- RESET push button
- 3 user push buttons
- 4 user LEDs
- 2 trimmers to ADC (fast ADG evaluation)
- LCD TFT display (320 x 240) with touch screen (option)
- 12 V DC power supply (external PSU)
- 40 MHz and 32.768 KHz crystals

2 Hardware description

2.1 Power supply

Figure 1 shows the PSU block diagram.

Figure 1. PSU block diagram



The DC input source is 12 V DC: L5963 is used to generate 3.3 V (VDD_HV_xxx), 1.2 V (VDD_LV_xx) and 3.3 V for ADC section. A linear regulator is used to generate 5 V for ADC.

The LEDs LD2, LD3, LD4, and LD5 are used to check the output of each voltage regulator and 12 V input source.

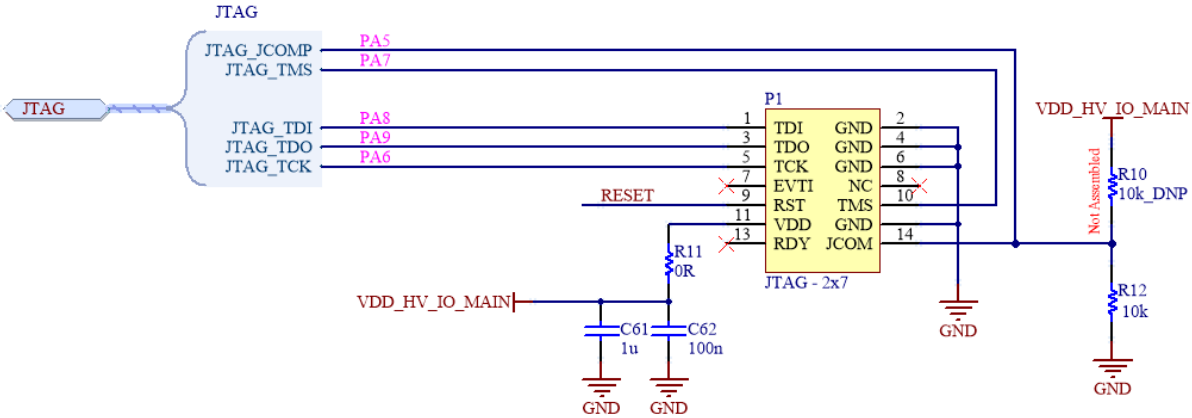
A resettable fuse (F1) protects the application against the overload or short-circuit.

2.2 Microcontroller

2.2.1 JTAG

A standard JTAG connector 14x0.1” is available for programming and debugging.

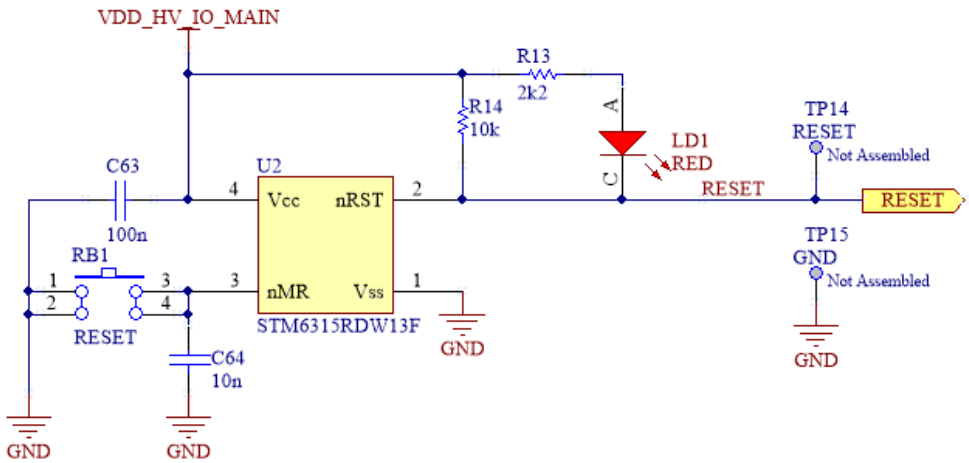
Figure 2. JTAG



2.2.2 Reset

Figure 3 shows the reset circuit.

Figure 3. Reset



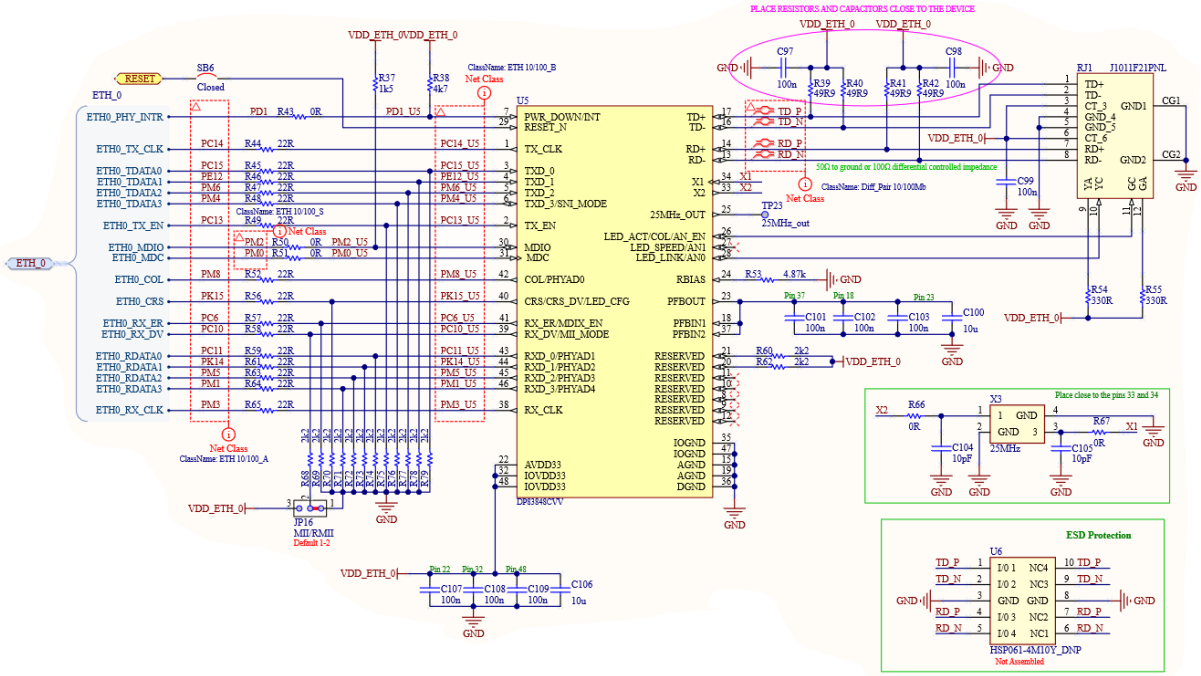
The reset signal level is driven to low level when:

- VDD_HV is lower than a fixed level. This feature is used to monitor the VDD_HV level and then to reset the microcontroller when the level is out of specification. This feature allows to set the reset only when the VDD_HV is stable.
- the pushbutton is pressed (manual reset); the reset pulse width is fixed.

2.3 Ethernet 10/100 Mbps

Section 2.3 shows the ethernet 10-100 Mbps communication channel.

Figure 4. Ethernet 10/100 Mbps



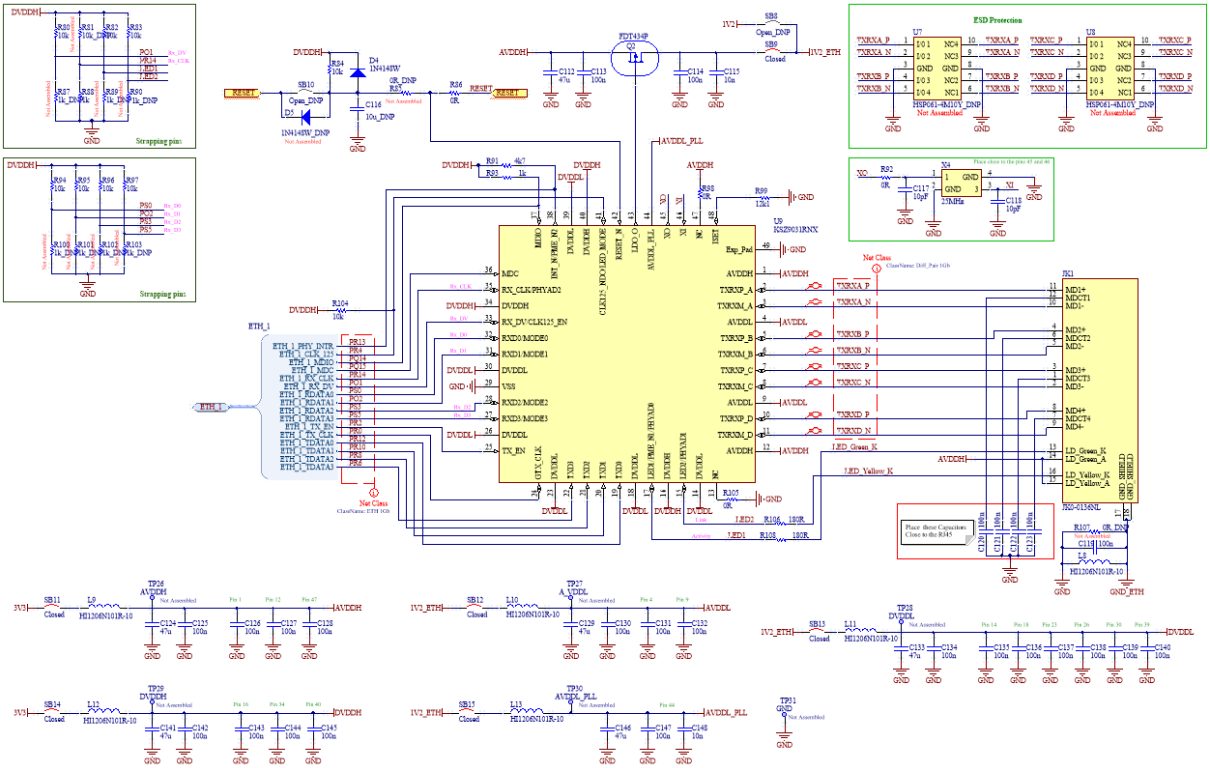
JP15 allows configuring the communication in MII or RMII mode.

The current absorption of this section can be estimated by removing SB7 then applying a low impedance current meter or a current probe.

2.4 Ethernet 1 Gbps

The ethernet 1 Gbps section is depicted here below.

Figure 5. Ethernet 1 Gbps



The resistors from R85 to R84, from R88 to R91, from R95 to R98 and from R100 to R103 are used to configure the device.

With SB9 close and SB8 left open, the 1V2_ETH supply voltage is controlled by an integrated LDO and an external MOSFET. The user can exclude the LDO regulator and connect the 1V2_ETH to the 1.2 V source form the PSU section setting SB9 open and SB8 close.

2.5 eMMC and µSD

Figure 6 and Figure 7 are showing the eMMC and µSD card reader section respectively.

From the microcontroller, the signals Data 0÷3, CMD, CLK and FBCLK are shared among these sections and this means only one section can be active at a time.

These signals must be connected to the active section by selecting the jumpers from JP17 to JP22 properly: see Figure 8.

Figure 6. eMMC card

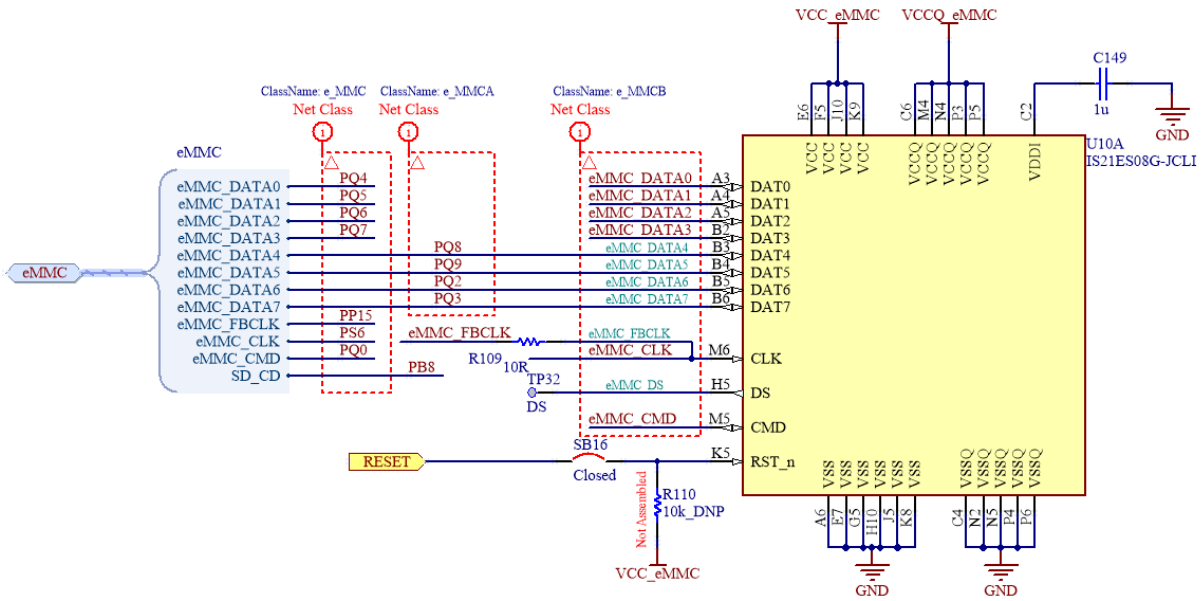


Figure 7. µSD card

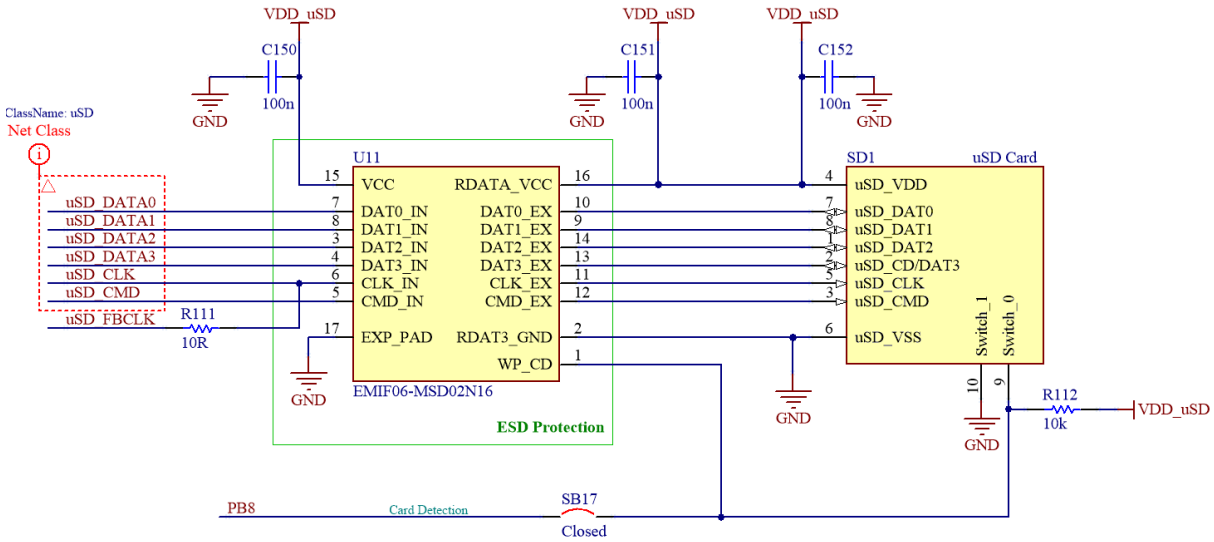
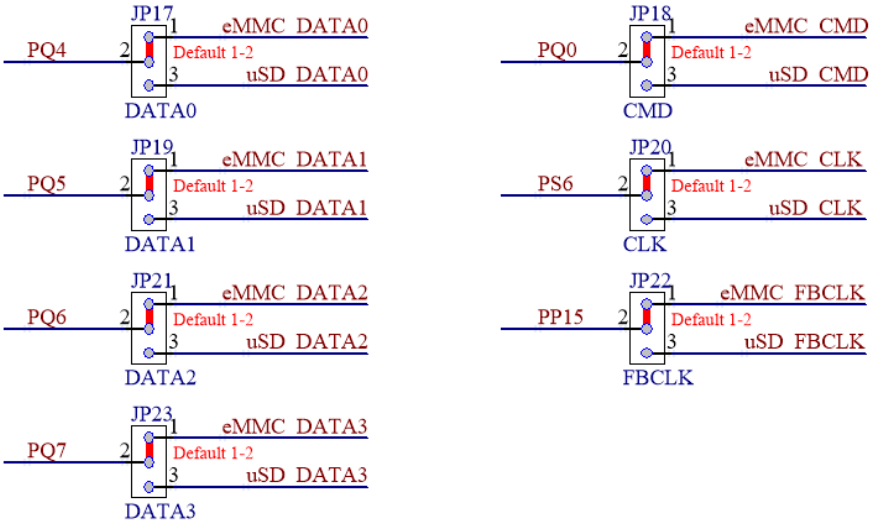


Figure 8. **eMMC and µSD jumpers configuration**

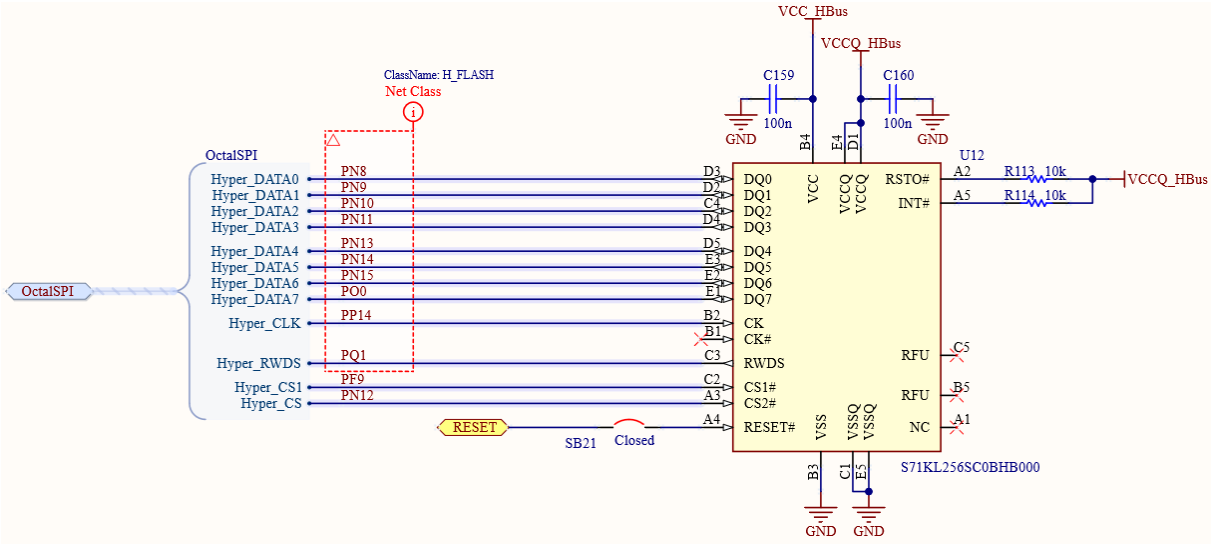


2.6 Octal SPI

The OctalSPI section is visible in Section 2.6 . In this application the OctalSPI is connected to a HyperFlash and HyperRAM device.

The microcontroller ports PF[4] and PN[12] are used to drive CS1# and CS2#.

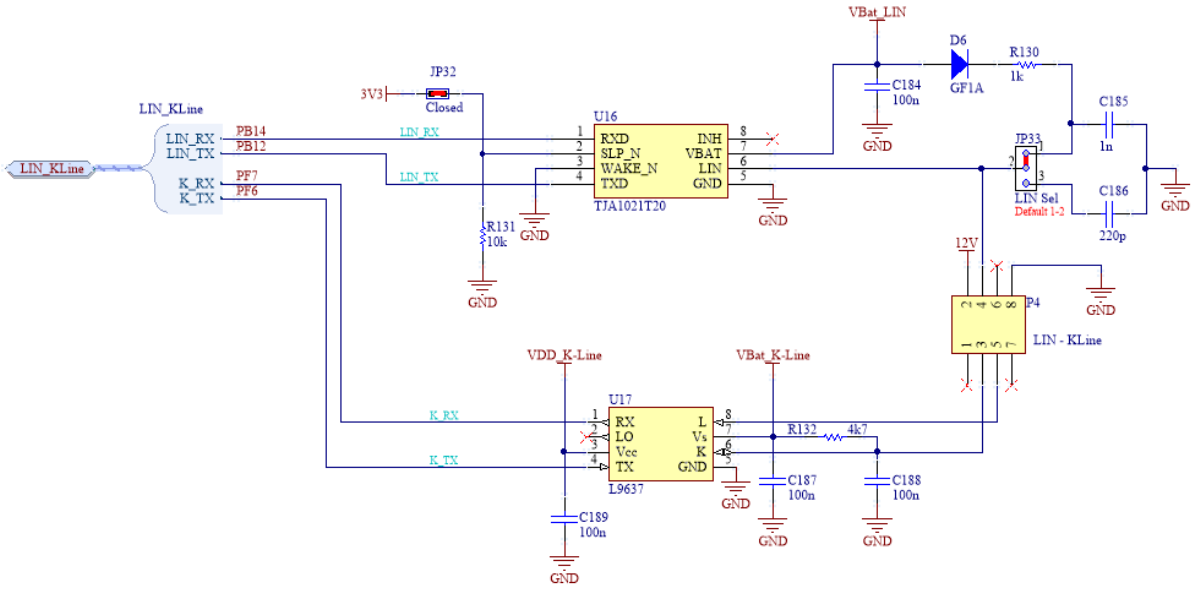
Figure 9. **HyperFlash and HyperRAM**



2.7 LIN and K-Line

LIN and K-Line channels with the dedicated transceivers are described in the Figure 10.

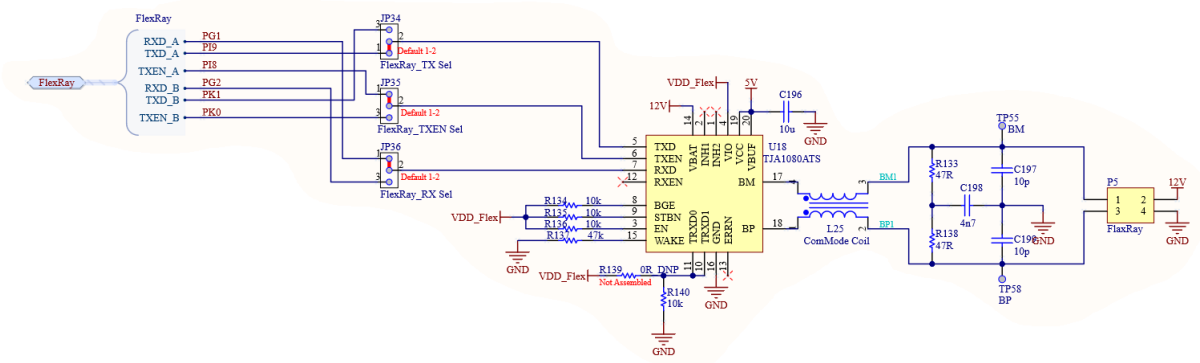
Figure 10. LIN and K-Line



2.8 Flex Ray

Flex Ray section is reported in Section 2.8 ; JP33, JP34 and JP35 allow selecting which channel from the microcontroller is connected to the transceiver.

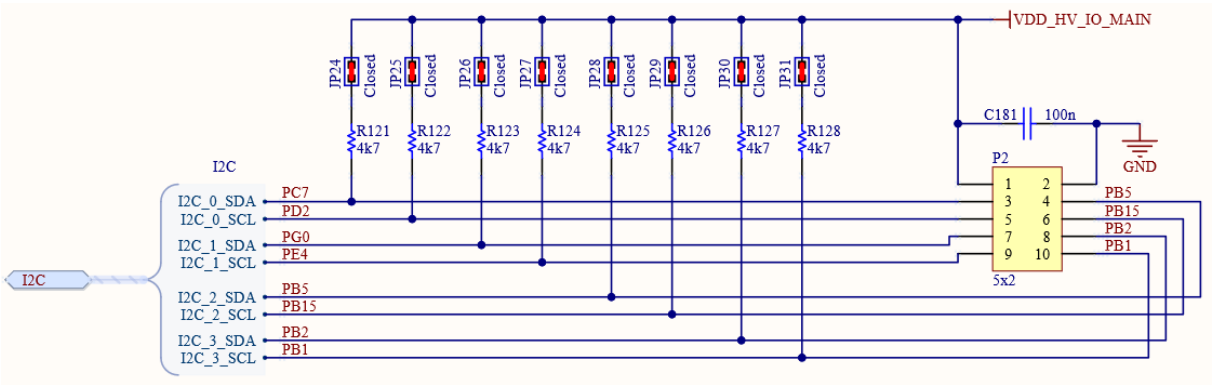
Figure 11. Flex Ray



2.9 I²C

Four I²C channels are available. A pull-up resistor is connected to each line and a jumper allows disconnecting it.

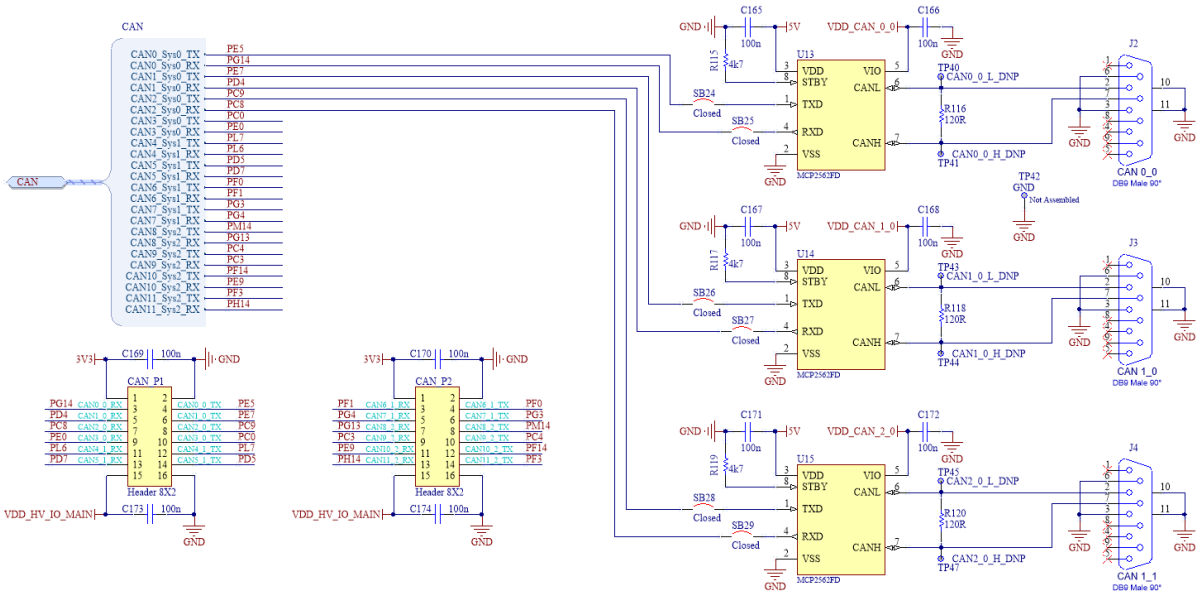
Figure 12. I²C



2.10 CAN-FD

Three CAN-FD channels with fast transceivers are connected to DB9 connectors. Further 6 + 6 channels are connected to 2 connectors without transceivers (GPIO level).

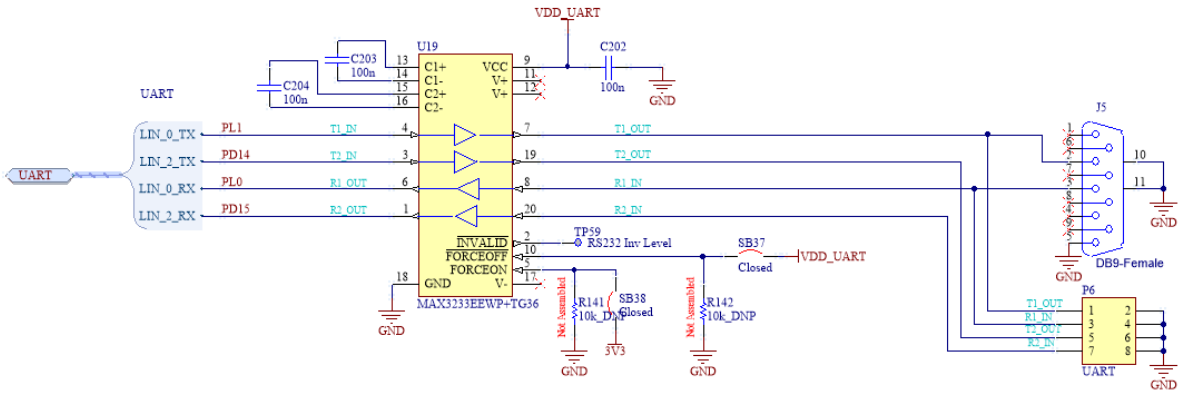
Figure 13. CAN-FD



2.11 UART

Two UART channels with transceiver are available and connected to a 2x4 connector. The channel T1 (ports PL[0] and PL[1]) is connected to J5 (DB9 connector).

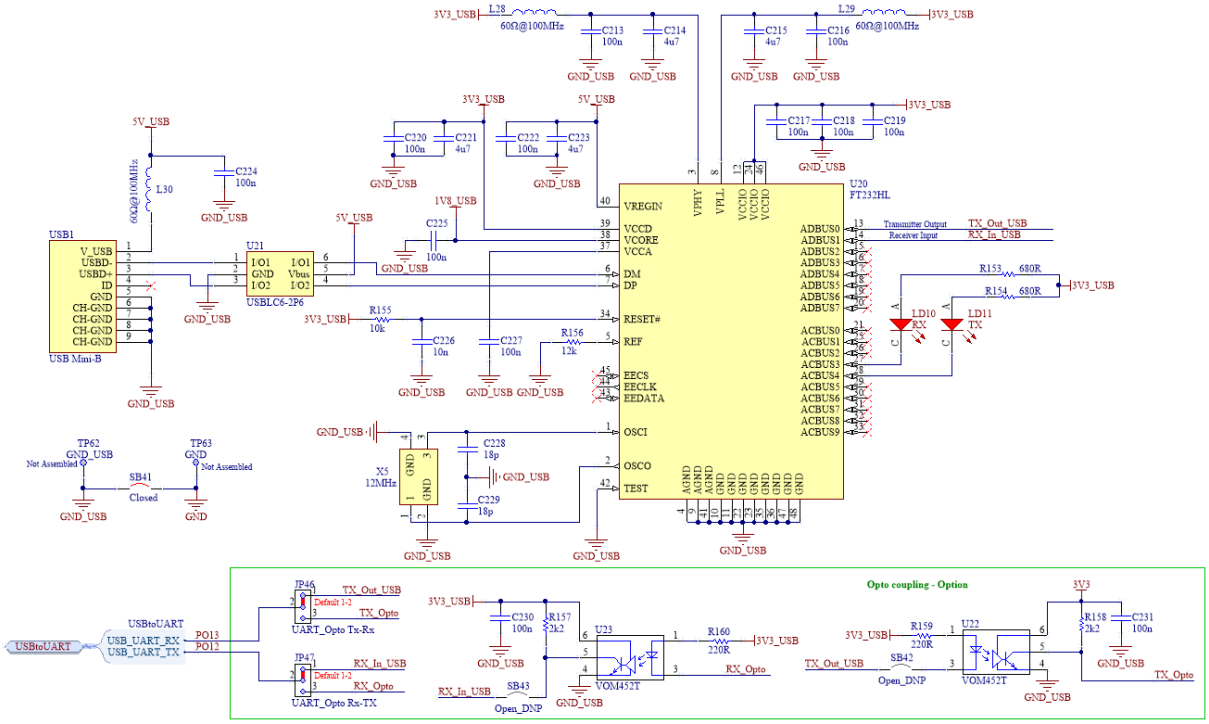
Figure 14. UART



2.12 USB to UART

This section shows a USB to UART communication channel. An option allows to include opto-couplers in order to have the USB port electrically insulated with respect to all the sections.

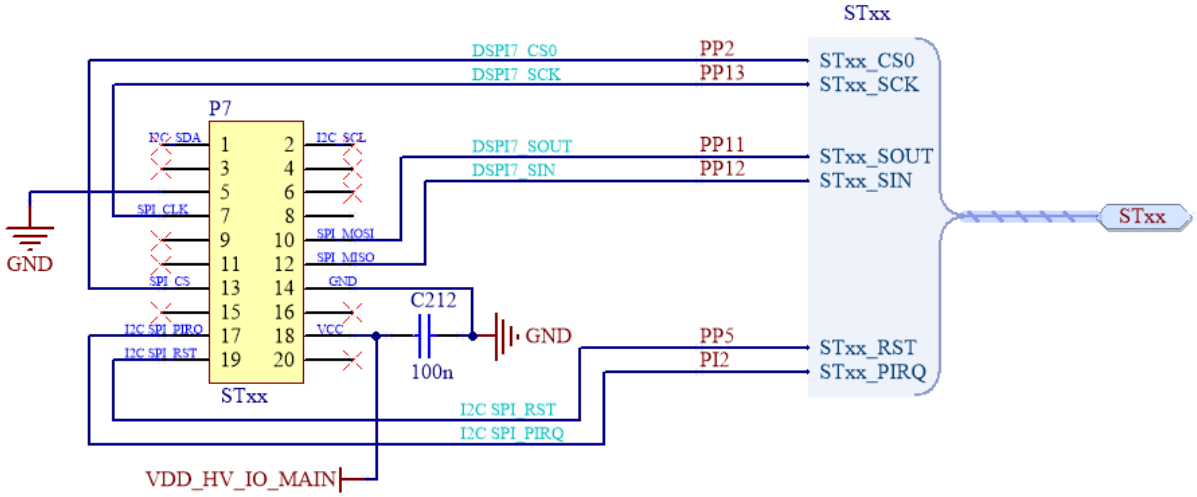
Figure 15. USB to UART



2.13 ST33 connector

The aim of this connector is to allow plugging an evaluation board to evaluate and to demonstrate security features.

Figure 16. ST33 connector

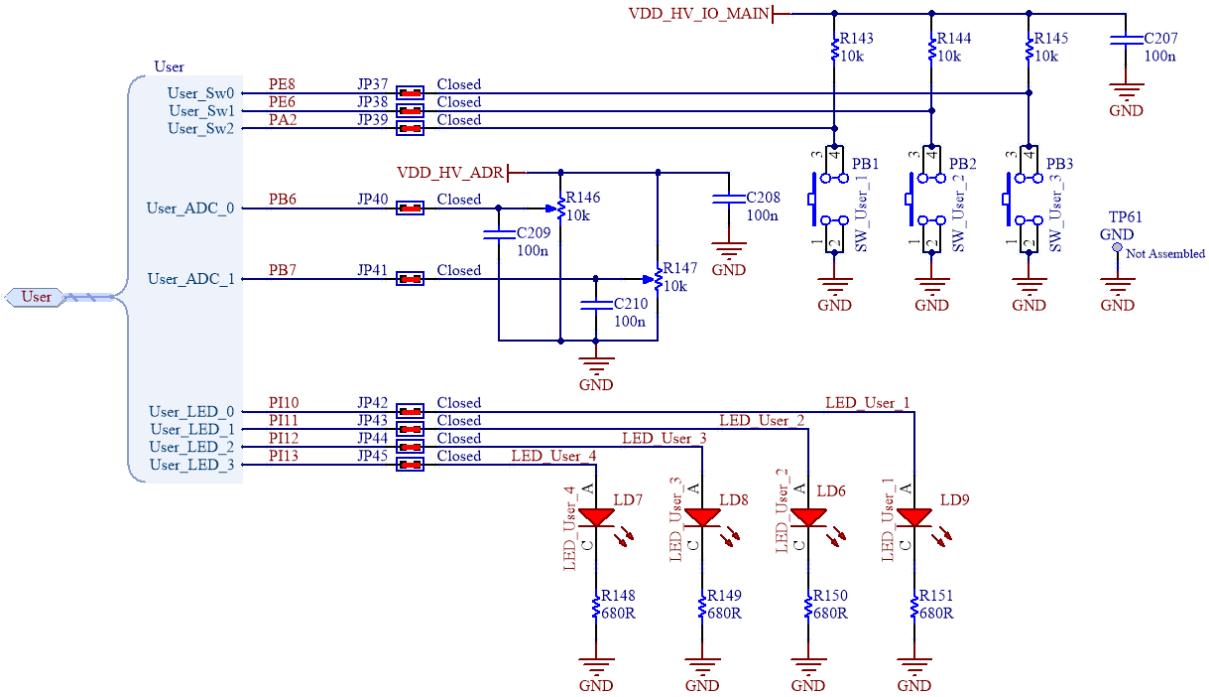


2.14 User interface

The user interface section includes 3 pushbuttons, 4 LEDS for user purpose, to simplify the debug and in addition to have a user interface port.

Two potentiometers allow the evaluation of the ADC module; each potentiometer is connected to the VDD_HV_ADR supply source, it is the reference level of the ADC converters in the microcontroller.

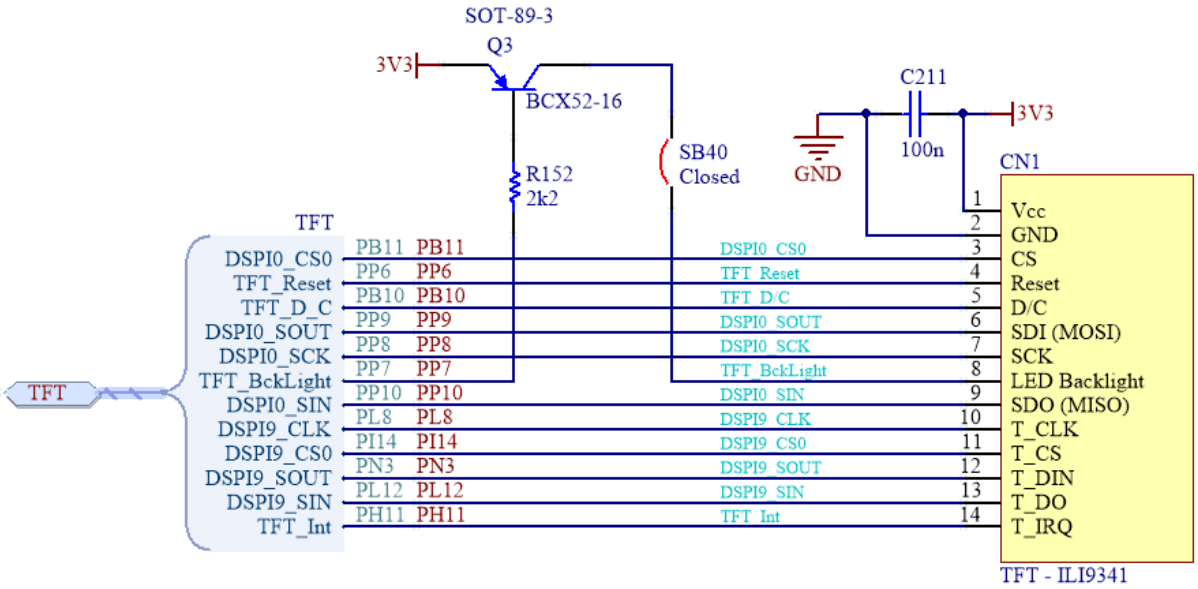
Figure 17. User interface



2.15 LCD

A display with SPI can be plugged in the board using two male pin arrays (one of them is used only as mechanical support). Figure 18 shows how the signals are connected.

Figure 18. LCD module

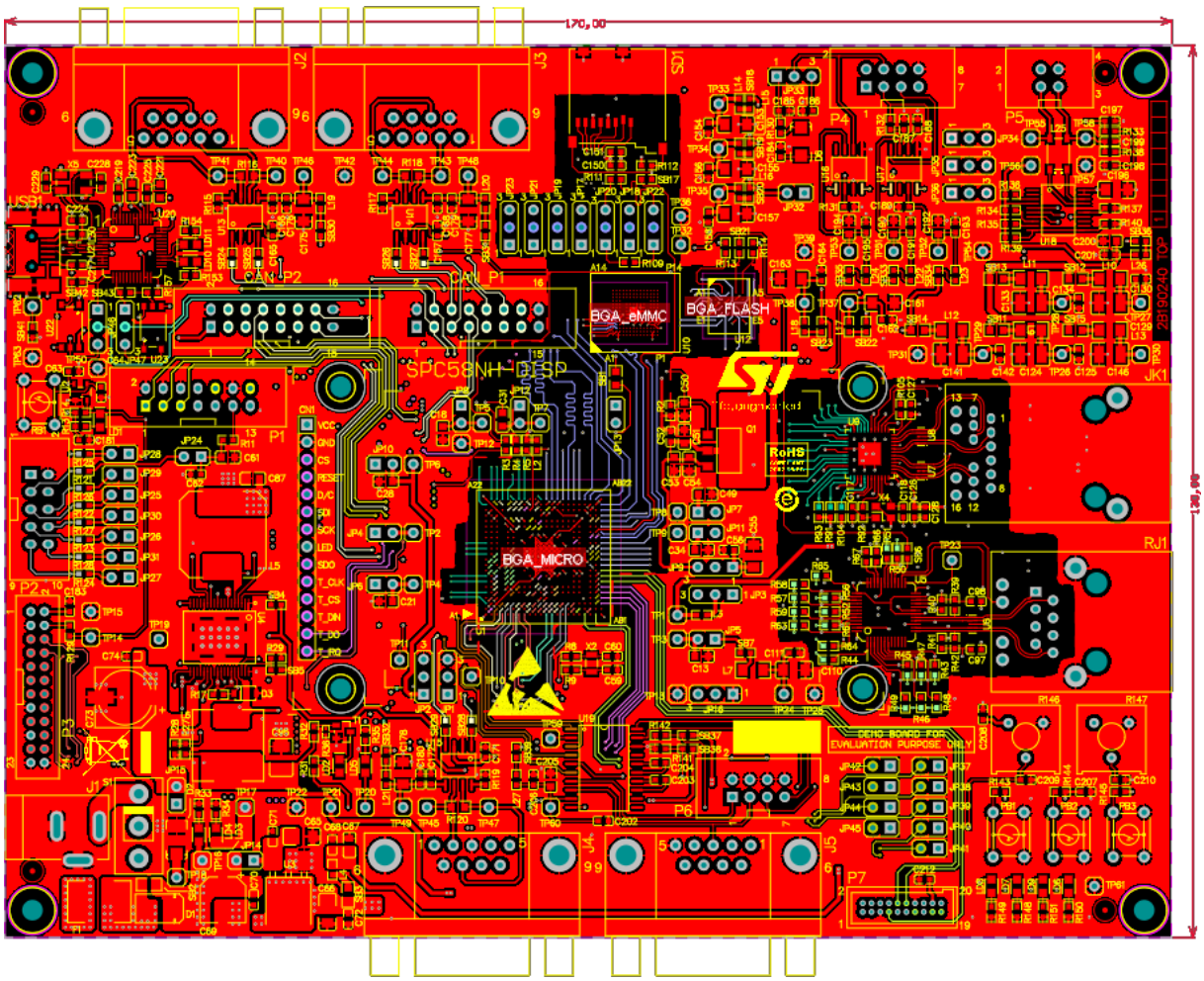


3 PCB layout

The PCB layout is reported in Figure 19.

Some copper tracks have been placed paying attention to have the same mechanical length and a specific impedance; in detail the critical paths involve the ethernet 1 Gbps - ethernet 10/100 Mbps sections as well as the eMMC and the Hyper bus signals.

Figure 19. PCB layout



Revision history

Table 1. Document revision history

Date	Version	Changes
13-Mar-2020	1	Initial release.
24-Feb-2021	2	Updated Figure 4. Ethernet 10/100 Mbps. Updated Figure 9. HyperFlash and HyperRAM. Updated Figure 11. Flex Ray. Updated Figure 12. I²C. Minor text changes.

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