UM1893
User Manual

STSW-RFSOL001 – STWPLLSim simulation tool for STW81200/STuW81300

Introduction

The STWPLLSim software is a powerful software tool developed to allow the end-user of the ST PLL Synthesizer products to optimize the PLL design and simulate accurately the performance (both phase noise and transient).

STWPLLSim_v5.2 has an embedded model of the PLL synthesizers integrated in the STW81200 product (46.875-6000 MHz wideband RF fractional/integer synthesizer) and in the new STuW81300 (1.925-16 GHz wideband RF/microwave fractional/integer synthesizer).

The environment for design and simulation using STW8110x family product is still available.

Contents

1 Installation

The STWPLLSim software is written in Java and designed to run on Windows 2000/XP/7.

In order to allow time-domain simulations, STWPLLSim requires the MATLAB Component Runtime (MCR) Libraries (Copyright 1984-2011, The MathWorks, Inc.).

Note: Microsoft Visual C++ 2008 and 2010 Redistributable is required on the host PC. It is automatically installed if not present.

1.1 Installation steps

1. Refer to the README file and check the recommendations.
2. Run *SETUP.bat* to launch the installation of the MCR, Microsoft Visual C++ products (if not already installed on the system) and STWPLLSim.

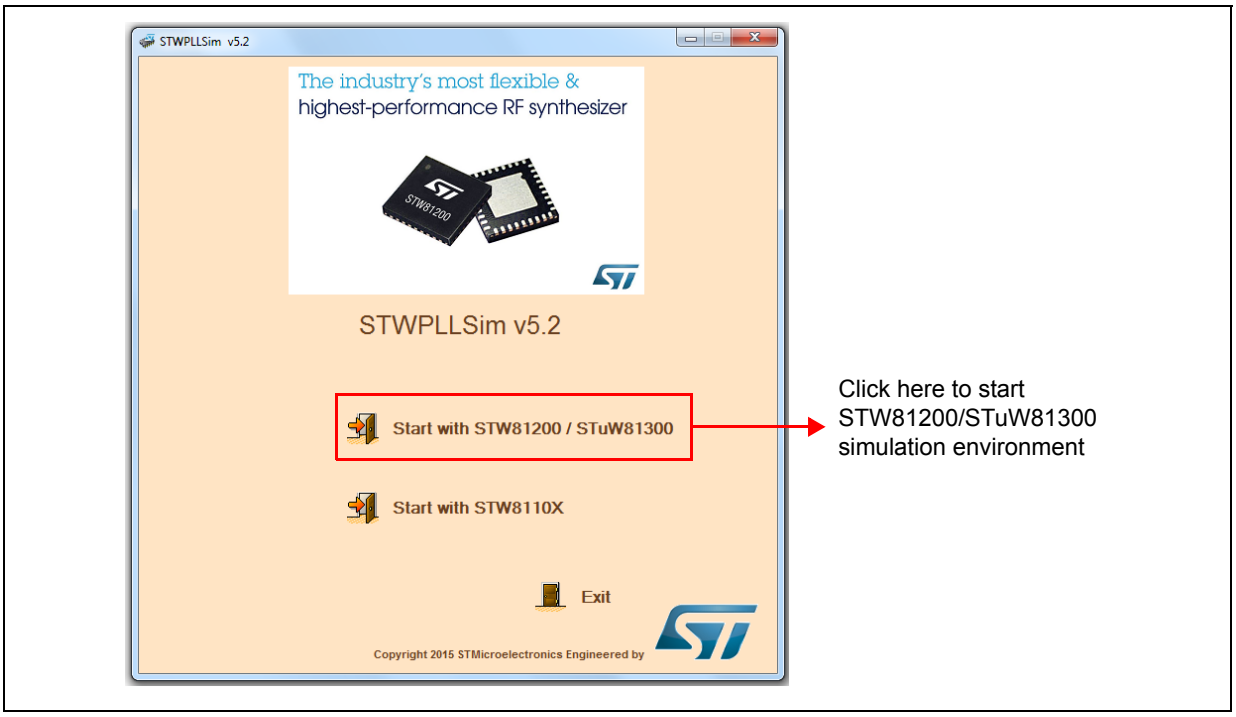
After installation double-click on the 'STWPLLSim_v5.2' icon to run the program.

1.2 Product selection

Once STWPLLSim_v5.2 is launched, the product selection form appears (*Figure 1*). Select the simulation environment for the desired product (STW81200/STuW81300 or the STW8110x family).

This document explains only the STW81200/STuW81300 simulation environment. The user guide for the STW8110x product simulator is available separately *[1]*.

Figure 1. Product selection window

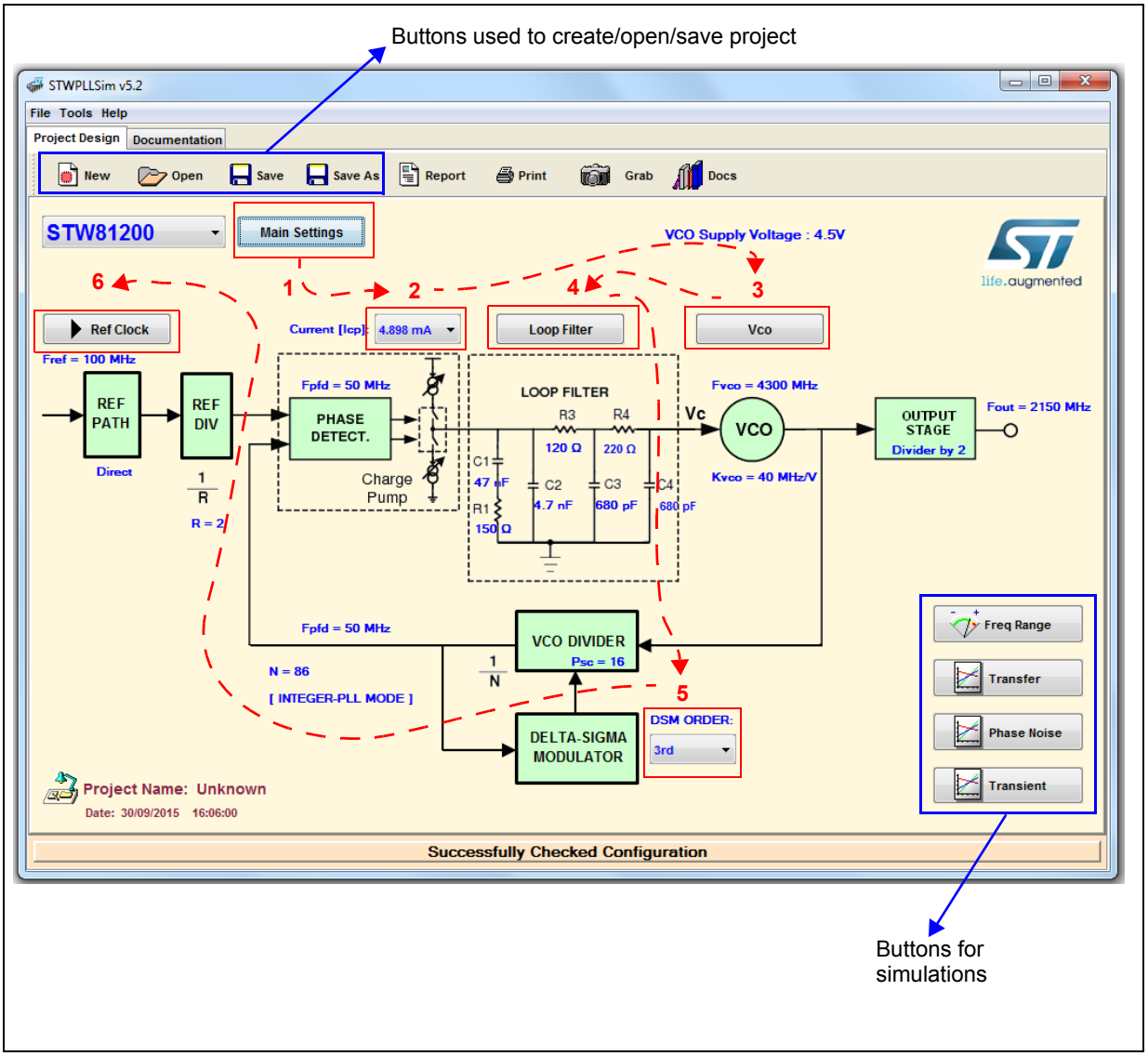


2 Main form

The main form window (*Figure 2*) gives access to the project elements. The project flow comprises 6 steps described in the following sections:

- *Section 2.2.1: Main settings (step 1)*
- *Section 2.2.2: Charge pump and VCO settings (steps 2, 3)*
- *Section 2.2.3: Loop filter design form (step 4)*
- *Section 2.2.4: DSM order and reference frequency/noise settings (steps 5,6)*.

Figure 2. STWPLLSim main form and project flow



2.1 Creating and managing projects

The New and **Open** buttons allow the user to create a new project or to open an existing one.

The project can be saved by pressing the **Save**/**Save As** buttons.

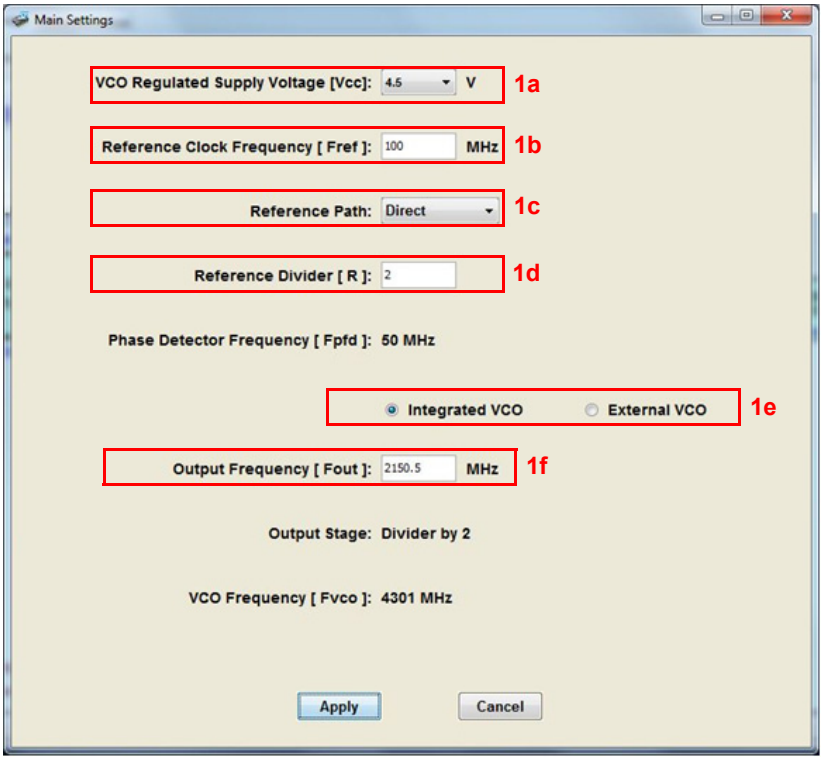
2.2 Project flow

2.2.1 Main settings (step 1)

The following steps are applied through the Main settings window.

1. Open the Main settings window (see the screen shot in *Figure 3*):
   a) Select VCO regulated voltage (V)
   b) Set reference clock frequency (800 MHz max.)
   c) The reference path is automatically set
   d) Set the reference divider to get the desired PFD
   e) Set the VCO type (integrated or external)
   f) Set the output frequency (50 to 6000 MHz for STW81200 and 1925 to 16000 MHz for STuW81300) or VCO frequency when external VCO is selected.

Figure 3. Main settings window

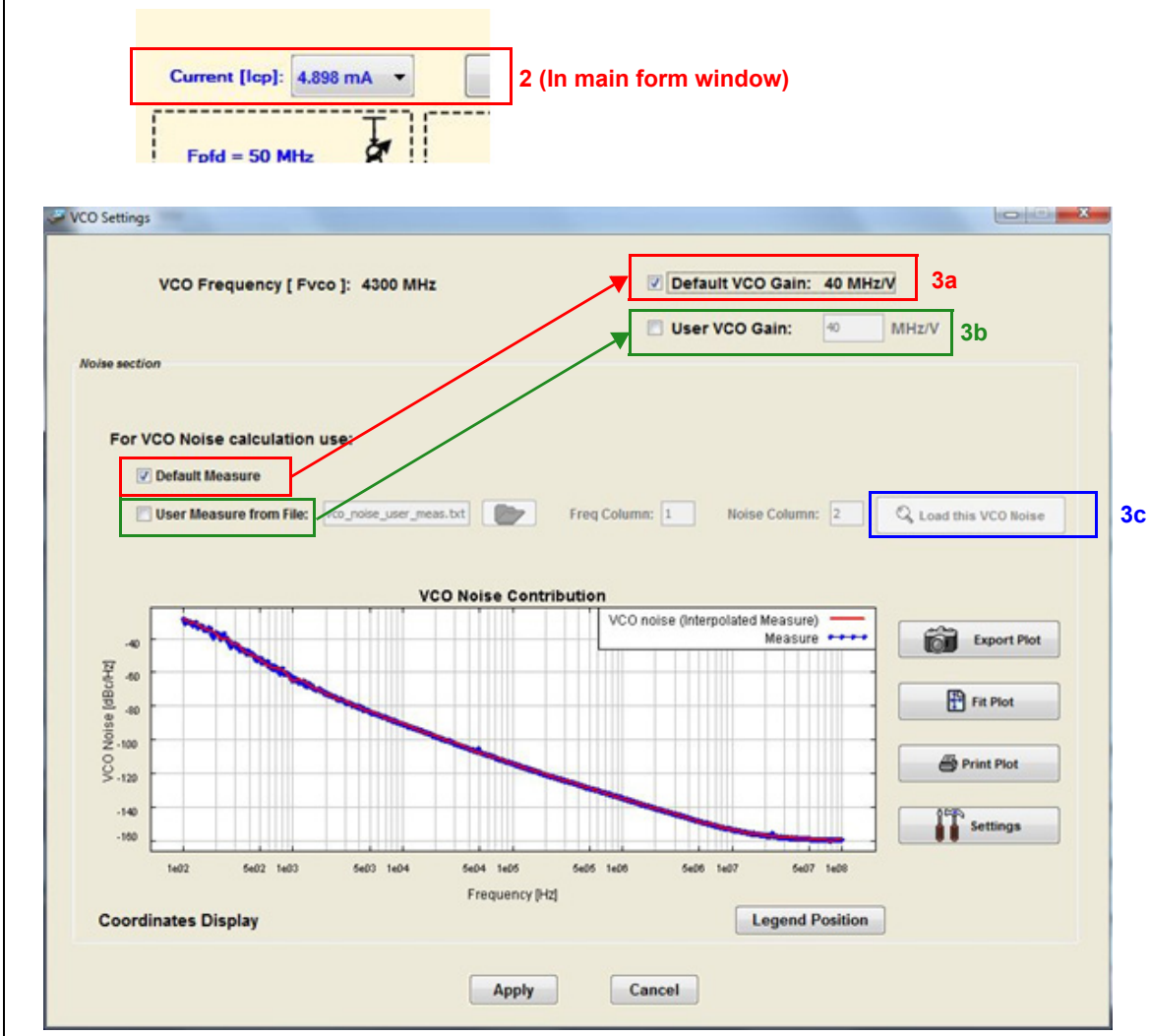


2.2.2 Charge pump and VCO settings (steps 2, 3)

The following steps are applied through the VCO settings window, shown in *Figure 4*.

2. In the Main form window select the desired Charge Pump current (~5 mA max.,0.156 mA step).
3. Select default or user defined VCO settings:
   a) Default VCO gain and phase noise data are automatically updated based upon VCO frequency and VCO regulated supply settings (default settings are strongly advised when using integrated VCOs).
   b) User-defined VCO gain value and noise data can be introduced (mandatory when external VCO is selected).
   c) Pushing the **Load this VCO noise** button uploads user-defined data from a file (not required when default settings are selected).

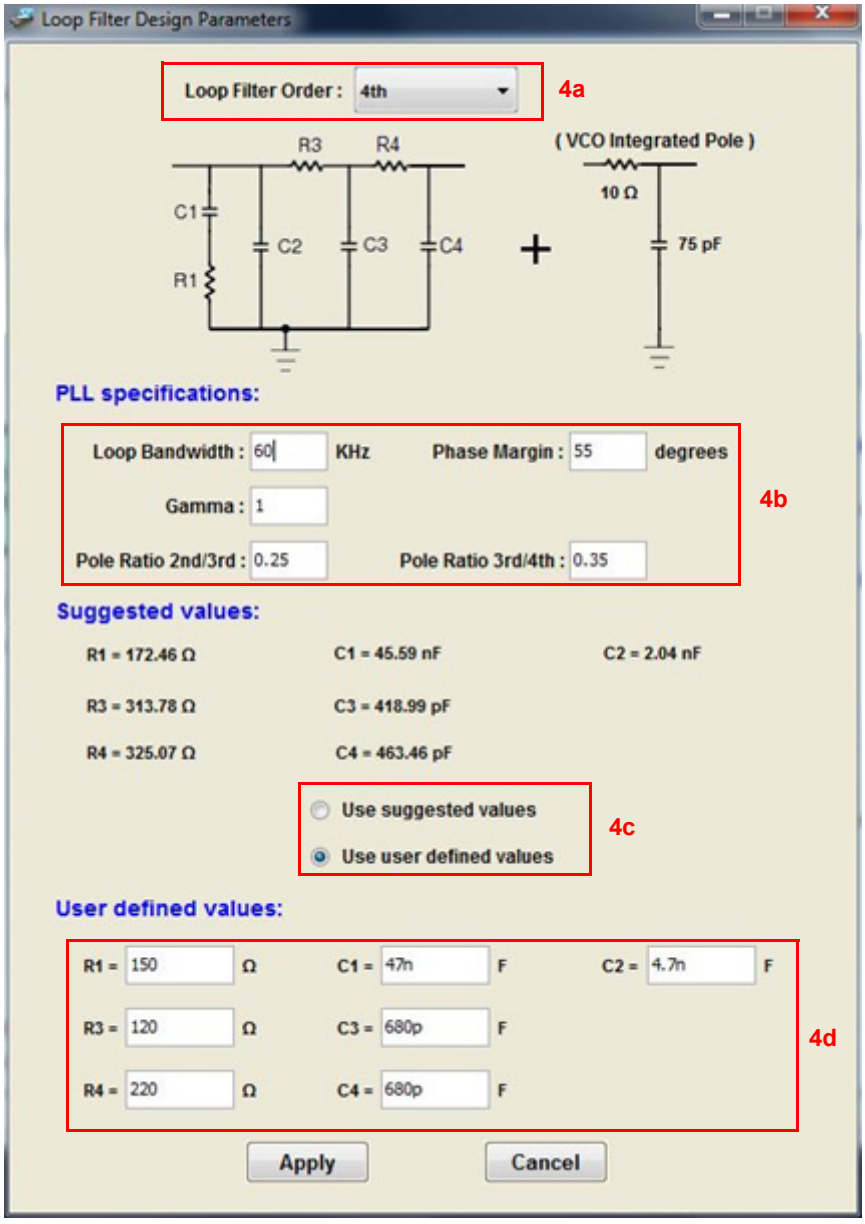
Figure 4. Charge pump and VCO settings



2.2.3 Loop filter design form (step 4)

4. The following steps are applied through the VCO settings window, shown in *Figure 5*:
   a) Select the desired loop filter order (2nd, 3rd and 4th available).
   b) Set PLL high-level specifications (desired PLL bandwidth and phase margin) and tuning parameters (ratio between poles).
   c) Select the desired component setting values (suggested or user-defined).
   d) When using user-defined components, valid unit prefixes are ‘K’ for resistor, ‘n’ and ‘p’ for capacitors.

Figure 5. Loop filter design form window

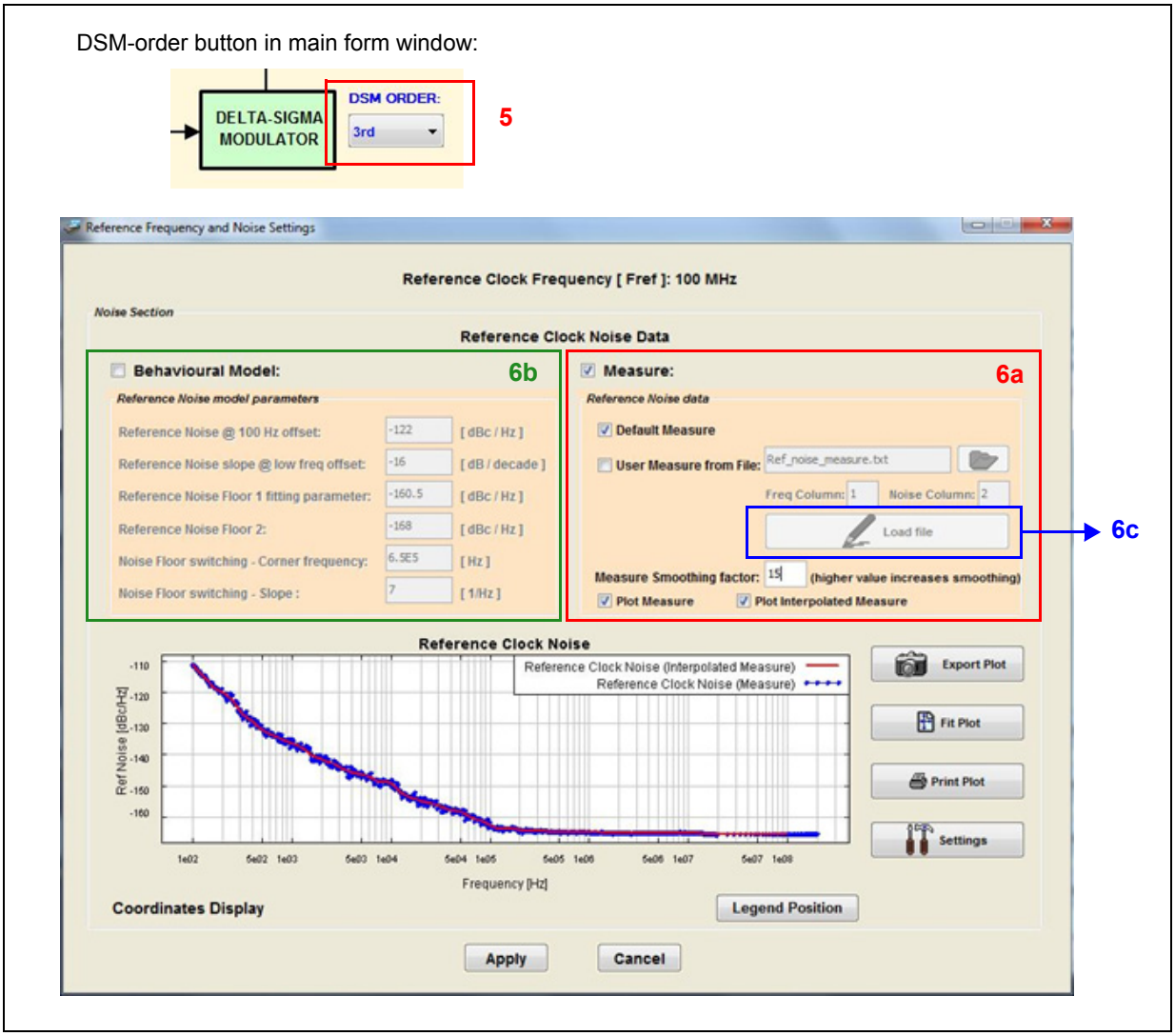


2.2.4 DSM order and reference frequency/noise settings (steps 5,6)

The following steps are applied through the DSM order and reference frequency/noise settings window, shown in *Figure 6*.

5. Select the desired DSM order (default 3rd)
6. Reference clock noise source can be introduced as a behavioral model or as measurement data.
   a) Measurement options area:
   – 'Default' uses measured phase noise data related to the 100MHz VCXO mounted on the STW81200/STuW81300 Evaluation board.
   – User-Measured data can be loaded.
   b) Reference noise can be described by settings the parameters of the behavioral model.
   c) Pushing the 'Load File' button uploads user-defined data from a file (not required when default settings are selected).

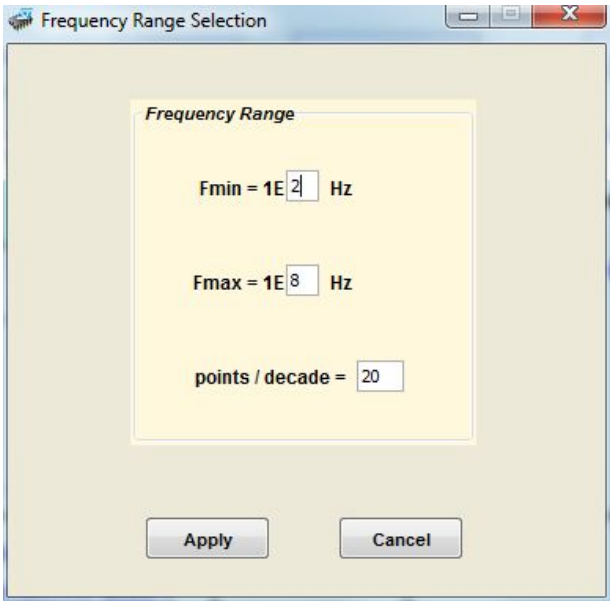
Figure 6. DSM order and reference frequency/noise settings window



2.2.5 Simulation frequency settings

The frequency limits (minimum and maximum) and number of points to be used for simulations are set in the frequency range selection window, shown in *Figure 7*.

Figure 7. Frequency range selection window



3 Waveform viewers

3 waveform viewers are available and are described in the following sections:

- *Section 3.1: Transfer function*
- *Section 3.2: Phase noise*
- *Section 3.3: Transient simulations*.

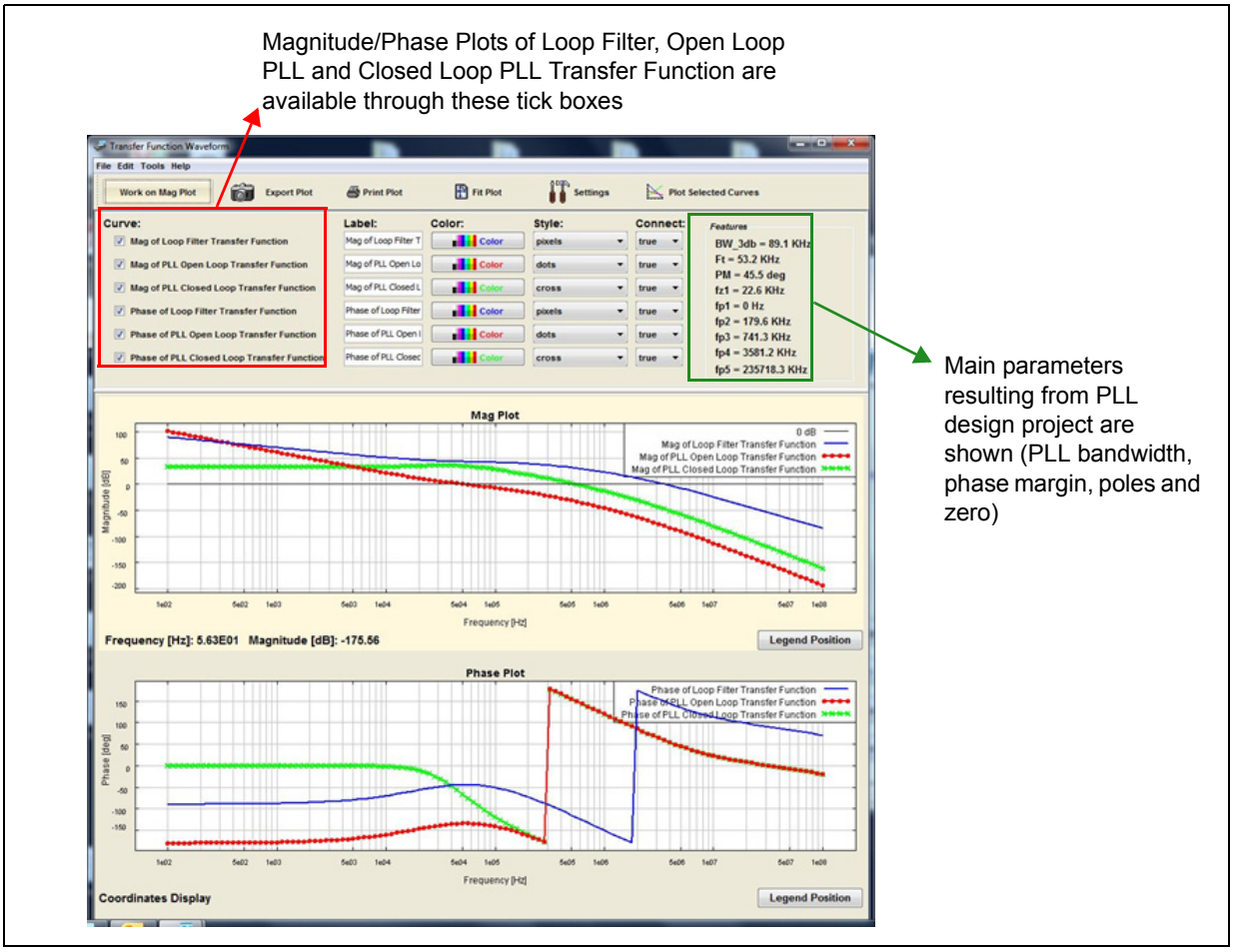
3.1 Transfer function

The transfer function waveform viewer window (*Figure 8*) allows the following transfer functions to be plotted by selecting the **Curve** tick boxes in the window:

- Loop filter
- PLL open loop
- PLL closed loop

The main parameters resulting from the PLL design project (PLL bandwidth, phase margin, poles and zero) are shown under the **Features** dialog.

Figure 8. Transfer function waveform viewer window



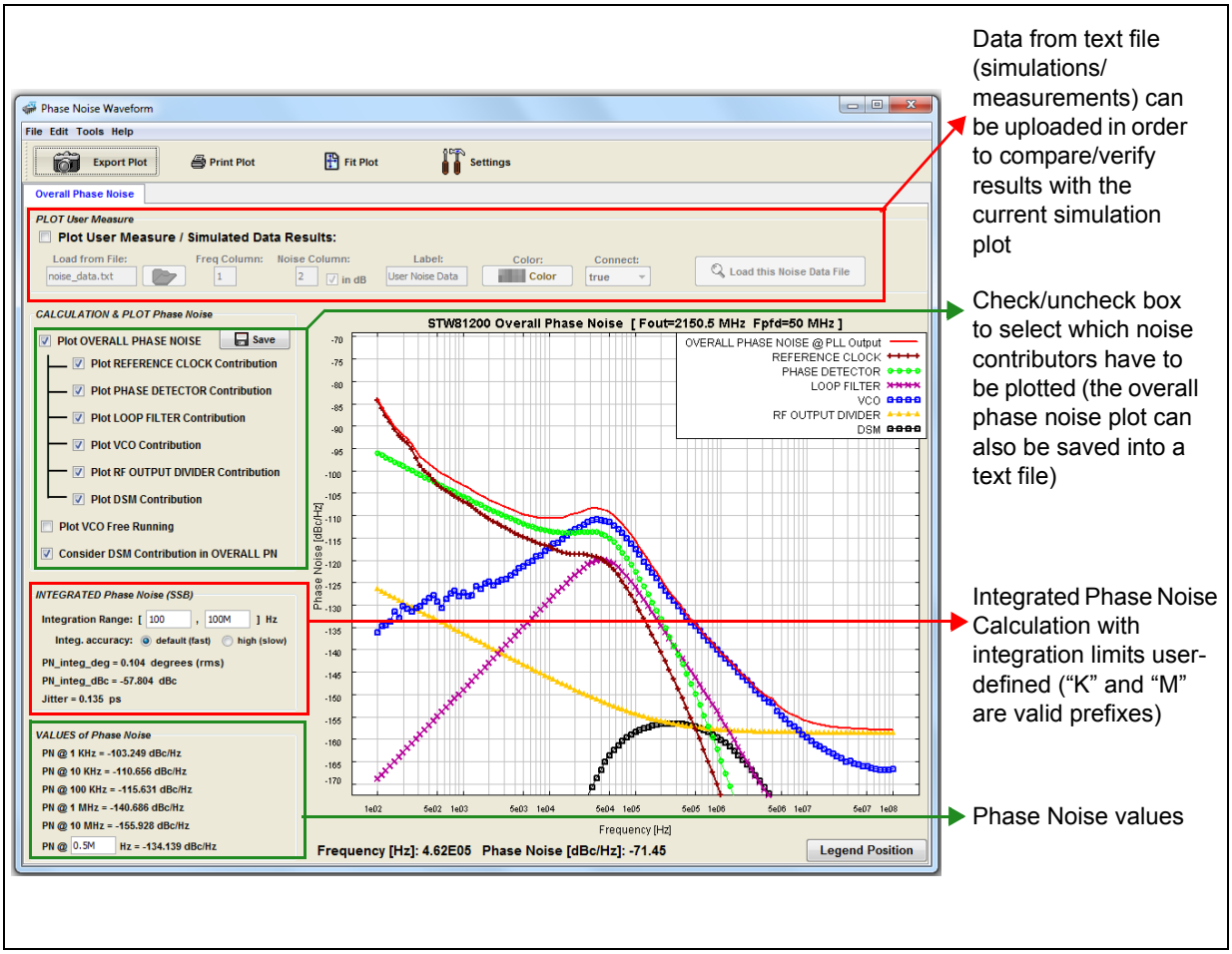
3.2 Phase noise

The following functions are available in the phase noise waveform viewer window (*Figure 9*):

- Plot the overall phase noise and the following contributions:
  - reference clock
  - phase detector
  - loop filter
  - VCO
  - DSM and RF output divider stage.
- Save the overall phase noise to a text file.
- Load user measured/simulated data from a text file.
- Calculate the integrated phase noise by inserting the integration range limits and pressing **Enter**. 'K' and 'M' are valid unit prefixes for the frequency.
- Calculate phase noise values for five fixed frequencies and for one user frequency.

*Note: You can modify the frequency range from the Main form by clicking the **Freq Range** button (see Figure 2).*

Figure 9. Phase noise waveform viewer window



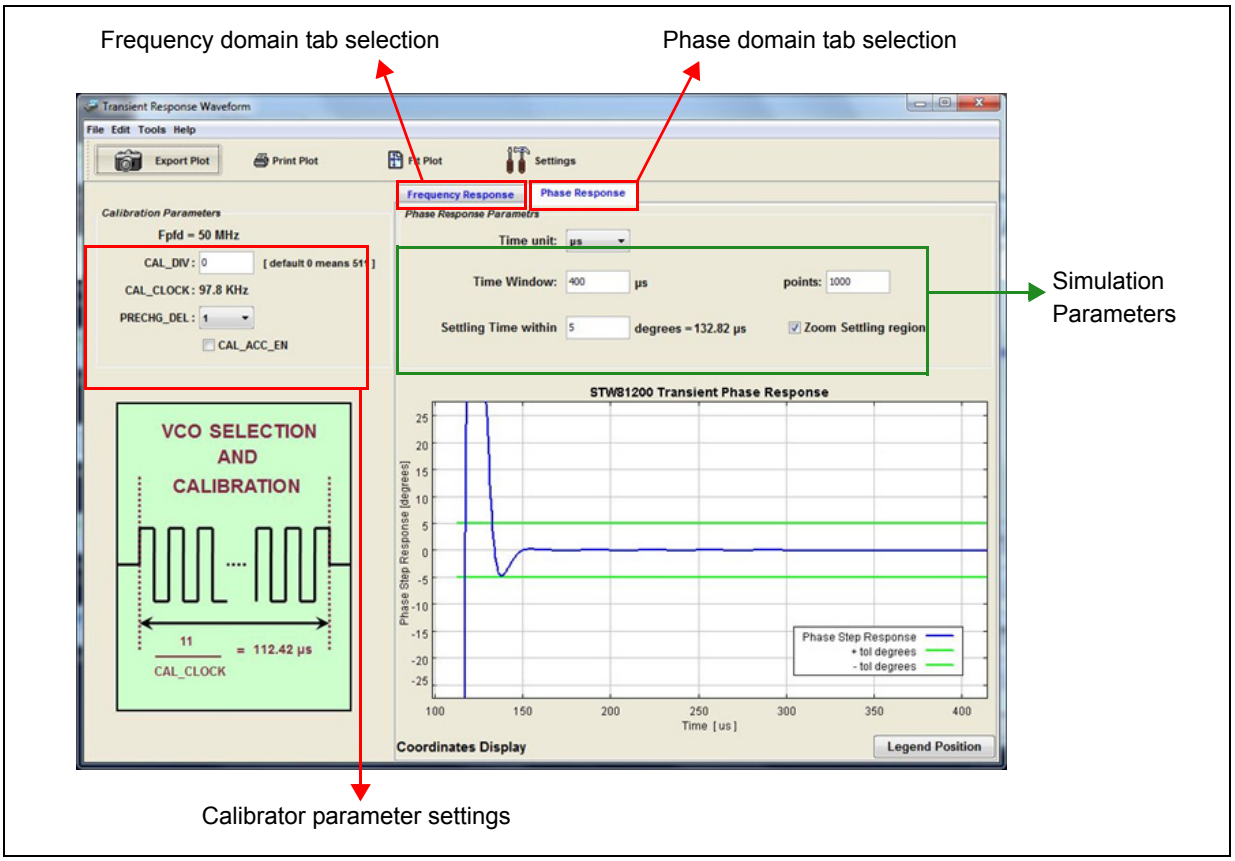
3.3 Transient simulations

The step time response is plotted and the following parameters can be set.

- Simulation response
  - Time unit: µs or ms
  - Time Window: set duration of the transient simulation
  - Points: number of points
  - Settling time within frequency error (in ppm) with respect to the Fout final value or phase error (in degrees), depending on the domain tab selected.
  - Time unit (µs or ms).
  - Zoom on settling region (default: on).
- Calibrator Parameters:
  - CAL_DIV: sets the PFD frequency divider ratio to determine the clock frequency of the VCO calibrator (must be below 1 MHz)
  - PRECHG_DEL: sets the number of slots used to charge the Vctrl node to the reference voltage (default value:1)
  - CAL_ACC_EN: increases the accuracy (and duration) of the last calibration step (default: unchecked).

The VCO calibration time is calculated according to the F_{PFD} value together with the above calibrator parameters (CAL_DIV, PRECHG_DEL, CAL_ACC_EN) and taken into account in the settling time value

Figure 10. Transient response waveform viewer window (phase domain)

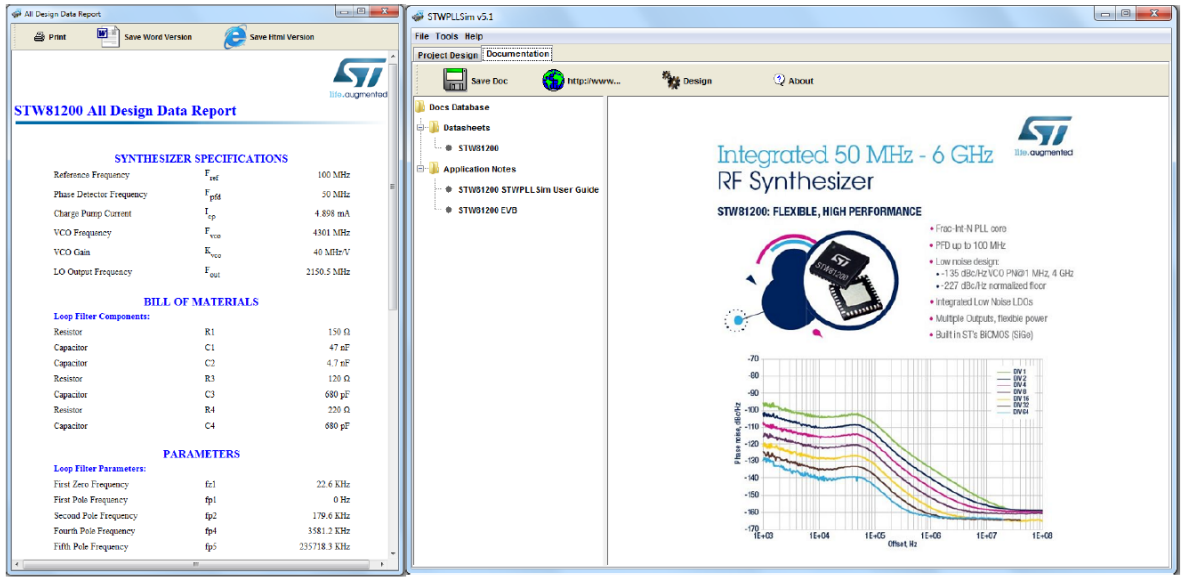


3.4 Project report and documentation

A report containing the synthesizer specification, the bill of materials and the design parameters can be generated by the tool.

The documentation form contains STW81200/STuW81300 data sheets *[2]*, *[3]* and application notes.

Figure 11. Project report and documentation output



4 Reference documents

Table 1. Reference documents

Reference	Revision	Title
[1]	Latest version	ST Application Note AN2455 STWPLLSim phase noise and settling time simulator for STW8110x. (Can be downloaded from www.st.com)
[2]	Latest version	STW81200 widebandRF PLL fractional/integer frequency synthesizer with integrated VCOs and LDOs datasheet, Document ID 025943
[3]	Latest version	STuW81300 wideband/microwave RF PLL fractional/integer frequency synthesizer with integrated VCOs and LDOs datasheet, Document ID 028443

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
09-Jun-2015	1	First release.
13-Jan-2016	2	Updated to scope STW81200 and STuW81300. Updated introductory part of *Section 1: Installation*.