UM1688
User manual

EVAL6470H, EVAL6470PD, EVAL6472H and EVAL6472PD: fully integrated microstepping motor drivers

Introduction

The EVAL6470H, EVAL6470PD, EVAL6472H and EVAL6472PD are four demonstration boards based on the L6470 and L6472 devices implementing a complete stepper motor driver solution. They are designed for operate with a supply voltage ranging from 8 V to 45 V and can drive up to 3 $A_{r.m.s.}$ for each phase.

In combination with the STEVAL-PCC009V2 demonstration board and the SPINFamily evaluation tool, the boards provide a complete and easy to use evaluation environment allowing the user to investigate all the features of the L6470 and L6472 devices. Both the boards support the daisy chain configuration making them suitable for the evaluation of the devices in multi motor applications.

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1 Boards description

1.1 EVAL6470H

Table 1. EVAL6470H - specifications

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 $A_{r.m.s.}$
Logic supply voltage (VREG)	Externally supplied: 3.3 V, internally supplied: 3 V (typ.)
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V, internally supplied: VREG
Low level logic inputs voltage	0 V
High level logic input voltage	VDD(1)
Operating temperature	-25 to +125 °C
L6470H thermal resistance junction to ambient	21 °C/W (typ.)

1. All logic inputs are 5 V tolerant.

Figure 1. EVAL6470H - jumpers and connectors location

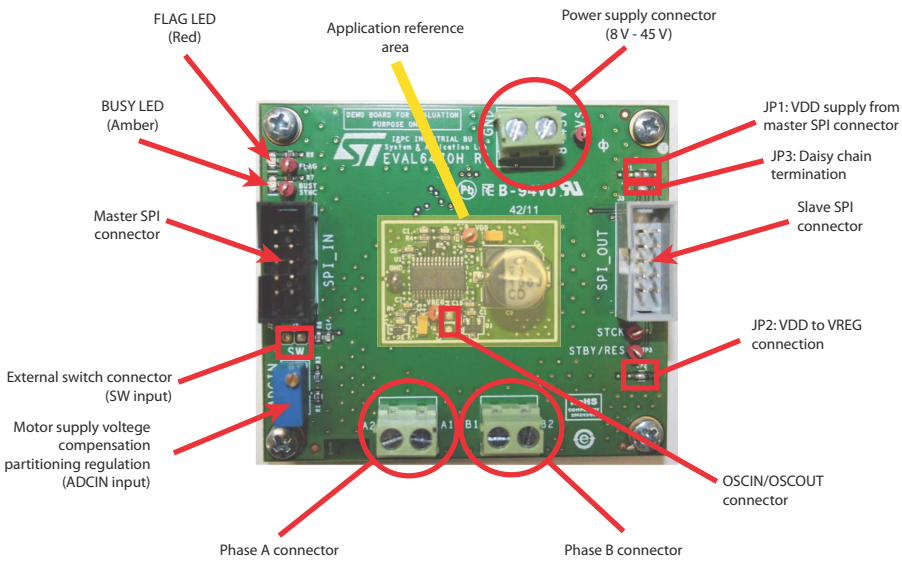

Table 2. EVAL6470H - jumpers and connectors description

Name	Type	Function
J1	Power supply	Motor supply voltage
J5	Power output	Bridge A outputs
J6	Power output	Bridge B outputs
J2	SPI connector	Master SPI
J3	SPI connector	Slave SPI
J4	NM connector	OSCIN and OSCOUT pins
J7	NM connector	External switch input
TP1 (VS)	Test point	Motor supply voltage test point
TP4 (VDD)	Test point	Logic interface supply voltage test point
TP5 (VREG)	Test point	Logic supply voltage/L6470 internal regulator test point
TP6 (GND)	Test point	Ground test point
TP2 (STCK)	Test point	Step-clock input test point
TP3 (STBY/RES)	Test point	Standby/reset input test point
TP7 (FLAG)	Test point	FLAG output test point
TP8 (BUSY/SYNC)	Test point	BUSY/SYNC output test point

Table 3. EVAL6470H - master SPI connector pinout (J10)

Pin number	Type	Description
1	Open drain output	L6470 BUSY/SYNC output
2	Open drain output	L6470 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to L6470 SDO output through daisy-chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6470 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6470 SDI input)
8	Digital input	SPI slave select signal (connected to L6470 CS input)
9	Digital input	L6470 step-clock input
10	Digital input	L6470 STBY/RST input

Table 4. EVAL6470H - slave SPI connector pinout (J11)

Pin number	Type	Description
1	Open drain output	L6470 BUSY/SYNC output
2	Open drain output	L6470 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to pin 5 of J10)
6	Digital input	SPI serial clock signal (connected to L6470 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6470 SDO output)
8	Digital input	SPI slave select signal (connected to L6470 CS input)
9	Digital input	L6470 step-clock input
10	Digital input	L6470 STBY/RST input

Figure 2. EVAL6470H - schematic

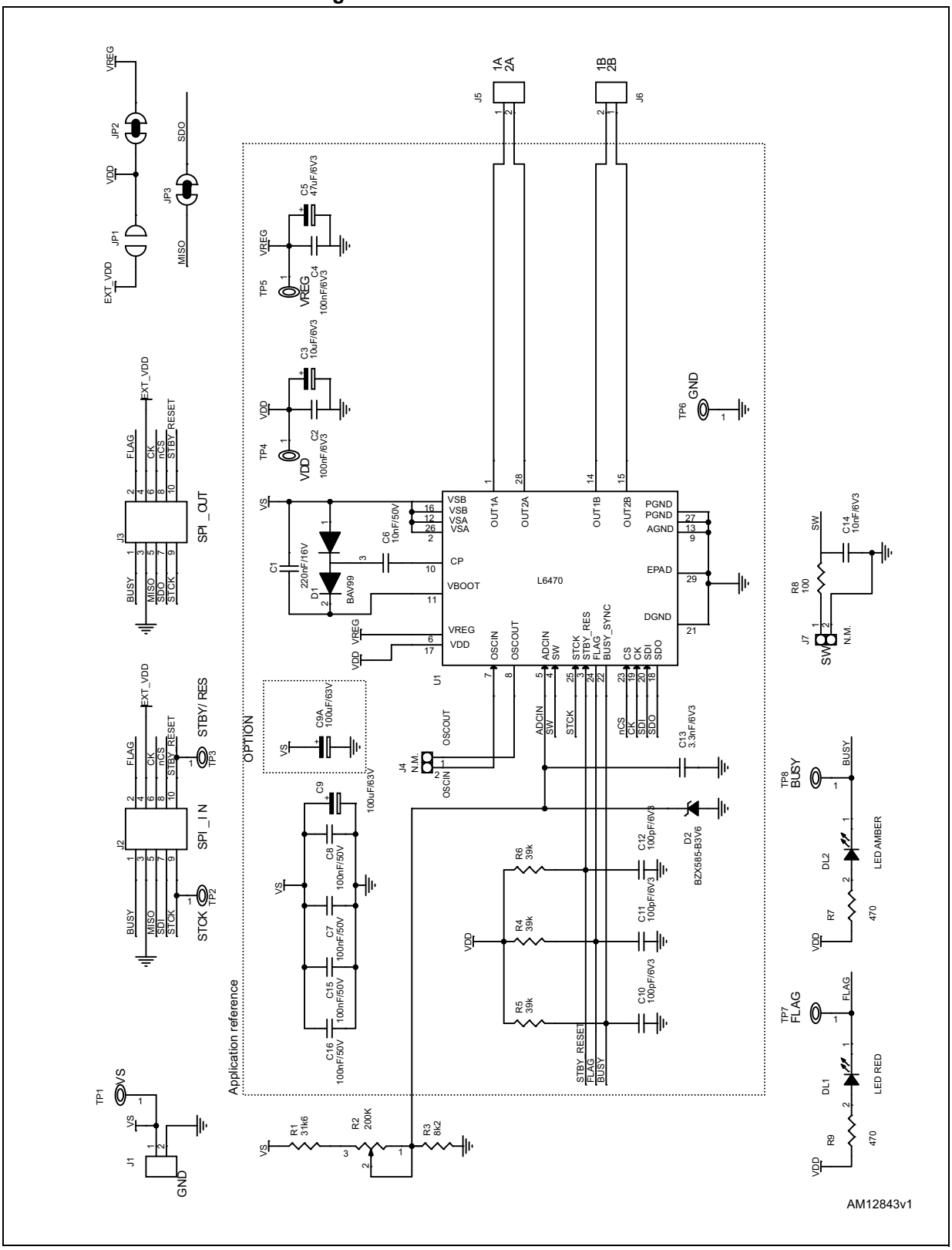

Table 5. EVAL6470H - bill of material

Item	Quantity	Reference	Value	Package
1	1	C1	220 nF/16 V	CAPC-0603
2	2	C2,C4	100 nF/6.3 V	CAPC-0603
3	1	C3	10 µF/6.3 V	CAPC-3216
4	1	C5	47 µF/6.3 V	CAPC-3216
5	1	C6	10 nF/50 V	CAPC-0603
6	4	C7, C8, C15, C16	100 nF/50 V	CAPC-0603
7	1	C9A	100 µF/63 V	CAPE-R8H12-P35
8	1	C9	100 µF/63 V	CAPES-R10HXX
9	3	C10, C11, C12	100 pF/6.3 V	CAPC-0603
10	1	C13	3.3 nF/6.3 V	CAPC-0603
11	1	C14	10 nF/6.3 V	CAPC-0603
12	1	DL1	LED diode (red)	LEDC-0805
13	1	DL2	LED diode (amber)	LEDC-0805
14	1	D1	BAV99	SOT23
15	1	D2	BZX585-B3V6(1)	SOD523
16	1	JP1	Jumper - OPEN	JP2SO
17	2	JP2, JP3	Jumper - CLOSED	JP2SO
18	3	J1, J5, J6	Screw connector 2 poles	MORSV-508-2P
19	2	J2,J3	Pol. IDC male header vertical 10 poles	CON-FLAT-5X2-180M
20	2	J4,J7	N.M.	STRIP254P-M-2
21	1	R1	31.6 kΩ	RESC-0603
22	1	R2	200 kΩ	TRIMM-100X50X110-64W
23	1	R3	8.2 kΩ	RESC-0603
24	3	R4, R5, R6	39 kΩ	RESC-0603
25	2	R7, R9	470 Ω	RESC-0603
26	1	R8	100 Ω	RESC-0603
27	8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test point	TH
28	1	U1	L6470	HTSSOP28

Figure 3. EVAL6470H - layout (top layer)

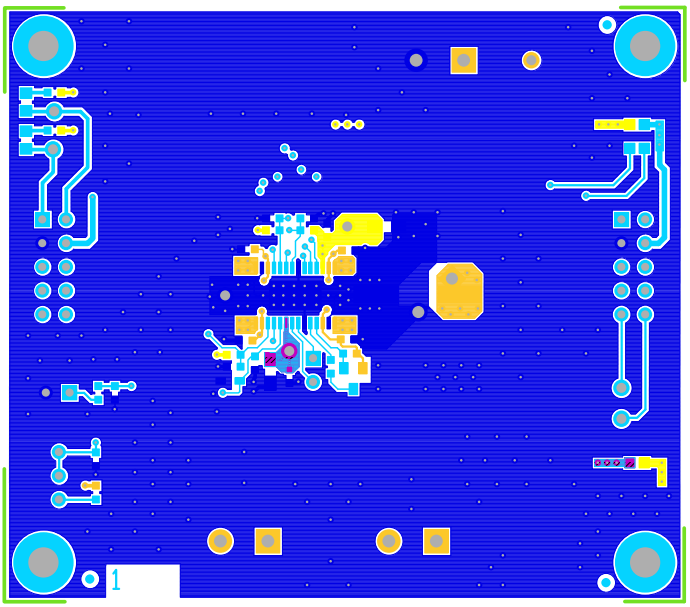

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Figure 4. EVAL6470H - layout (inner layer 2)

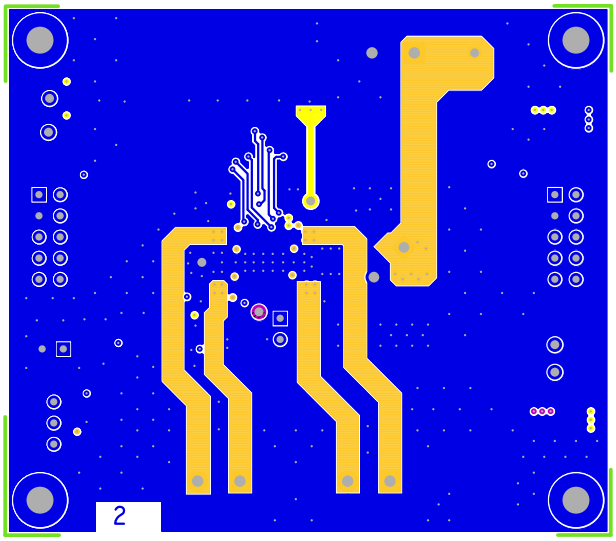

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Figure 5. EVAL6470H - layout (inner layer 3)

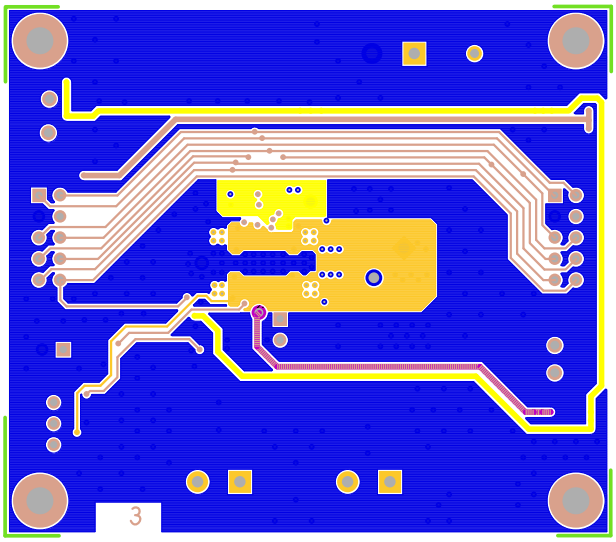

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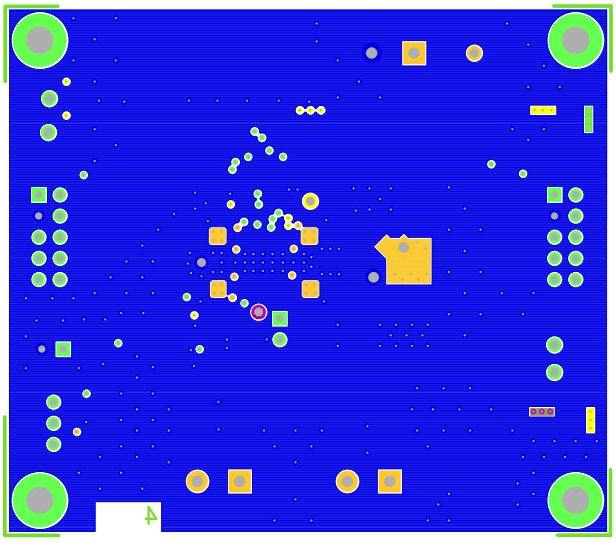
Figure 6. EVAL6470H - layout (bottom layer)



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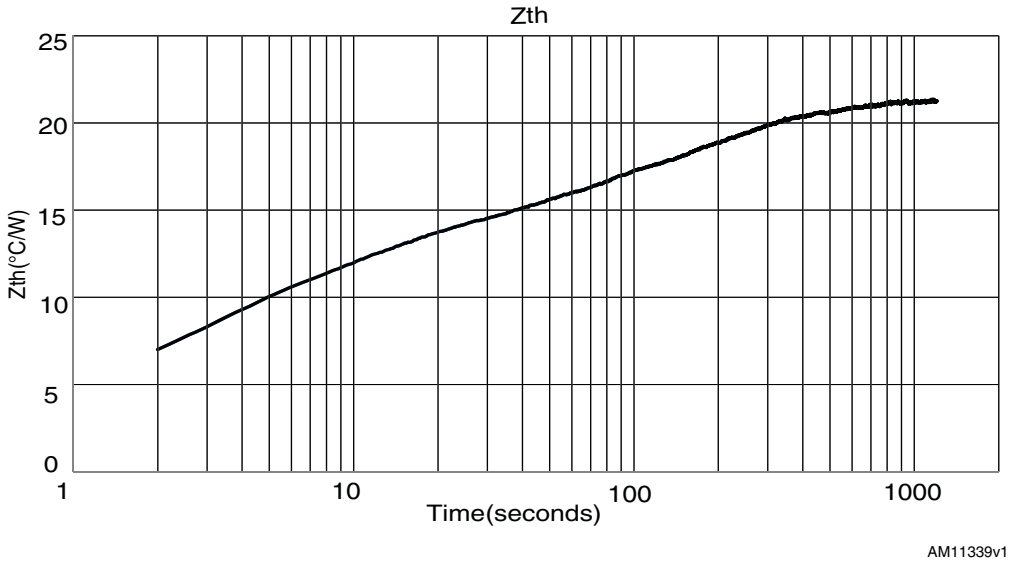
EVAL6470H - thermal data

Figure 7. EVAL6470H - thermal impedance graph



1.2 EVAL6470PD

Table 6. EVAL6470PD - specifications

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 $A_{r.m.s.}$
Logic supply voltage (VREG)	Externally supplied: 3.3 V internally supplied: 3 V typical
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V internally supplied: VREG
Low level logic input voltage	0 V
High level logic input voltage	VDD(1)
Operating temperature	-25 to +125 °C
L6470PD thermal resistance junction to ambient	12 °C/W typical

1. All logic inputs are 5 V tolerant.

Figure 8. EVAL6470PD - jumper and connector location

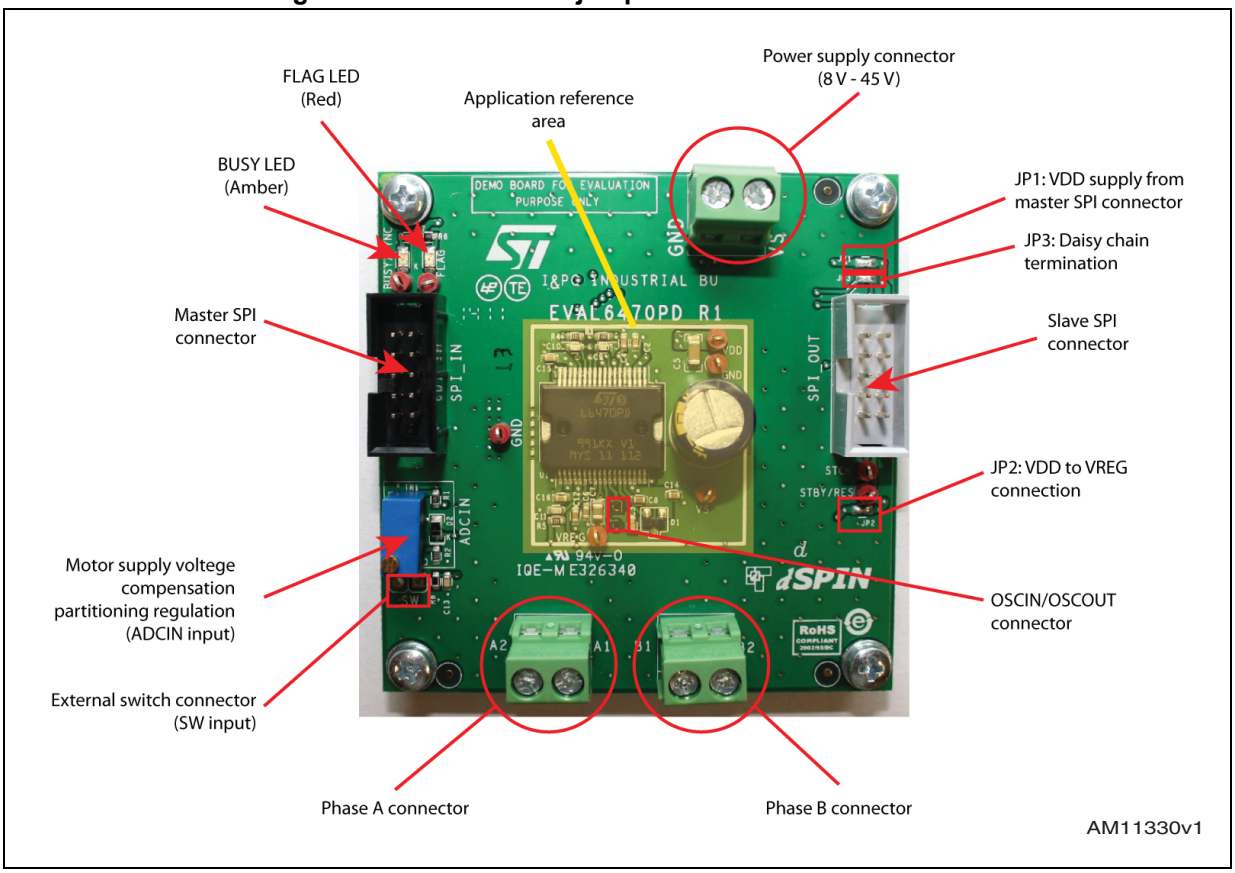


Table 7. EVAL6470PD - jumper and connector description

Name	Type	Function
M1	Power supply	Motor supply voltage
M2	Power output	Bridge A outputs
M3	Power output	Bridge B outputs
CN1	SPI connector	Master SPI
CN2	SPI connector	Slave SPI
CN3	NM connector	OSCIN and OSCOUT pins
CN4	NM connector	External switch input
TP1 (VS)	Test point	Motor supply voltage test point
TP2 (VDD)	Test point	Logic interface supply voltage test point
TP3 (VREG)	Test point	Logic supply voltage/L6470 internal regulator test point
TP5 (GND)	Test point	Ground test point
TP6 (GND)	Test point	Ground test point
TP8 (STCK)	Test point	Step-clock input test point
TP9 (STBY/RES)	Test point	Standby/reset input test point
TP10 (FLAG)	Test point	FLAG output test point
TP11 (BUSY/SYNC)	Test point	BUSY/SYNC output test point

Table 8. EVAL6470PD - master SPI connector pinout (J10)

Pin number	Type	Description
1	Open drain output	L6470 BUSY/SYNC output
2	Open drain output	L6470 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to the L6470 SDO output through the daisy chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6470 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6470 SDI input)
8	Digital input	SPI slave select signal (connected to L6470 CS input)
9	Digital input	L6470 step-clock input
10	Digital input	L6470 STBY/RST input

Table 9. EVAL6470PD - slave SPI connector pinout (J11)

Pin number	Type	Description
1	Open drain output	L6470 BUSY/SYNC output
2	Open drain output	L6470 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to pin 5 of J10)
6	Digital input	SPI serial clock signal (connected to L6470 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6470 SDO output)
8	Digital input	SPI slave select signal (connected to L6470 CS input)
9	Digital input	L6470 step-clock input
10	Digital input	L6470 STBY/RST input

Figure 9. EVAL6470PD - schematic

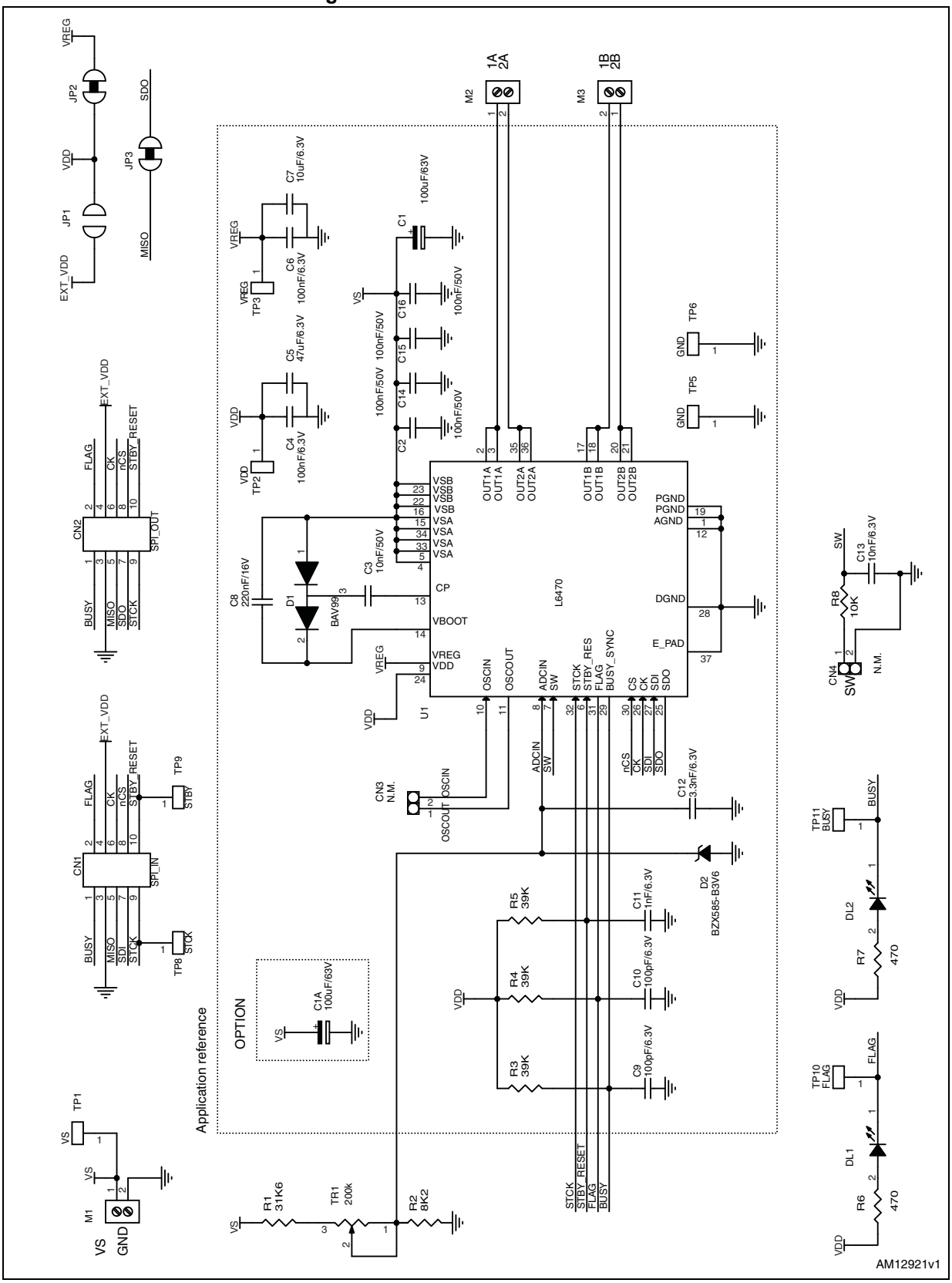


Table 10. EVAL6470PD - bill of material

Index	Quantity	Reference	Value	Package
1	1	CN1	Pol. IDC male header vertical 10 poles (black)	CON-FLAT-5X2-180M
2	1	CN2	Pol. IDC male header vertical 10 poles (gray)	CON-FLAT-5X2-180M
3	2	CN3, CN4	N. M.	STRIP254P-M-2
4	1	C1A	100 µF/63 V (option)	CAPE-R10HXX-P5
5	1	C1	100 µF/63 V	CAPES-R10HXX
6	4	C2, C14, C15, C1	100 nF/50 V	CAPC-0603
7	1	C3	10 nF/50 V	CAPC-0603
8	2	C4, C6	100 nF/6.3 V	CAPC-0603
9	1	C5	47 µF/6.3 V	CAPC-1206
10	1	C7	10 µF/6.3 V	CAPC-0805
11	1	C8	220 nF/16 V	CAPC-0603
12	2	C9, C10	100 pF/6.3 V	CAPC-0603
13	1	C11	1 nF/6.3 V	CAPC-0603
14	1	C12	3.3 nF/6.3 V	CAPC-0603
15	1	C13	10 nF/6.3 V	CAPC-0603
16	1	DL1	LED red	LEDC-0805
17	1	DL2	LED amber	LEDC-0805
18	1	D1	BAV99	SOT23
19	1	D2	BZX585-B3V6	SOD523
20	1	JP1	Jumper OPEN	JP2SO
21	2	JP2, JP3	Jumper CLOSED	JP2SO
22	3	M1, M2, M3	Screw connector 2 poles	MORSV-508-2P
23	1	R1	31.6 kΩ	RESC-0603
24	1	R2	8.2 kΩ	RESC-0603
25	3	R3, R4, R5	39 kΩ	RESC-0603
26	2	R6, R7	470 kΩ	RESC-0603
27	1	R8	10 kΩ	RESC-0603
28	9	TP1, TP2, TP3, TP5, TP6, TP8, TP9, TP10, TP11	TPTH-RING-1MM	TH
29	1	TR1	200 kΩ	TRIMM-100x50x110-64W
30	1	U1	L6470	PowerSO36

Figure 10. EVAL6470PD - layout (top layer)

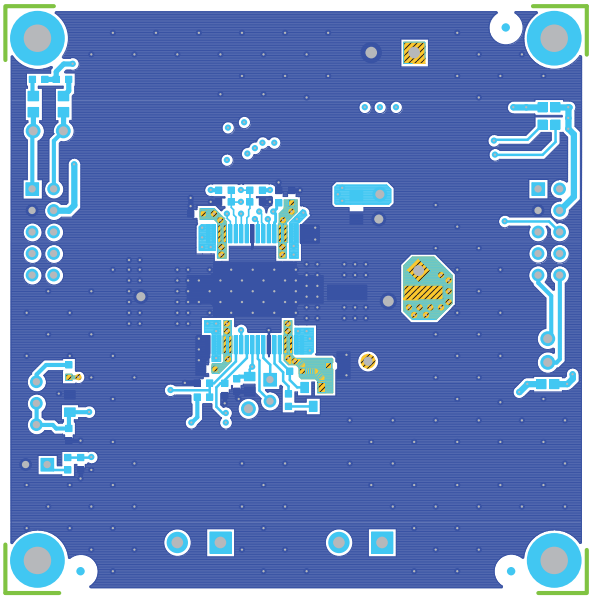


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Figure 11. EVAL6470PD - layout (inner layer 2)

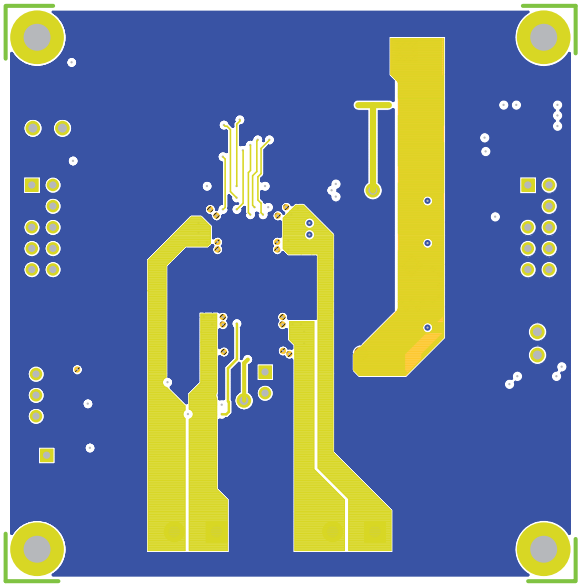

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Figure 12. EVAL6470PD - layout (inner layer 3)

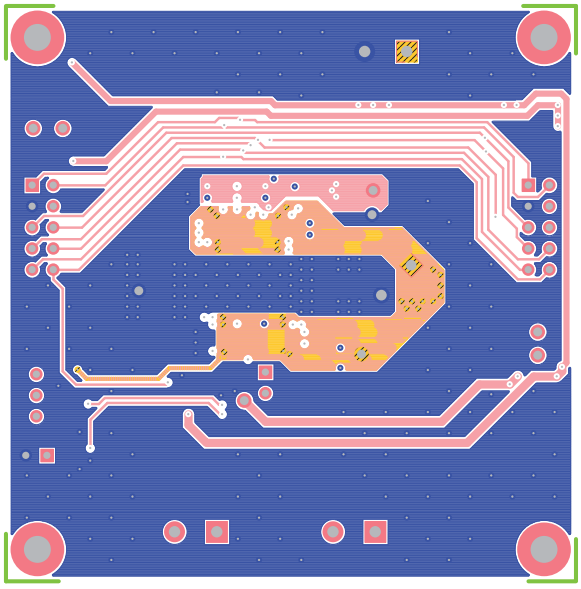

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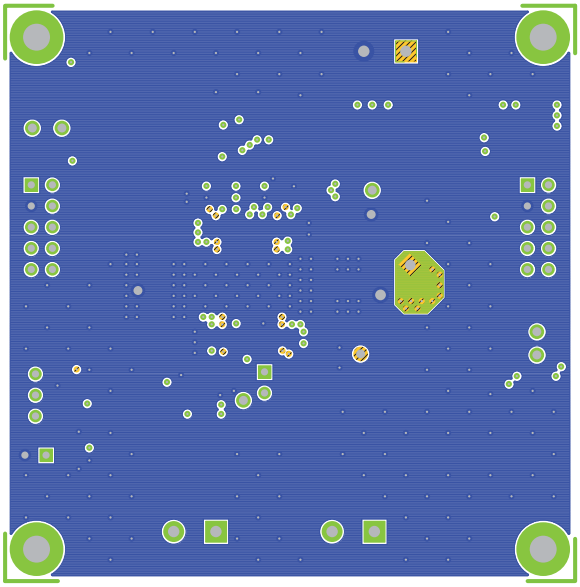
Figure 13. EVAL6470PD - layout (bottom layer



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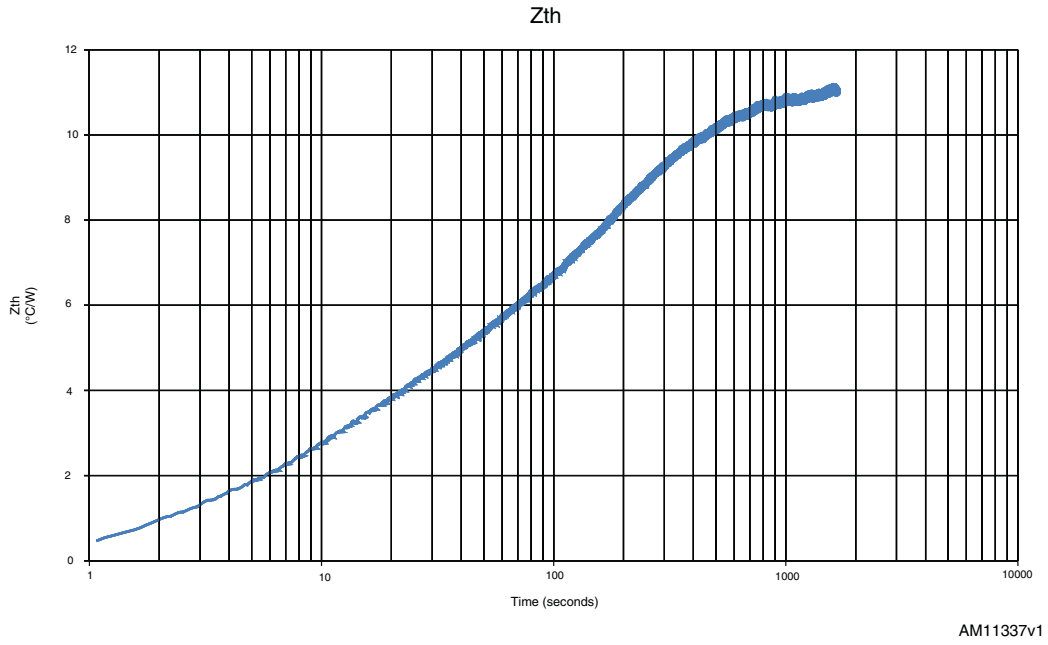
EVAL6470PD - thermal data

Figure 14. EVAL6470PD - thermal impedance graph



1.3 EVAL6472H

Table 11. EVAL6472H - specifications

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 $A_{r.m.s.}$
Logic supply voltage (VREG)	Externally supplied: 3.3 V Internally supplied: 3 V typical
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V Internally supplied: VREG
Low level logic input voltage	0 V
High level logic input voltage	VDD(1)
Operating temperature	-25 to +125 °C
L6472H thermal resistance junction to ambient	21 °C/W typical

1. All logic inputs are 5 V tolerant.

Figure 15. EVAL6472H - jumpers and connectors location

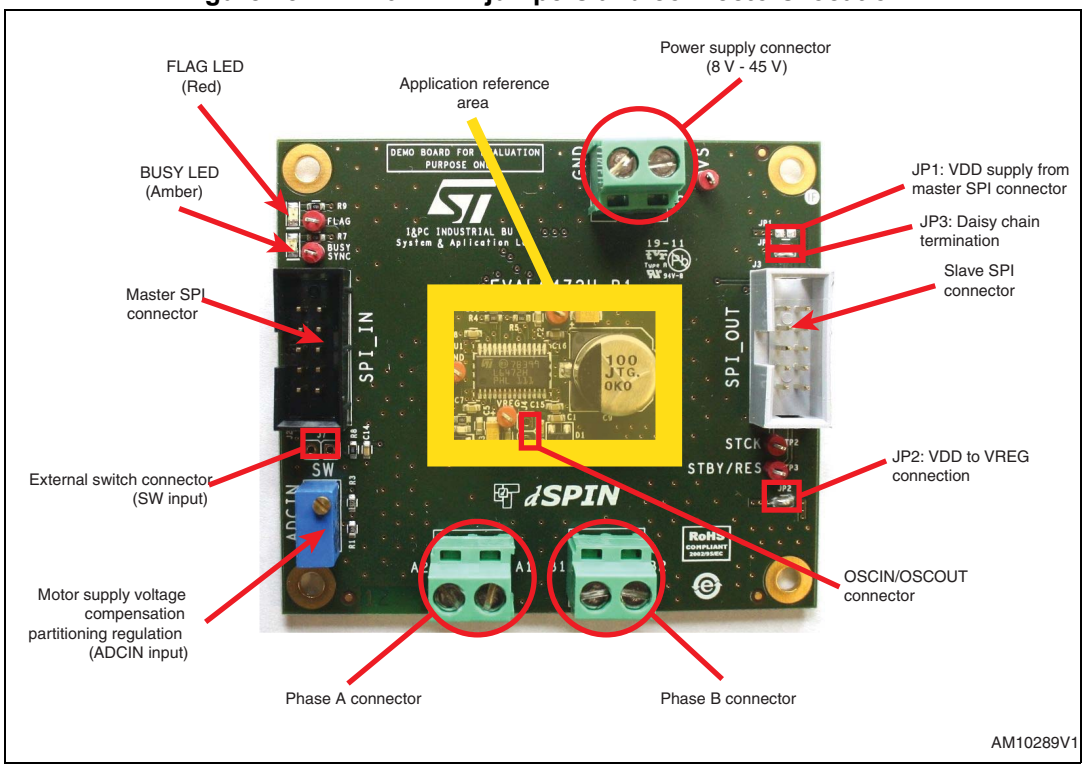


Table 12. EVAL6472H - jumpers and connectors description

Name	Type	Function
M1	Power supply	Motor supply voltage
M2	Power output	Bridge A outputs
M3	Power output	Bridge B outputs
CN1	SPI connector	Master SPI
CN2	SPI connector	Slave SPI
CN3	NM connector	OSCIN and OSCOUT pins
CN4	NM connector	External switch input
TP1 (VS)	Test point	Motor supply voltage test point
TP2 (VDD)	Test point	Logic interface supply voltage test point
TP3 (VREG)	Test point	Logic supply voltage/L6470 internal regulator test point
TP5 (GND)	Test point	Ground test point
TP6 (GND)	Test point	Ground test point
TP8 (STCK)	Test point	Step-clock input test point
TP9 (STBY/RES)	Test point	Standby/reset input test point
TP10 (FLAG)	Test point	FLAG output test point
TP11 (BUSY/SYNC)	Test point	BUSY/SYNC output test point

Table 13. EVAL6472H - master SPI connector pinout (J10)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to L6472 SDO output through daisy chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6472 SDI input)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

Table 14. EVAL6472H - slave SPI connector pinout (J11)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to pin 5 of J10)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6472 SDO output)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

Figure 16. EVAL6472H - schematic

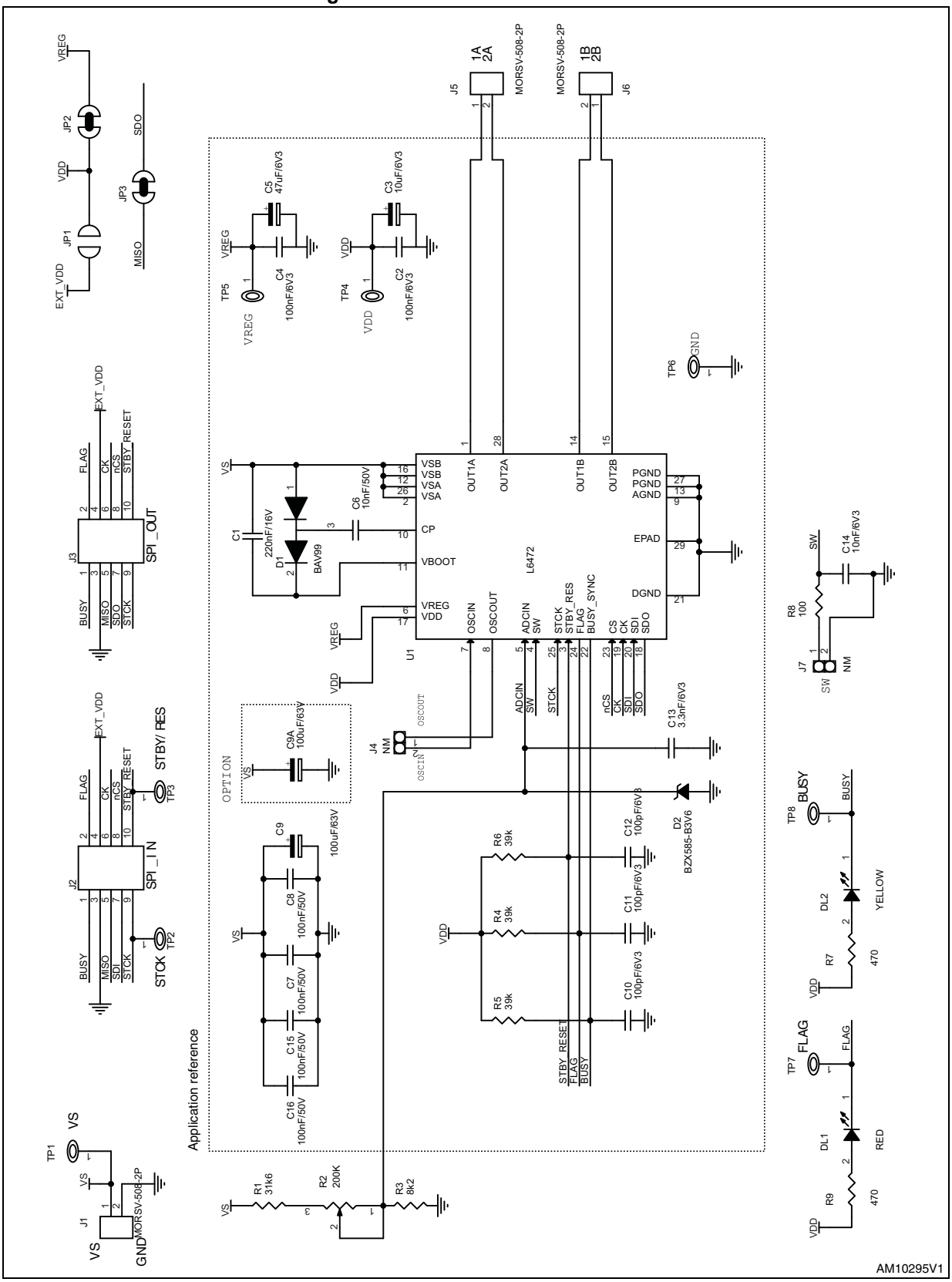


Table 15. EVAL6472H - bill of material

Index	Quantity	Reference	Value	Package
1	1	C1	220 nF/16 V	CAPC-0603
2	2	C2, C4	100 nF/6.3 V	CAPC-0603
3	1	C3	10 µF/6.3 V	CAPC-3216
4	1	C5	47 µF/6.3 V	CAPC-3216
5	1	C6	10 nF/50 V	CAPC-0603
6	4	C7, C8, C15, C16	100 nF/50 V	CAPC-0603
7	1	C9A	100 µF/6.3 V (option)	CAPE-R10HXX-P5
8	1	C9	100 µF/6.3 V	CAPES-R10HXX
9	3	C10, C11, C12	100 pF/6.3 V	CAPC-0603
10	1	C13	3.3 nF/6.3 V	CAPC-0603
11	1	C14	10 nF/6.3 V	CAPC-0603
12	1	DL1	LED diode (red)	LEDC-0805
13	1	DL2	LED diode (amber)	LEDC-0805
14	1	D1	BAV99	SOT23
15	1	D2	BZX585-B3V6	SOD323
16	1	JP1	Jumper - open	JP2SO
17	2	JP2, JP3	Jumper - closed	JP2SO
18	3	J1, J5, J6	Screw connector 2 poles	MORSV-508-2P
19	2	J2,J3	Pol. IDC male header vertical 10 poles	CON-FLAT-5X2-180M
20	2	J4, J7	NM	STRIP254P-M-2
21	1	R1	31.6 kΩ	RESC-0603
22	1	R2	200 kΩ	TRIMM-100X50X110-64W
23	1	R3	8.2 kΩ	RESC-0603
24	3	R4, R5, R6	39 kΩ	RESC-0603
25	2	R7, R9	470 Ω	RESC-0603
26	1	R8	100 Ω	RESC-0603
27	7	TP1, TP2, TP3, TP4, TP5, TP7, TP8	TPTH-ring-1 mm red	TH
28	1	TP6	TPTH-ring-1 mm black	TH
29	1	U1	L6472	HTSSOP28

Figure 17. EVAL6472H - layout (top layer)

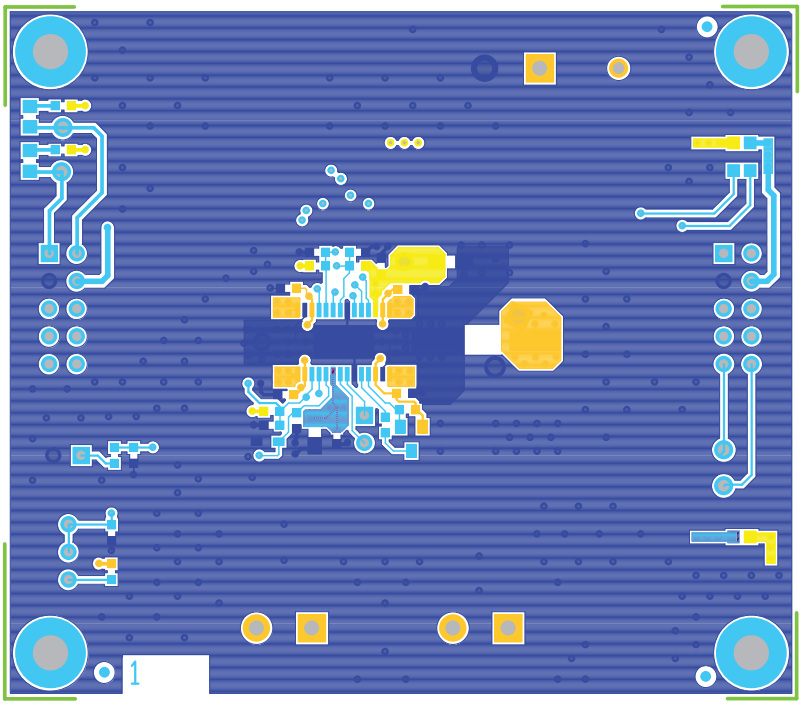


Figure 18. EVAL6472H - layout (inner layer2)

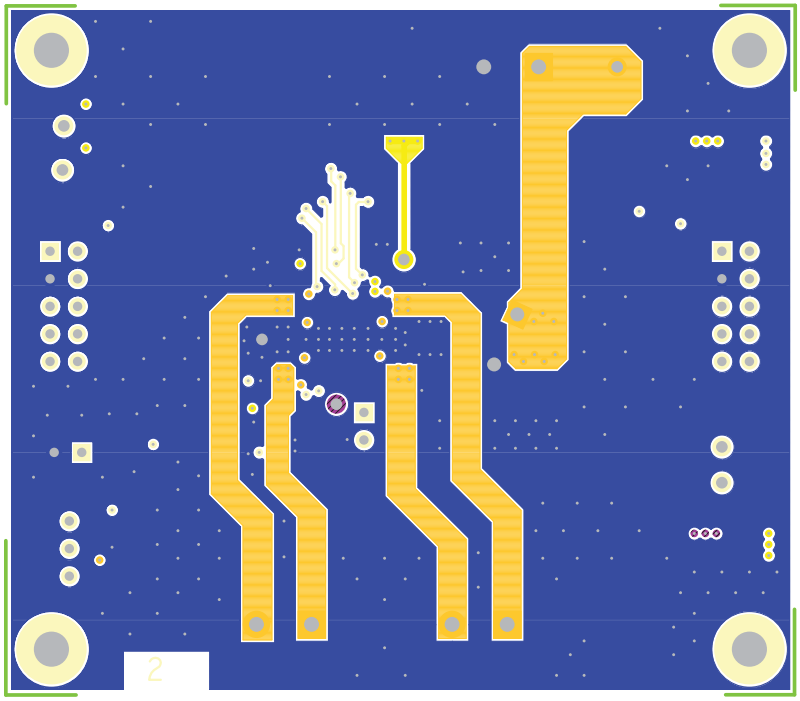


Figure 19. EVAL6472H - layout (inner layer3)

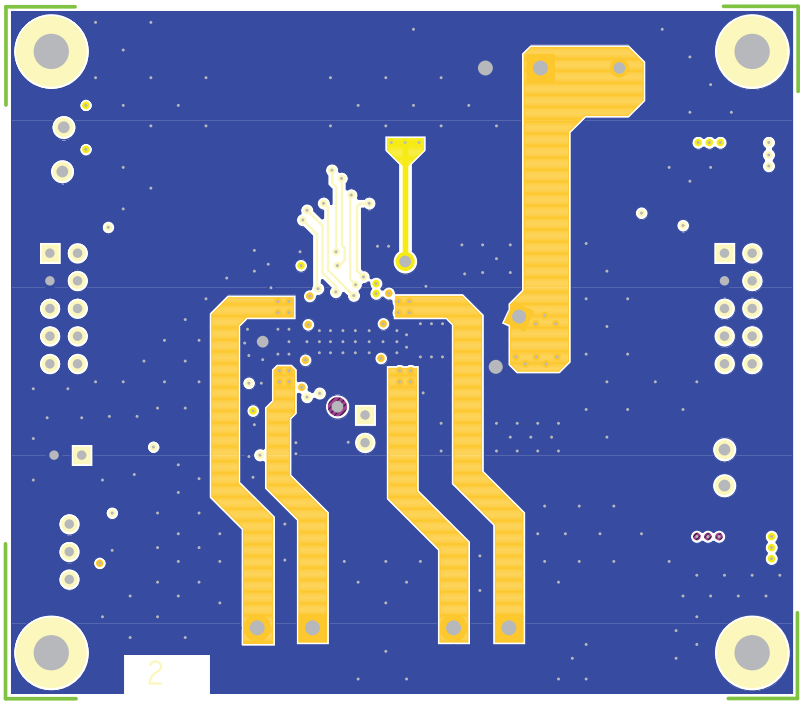


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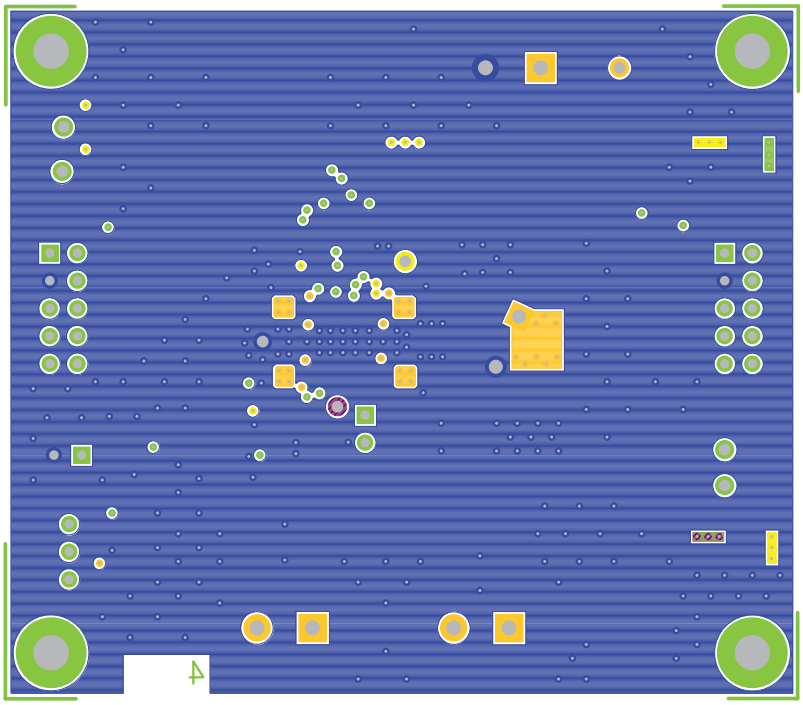
Figure 20. EVAL6472H - layout (bottom layer3)



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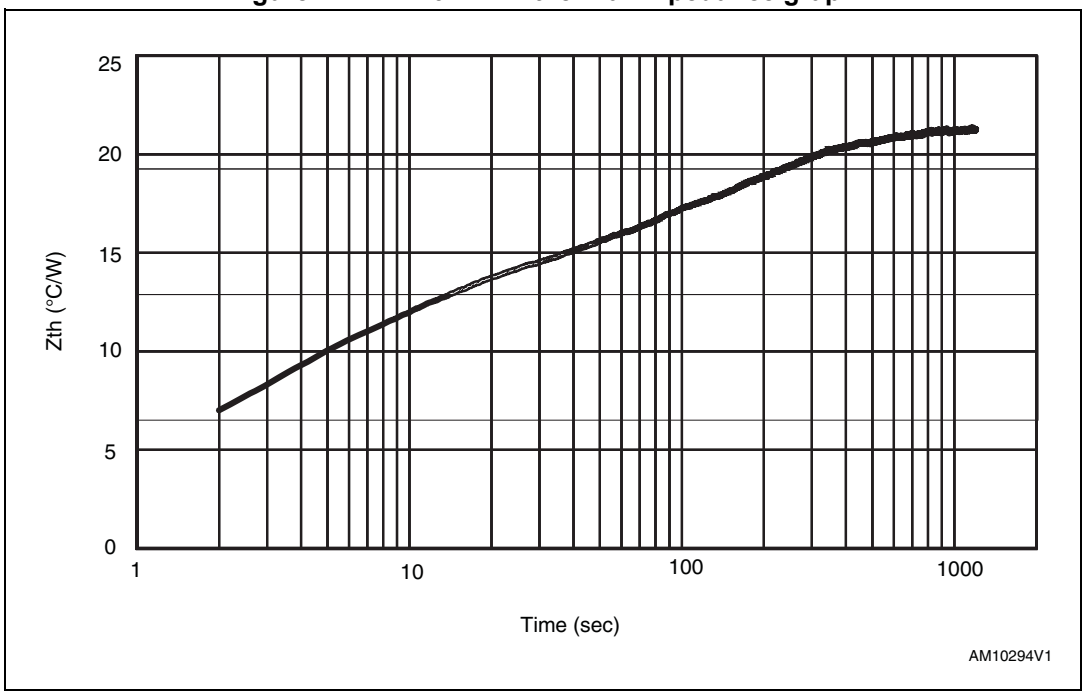
EVAL6472H - thermal data

Figure 21. EVAL6472H - thermal impedance graph



1.4 EVAL6472PD

Table 16. EVAL6472PD - specifications

Parameter	Value
Supply voltage (VS)	8 to 45 V
Maximum output current (each phase)	3 $A_{r.m.s.}$
Logic supply voltage (VREG)	Externally supplied: 3.3 V Internally supplied: 3 V typical
Logic interface voltage (VDD)	Externally supplied: 3.3 V or 5 V Internally supplied: VREG
Low level logic input voltage	0 V
High level logic input voltage	VDD(1)
Operating temperature	-25 to +125 °C
L6472PD thermal resistance junction to ambient	12 °C/W typical

1. All logic inputs are 5 V tolerant.

Figure 22. EVAL6472PD - jumper and connector location

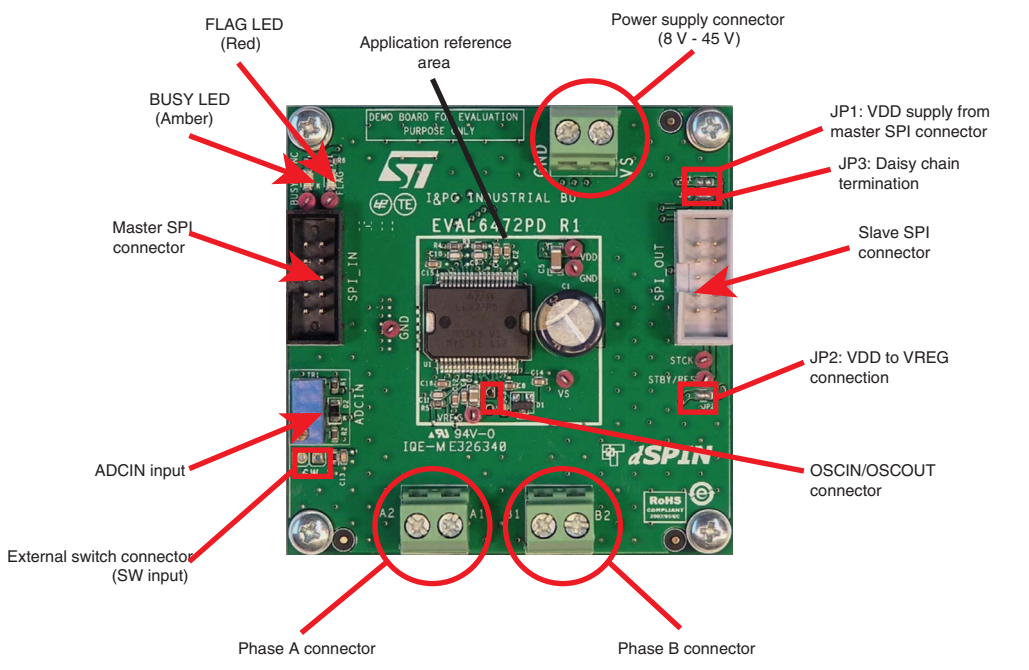


Table 17. EVAL6472PD - jumper and connector description

Name	Type	Function
M1	Power supply	Motor supply voltage
M2	Power output	Bridge A outputs
M3	Power output	Bridge B outputs
CN1	SPI connector	Master SPI
CN2	SPI connector	Slave SPI
CN3	NM connector	OSCIN and OSCOUT pins
CN4	NM connector	External switch input
TP1 (VS)	Test point	Motor supply voltage test point
TP2 (VDD)	Test point	Logic interface supply voltage test point
TP3 (VREG)	Test point	Logic supply voltage/L6472 internal regulator test point
TP5 (GND)	Test point	Ground test point
TP6 (GND)	Test point	Ground test point
TP8 (STCK)	Test point	Step-clock input test point
TP9 (STBY/RES)	Test point	Standby/reset input test point
TP10 (FLAG)	Test point	FLAG output test point
TP11 (BUSY/SYNC)	Test point	BUSY/SYNC output test point

Table 18. EVAL6472PD - master SPI connector pinout (J10)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to L6472 SDO output through daisy chain termination jumper JP2)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6472 SDI input)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

Table 19. EVAL6472PD - slave SPI connector pinout (J11)

Pin number	Type	Description
1	Open drain output	L6472 BUSY output
2	Open drain output	L6472 FLAG output
3	Ground	Ground
4	Supply	EXT_VDD (can be used as external logic power supply)
5	Digital output	SPI master IN slave OUT signal (connected to pin 5 of J10)
6	Digital input	SPI serial clock signal (connected to L6472 CK input)
7	Digital input	SPI master OUT slave IN signal (connected to L6472 SDO output)
8	Digital input	SPI slave select signal (connected to L6472 CS input)
9	Digital input	L6472 step-clock input
10	Digital input	L6472 standby/reset input

Figure 23. EVAL6472PD - schematic

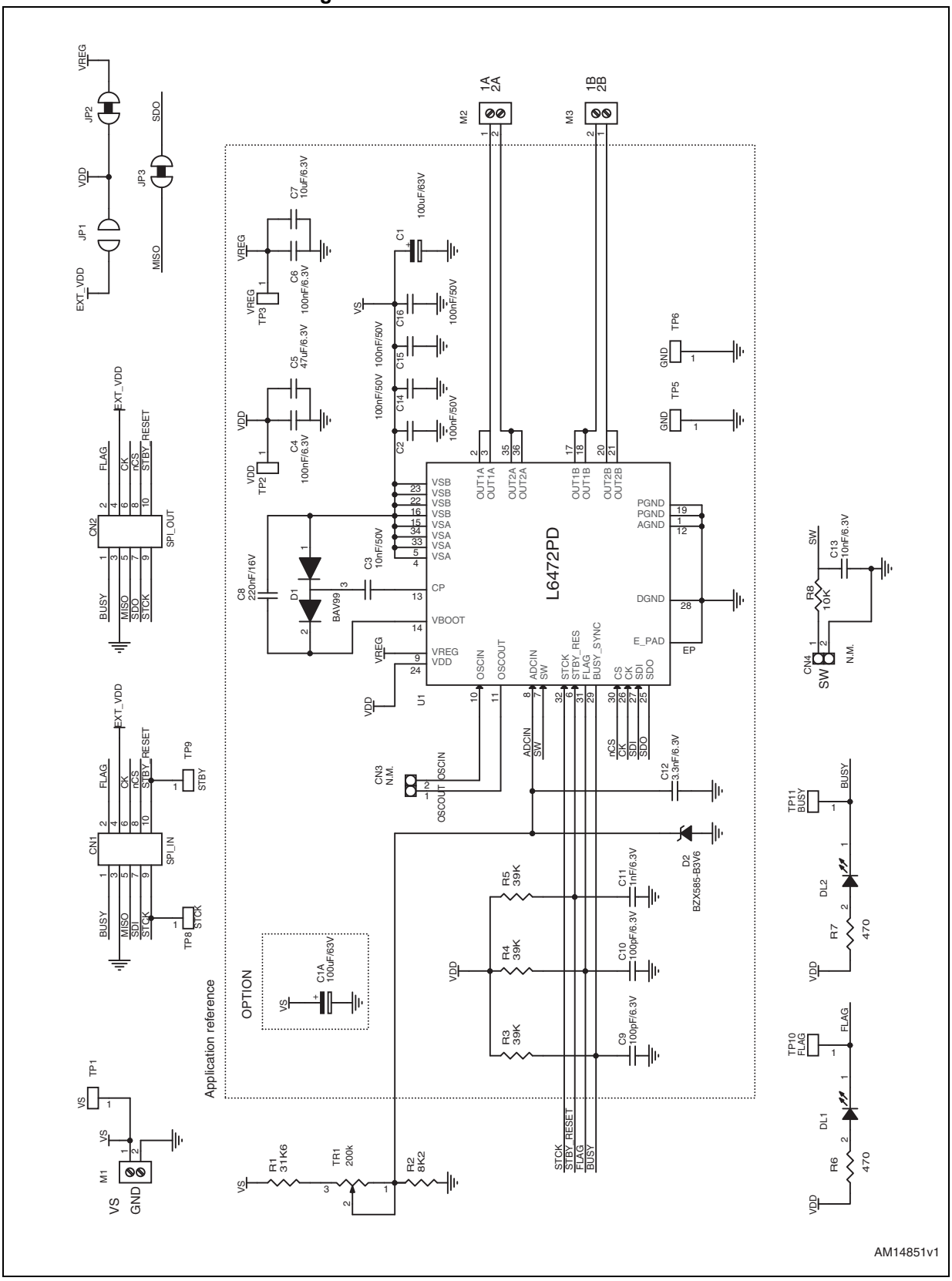


Table 20. EVAL6472PD - bill of material

Index	Quantity	Reference	Value	Package
1	1	CN1	Pol. IDC male header vertical 10 poles (black)	CON-FLAT-5X2-180M
2	1	CN2	Pol. IDC male header vertical 10 poles (gray)	CON-FLAT-5X2-180M
3	2	CN3, CN4	N.M	STRIP254P-M-2
4	1	C1A	100 µF/63 V	CAPE-R10HXX-P5
5	1	C1	100 µF/63 V	CAPES-R10HXX
6	4	C2, C14, C15, C16	100 nF/50 V	CAPC-0603
7	1	C3	10 nF/50 V	CAPC-0603
8	2	C4, C6	100 nF/6.3 V	CAPC-0603
9	1	C5	47 µF/6.3 V	CAPC-1206
10	1	C7	10 µF/6.3 V	CAPC-0805
11	1	C8	220 nF/16 V	CAPC-0603
12	2	C9, C10	100 pF/6.3 V	CAPC-0603
13	1	C11	1 nF/6.3 V	CAPC-0603
14	1	C12	3.3 nF/6.3 V	CAPC-0603
15	1	C13	10 nF/6.3 V	CAPC-0603
16	1	JP1	LED red	LEDC-0805
17	1	DL2	LED amber	LEDC-0805
18	1	D1	BAV99	SOT23
19	1	D2	BZX585-B3V6	SOD523
20	1	JP1	Jumper OPEN	JP2SO
21	2	JP2,JP3	Jumper CLOSED	JP2SO
22	3	M1, M2, M3	Screw connector 2 poles	MORSV-508-2P
23	1	R1	31.6 kΩ	RESC-0603
24	1	R2	8.2 kΩ	RESC-0603
25	3	R3, R4, R5	39 kΩ	RESC-0603
26	2	R6, R7	470 Ω	RESC-0603
27	1	R8	10 kΩ	RESC-0603
28	7	TP1, TP2, TP3, TP8, TP9, TP10, TP11	TPTH-ring-1 mm (red)	TH
29	2	TP5, TP6	TPTH-ring-1 mm (black)	TH
30	1	TR1	200 kΩ	TRIMM-100x50x110-64W
31	1	U1	L6472	PowerSO36

Figure 24. EVAL6472PD - layout (inner layer2)

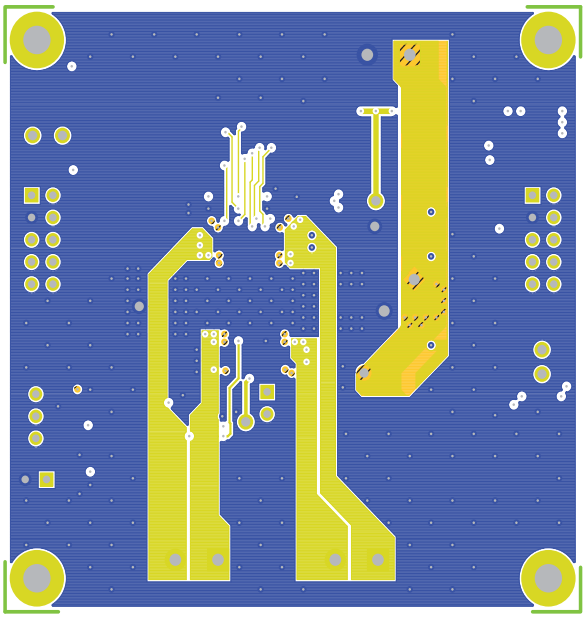


Figure 25. EVAL6472PD - layout (inner layer3)

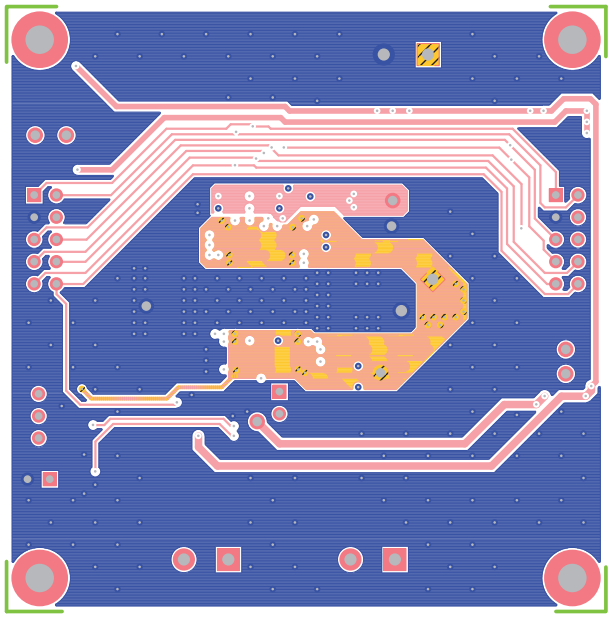
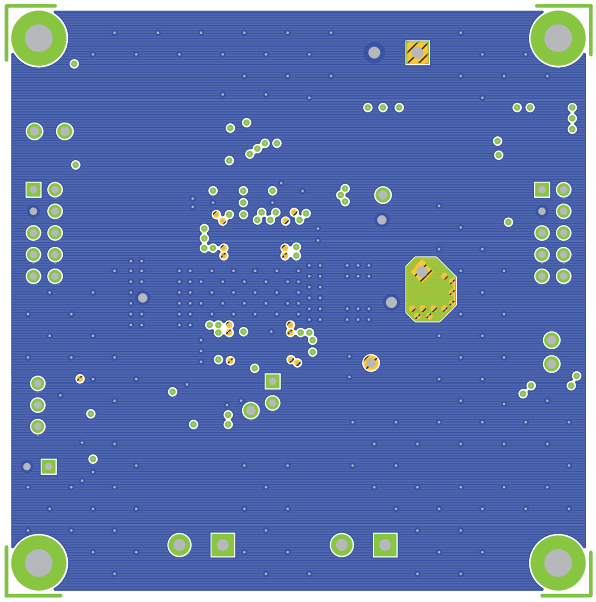
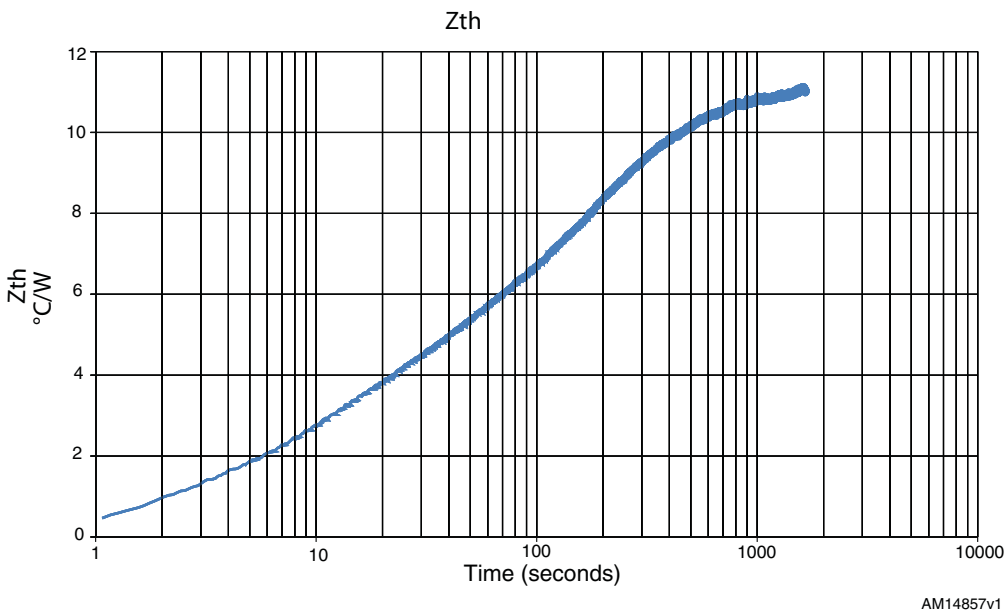


Figure 26. EVAL6472PD - layout (bottom layer3)



EVAL6472PD - thermal data

Figure 27. EVAL6472PD - thermal impedance graph



2 Evaluation environment setup

The evaluation environment is composed by:

- One or more EVAL6470H\PD or EVAL6472H\PD.
- One STEVAL-PCC009V2 demonstration board.
- A USB cable.
- A stepper motor with a small mechanical load (unloaded stepper motors suffer of strong resonance issues).
- A power supply with an output voltage within the operative range of the evaluation board.
- A Windows® 7 or Windows XP PC with a free USB port.
- The SPINFamily evaluation tool (the last version can be downloaded from the STMicroelectronics® website).

In order to start using the evaluation environment the following steps are required:

1. Install the SPINFamily evaluation tool
2. Start the SPINFamily evaluation tool (by default it is in Start menu > All programs > STMicroelectronics > SPINFamily Evaluation Tool).
3. Select the proper device when requested by the application.
4. Plug the STEVAL-PCC009V2 demonstration board to a free USB port.
5. Wait a few seconds for board initialization.
6. Connect the SPI_IN connector (black) of the demonstration board to the 10-pin connector of the STEVAL-PCC009V2 board using the provided cable.
   For connecting more devices to the same board, please consult the daisy chain connection paragraph (*Section 5: Daisy chaining on page 40*).
7. Power-up the demonstration boards. The FLAG LED should turn on.
8. Click on the button with the USB symbol to connect the STEVAL-PCC009V2 board to the PC and initialize the evaluation environment.
   The application automatically identifies the number of demonstration boards connected.
9. The evaluation environment is ready.

Before start working with the demonstration board, the device must be configured according to the indications in *Section 3: Device configuration*.

Warning: Important - the device configuration is mandatory. The default configuration is not operative.

---

3 Device configuration

This section offers an overview of the basic configuration steps which are required for make the demonstration board operative.

Warning: **Important - the device configuration is mandatory. The default configuration is not operative.**

Important - before changing the device configuration verify that the device is in high impedance status (power stage is disabled).

3.1 Voltage mode driving (EVAL6470H/PD)

The configuration parameters of the voltage mode driving can be obtained through the BEMF compensation tool embedded into the SPINFamily software.

A wrong setup of these parameters could cause several issues, in particular:

- The phase current decreases with the speed and the motor will stall.
- The wrong voltage is applied to the motor and the system is very noisy.
- The phase current reaches the overcurrent limit.

The BEMF compensation form uses the application parameters as inputs in order to evaluate the proper device setup.

The required inputs are:

- Supply voltage.
- Target phase current (r.m.s. value) at different motion conditions (acceleration, deceleration, constant speed and holding).
- Target operating speed (maximum speed).
- Motor characteristics.

The motor characteristics are: electrical constant (Ke), phase inductance and resistance. The inductance and the resistance of the phase are given in the motor datasheet. The Ke is rarely given in the specification and must be measured.

In the help section of the SPINFamily software a step by step procedure is explained. The same procedure can also be found in the application note “AN4144: Voltage mode control operation and parameter optimization” on www.st.com.

Click on the “evaluate” button to get the suggested setup for the voltage mode driving. Then click on “write” button to copy the data in the registers of the device.

3.2 Advanced current control (EVAL6472H/PD)

The following configuration gives good results with most of motors:

- Minimum ON time = 4 µs.
- Minimum OFF time = 21 µs.
- Max. fast decay = 10 µs.
- Max. fast decay at step change = 16 µs.
- Target switching time = 48 µs.
- Predictive current control enabled.

The impact of the timing parameters are explained in the application note “AN4158: Peak current control with automatic decay adjustment and predictive current control: basics and setup”.

The target phase current is set through the TVAL registers. The TVAL determinates the current corresponding to the peak of the sine wave (microstepping operation).

3.3 Overcurrent and stall detection thresholds

The overcurrent protection and the stall detection (EVAL6470H\PD only) are implemented measuring the current flowing into each integrated MOSFET.

The overcurrent protection threshold should be set just above the current rating of the motor:

$$I_{OCDth} > I_{max,r.m.s.} \times \sqrt{2}$$

For example: if the maximum phase current of the motor is 2 $A_{r.m.s.}$, the overcurrent protection should be set to about 3 A.

Warning: Important - it is strongly discouraged to disable the overcurrent shutdown. It may result in critical failures.

The stall detection threshold should be just above the operating peak current of the application. During the preliminary stages of evaluation, it can be set to the maximum value.

3.4 Speed profile

The max. speed parameter is the maximum speed the motor will run. By default, it is about 1000 step/s. That means, if you send a command to run at 2000 step/s, the motor speed is limited at 1000 step/s.

This is an important safety feature in the final application, but not necessarily useful to evaluate the device performances. Setting the parameter to high values (e.g. 6000 step/s) allows evaluating the maximum speed which can be achieved by the application under test through the speed tracking command (Run), but it probably limits the possibility to use positioning commands (Move, GoTo, etc.).

The Full-step speed parameter indicates the speed at which the system switches from microstepping to full step operation.

In voltage mode driving devices (EVAL6470H\PD), it is always recommended to operate in microstepping and not to switch to full step. Hence, this parameter should be greater than the maximum speed.

4 How to change the supply configuration of the board

The configuration of the supply voltages can be changed through the jumpers from J1 to J6 as listed in *Table 21*.

Table 21. Device supply configurations

Configuration	JP1	JP2	Logic levels	Notes
Logic supplied by the integrated voltage regulator and VDD shorted to VREG.	Open	Closed	3.3 V logic compliant.	Default.
Logic supplied by the integrated voltage regulator and VDD floating.	Open	Open	According to VDD voltage.	The VDD must be supplied through the respective test point.
Logic supplied by the integrated voltage regulator and VDD supplied through the SPI connector.	Closed	Open	According to VDD voltage.	The VDD must be supplied through the SPI connector.
Logic and VDD supplied through the SPI connector.	Closed	Closed	3.3 V logic compliant.	The supply voltage from the SPI connector must be 3.3 V.

When VREG pin is supplied through an external voltage source, particular care must be taken in order to avoid that VS voltage falls below the VREG one (e.g. VS is floating and VREG is supplied). In this case the internal ESD diode is turned on and the device could be damaged.

Adding a low drop diode between VREG and VS protects the internal ESD diode from this event.

5 Daisy chaining

More demonstration boards can be connected in daisy chain mode.

To drive two or more boards in daisy chain configuration:

1. Connect the STEVAL-PCC009V2 board 10-pin connector to the SPI_IN connector of the first demonstration board through the 10-pole flat cable.
2. Open the termination jumper (see *Section 1.1: EVAL6470H on page 5*, *Section 1.2: EVAL6470PD on page 12*, *Section 1.3: EVAL6472H on page 21* and *Section 1.4: EVAL6472PD on page 28*).
3. Connect the SPI_OUT connector of the first demonstration board to the SPI_IN of the next one through the 10-pole flat cable.
4. Repeat point 2 and 3 for all the others board of the chain but the last one.
5. Check the termination jumpers of the demonstration boards: all the jumpers but the last one should be opened.

Note: Increasing the number of devices connected in chain could degrade SPI communication performances. If communication issues occur, try reducing the SPI clock speed.

6 Revision history

Table 22. Document revision history

Date	Revision	Changes
15-Nov-2013	1	Initial release.
16-Apr-2015	2	Updated *Section : Introduction on page 1* (replaced “dSPIN™ family devices” and “dSPIN™” by “L6470 and L6472 devices”). Updated *Section : Introduction on page 1* and *Section 2: Evaluation environment setup on page 35* (replaced “SPIN family evaluation tool” by “SPINFamily evaluation tool”). Removed Figure 3. EVAL6470H - layout (silk screen) from page 10, Figure 11. EVAL6470PD - layout (silk screen) from page 18, Figure 19. EVAL6472H - silkscreen from page 26, and Figure 27. EVAL6472PD - silkscreen from page 34. Updated value in *Table 5: EVAL6470H - bill of material on page 9*, and packages in *Table 10: EVAL6470PD - bill of material on page 17* and *Table 20: EVAL6472PD - bill of material on page 32*. Minor modifications throughout document.

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