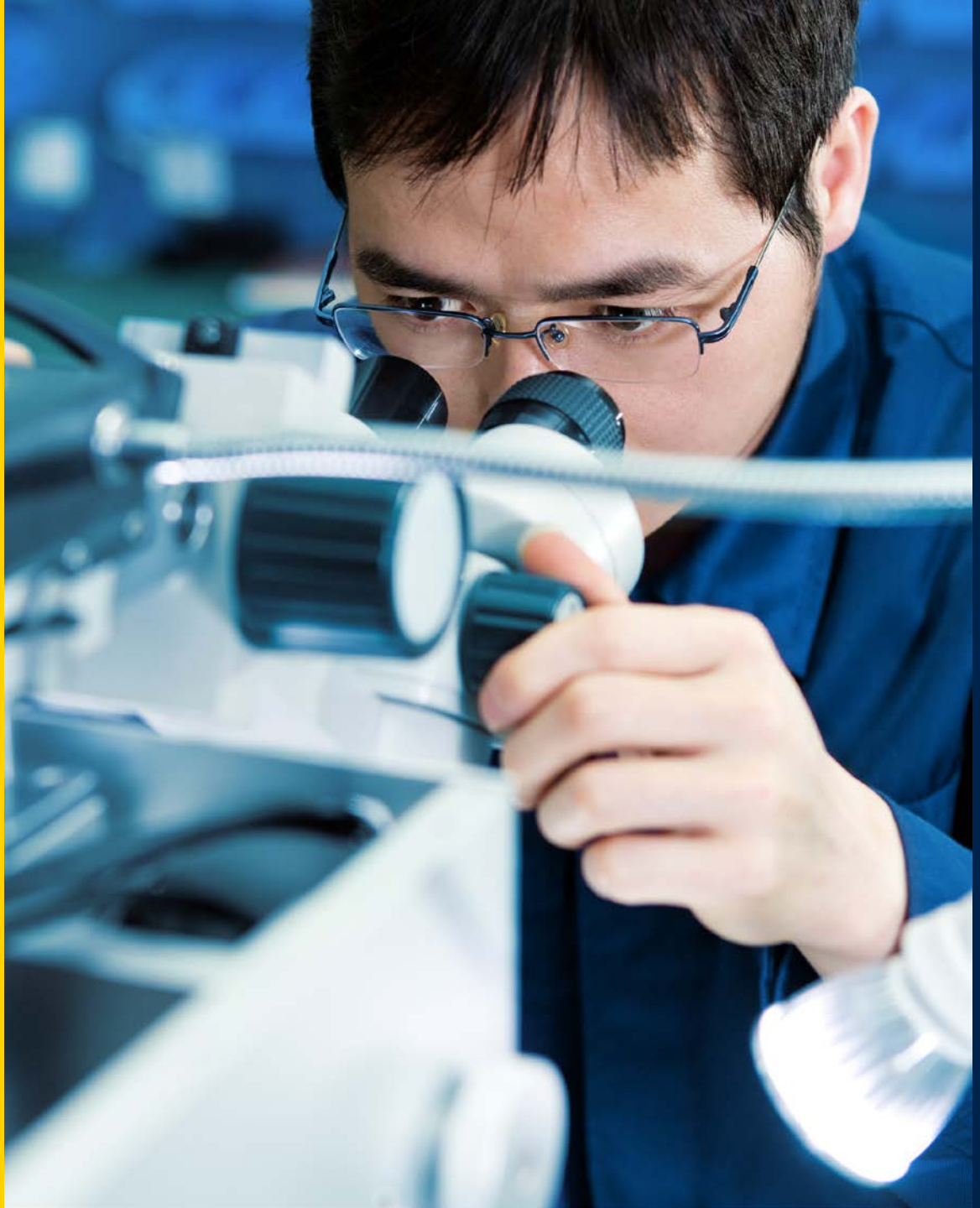


Driving SiC MOSFETs with unipolar gate voltage

Theory and experimental data on 1200 V Gen3

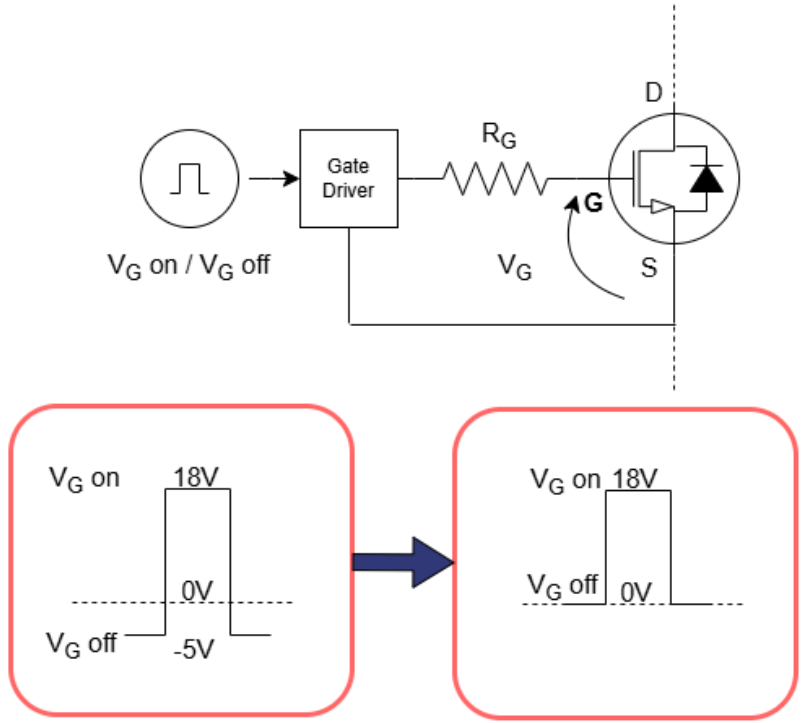
Advancements in SiC MOSFET turn-off driving: From negative bias to 0 V

We test the differences between unipolar (Vgs-on, Vgs-off: 18V, 0V) and bipolar (18V, -5V) gate driving strategies on a SiC MOSFET

SiC MOSFETs are finding increasing application in high power converters due to better electrical, mechanical, and thermal performances than traditional Si MOSFETs and IGBT.

The most common automotive and industrial power converters are based on simple legs that are combined to form more complex topologies. Historically, a negative bias for driving turn-off of SiC MOSFETs was a standard recommendation for hard-switched half-bridge based topologies.

This is manly to avoid the very famous Miller turn-on effect (known also as parasitic turn-on) and any undesired spurious turn-on events.

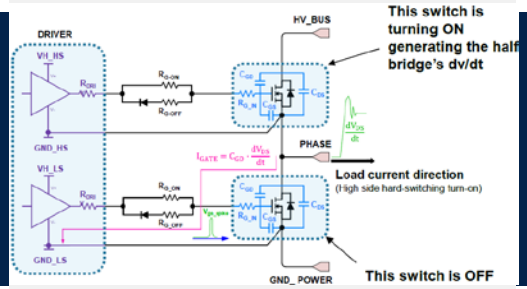


0V turn-off offers design advantages in terms of simplifying the transition from silicon to SiC, and allowing easier driving circuits that can save space in highly space-constrained applications.

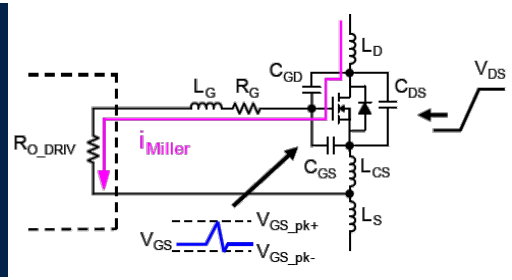
Miller turn-on effect during transitions

In power converters, minimizing the undesired Miller turn-on effect is crucial for enhancing efficiency and reducing power losses

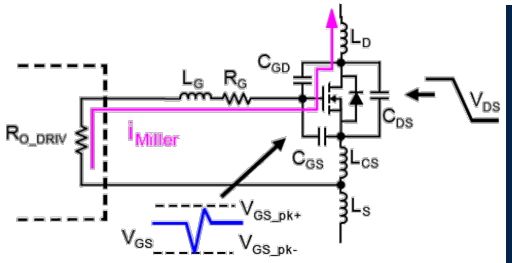
Miller turn-on due to high dv/dt transient in HB topology



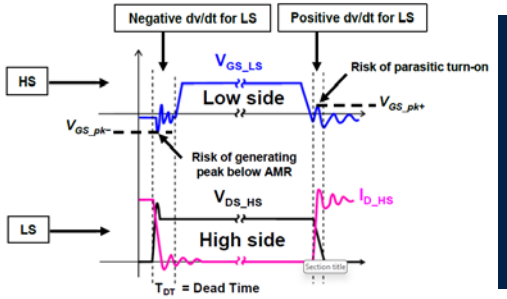
Miller current generation with positive dv/dt



Miller current generation with negative dv/dt



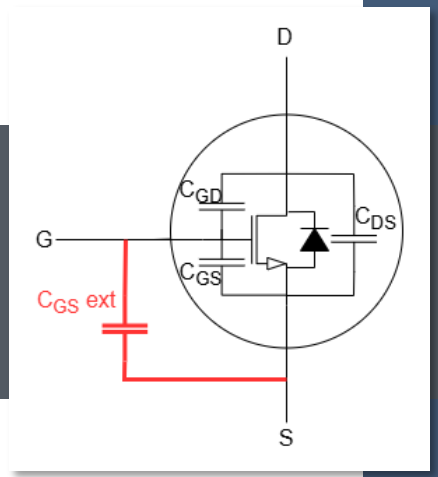
Duality of glitch phenomena



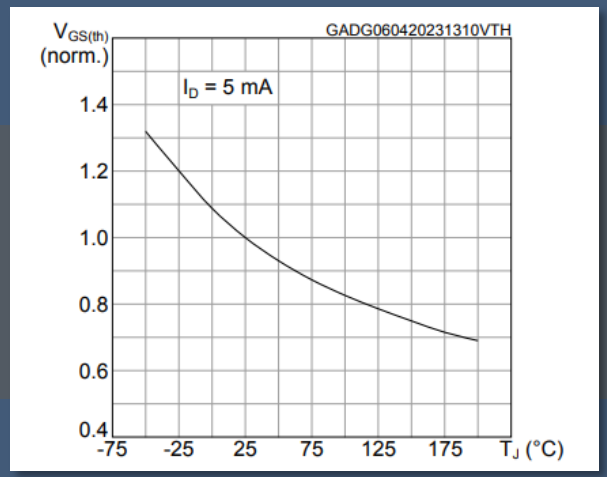
One effective strategy is to use a negative gate-source voltage Vgs-off during turn-off. This approach helps to mitigate the effects of ringing and overshoot, which can otherwise lead to unintended turn-on due to the Miller effect.

K elements in Miller turn on phenomenon

Vgs(th) threshold voltage is the minimum gate-to-source voltage to create a conducting path between MOSFET source & drain terminals



Normalized gate threshold voltage vs. temperature



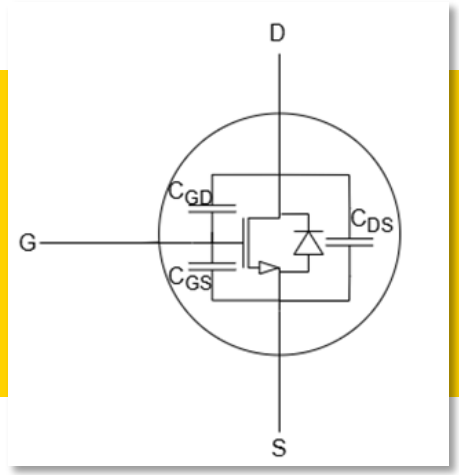
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 5 mA	1.8	3.0	4.2	V

Room temperature testing:
The threshold voltage is tested at room temperature during production to ensure that the devices meet the specified minimum threshold voltage.

Temperature effects:
Vgs(th) tends to decrease at higher temperatures, although this parameter is not typically measured during production. This behavior must be considered in applications where devices operate at elevated temperatures.

Why the capacitance ratio is important

Parasitic capacitance can lead to undesired energy storage and release during switching, causing delays or unwanted oscillations



$$Ratio = \frac{C_{GD}}{C_{GS}} = \frac{Crss}{Ciss - Crss} << 1$$

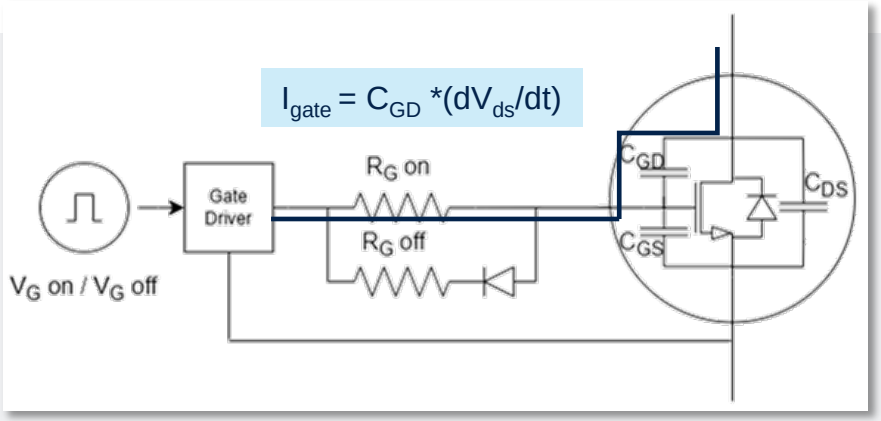
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 800 V, f = 1 MHz, V_{GS} = 0 V	-	1990	-	pF
C_{oss}	Output capacitance		-	102	-	pF
C_{rss}	Reverse transfer capacitance		-	12	-	pF

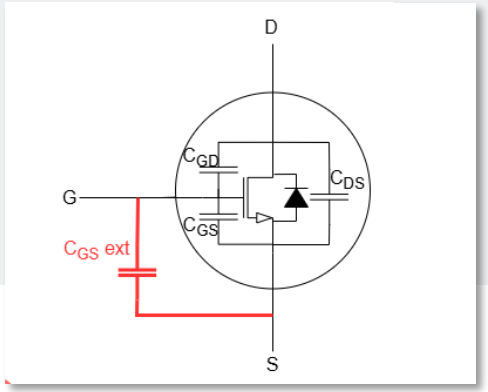
A lower capacitance ratio in a device can reduce susceptibility to the false turn-on phenomenon. This means that the device is less likely to experience unintended turn-on events during switching, which can lead to additional power losses.

To improve device performance and reliability, it is crucial to manage parasitic capacitance carefully. This might involve optimizing the device design, selecting appropriate materials, and using external components to dampen unwanted effects.

Miller turn-on mitigation in MOSFETs

The designer can find a list of the most important key elements which allows optimizing performance



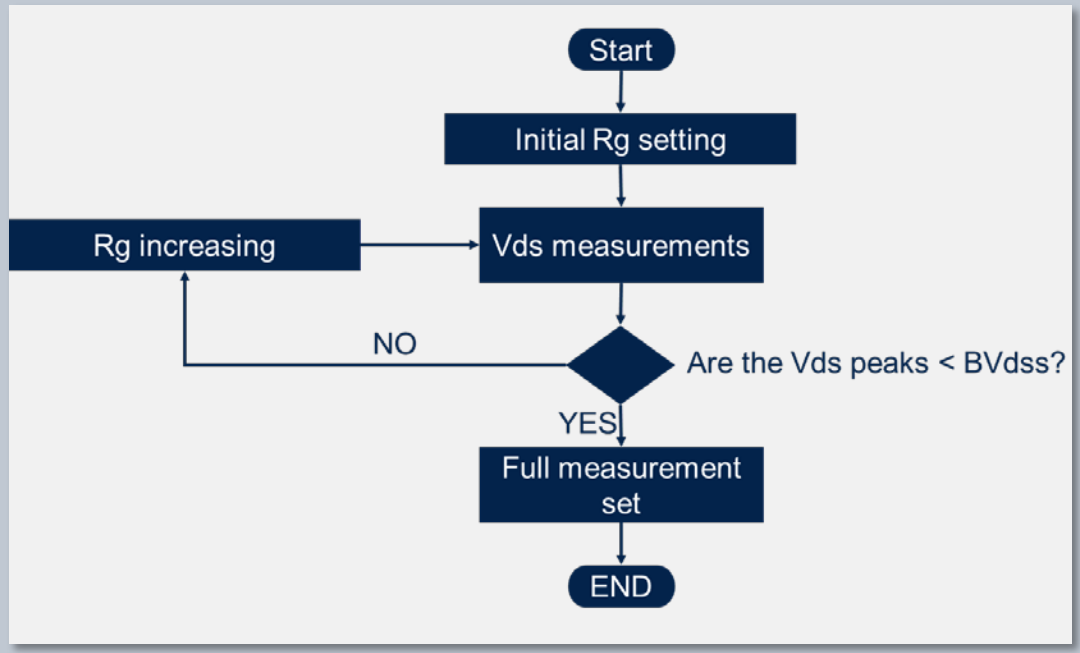


- **Gate resistance**: select a gate resistance such that the ratio is Rgon/Rgoff ≥ 1.5. This ensures faster turn-off compared to turn-on, reducing the risk of Miller turn-on.
- **External capacitance (**Cgs-ext**)**: add an external capacitance between the gate and source. A few nF can be enough to improve performance and reduce Vgs spikes.
- **Active Miller clamp**: use a gate driver with an active Miller clamp to prevent the gate voltage from rising due to the Miller effect during switching.
- **PCB layout**: optimize the PCB layout to minimize stray inductances, which can exacerbate the Miller effect.
- **Miller capacitance ratio**: choose MOSFETs with a gate-drain to gate-source capacitance ratio (Cgd/Cgs) as low as possible (much less than 1). This helps reduce the Miller effect.
- **Threshold voltage** (Vgs(th)): threshold voltage is key and the worst-case condition must be considered for appropriate design robustness.
- **Driving network**: optimize the network according to the design boundary conditions.

Measurement results V_{gsoff} = 0 V

Driving Rg choice

Choosing the right gate resistance involves a tradeoff between switching speed and safe operation (Vds spike < Vdss)

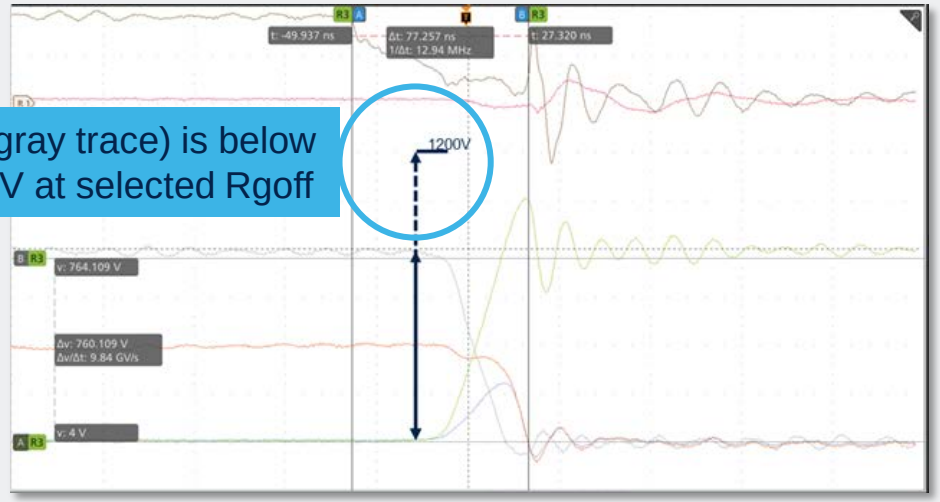


- **For Rgoff**, use the lowest value that ensures the Absolute Maximum Rating is not exceeded (with appropriate margin) at Vgs-off = -5V. Then, for 0V OFF, you can simply reduce it to match the speed you would obtains with a negative driving voltage.
- The same sequence on the left can then be used to choose the **proper Rgon** to mitigate the Vds spike across the complementary switch in the half bridge. In this case, you don't need to tune the Rgon value when moving to unipolar driving.
- Once identified the Rgon and Rgoff which can optimize losses and mitigate the voltage spikes, measurements will be performed at room and high temperatures, to check the behavior.
- Configurations with and without the Active Miller clamp were considered.

An example of how to select Rg

In these comparisons, a typical and safe switching speed is applied, and the same speed is imposed in all the configurations tested

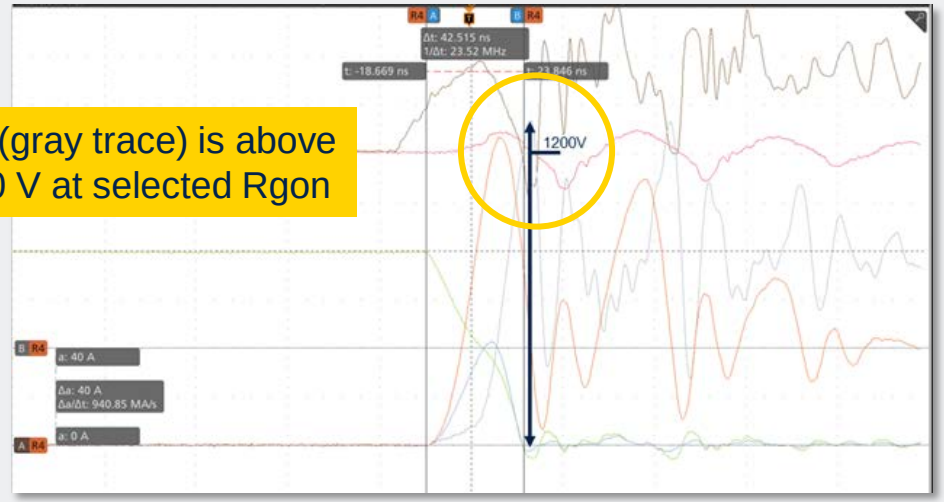
Turn off



Vds (gray trace) is below 1200 V at selected Rgoff

Selected Rgoff is OK

Turn on

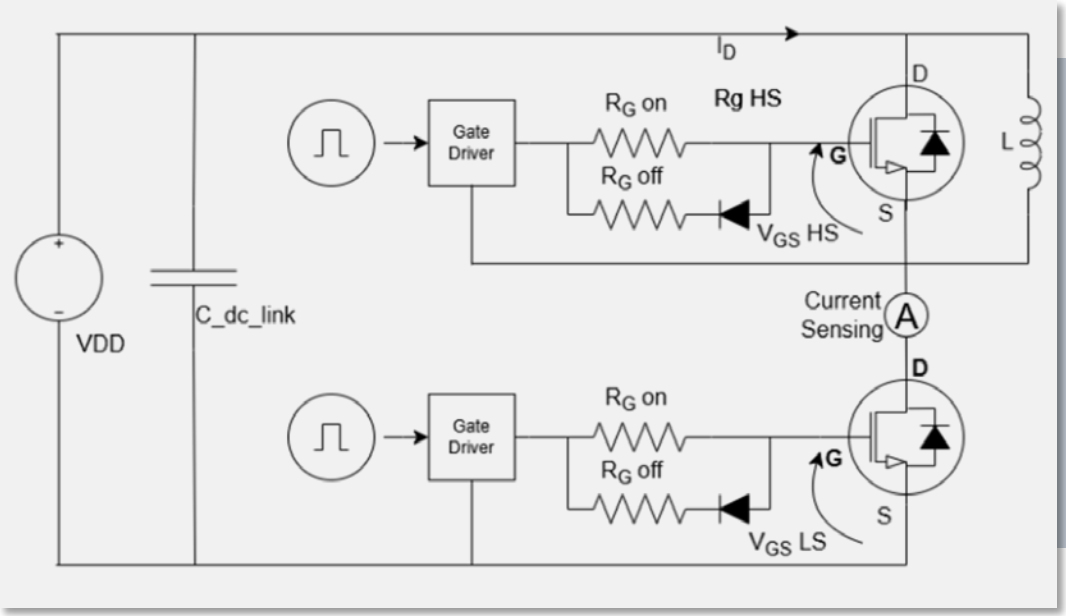


Vds (gray trace) is above 1200 V at selected Rgon

Need to increase Rgon and test again

Double pulse test schematic and test conditions

The comparison represents the E_{sw} vs I_D using a 1200 V device with 27 mΩ_{typ} Gen3 SiC MOSFET as test vehicle

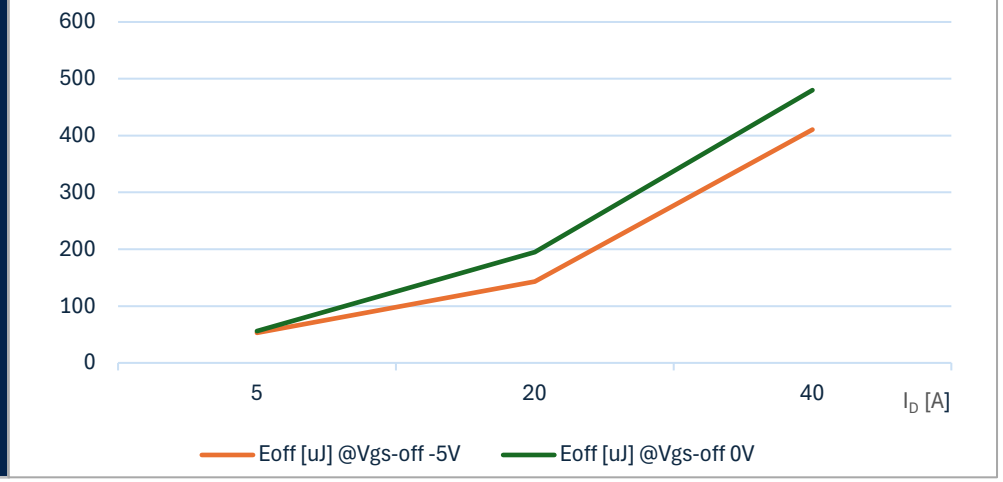


Test conditions:

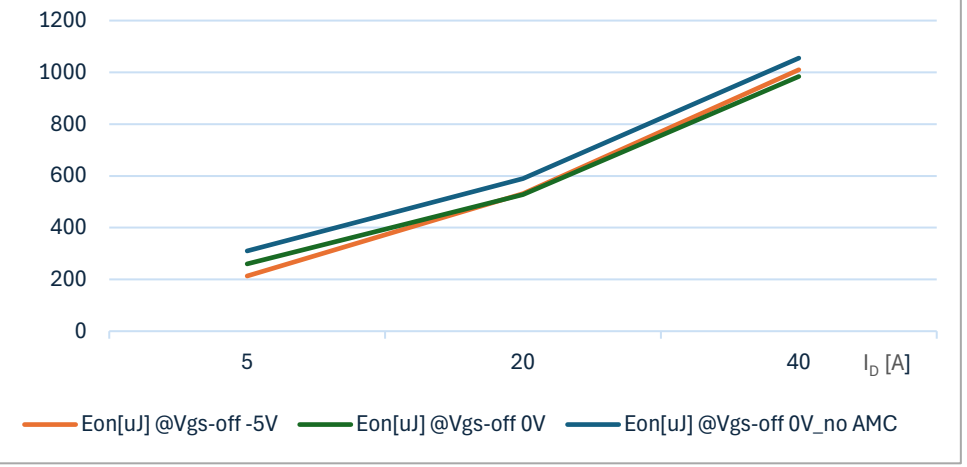
- T_J = 150°C
- Turn-on speed: di/dt_{ON} ≈ 2 A/ns
- Turn-off speed: dv/dt_{OFF} ≈ 35 V/ns
- V_{DD} ≈ 800 V
- 0 Vgs-off with and without Active Miller clamp vs negative driving voltage as PoR
- V_{th} = 2.8 V

Energy comparison bipolar vs unipolar driving

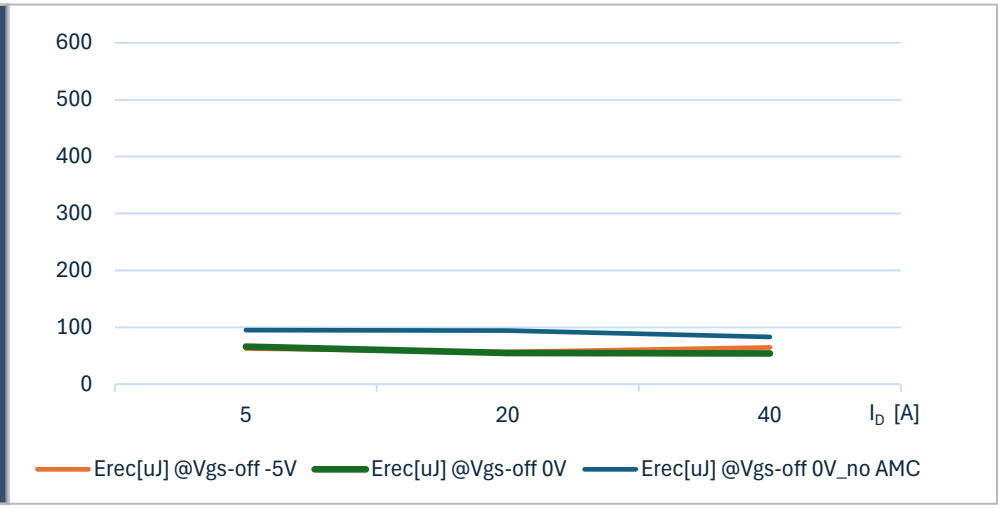
E^*_{OFF} [µJ] @150°C



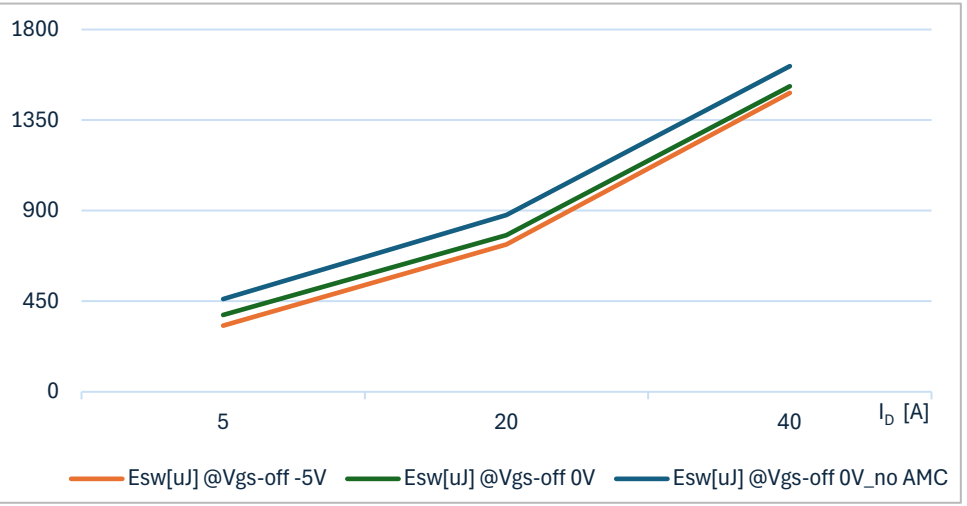
E_{ON} [µJ] @150°C



E_{REC} [µJ] @150°C



E_{SW} [µJ] @150°C

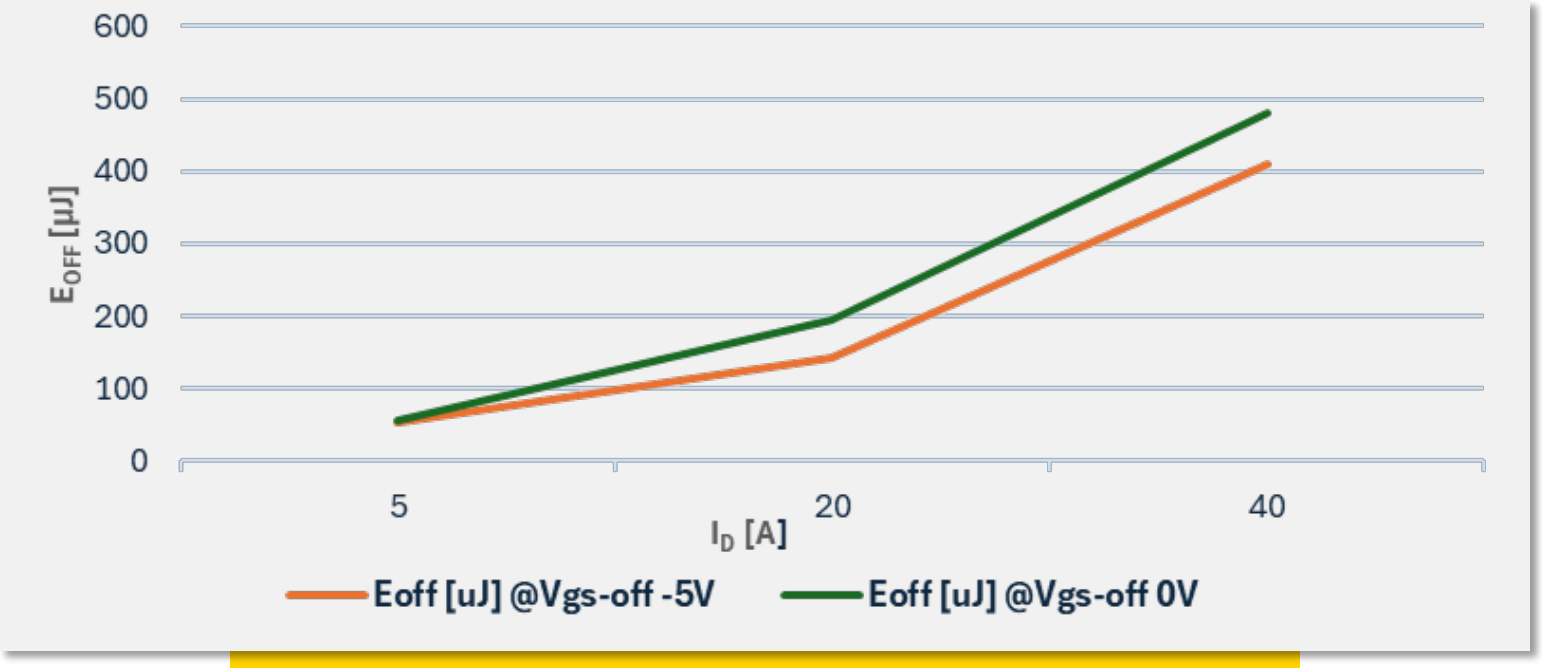


**Eoff is not influenced by Active Miller clamp*

Energy comparison bipolar vs unipolar driving

Eoff (turn-off speed: dv/dt_{OFF} ≈ 35 V/ns)

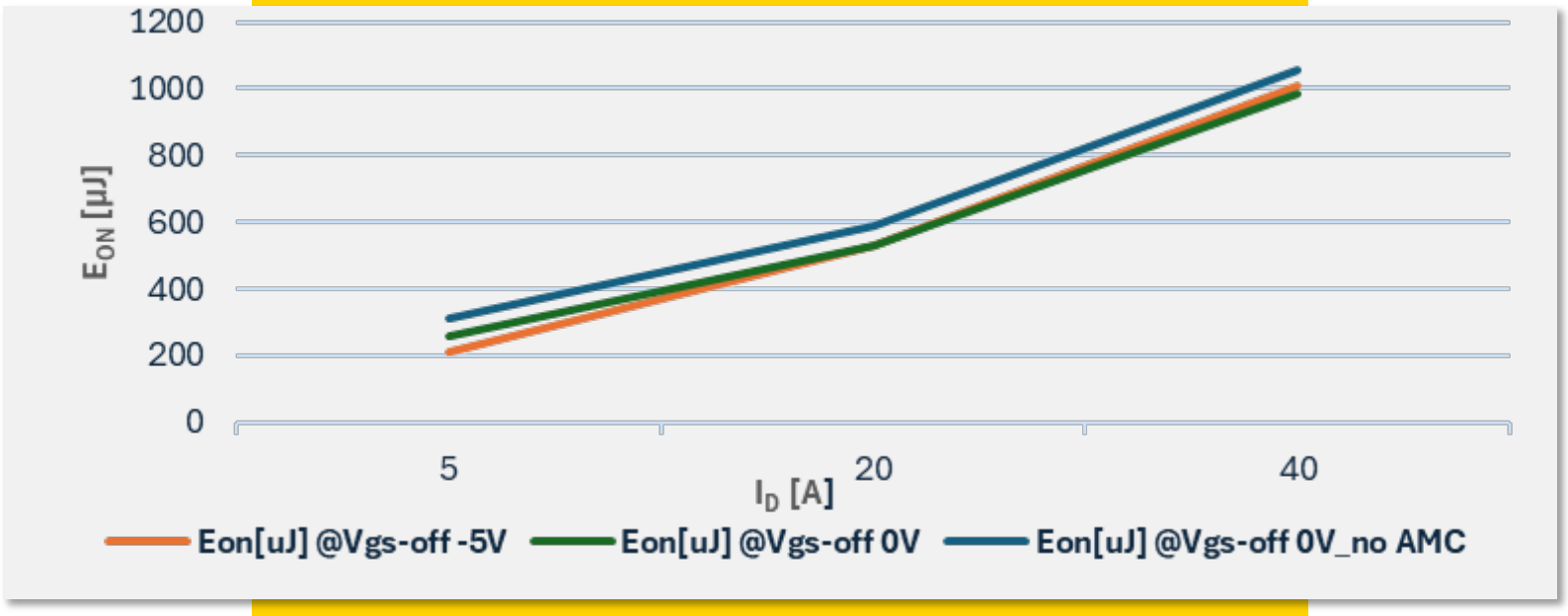
From 0 to 20% higher loss with 0 V turn off



Energy comparison bipolar vs unipolar driving

Eon (turn-on speed: $di/dt_{ON} \approx 2A/ns$)

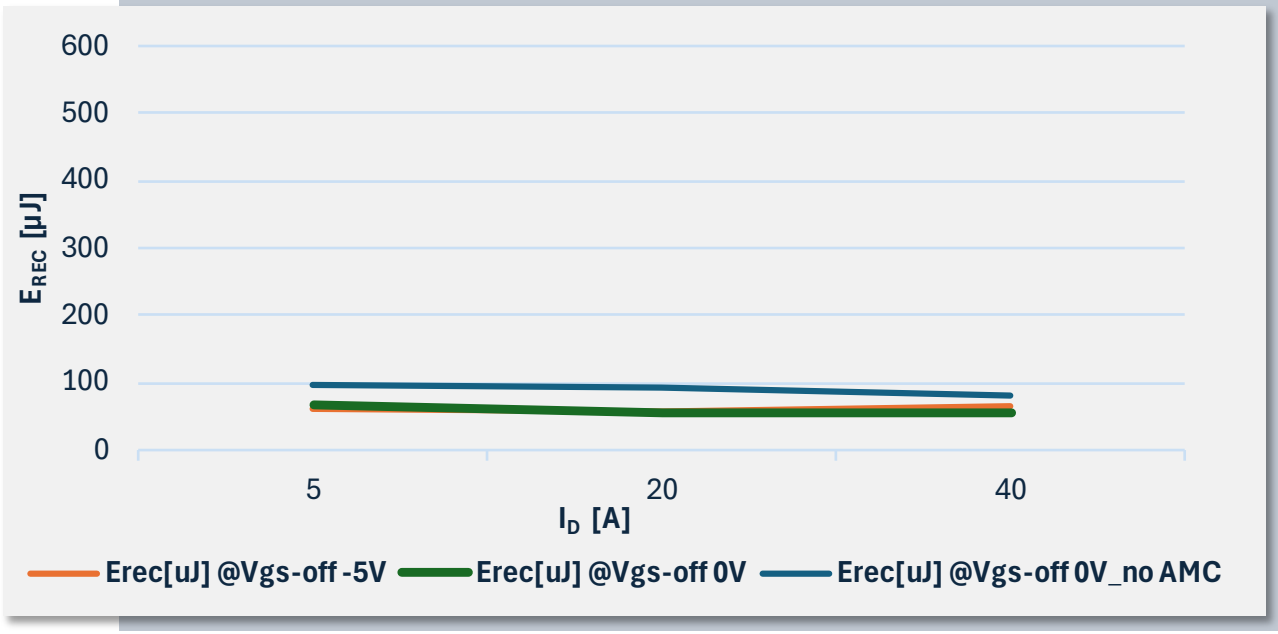
Almost no differences between negative and 0 Vgs-off with Active Miller clamp

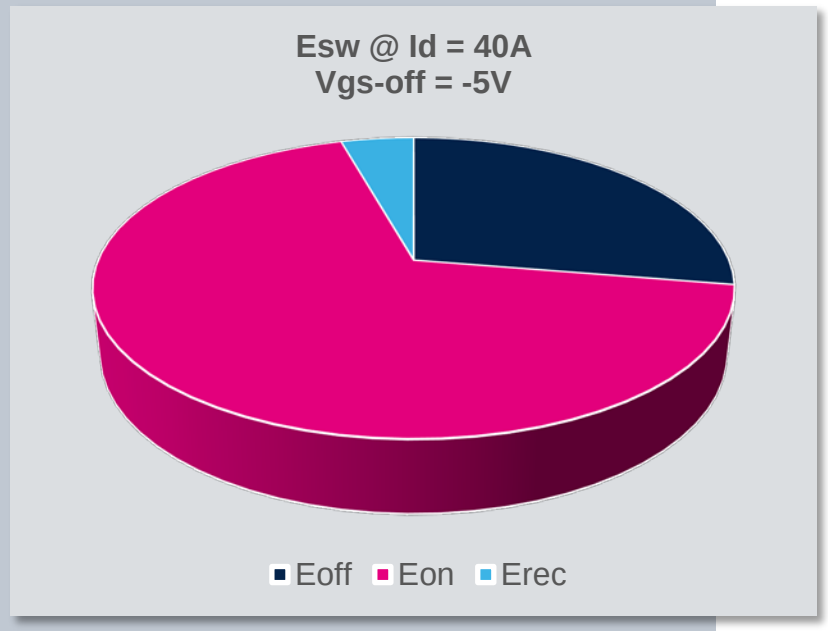


Energy comparison bipolar vs unipolar driving

Erec (turn-on speed: $di/dt_{ON} \approx 2A/ns$)

In all the analyzed cases the contribution of Erec is very small in comparison with Eon and Eoff. Even if there are small differences between negative and 0 Vgs-off, their contribution to the overall power losses is negligible

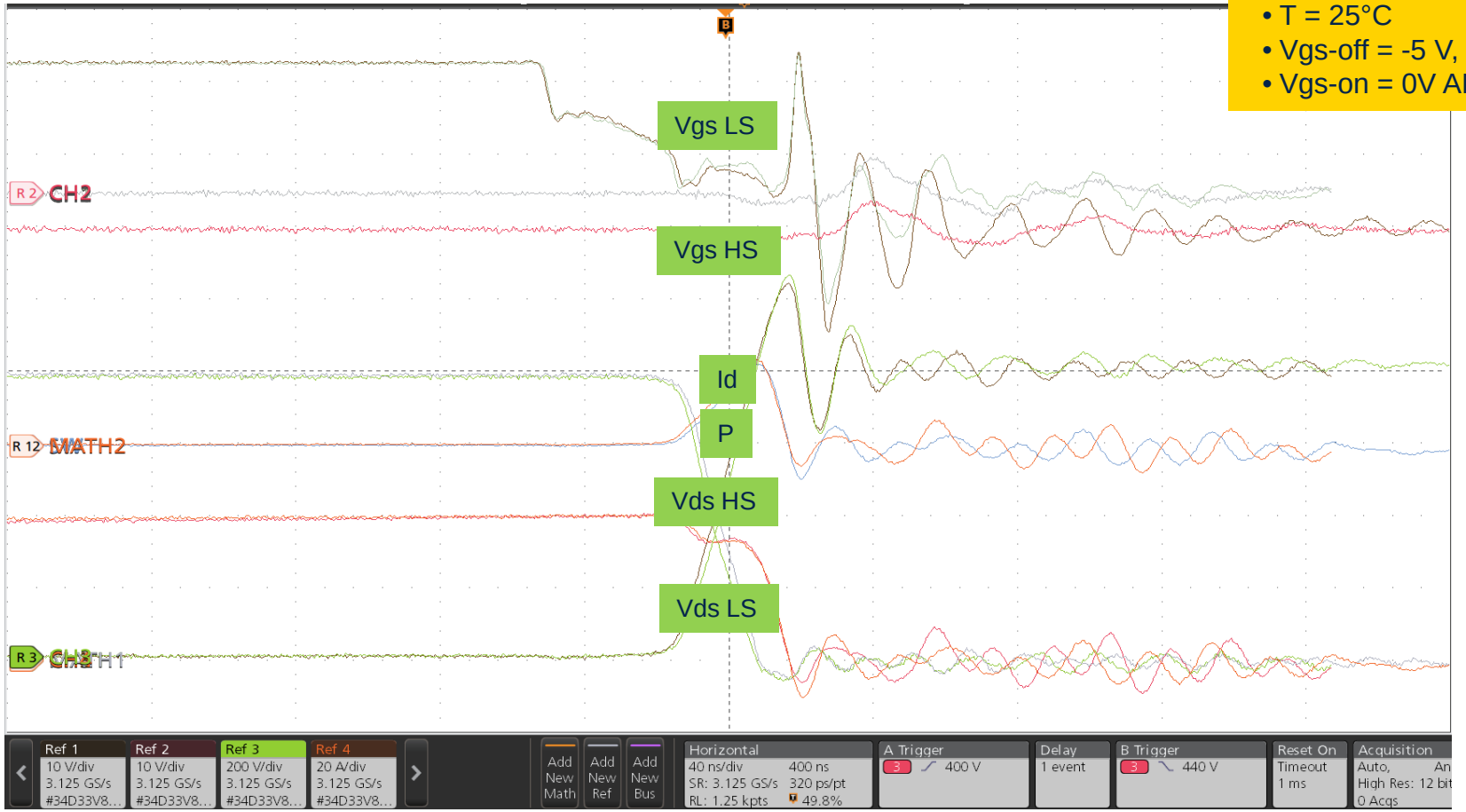




Experimental results: waveforms

Turn off waveform comparisons

Test conditions:
- VDD = 800 V
- ID = 40 A
- T = 25°C
- Vgs-off = -5 V, Rgon = 27 Ω, Rgoff = 8.2 Ω
- Vgs-on = 0V AMC (and no AMC), Rgon = 27 Ω, Rgoff = 4.7Ω



	Eoff [uJ]
-5V	407
0V AMC / 0V no AMC	460

Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V AMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn off waveform comparisons

Test conditions:
- VDD = 800V
- ID = 40A
- T = 150°C
- Vgs-off = -5V, Rgon = 27Ω, Rgoff = 8.2Ω
- Vgs-on = 0V AMC Rgon = 27Ω, Rgoff = 4.7Ω

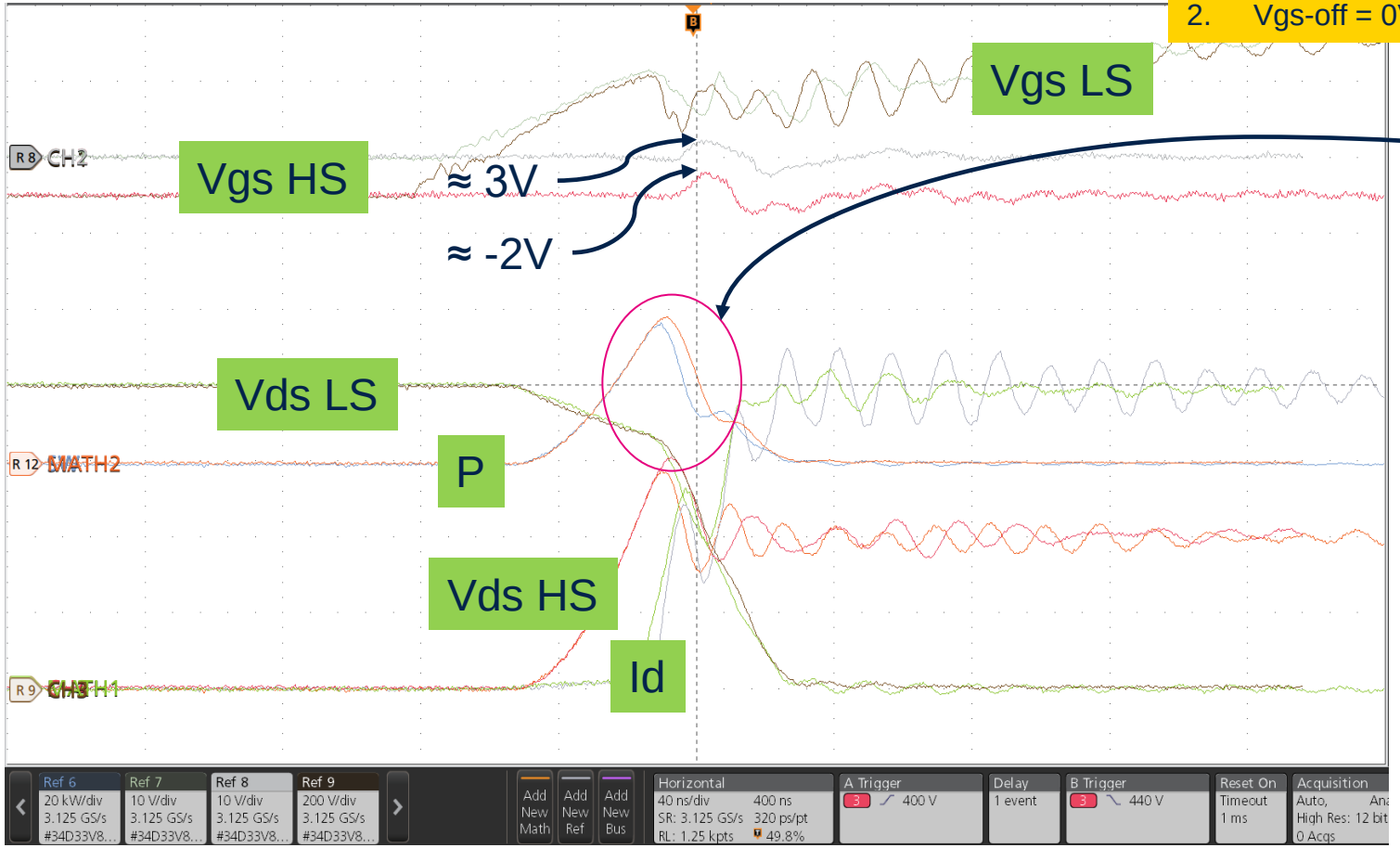
	Eoff [uJ]
-5V	410
0V AMC / 0V no AMC	480

Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V AMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn on waveform comparisons

Working conditions:
VDD = 800V, ID = 40A, T = 25°C
1. Vgs-off = -5V, Rgon = 27Ω, Rgoff = 8.2Ω
2. Vgs-off = 0V AMC, Rgon = 27Ω, Rgoff = 4.7Ω



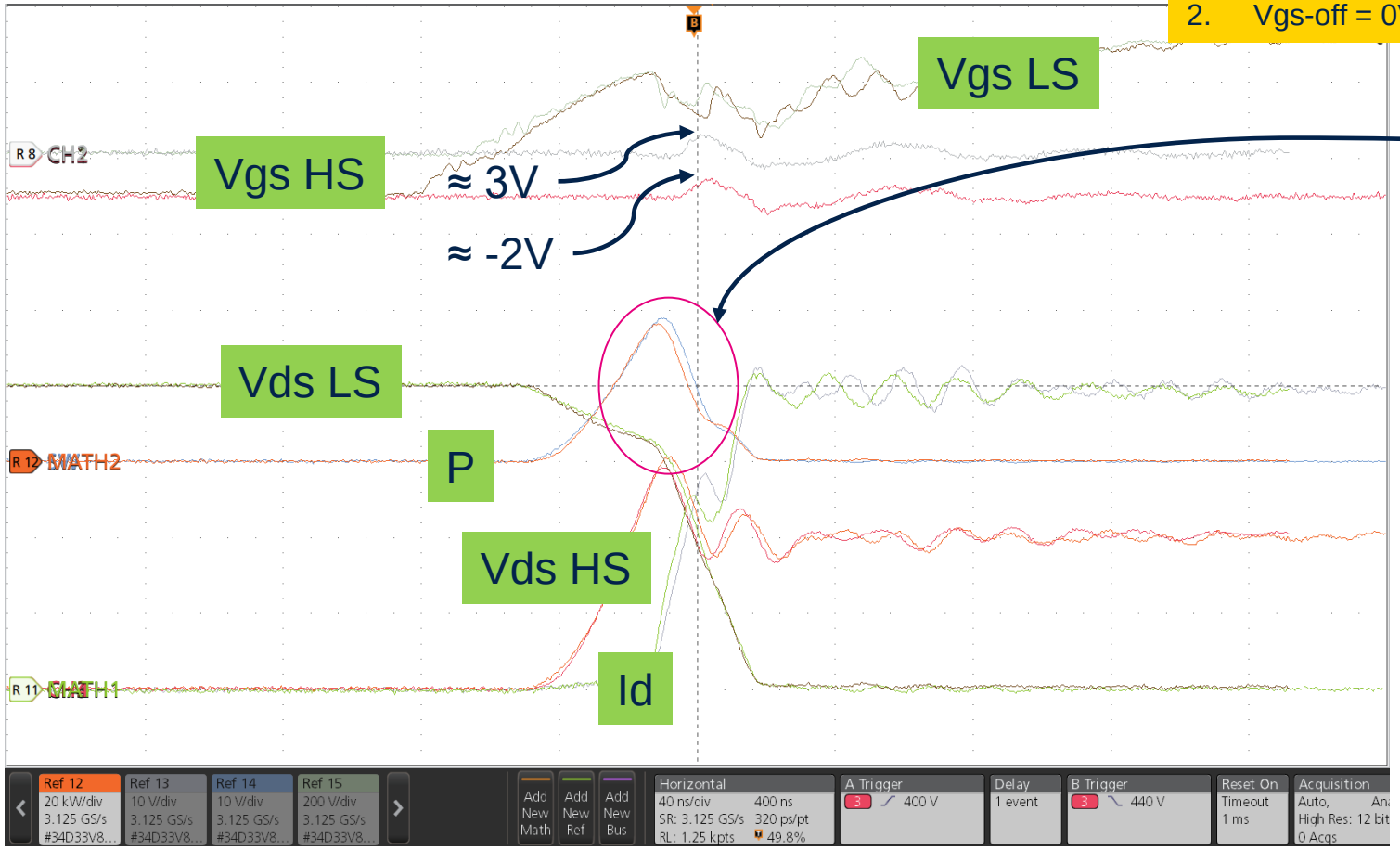
	Eon [uJ]
-5V	1100
0V AMC	1220

Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V AMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn on waveform comparisons

Working conditions:
VDD = 800V, ID = 40A, T = 150°C
1. Vgs-off = -5V, Rgon = 27Ω, Rgoff = 8.2Ω
2. Vgs-off = 0V AMC, Rgon = 27Ω, Rgoff = 4.7Ω



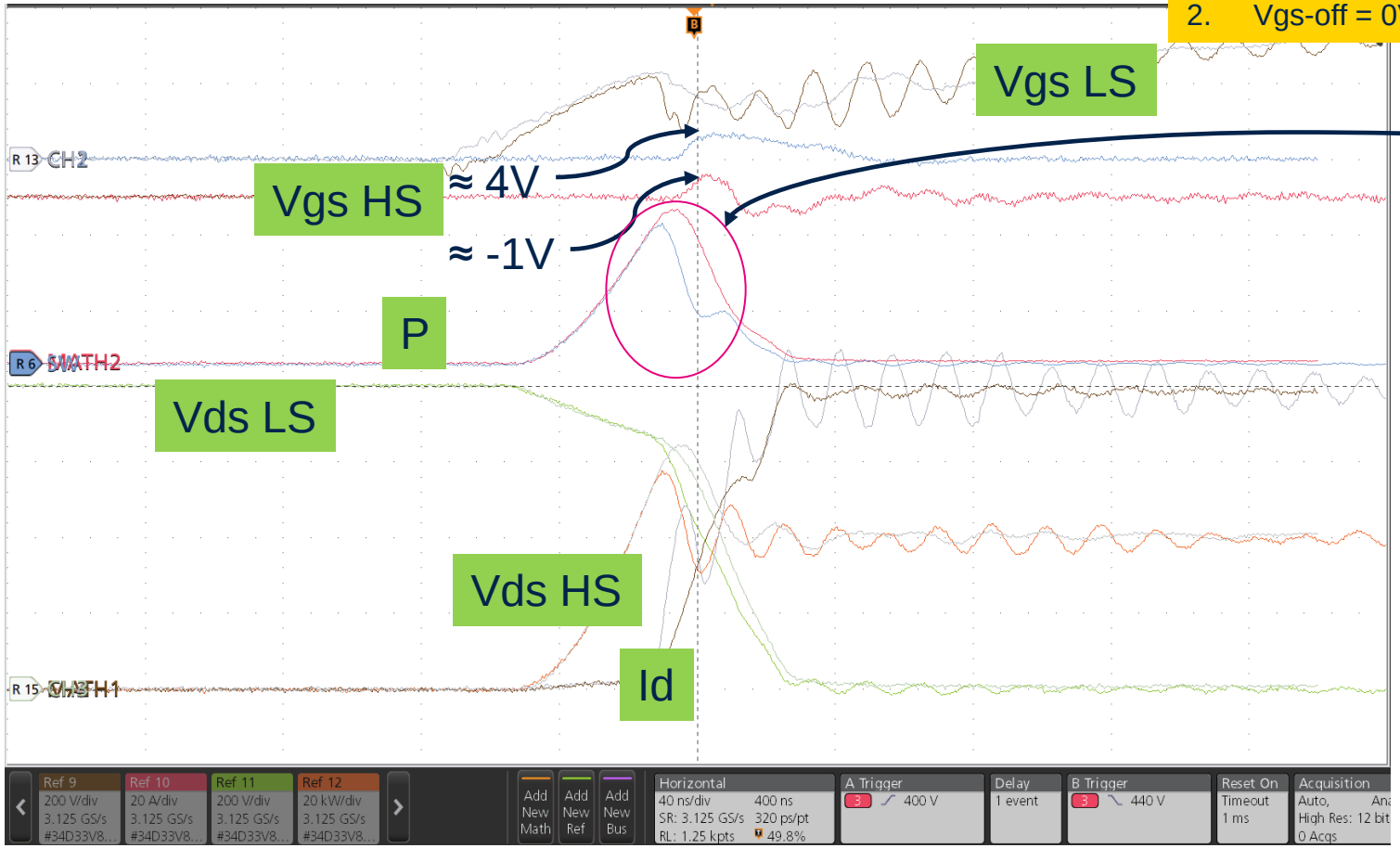
	Eon [uJ]
-5V	1055
0V AMC	984

Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V AMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn on waveform comparisons

Working conditions:
VDD = 800V, ID = 40A, T = 25°C
1. Vgs-off = -5V, Rgon = 27Ω, Rgoff = 8.2Ω
2. Vgs-off = 0V no AMC, Rgon = 27Ω, Rgoff = 4.7Ω



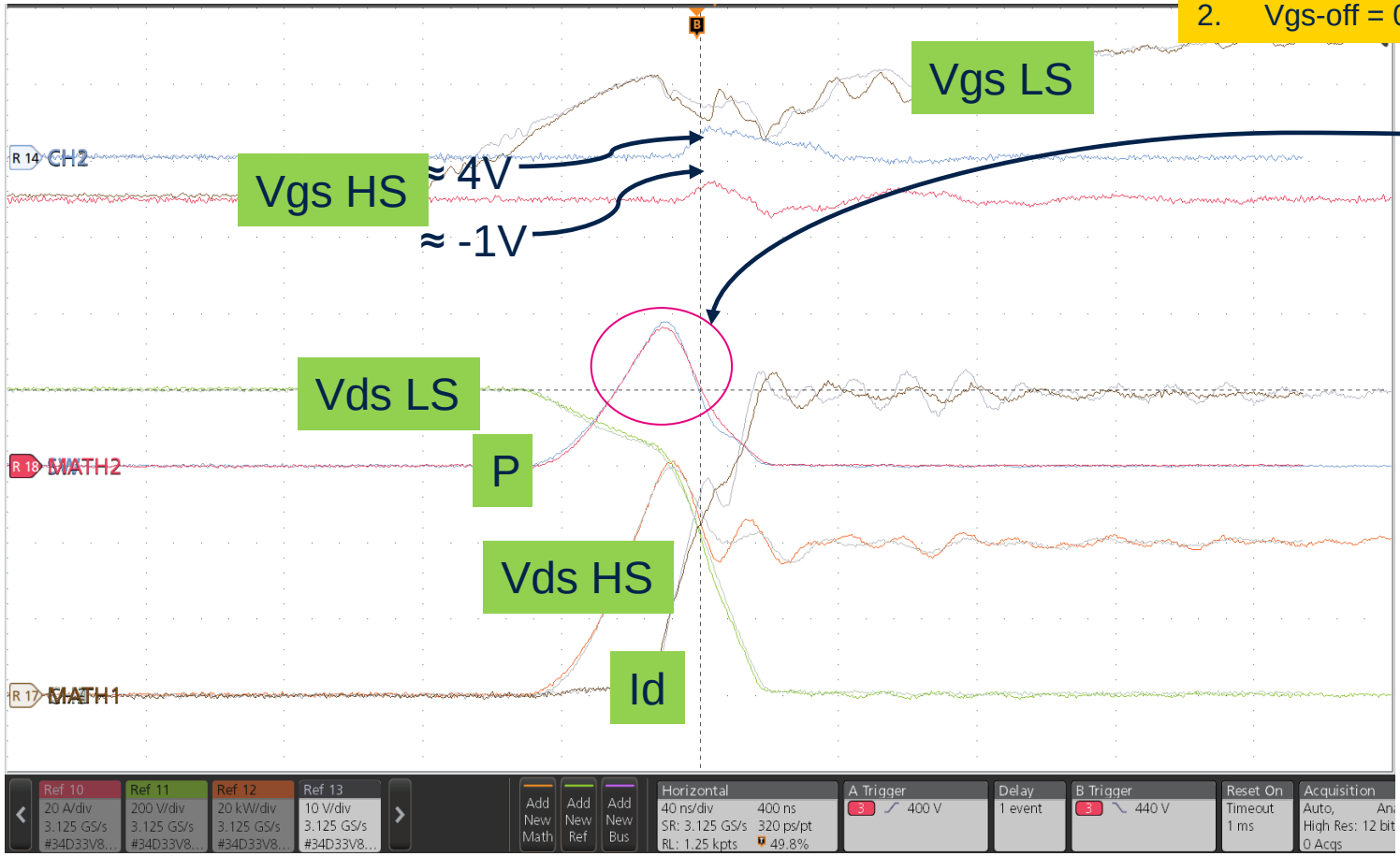
	Eon [uJ]
-5V	1100
0V NO AMC	1370

Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V NAMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn on waveform comparisons

Working conditions:
VDD = 800V, ID = 40A, T = 150°C
1. Vgs-off = -5V, Rgon = 27Ω, Rgoff = 8.2Ω
2. Vgs-off = 0V no AMC, Rgon = 27Ω, Rgoff = 4.7Ω



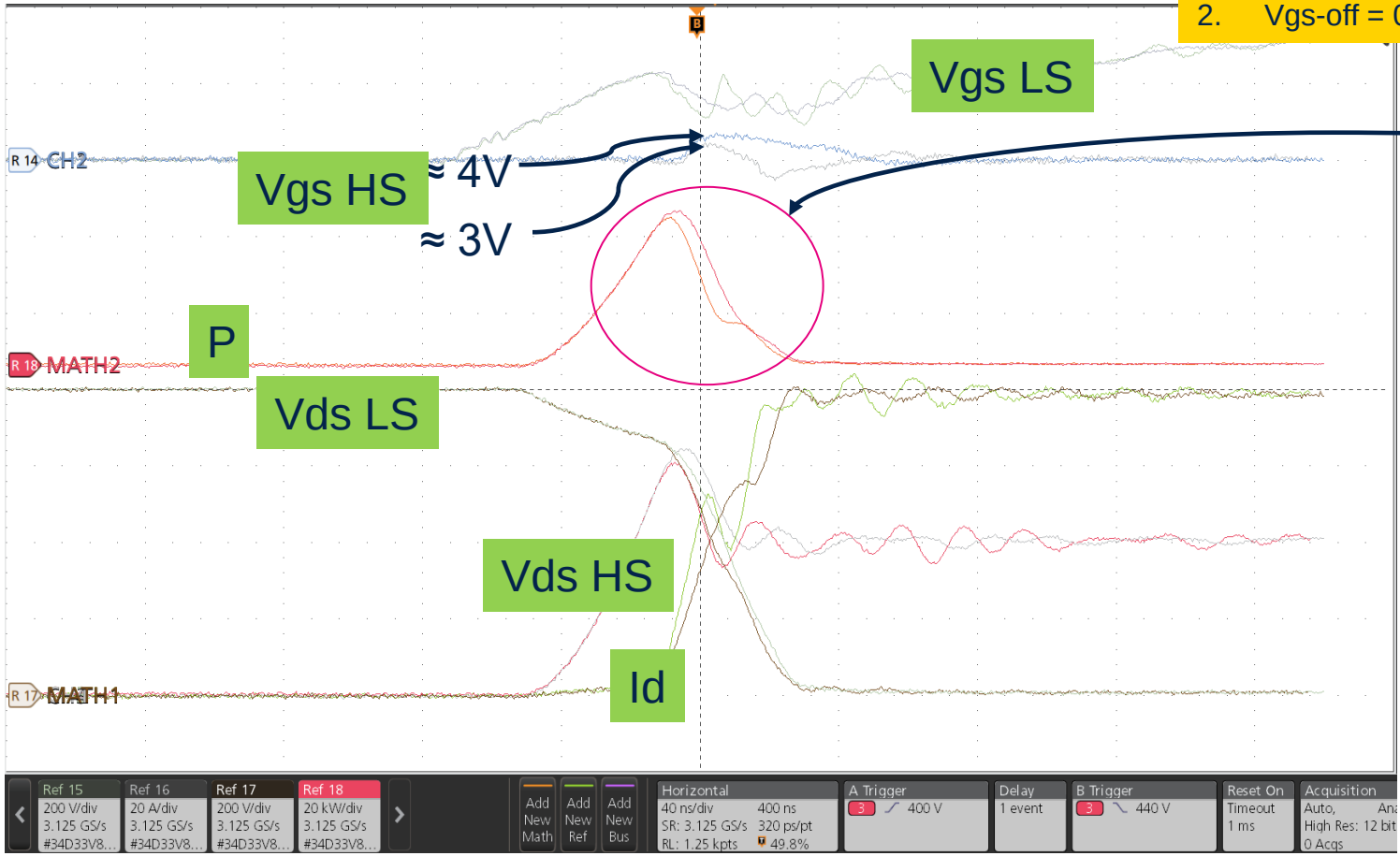
	Eon [uJ]
-5V	1055
0V NO AMC	1055

Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V NAMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn on waveform comparisons

Working conditions:
VDD = 800V, ID = 40A, T = 25°C
1. Vgs-off = 0V AMC, Rgon = 27Ω, Rgoff = 4.7Ω
2. Vgs-off = 0V no AMC, Rgon = 27Ω, Rgoff = 4.7Ω



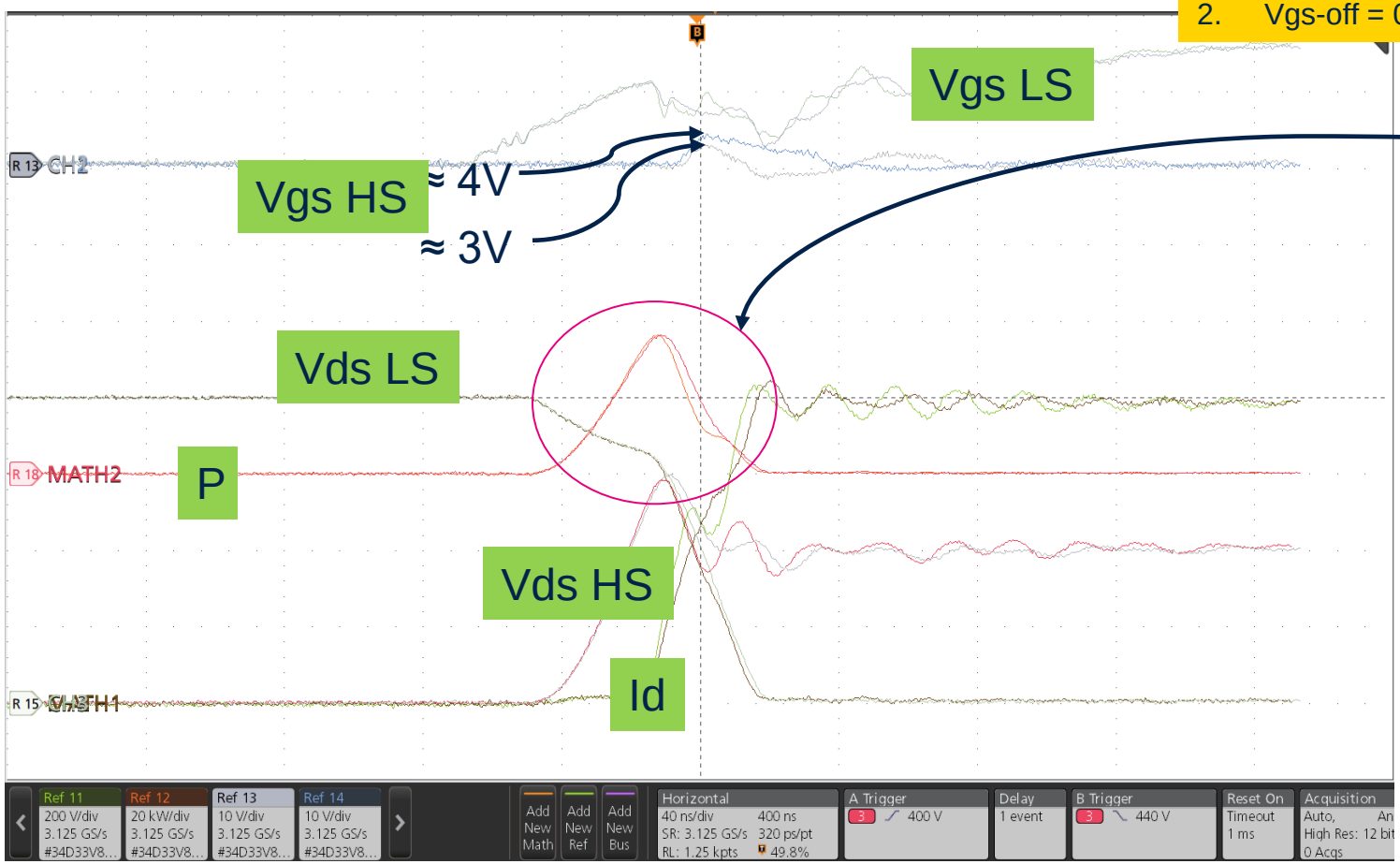
	Eon [uJ]
0V AMC	1220
0V NO AMC	1370

Colors of the traces

Legend	CASE Vgs OFF = 0V AMC	CASE Vgs OFF = 0V NAMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Turn on waveform comparisons

Working conditions:
VDD = 800V, ID = 40A, T = 150°C
1. Vgs-off = 0V AMC, Rgon = 27Ω, Rgoff = 4.7Ω
2. Vgs-off = 0V no AMC, Rgon = 27Ω, Rgoff = 4.7Ω



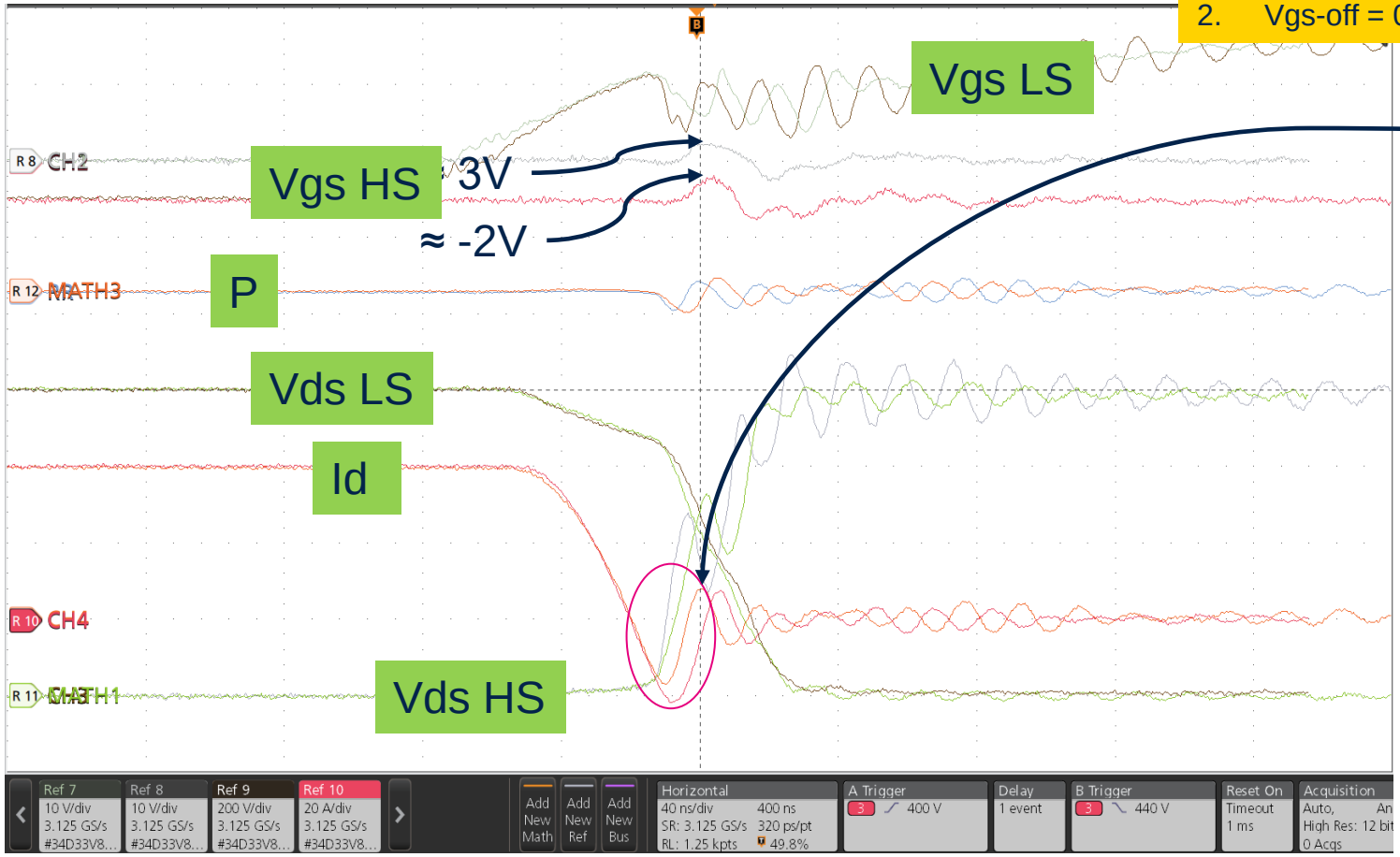
	Eon [uJ]
0V AMC	984
0V NO AMC	1055

Colors of the traces

Legend	CASE Vgs OFF = 0V AMC	CASE Vgs OFF = 0V NAMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Reverse recovery waveforms comparison

Working conditions:
VDD = 800V, ID = 40A, T = 25°C
1. Vgs-off = -5V, Rgon = 27Ω, Rgoff = 8.2Ω
2. Vgs-off = 0V AMC, Rgon = 27Ω, Rgoff = 4.7Ω



	Erec [uJ]	Irm [A]
-5V	45	17
0V AMC	57	21

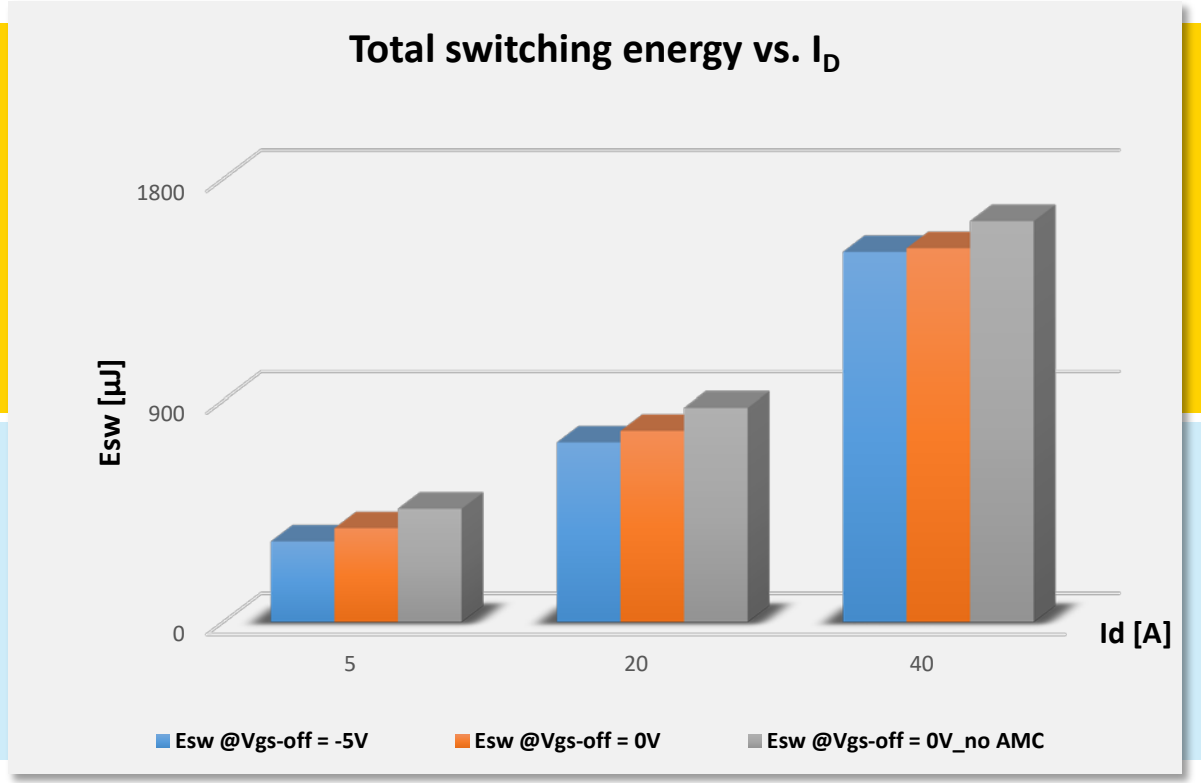
Colors of the traces

Legend	CASE Vgs OFF = -5V	CASE Vgs OFF = 0V AMC
Vgs LS		
Vgs HS		
Vds LS		
Vds HS		
Id		
P		

Summary and conclusions

Energy comparison bipolar vs unipolar driving
Summary of test results

Experimental data on 1200V; SiC MOSFET Gen3; 27mΩ typ



Test condition:

- TJ = 150°C,
- Turn-on speed: $di/dt_{ON} \approx 2A/ns$
- Turn-off speed: $dv/dt_{OFF} \approx 35V/ns$
- VDD ≈ 800V
- 0 Vgs-off with and without Active Miller clamp vs negative driving voltage as PoR

Results:

- In the case investigated (0V Vgs-off and AMC) the gap between unipolar and bipolar driving is negligible especially at high load
- Removing the Active Miller clamp introduces additional switching losses in the range of 5-10%.

Conclusions

Active miller clamp is recommended when applying 0V OFF Vgs

- **R_{gon} and R_{goff}** (and in general the driving circuit) **can be fine-tuned to optimize the performance, minimizing spikes** and switching losses with negative and with zero-volt $V_{gs\text{-}off}$.
- The comparison between -5V and 0V shows negligible differences in case of typical threshold voltage ($V_{TH(typ)}$).
- For design robustness, it is suggested to design the system and the driving circuit considering the **worst case in terms of V_{TH} and temperature**, paying attention to the additional amount of energy loss in comparison with the case @ typical V_{TH}.

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