

Stellar SR5 E1 line - isolated current sensing in electric motor control demo

Introduction

The SR5 E1 line 32-bit Arm[®] Cortex[®]-M7 microcontrollers are specifically developed for embedded applications integrate technologies that are particularly suited for driving electrical vehicles. SR5 E1 line typical applications include on-board charger, DC/DC converters, traction inverter, advanced electric motor control, all applications where sensing and/or controlling current flow is a fundamental requirement.

This technical note focuses on isolated current sensing technique implementation with SR5 E1 microcontrollers. After an overview of the electric motor field oriented control, it is described in detail the configuration and usage of the SR5 E1 peripherals in isolated current sensing topology implemented in SR5 E1 motor control tool kit (MCTK) demo application (refer to STMicroelectronics local representative for reference hardware and software).





1 FOC

1.1 Introduction to PMSM FOC drive

The field oriented control (FOC) is a vectorial control strategy for driving permanent-magnet synchronous motors (PMSM). It consists of controlling the stator currents represented by a space vector, a phase angle and magnitude, from which the terminology "vector control" derives.

With this approach, it is possible to offer electromagnetic torque (Te) regulation and, to some extent, flux weakening capability by controlling the two currents iqs and ids, which are mathematical transformations of the stator currents. Therefore, FOC consists in controlling and orienting stator currents in phase and quadrature with the rotor flux. So, it is clear that the fundamental is the measuring of stator currents and the rotor angle.

The structure of the FOC algorithm is represented in the following figure.

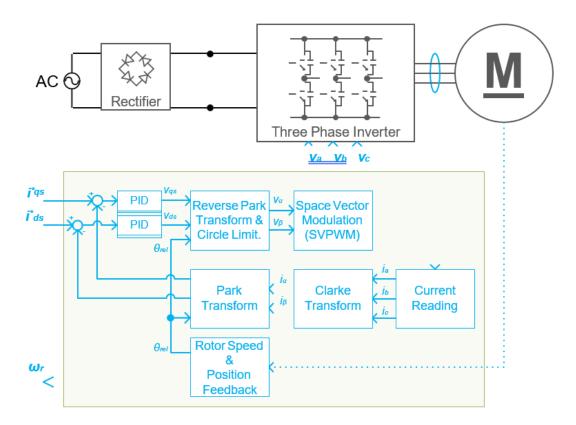


Figure 1. Basic FOC algorithm structure, torque control

- The iq*s and id*s current references can be selected to perform electromagnetic torque and flux control.
- The space vector PWM block (SVPWM) implements an advanced modulation method that reduces current harmonics, thus optimizing DC bus exploitation.
- The current reading block allows the system to measure stator currents correctly, using either cheap shunt resistors or market-available hall sensors or isolated current sensors (ICS).
- The rotor speed/position feedback block allows the system to handle resolver sensor, hall sensor or incremental encoder signals to correctly acquire the rotor angular velocity or position. The PID controller implements proportional, integral, and derivative feedback controllers (current regulation).
- The clarke, park, reverse park, and circle limitation blocks implement the mathematical transformations required by FOC.

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Isolated current sensing in SR5 E1 electric motor control demo

As described in Section 1.1 Introduction to PMSM FOC drive, field oriented electric motor control depends, besides the rotor angle position, upon accurate acquisition of motor phase currents. Additionally, the currents need to be acquired at specific conditions of the motor drive. These conditions are given in terms of pulse width modulation (PWM) signals. The phase current acquisition has to be initiated when all three PWM signals are either at logic 0 or when all three are at logic 1.

There are different possible current sensing topologies: one shunt topology on low side or high side of the inverter, three shunts topology on the legs of inverter and isolated current sensing topology (ICS) on the phases of the motor. Each topology has its pros and cons in terms of hardware costs, simplicity of software implementation and the accuracy in the current measurement.

ICS topology is the best method to precisely know the phase current flowing into the motor. This current measurement offers the best information that can be used in feedback motor control, to optimize the motor performance.

In the following paragraphs, the focus is on isolated current sensing implementation and details are given about SR5 E1 peripherals and techniques used to trigger the ADC current acquisition synchronized with the PWM signals.

2.1 Current sampling in isolated current sensor topology

The following figure shows the ICS topology, largely used in the traction inverter. The sensors are on the three phases of the motor.

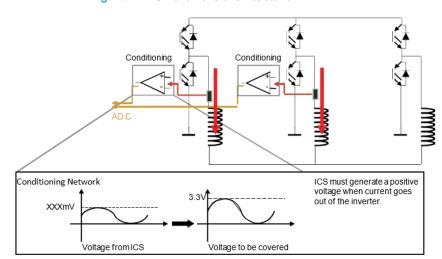


Figure 2. ICS hardware architecture

The three currents I₁, I₂, and I₃ flowing through a three-phase system follow the Kirchhoff's law:

$$I_1 + I_2 + I_3 = 0 (1)$$

For this reason, to reconstruct the currents flowing through a generic three-phase load, it is sufficient to sample only two out of the three currents while the third one can be computed by using the above relation Eq. (1). The flexibility of the SR5 E1 A/D converter makes it possible to simultaneously trigger the two A/D conversions needed for reconstructing the two currents flowing through the two phases of the motor. The ADC is used to

synchronize the currents sampling point with the PWM output taking advantage of its external triggering capability. In fact by means of ADC external trigger capability, the current acquisition can be performed at any given time during the PWM period and in our case, as it is shown in the following figure, the acquisition is done in the middle of PWM high time frame that is in the instant when the average level of current is equal to the sampled current.

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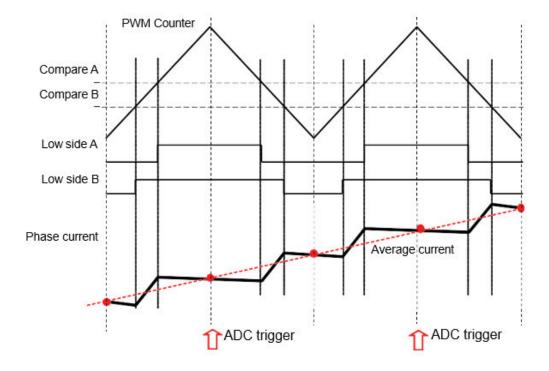


Figure 3. Stator currents sampling in ICS configuration

2.2 Current sensing peripherals in SR5 E1 electric motor control demo

The peripherals used in the SR5 E1 line motor control tool kit demo application (MCTK) to implement the isolated current sensing are:

- TIM1/TIM8 advanced-control timers dedicated to generating PWM signals to drive the legs of the inverter
 to apply the desired voltage on three phases of the motor. The trigger of current measurement must be
 synchronized with generated PWM signals.
- ADC1/ADC2 for single motor and ADC3/ADC4 for dual motor dedicated for measuring the current that flows into three phases of the motors.

The SR5 E1 microcontrollers offer a mechanism to link TIMs to ADCs that can be used to synchronize the current measurement, carried out by the ADC, with the PWM signals generation, generated by the TIM.

The following table summarizes the peripherals allocated to drive a single or dual motor in the SR5 E1 line MCTK.

Adv. timer ADC **ISR** Note Used by the first or second motors configured in ICS topology, TIM1 ADC1 ADC2 TIM1_UP depending on the user selection. ADC is used in time sharing. Trigger selection is performed in the TIM UP ISR. Used by the first or second motor configured in ICS topology, TIM8 TIM8 UP ADC3 ADC4 depending on the user selection. ADC is used in time sharing. Trigger selection is performed in the TIM_UP ISR.

Table 1. ICS topology, peripherals resource allocation (single or dual drive)

2.3 TIM1/TIM8 timers-PWM generation

The SR5 E1 TIM1/TIM8 modules, used to generate PWM signals, consist of a 16-bit auto reload counter driven by a programmable counter clock that can be divided by a prescaler. The counter can count-up, down or both directions.

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The PWM center aligned mode, used in the MCTK is configured in the TIMx_CR1 register setting field CMS to b10 (TIMx_CR1.CMS=b10).

In this mode, the TIMx counter counts from 0 to the auto reload value set in the field ARR of the TIMx_ARR register. Once reached the auto reload value-1, an overflow event is generated and the counter starts counting from the auto reload value down to zero generating a counter underflow event when the counter value reaches 0. Then it restarts counting from 0 up to auto reload value, and so on, as described above.

The TIM1/TIM8 modules contain, each, four PWM channels:

- TIMx_CH1, TIMx_CH2 and TIMx_CH3 are used in electric motor to generate PWM signals to apply the desired voltage on three phases.
- Complementary signals are automatically generated (TIMx_CH1N, TIMx_CH2N and TIMx_CH3N) with deadtime insertion.
- TIMx_CH4 is used to synchronize the ADC conversions (tim_oc4refc signal is used).

The figure below shows the synchronization strategy between the TIM1 PWM output and the ADC1/ADC2 currents acquisition (TIM8 and ADC3/ADC4 are used for the second motor). The TIM1_CH4 triggering pulse is generated when the timer counter reaches the capture compare register 4 (CCR4) value set to PWM_Period/2 – five ticks. In this way, the ADC conversion for the two currents is done just before the overflow value of the counter register set to PWM_Period/2 ensuring that the currents measurement is done in the middle of the PWM period. The ADCs acquisition is triggered by the rising edge of TIM1_CH4 signal.

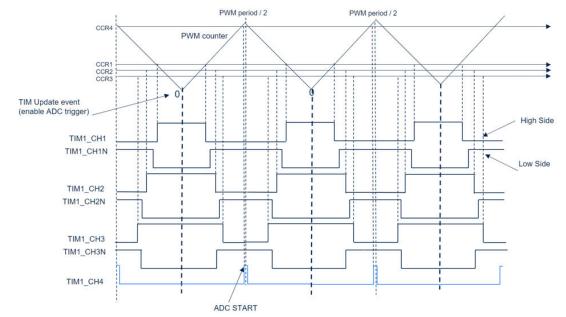


Figure 4. Generation of TIM_CH4 to trigger ADC1/ADC2 acquisition

2.4 SAR ADC modules – Current acquisition

Isolated current phases are routed to SR5 E1 12-bit SAR analog converters (SAR-ADC). The SR5 E1 has 5 SAR-ADC instances:

- ADC1 and ADC2 are tightly coupled and can operate in dual mode (ADC1 is master).
- ADC3 and ADC4 are tightly coupled and can operate in dual mode (ADC3 is master).
- ADC5 is controlled independently.

Each ADC consists of a 12-bit successive approximation analog-to-digital converter. The result of ADC is stored in a left-aligned or right-aligned 16-bit data register.

Start-of-conversion is initiated by hardware triggers with configurable polarity. In MCTK demo Injected conversions are preferred to have maximum priority on the current sensing (prevent ADC conversions from being interrupted by other).

The following ADC allocation to phase currents is done for Single and Dual motor in the MCTK:

Motor 1 Phase A current is measured by ADC1 Channel 1

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- Motor 1 Phase B current is measured by ADC2 Channel 1
- Motor 2 Phase A current is measured by ADC3 Channel 1
- Motor 2 Phase B current is measured by ADC4 Channel 1

For correct calculation of the FOC algorithm, the phase A and phase B current measurement must be executed at the same time; thanks to SAR ADC DUAL mode available in SR5 E1, the start of conversion is triggered simultaneously and the converted data of the ADC1/ADC2 and ADC3/ADC4 can be read in parallel, by reading the ADC common data register (ADCx_CDR).

2.5 TIMs and ADCs synchronization

The timer (TIM1/TIM8) can generate an ADC triggering event with various internal signals setting MMS[2:0] bits in the TIMx_CR2 register. In the MCTK, the ADC trigger event is generated on the rising edge of the TIM1_CH4 signal. In a particular setting TIMx_CR2.MMS=b0111, tim_oc4refc signal is used as trigger output (tim_trgo)

To start an ADC conversion in dual mode synchronized with PWM generated by the TIM, the user must program the external trigger enable and polarity selection bit (JEXTEN) and external trigger selection for an injected group bit (JEXTSEL) of ADC injected sequence register (ADC_JSQR).

In particular:

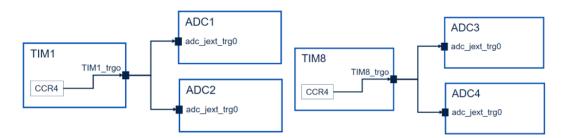
- JEXTEN is configured as a trigger enabling and detection on the rising edge, ADC JSQR.JEXTEN=b01
- JEXTSEL is used to select the external trigger source adc_jext0_trg coming from the injected group multiplexer of the ADC, ADC_JSQR.JEXTSEL=b00000. adc_jext0_trg is connected to tim_trgo

Summarizing:

- The timer output is on signal tim1_trgo of output compare TIM1 channel 4 (tim_oc4refc from CCR4 is routed to tim1_trgo).
- Input to ADC is on adc_jext0_trg signal
- Connection between TIM and ADC is enabled with JEXTEN bit

In the following figure, it is shown the connection between TIM and ADCs for currents phase A and phase B simultaneous acquisition synchronized with PWM period.

Figure 5. TIM/ADC connection for synchronized phase A, phase B current acquisition in single or dual motor



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Appendix A Other information

A.1 Acronyms

The following table shows the list of acronyms used in this document.

Table 2. Terms and abbreviations

Acronym	Definition
A/D	Analog to digital
ADC	Analog to digital converter
MCTK	Motor Control Tool Kit
FOC	Field oriented control
ICS	Isolated current sensor
MC	Motor control
MCU	Microcontroller unit
PID	Proportional-integral-derivative (controller)
PMSM	Permanent magnet synchronous motor
PWM	Pulse width modulation
SVPWM	Space vector pulse width modulation

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Revision history

Table 3. Document revision history

Date	Version	Changes
07-Nov-2023	1	Initial release.

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