Information about the mounting on PCB of SMD.5 ceramic package devices

Introduction

This technical note provides information about the mounting of SMD.5 ceramic package on printed board. The SMD.5 ceramic hermetic package, commonly used for space applications, shows recurrent mounting failures during its mounting qualification as per ECSS-Q-ST-70-61C. The French space agency CNES and STMicroelectronics have done a study to evaluate the crack failures impact on the electrical parameters and the reliability of the components and identify potential stress factors.

Following these trials, the parts with cracks in the ceramic are submitted to some reliability tests to confirm if the observed defects during the mounting qualification have no impact on the system reliability.

The results presented in this document only apply to the tested configuration, which is the one used by STMicroelectronics for its SMD.5 packaged products. Extrapolation to other cases cannot be guaranteed.

1 Design of experience and parameters under evaluation

1.1 Design of experience description

Forty-five bipolar transistors have been assembled in the SMD.5 package by mixing three manufacturing options, leading to nine manufacturing configurations. Each configuration is tested with five identical parts.

These forty-five parts are mounted on a printed circuit board (PCB) in a stack-up, which is known to be stressful.

The parts are submitted to a thermal cycling test according to space standard requirements. All during this test, the parts are carefully inspected for cracks.

Following these trials, the parts with cracks in the ceramic were subjected to reliability tests to confirm if the defects observed during mounting qualification have no impact on system reliability.

1.2 Parameters under evaluation

The parameters are potential stress factors for crack appearance, and they are following ones:

- Base supplier of ceramic package (supplier B1, supplier B2)
- Sealing process: between parallel seam welding (PSW), using two different equipment (PSW1 for equipment 1 and PSW2 for equipment 2) and furnace sealing
- Gold removal and hot solder dipping on the external pads in solder bath: the impact of this process was evaluated by comparison with the gold-plated parts
- The die-attach (DA) process selected for this study is a eutectic DA because it is the worst case in terms of thermal constraints applied on the part during manufacturing
- Thermal cycling: A thermal cycling test is done at the end of the assembly phase: 20 cycles between the stressing temperatures from -65°C to +200°C as defined in the relevant ESCC detail specification. Since this test is also done on bipolar transistor structure, it is the worst case.
- Parts configuration: five parts per configuration are tested, all with hot-soldering finish. One configuration is not studied: the parts sealed on PSW2 and assembled with base B2. The whole 45 parts were submitted: Three suppliers, three sealing equipment, and two finishing processes. All parts were marked and serialized for better traceability.

Note: Addendum on Rev2, the semi-sintering die attach process, now used, was not qualified at the time of the study, and this new die attach is less stressing thermally for the ceramic of the package than the former eutectic process, so the study here after also covers the new assembly version.

Table 1. Matrix of tests

Die-Attach	Thermal cycling	Stabilization bake	Base supplier	Sealing process	Finishing	Quantity
Eutectic	20 cycles -65 °C/+200 °C	25 hours at 200 ±3 °C	B1	Furnace	Gold	5
					Hot solder	5
				PSW1	Gold	5
					Hot solder	5
				PSW2	Hot solder	5
			B2	Furnace	Gold	5
					Hot solder	5
				PSW1	Gold	5
					Hot solder	5

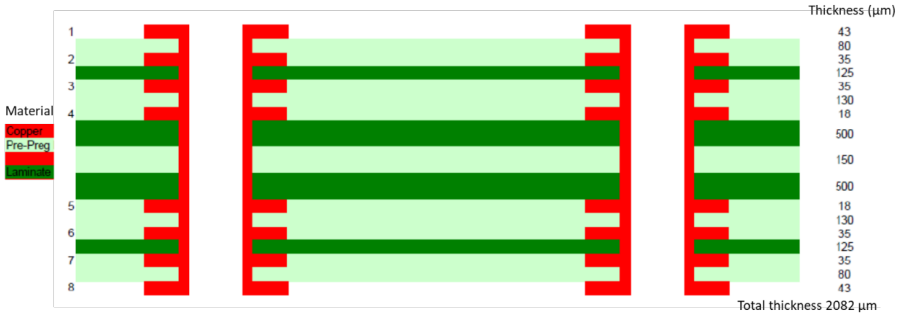
2 Test conditions

After assembly, the parts were submitted to the following trials.

2.1 PCB mounting

All the parts were mounted on a 2 mm thick printed circuit board (PCB). The PCB stackup is shown in the Figure 1:

Figure 1. PCB stack up



Before the part mounting, all PCBs were steamed for 12 hours at 125 °C.

The parts were mounted using the henkel soldering paste *SN62MP218AGS89.5V* with a stencil thickness of 150 µm. This solder paste corresponds to the *Sn62Pb36Ag2* alloy.

The parts were mounted in a batch furnace under vacuum (without any vapor phase) with a reflow profile at maximum temperature of 220 °C.

The PCB was cleaned after the reflow process to remove flux residues, and then each part was inspected.

None of the 45 parts showed cracks after mounting.

2.2 Tests covering the space applications

After mounting the parts, the printed circuit board (PCB) was subjected to thermal cycling (TC) stress. The temperature cycles ranged from -55 °C to +100 °C with a maximum slope of 10 °C/min.

A visual inspection of the parts was conducted after 10, 30, 50, and 100 cycles, and subsequently every 100 cycles up to 500 cycles, to check for the presence or absence of cracks in the packages.

Once the temperature cycling trials and visual inspections were completed, 10 components (parts with and without cracks) were manually desoldered from the PCB. These components were subjected to hermeticity tests and electrical measurements at ambient temperature.

Due to the stringent storage conditions of the space industry and the vacuum conditions in orbit, a temperature-humidity bias (THB) test with 85 °C/85 % relative humidity (RH) was performed on the 10 parts for 168 hours to evaluate the influence of high humidity in the device cavity on reliability.

2.3 Tests covering other high-reliability applications

Following the 168-hour temperature-humidity bias (THB) test conducted to address space applications, a steady-state temperature-humidity bias life test was conducted on 10 parts under the following conditions:

- Temperature: 85 ± 2 °C
- Humidity: 85 ± 5 %
- Duration: 1144 hours

The test was performed in multiple steps to accommodate the production constraints of the equipment. At each step, the parts were measured at ambient temperature and over a temperature range of 0 °C to 30 °C to encourage potential condensation on the die below the dew point.

At the conclusion of the test, the parts were subjected to a 5 mbar vacuum for 12 hours, followed by an electrical test.

Finally, an internal visual inspection was conducted on each part to identify potential signs of corrosion.

3 Test results

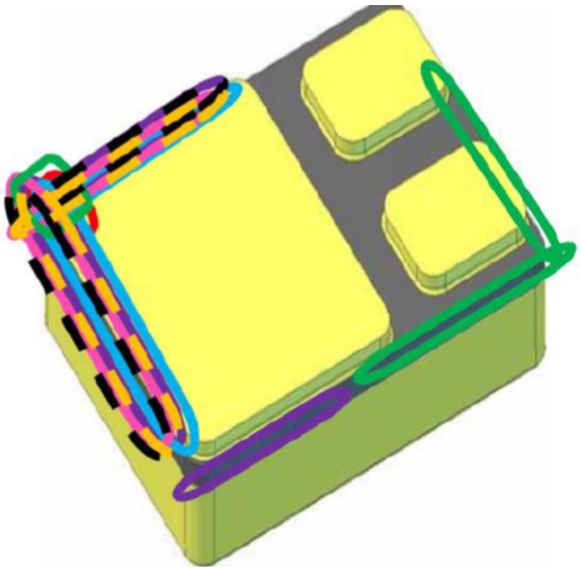
3.1 Cracks generation after thermal cycles

The test matrix did not identify a predominant parameter in the generation of cracks. All populations were affected, including base suppliers, golden and hot solder finishes, furnace, and parallel seam welding sealing processes.

Consequently, the cracks do not appear to result from stress induced during the manufacturing process of the component but are intrinsically present in the package due to its construction.

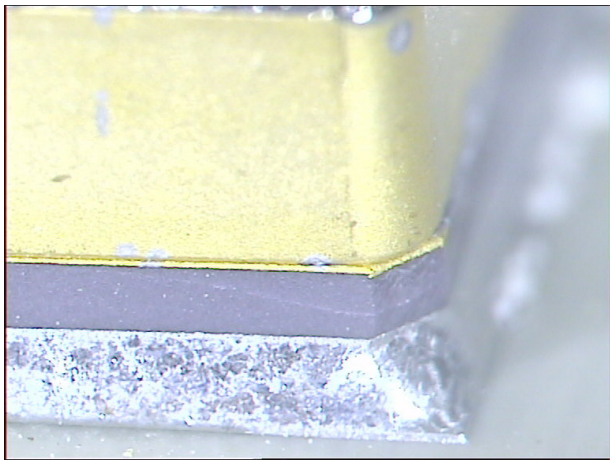
All the cracks are located in the ceramic part of the package, and almost all cracks (5 out of 7) are near the largest contact pad.

Figure 2. Cracks overview



The first cracks were observed after 10 cycles for base supplier B1 and after 50 cycles for base supplier B2.

Figure 3. Crack in the ceramic



From a visual perspective, the cracks do not evolve during thermal cycling stress.

Table 2. **Thermal cycles results**

Base supplier	Sealing process	Finishing	Quantity	Number of parts presenting cracks versus number of thermal cycles							
				10	30	50	100	200	300	400	500
B1	Furnace	Gold	5	1	1	1	1	1	2	2	2
		Hot solder	5	0	0	0	0	0	0	0	0
	PSW1	Gold	5	1	1	1	2	2	2	2	2
		Hot solder	5	0	0	0	0	0	0	0	0
	PSW2	Hot solder	5	0	0	0	0	0	0	0	0
B2	Furnace	Gold	5	0	0	0	0	0	0	0	0
		Hot solder	5	0	0	0	1	1	1	1	1
	PSW1	Gold	5	0	0	0	0	0	0	0	0
		Hot solder	5	0	0	2	2	2	2	2	2

4 Cracks consequences for space application

4.1 Influence of the cracks in package on electrical performances

Seven parts with cracks and three parts without cracks were subjected to the leak test and electrical measurement at room temperature, T_{amb}.

All the results are summarized in the Table 3:

Table 3. Summary about TC

Step	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10
Test matrix	B2 Furnace hot solder	B2 PSW1 gold	B2 Furnace hot solder	B2 PSW1 hot solder	B1 Furnace gold	B1 PSW1 gold	B1 Furnace gold	B1 PSW1 gold	B2 Furnace gold	B2 PSW1 hot solder
Cracks	Y	N	N	Y	Y	Y	Y	Y	N	Y
Hermiticity	Failed	Pass	Pass	Failed	Failed	Failed	Failed	Pass	Pass	Failed
Electrical test at RT (T_{amb})	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

Note: S/N = Sample number.

Almost all parts with cracks were no longer hermetic.

None of the parts exhibited a drift in any of the electrical parameters despite several months of storage between thermal cycling and electrical measurements outside a cleanroom environment and without any specific precautions taken to protect the parts from ambient atmospheric conditions.

Table 4. **Electrical tests results before and after TC**

Parameter	Step	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10
I_{EB} at 5 V (A) < 1 µA	Before TC	2.2E-10	1.2E-10	1E-10	1.9E-10	1.6E-10	2E-10	1.7E-10	2.2E-10	2.2E-10	1.8E-10
	After TC	1.3E-10	1.9E-10	1.4E-10	1.4E-10	1.4E-10	1E-10	1.4E-10	1.7E-10	2E-10	1.6E-10
I_{EB} at 6 V (A) < 1 mA	Before TC	1.6E-10	1.3E-10	1.4E-10	1.1E-10	8.0E-11	8.0E-11	1.2E-10	1.3E-10	8.0E-11	1.2E-10
	After TC	8.0E-11	1.5E-10	9.0E-11	9.0E-11	1.1E-10	8.0E-11	1.1E-10	1.4E-10	1.5E-10	1.2E-10
I_{CES} at 60 V (A) < 1 µA	Before TC	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10
	After TC	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10
I_{CEO} at 40 V (A) < 50 µA	Before TC	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12
	After TC	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12
BV_{CEO} (V) > 80 V	Before TC	85.73	85.98	85.77	85.78	87.21	88.92	86.98	88.73	85.78	85.55
	After TC	85.85	86.09	86.19	85.89	87.43	89.19	87.15	88.97	86.15	85.96
h_{FE1} at 50 mA 50	Before TC	208.3	213.6	208.3	213.6	195.5	185.8	196.8	187.2	208.3	207.4
	After TC	208.3	215.5	218.3	209.2	196.8	185.8	197.6	187.9	213.6	210.9
h_{FE2} at 2.5 A 70 > x >200	Before TC	162.4	166.2	161.8	166.8	149.9	147.4	150.8	148.3	162.3	161.4
	After TC	161.2	166.5	168.4	162.0	150.1	146.5	150.9	147.4	163.7	163.2
h_{FE3} at 5 A > 40	Before TC	67.5	70.9	67.2	71.0	58.5	62.9	59.4	63.2	67.7	66.8
	After TC	66.9	69.9	69.1	66.6	57.9	61.7	58.9	62.0	64.2	66.8
V_{CESAT} at 5A (V) 1.5 V	Before TC	0.151	0.151	0.151	0.152	0.235	0.164	0.228	0.156	0.154	0.149
	After TC	0.153	0.154	0.156	0.152	0.237	0.167	0.230	0.159	0.154	0.156
V_{CESAT} at 2.5 A (V) > 1.45 V	Before TC	0.271	0.271	0.269	0.273	0.425	0.297	0.418	0.280	0.276	0.266
	After TC	0.273	0.276	0.279	0.272	0.431	0.301	0.421	0.285	0.274	0.279
V_{BESAT} at 2.5 A (V) >1.45 V	Before TC	0.887	0.887	0.888	0.888	0.887	0.888	0.885	0.887	0.888	0.889
	After TC	0.888	0.886	0.882	0.886	0.886	0.887	0.885	0.887	0.880	0.885
V_{BESAT} at 5 A (V) > 2.2 V	Before TC	0.973	0.972	0.973	0.972	0.974	0.973	0.971	0.972	0.972	0.975
	After TC	0.974	0.974	0.970	0.973	0.975	0.975	0.970	0.974	0.970	0.971

4.2 High humidity storage impact on electrical performances

Due to the stringent storage conditions of space equipment and the vacuum environment in orbit, the appearance of cracks in an SMD.5 package during on-ground tests or in orbit does not affect the component's electrical parameters.

However, a temperature-humidity-biased (THB) test at 85 °C/85 % RH was conducted on 10 parts for 168 hours to evaluate the influence of very high humidity in the device cavity on reliability. The bias applied to the parts was V_{CB} = 80 V, which is 80 % of the V_{CBO} and 100 % of the V_{CEO}.

Table 5. Electrical tests results after 168 hours THB

Step	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10
Test matrix	B2 Furnace hot solder	B2 PSW1 gold	B2 Furnace hot solder	B2 PSW1 hot solder	B1 Furnace hold	B1 PSW1 hold	B1 Furnace hold	B1 PSW1 hold	B2 Furnace hold	B2 PSW1 hot solder
Cracks	Y	N	N	Y	Y	Y	Y	Y	N	Y
168 hours THB										
Electrical test at RT	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

The temperature and humidity conditions selected for the test must not be considered relevant for space applications. According to [1]: Lide, David R., ed. (2004). CRC handbook of chemistry and physics (85th ed.). CRC Press. pp. 6–8. ISBN 978-0-8493-0485-9., the relative water content at 85 °C is approximately 25 times higher than the relative humidity content at 20 °C.

Note: [1]: Lide, David R., ed. (2004). CRC handbook of chemistry and physics (85th ed.). CRC Press. pp. 6–8. ISBN 978-0-8493-0485-9.

Electrical measurements after THB are summarized in the Table 6.

Table 6. Electrical measurements after 168 hours THB

Parameter	Step	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10
I_{EB} at 5 V (A)	Before	1.3E-10	1.9E-10	1.4E-10	1.4E-10	1.4E-10	1.0E-10	1.4E-10	1.7E-10	2.0E-10	1.6E-10
< 1 µA	After	3.1E-08	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	2.8E-08	1.0E-10	2.0E-10	1.0E-10
I_{EB} at 6 V (A)	Before	8.0E-11	1.5E-10	9.0E-11	9.0E-11	1.1E-10	8.0E-11	1.1E-10	1.4E-10	1.5E-10	1.2E-10
< 1 mA	After	3.5E-08	1.0E-10	1.0E-10	1.0E-10	2.0E-10	1.0E-10	2.1E-09	1.0E-10	1.0E-10	1.0E-10
I_{CES} at 60 V (A)	Before	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10
< 1 µA	After	6.7E-07	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.7E-07	1.0E-10	1.0E-10	1.0E-10
I_{CEO} at 40 V (A)	Before	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12
< 50 µA	After	1.7E-05	1.0E-12	1.0E-12	1.0E-12	1.0E-12	1.0E-12	9.7E-06	1.0E-12	1.0E-12	1.0E-12
BV_{CEO} (V)	Before	85.85	86.09	86.19	85.89	87.43	89.19	87.15	88.97	86.15	85.96
>80 V	After	85.89	86.32	85.88	85.98	87.48	89.05	87.18	88.99	85.93	86.05
h_{FE1} at 50 mA	Before	208.3	215.5	218.3	209.2	196.8	185.8	197.6	187.9	213.6	210.9
>50	After	207.4	215.2	208.3	210.2	194.5	186.2	197.1	187.2	209.2	204.0
h_{FE2} at 2.5 A	Before	161.2	166.5	168.4	162.0	150.1	146.5	150.9	147.4	163.7	163.2
70>x>200	After	160.9	166.3	161.3	165.3	149.2	146.2	150.8	147.1	162.3	160.2
h_{FE3} at 5 A	Before	66.9	69.9	69.1	66.6	57.9	61.7	58.9	62.0	64.2	66.8
>40	After	66.7	69.8	66.7	68.5	58.1	61.6	58.8	62.1	67.0	65.3
V_{CESAT} at 5 A (V)	Before	0.153	0.154	0.156	0.152	0.237	0.167	0.230	0.159	0.154	0.156
>1.5 V	After	0.153	0.153	0.152	0.154	0.237	0.167	0.230	0.159	0.155	0.151
V_{CESAT} at 2.5 A (V)	Before	0.273	0.276	0.279	0.272	0.431	0.301	0.421	0.285	0.274	0.279
>1.45 V	After	0.275	0.276	0.271	0.277	0.431	0.301	0.421	0.285	0.279	0.270
V_{BESAT} at 2.5 A (V)	Before	0.888	0.886	0.882	0.886	0.886	0.887	0.885	0.887	0.880	0.885
>1.45 V	After	0.889	0.888	0.887	0.889	0.888	0.890	0.885	0.887	0.886	0.888
V_{BESAT} at 5 A (V)	Before	0.974	0.974	0.970	0.973	0.975	0.975	0.970	0.974	0.970	0.971
>2.2 V	After	0.976	0.974	0.974	0.973	0.976	0.975	0.971	0.974	0.972	0.976

None of the parts exhibit an out-of-specification measurement after 168 hours of THB, which is an extremely severe storage condition. This condition cannot be compared with the cleanroom storage condition recommended for parts mounted on a PCB for space applications. It is observed that only the leakage current deviates from initial values, while all other parameters remain stable.

5 Cracks consequences for high-reliability applications other than space

5.1 Evaluation of cracks in package on electrical performances and reliability

To assess the impact of cracks in a package for high-reliability applications exposed to high humidity levels, the THB (85 °C/85 % RH) test was extended to 1000 hours on seven parts with cracks and three parts without cracks.

All the results are summarized in the Table 7:

Table 7. Reliability tests results

Step	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10
Test matrix	B2 Furnace Hot solder	B2 PSW1 Gold	B2 Furnace Hot solder	B2 PSW1 Hot solder	B1 Furnace Gold	B1 PSW1 Gold	B1 Furnace Gold	B1 PSW1 Gold	B2 Furnace Gold	B2 PSW1 Hot solder
Cracks	Y	N	N	Y	Y	Y	Y	Y	N	Y
168 hours THB										
Electrical test at RT	Failed	Pass	Pass	Failed	Pass	Pass	Failed	Pass	Pass	Pass
Electrical test with temp sweep	Failed	Pass	Pass	Failed	Pass	Pass	Failed	Pass	Pass	Pass
168 hours THB										
Electrical test at RT	Failed	Pass	Pass	Pass	Pass	Pass	Failed	Pass	Pass	Pass
Electrical test with temp sweep	Failed	Pass	Pass	Pass	Pass	Pass	Failed	Pass	Pass	Pass
12 hours vacuum at 5 mbar										
Electrical test at RT	Failed	Pass	Pass	Pass	Pass	Pass	Failed	Pass	Pass	Pass
500 hours THB										
Electrical test at RT	Failed	Pass	Pass	Pass	Pass	Pass	Failed	Pass	Pass	Pass
Electrical test with temp sweep	Failed	Pass	Pass	Pass	Pass	Pass	Failed	Pass	Pass	Pass
12 hours vacuum at 5 mbar										
Electrical test at RT	Failed	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
Internal visual inspection	Color ++	Color +	Color +	Color +	Color -	Color +	Color ++	Color +	Color +	Color +

1. *Abnormal measurements are probably linked to contact issue.*

5.2 Graphs of the room temperature electrical measurements

All the room temperature electrical measurements results are shown on the following graphs.

Figure 4. I_{EB} at 5 V

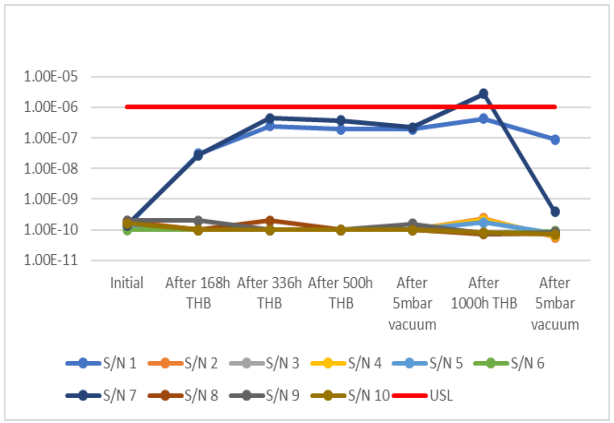


Figure 5. I_{EB} at 6 V

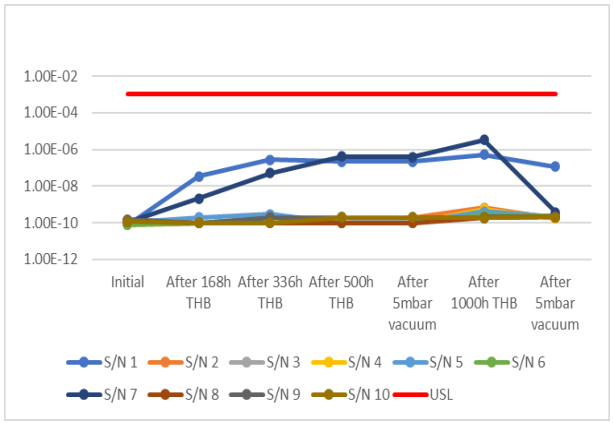


Figure 6. I_{CEO} at 40 V

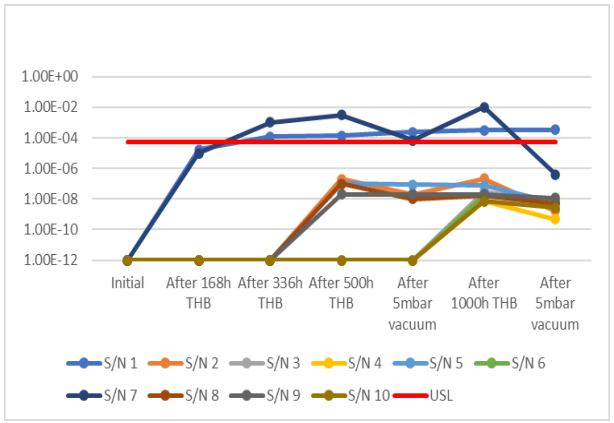


Figure 7. I_{CES} at 60 V

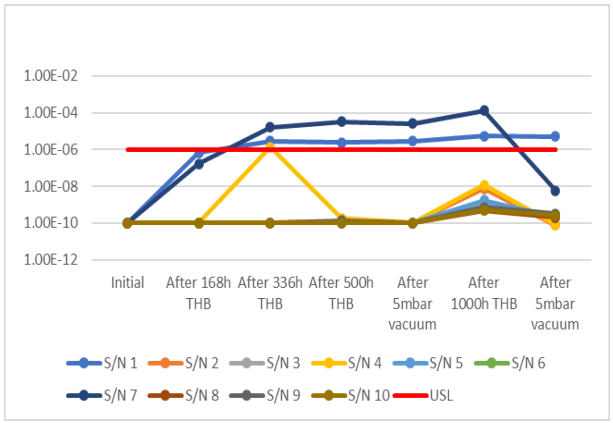


Figure 8. BV_{CEO}

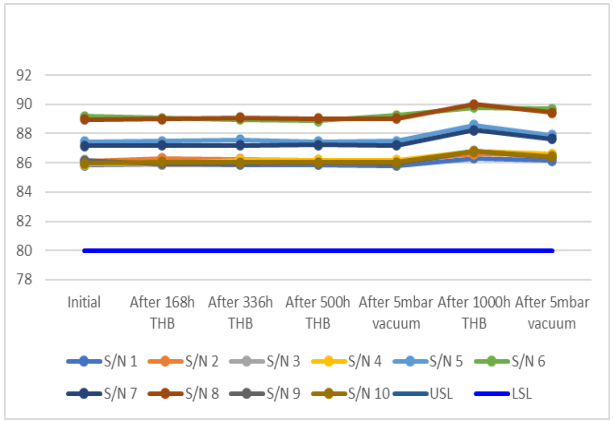


Figure 9. h_{FE1} at 50 mA

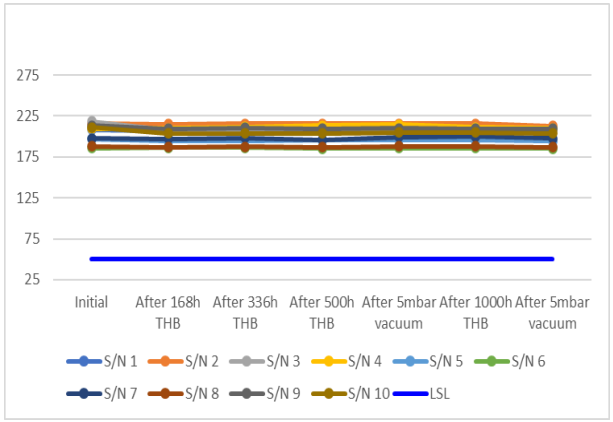


Figure 10. h_{FE2} at 2.5 A

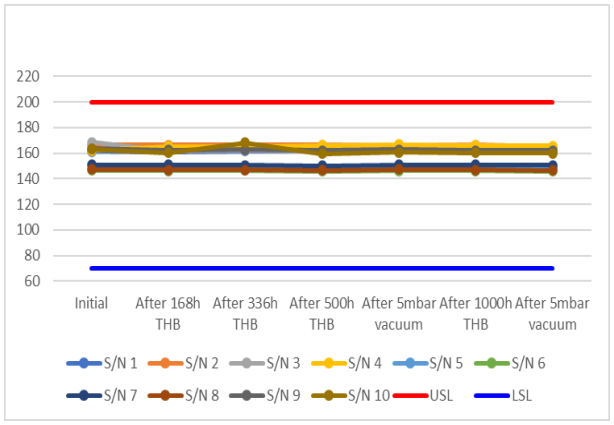


Figure 11. h_{FE3} at 5 A

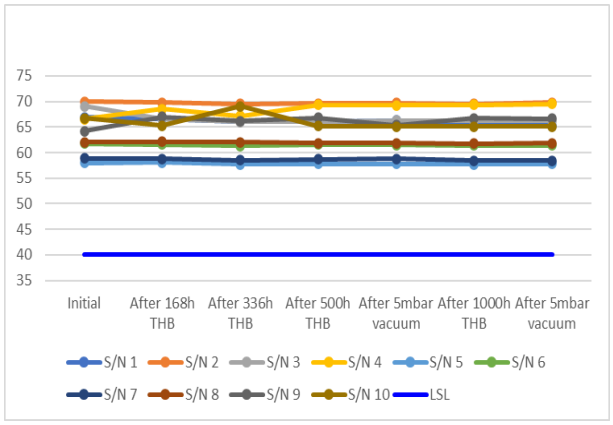


Figure 12. V_{CESAT} at 5 A

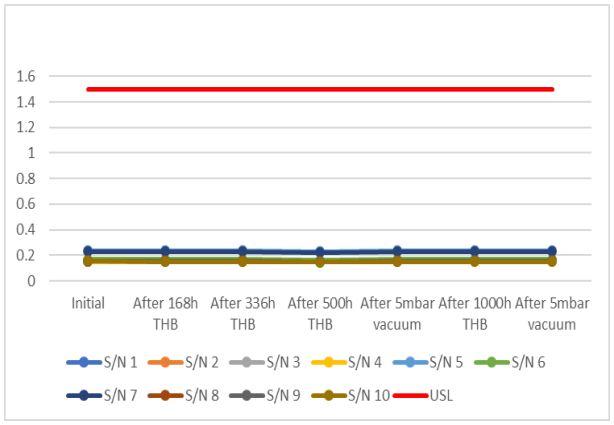


Figure 13. V_{CESAT} at 2.5 A

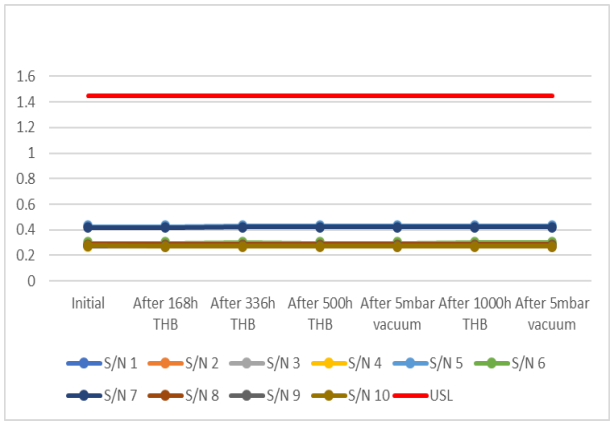


Figure 14. V_{BESAT} at 2.5 A

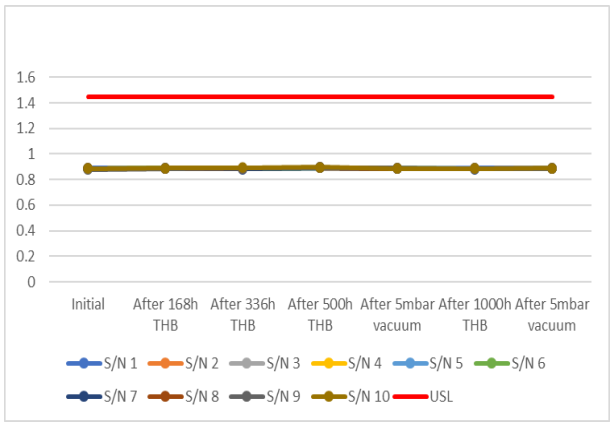
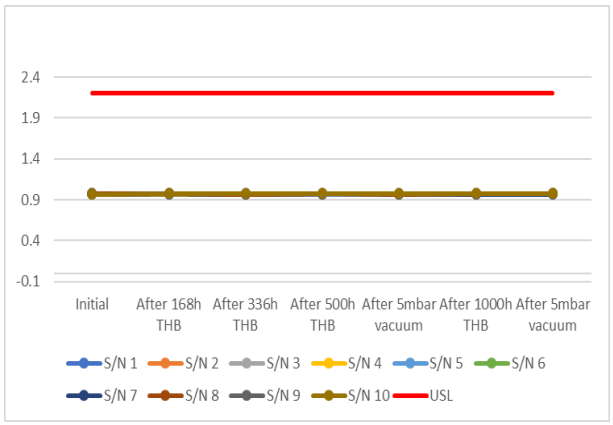


Figure 15. V_{BESAT} at 5 A



All parameters remain within the specification, except for leakage currents on two parts. These currents slightly exceed the specification limits after the first 500 hours of THB and remain stable throughout the following stress steps. One of the two parts recovers and returns to the specification after the final submission to a 5 mbar vacuum.

Even though the leakage currents increase, neither the gains nor the breakdown voltages are affected and remain stable within the specification limits. The slight deviation of leakage current from the specification is not expected to cause early failure of the part.

5.3 Internal visual inspections

Following reliability tests, the parts were de-encapsulated to perform an internal visual inspection. An orange color more or less marked is visible on the die pads on all parts.

Figure 16. S/N 1: Trace on the wires

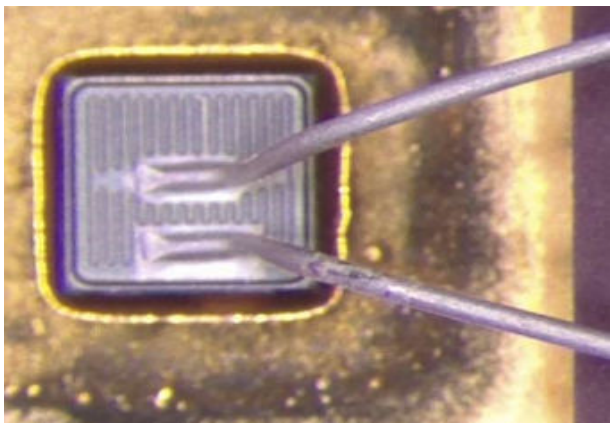


Figure 17. S/N 1bis: Color on pads

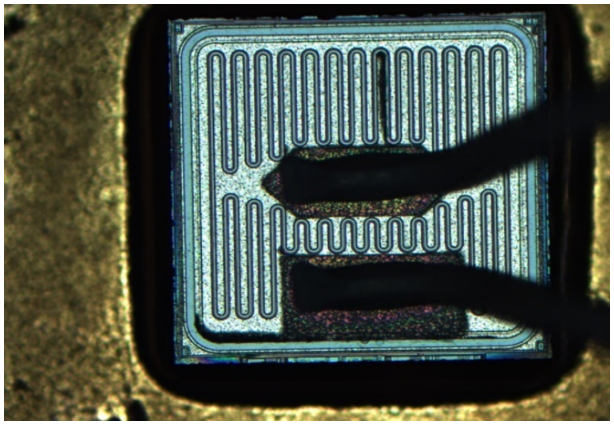


Figure 18. S/N 2: Slight color on pads

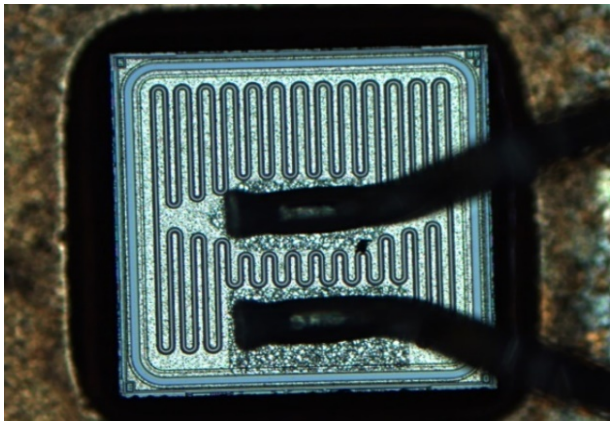


Figure 19. S/N 3: Slight color on pads

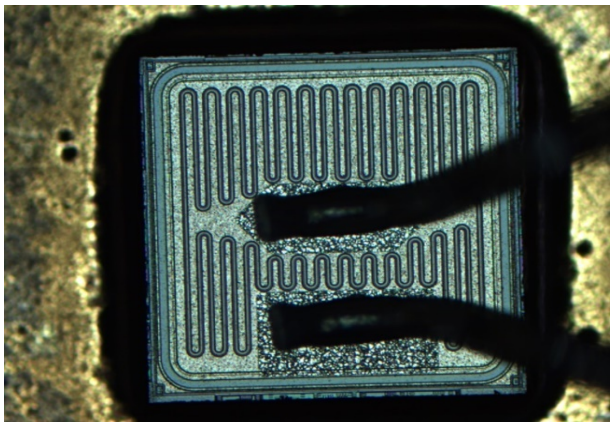


Figure 20. S/N 4: Slight color on pads

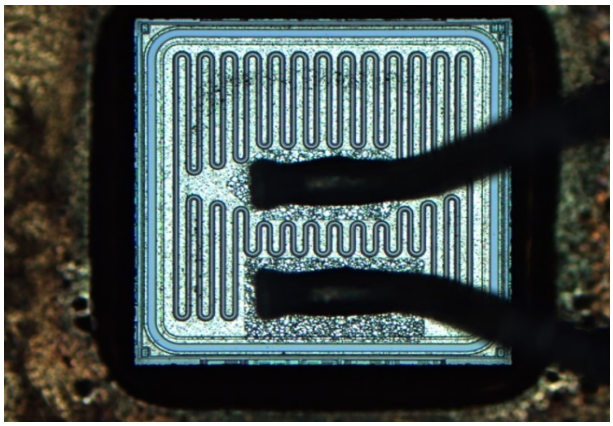


Figure 21. S/N 5: Slight color on a small part of one pad

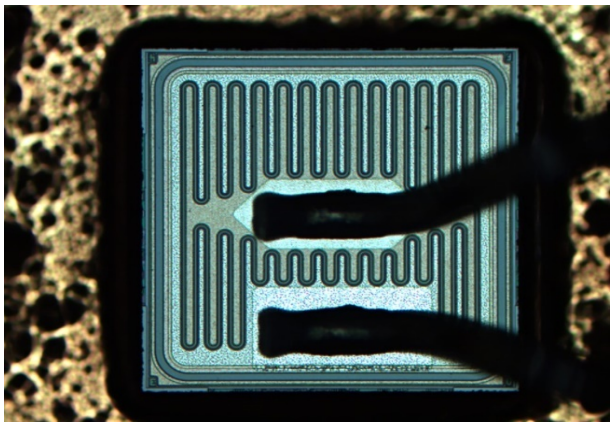


Figure 22. S/N 6: Slight color on pads

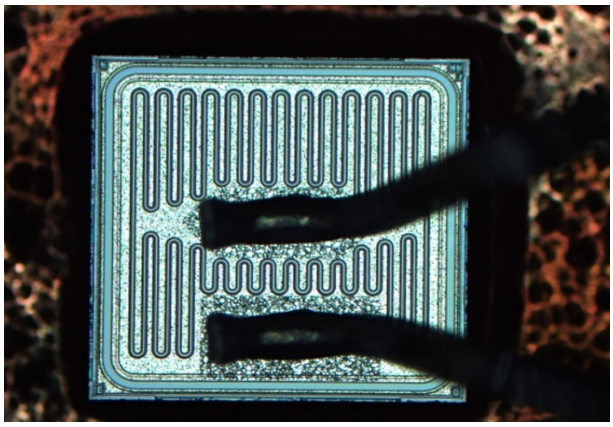


Figure 23. S/N 7: Color on pads

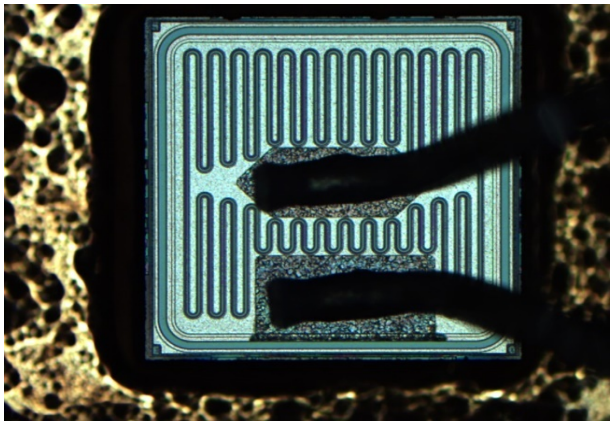


Figure 24. S/N 8: Slight color on pads

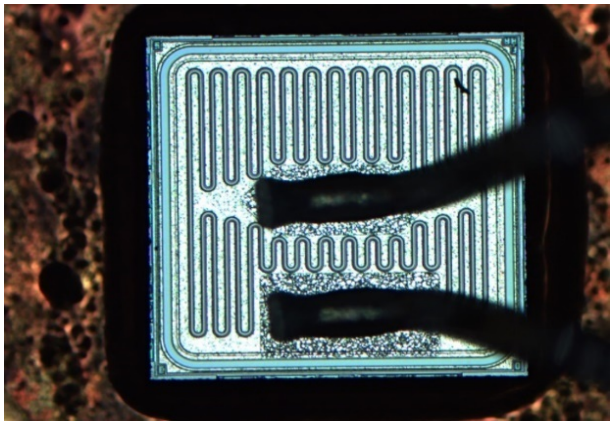


Figure 25. S/N 9: Slight color on pads

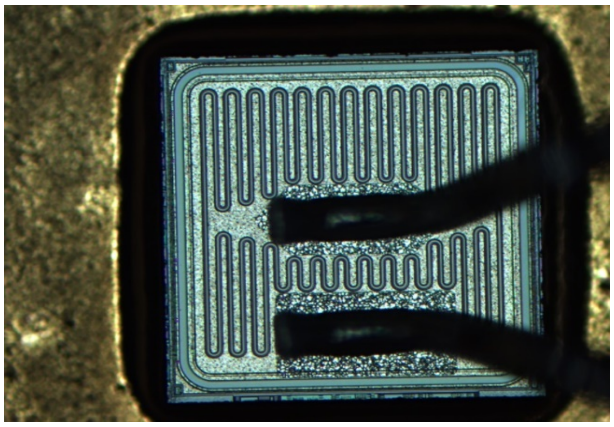
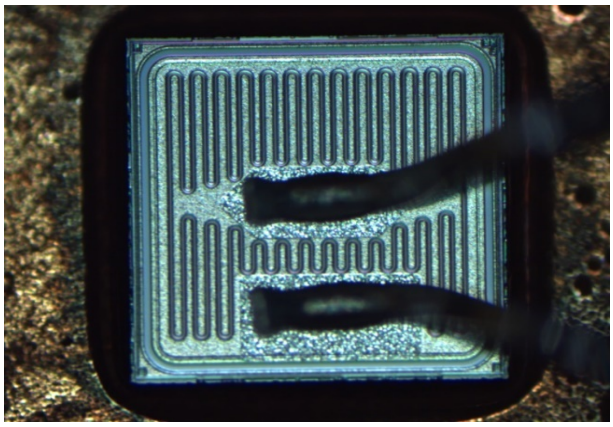


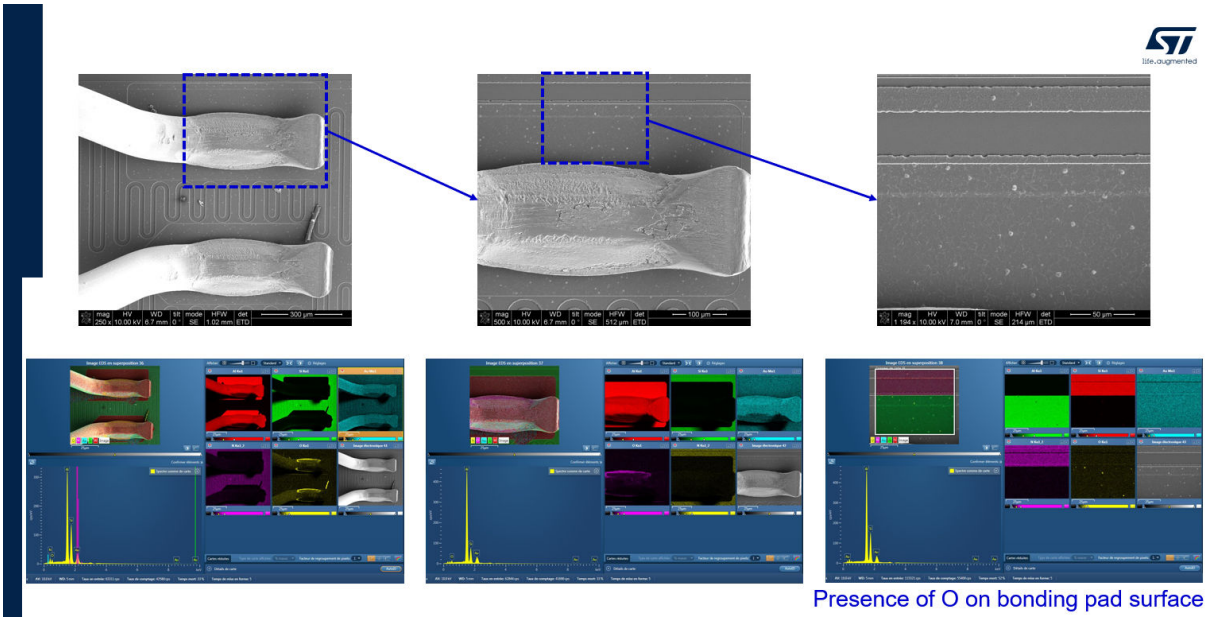
Figure 26. S/N 10: Slight color on pads



5.4 Failure analysis results

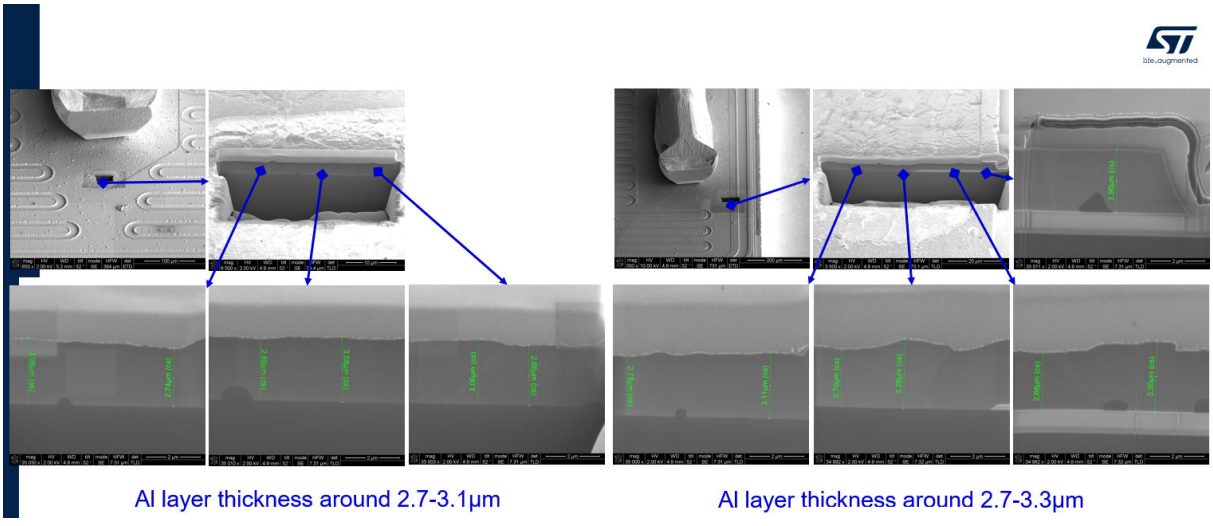
To understand the origin of the pad coloring, an energy dispersive X-ray (EDX) analysis was performed on a sample with a strong orange color (S/N 1). This analysis revealed the presence of oxygen on the bonding pad surface.

Figure 27. SEM/EDX - Sample SN#1



A focused ion beam (FIB) cross-section was conducted to verify whether oxidation compromised the integrity of the metal layer on the pad.

Figure 28. FIB cross-section - Sample #SN8-FE238-n3



The cross-section confirms that oxidation does not reduce the thickness of the metal layer.

6 Coverage by similarity

This study has been conducted on a 2N5154 bipolar transistor. The results obtained from this test vehicle cover the entire STMicroelectronics portfolio assembled in the SMD.5 package because this device represents the worst case in terms of dimensions across different voltages. The critical path lies between the two wires located on the front side of the die.

Below is a comparison of the 2N5154 die and the smallest power MOSFET die from the STMicroelectronics portfolio, both assembled in the SMD.5 package:

Figure 29. **2N5154**

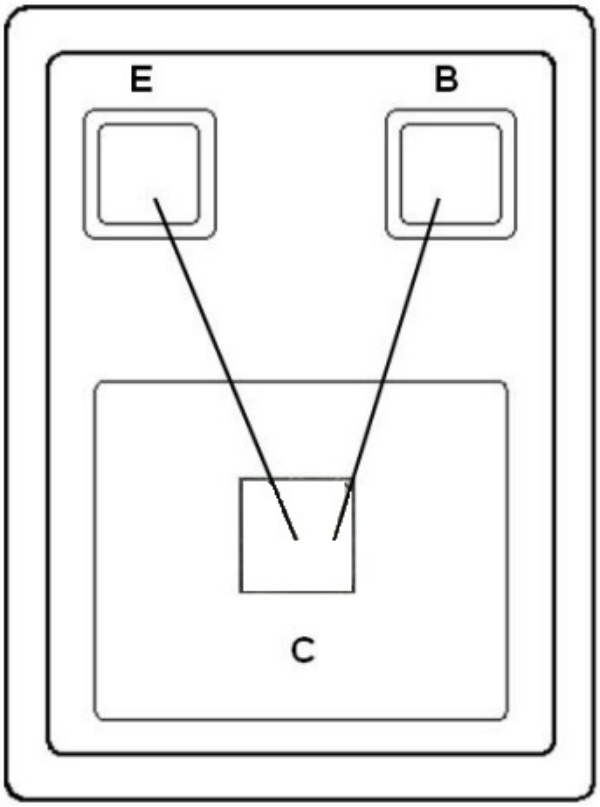
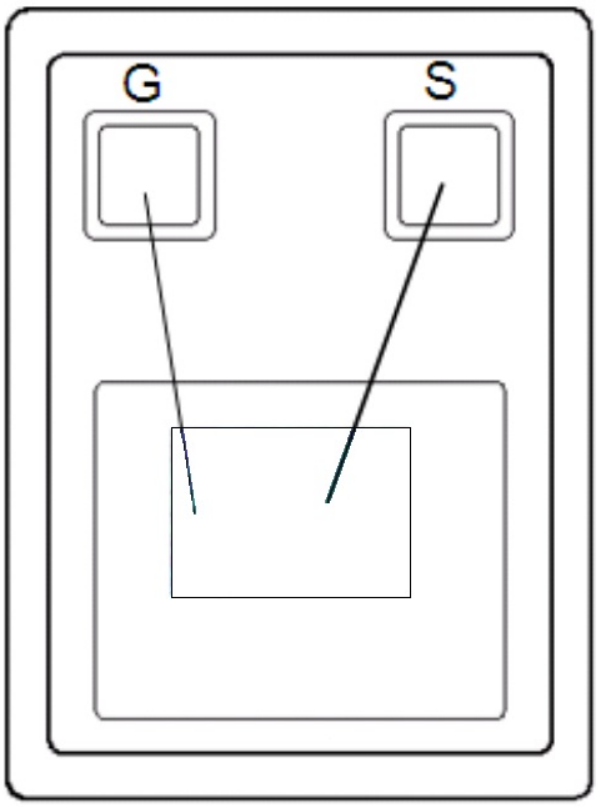


Figure 30. **STRH8N10**



These pictures confirmed this statement. Diodes are assembled with only one wire on the front side, so the wires are not considered as critical.

7 Conclusion

This study aims to identify the root cause of the crack failure's generation in the SMD.5 package during the PCB mounting qualification test. Although the exact root cause of the problem has not been identified yet, it appears to be due to a significant difference in the coefficient of thermal expansion (CTE) of the package materials, which generates excessive stress on the package.

This study shows that:

- The cracks in the SMD.5 shall not appear just after its mounting on the PCB. In case the cracks are present just after the mounting, the issue is related to the mounting process; and it should be optimized according to conditions described in documents such as ECSS-Q-ST-70-38C standard or in on Section 2.1: PCB mounting.
- The cracks may appear during the thermal cycling tests performed as part of the aerospace mounting qualification. This study demonstrates that this should not constitute a defect, as no drifts in the critical electrical parameters are observed when the components are subsequently stored under the recommended conditions for space applications, even over extended periods.

So, for space applications, the potential crack failure generation does not affect the functional reliability of the device.

For other high-reliability applications, a further temperature-humidity-bias (THB) test is performed on the samples, with and without cracks, to assess the effect of some stringent high humidity storage conditions on their critical electrical parameters. Some crack failed samples show a limited drift of their leakage current after the THB test while the other electrical parameters remain stable, thus making possible the use of those products.

As a general conclusion, this extensive study shows the generation of cracks in the ceramic of the SMD.5 package during the qualification TC tests does not affect the functional reliability of the device, regardless of its use in high-reliability applications.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
28-Feb-2023	1	Initial release.
24-Sep-2025	2	Document reworked to improve readability. No content changes.

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