Technical note

L99UDL01 independent channel control

Introduction

The L99UDL01 integrates six half bridges that can be used to control multiple DC motors in current regulation mode.

This technical note is intended to show how to independently control multiple motors.

This is done firstly by describing the mechanism; in a second step, some snapshots taken from a real application have been reported and detailed.

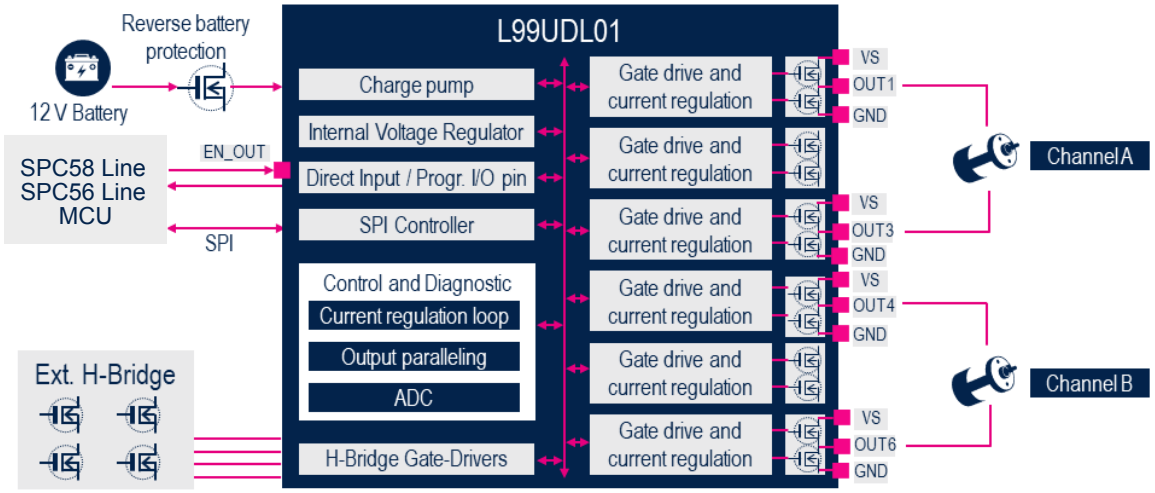
1 Independent channel control description

The L99UDL01 features six fully protected and programmable half bridges that can be configured to drive multiple DC motors in different applications.

With the purpose to simplify the description of the procedure to make the L99UDL01 independently control different channels, let us connect two DC motors by means of four of the six integrated half bridges, referring to channel A for the pair of half bridges (1 and 3) to control the first DC motor and channel B for the pair of half bridges (4 and 6) to control the second DC motor.

The figure below shows the main blocks composing the device and the chosen architecture previously described.

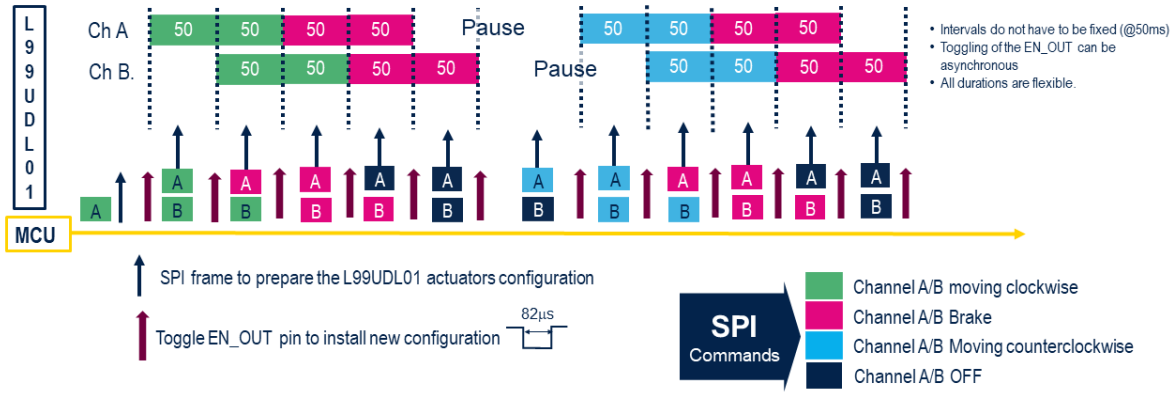
Figure 1. L99UDL01 block diagram



To make independent the driving of the multiple motors (for example each of the half bridges can be activated/ deactivated independently from the other ones), a dedicated procedure shall be implemented.

The figure below reports the procedure implemented.

Figure 2. Multiple motor smart control



Controlling a DC motor means mainly driving the following actions:

- moving the DC motor clockwise
- braking the DC motor
- moving counterclockwise the DC motor and switching OFF the DC motor

Each of these actions are performed by properly switching ON and OFF the high sides and the low sides of all the half bridges of the two channels A and B.

The L99UDL01 current regulation control allows to each of the half bridge to provide a predefined level of current (from 1A to 4A) for a predefined interval of time (from 100 ms to 1 second).

Referring to Figure 2. Multiple motor smart control, let's suppose to initially activate channel A for 50 ms; this is achieved by means of a predefined SPI configuration which can be transferred from the MCU to L99UDL01 at any moment. The activation for 50 ms of the channel A is triggered by the rising edge of the EN-OUT pin driven by a dedicated GPIO of the MCU.

The toggling (falling and rising) of the EN_OUT pin can be performed in a time interval that typically lasts 64 µs and that shall be at least of 82 µs (max value). This comes from the below reported parameter (t_{EN}) defined in L99UDL01 datasheet:

Table 1. EN_OUT filter time

Req ID	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
B.004	t_{EN}	EN_OUT filter time	Rising and falling edge of EN_OUT tested by scan		64	82	µs

During this toggling interval, all the outputs are switched OFF and, at the EN_OUT rising edge, the SPI configuration previously transferred from the MCU to L99UDL01 is actuated.

This means that (referring to Figure 2. Multiple motor smart control) after the first toggling of the EN_OUT pin, channel A starts to move clockwise.

Once the first configuration is actuated, the MCU can prepare and transfer via SPI to L99UDL01 the new configuration. At the completion of the second EN_OUT toggling, channel A continues to move clockwise and channel B starts to move clockwise too; it is important to say here that, if any configuration for channel A is transferred from the MCU, the EN_OUT toggling mechanism triggers the previous configuration (in this case channel A motor moves clockwise).

The third toggling triggers the previously transferred SPI configuration which brakes the channel A and maintain unchanged the configuration of channel B, which continues to move clockwise.

Clearly the mechanism continues in this way.

2 Test and measurements

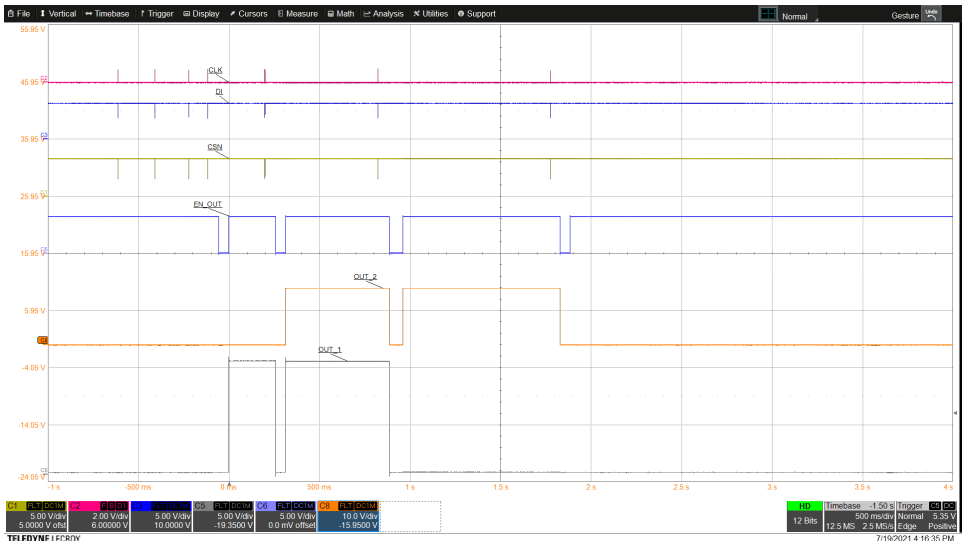
The following section is intended to report some snapshots from the oscilloscope done when controlling multiple motors with L99UDL01.

For this test, the following test equipment has been used:

- EVAL-L99UDL01 (evaluation board for L99UDL01)
- STSW-L99UDL01 (graphical user interface for L9UDL01)
- oscilloscope

The figure below shows all the signals involved in the procedure to independently control the L99UDL01 channels:

Figure 3. SPI configuration EN_OUT toggling and OUT1/OUT2 activations



At each step of the procedure, the SPI configuration is initially done; this is highlighted in the channels C1 (CSN), C2 (CLK) and C3 (DI) of the oscilloscope which are activated before the EN_OUT toggling.

The EN_OUT toggling (channel C6 of the oscilloscope) comes in a second step of the procedure and it is driven directly from the L99UDL01 GUI via a GPIO of the MCU directly connected to EN_OUT pin.

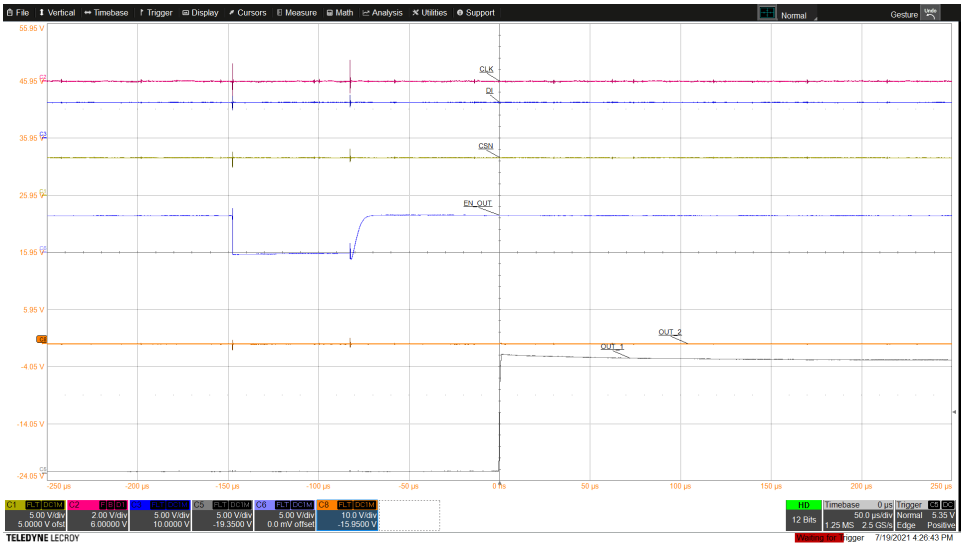
As described in the previous section, the EN_OUT toggling shall last for a time higher than t_{EN}, but to highlight the functional behavior of the mechanism, for the test here reported the EN_OUT toggling duration has been set to about 50 ms.

From Figure 3. SPI configuration EN_OUT toggling and OUT1/OUT2 activations it is evident that:

- the first EN_OUT toggling of the test activates only the OUT1
- the second EN_OUT toggling activates OUT2, keeping ON the OUT1
- the third EN_OUT toggling switches OFF the OUT1, keeping ON the OUT2
- the fourth EN_OUT toggling switches OFF the OUT2

For all the actuations, the MCU sends the SPI configuration to L99UDL01 well before triggering the EN_OUT toggling.

Figure 4. EN_OUT toggling interval and delay vs OUT1/OUT2 activation/deactivation



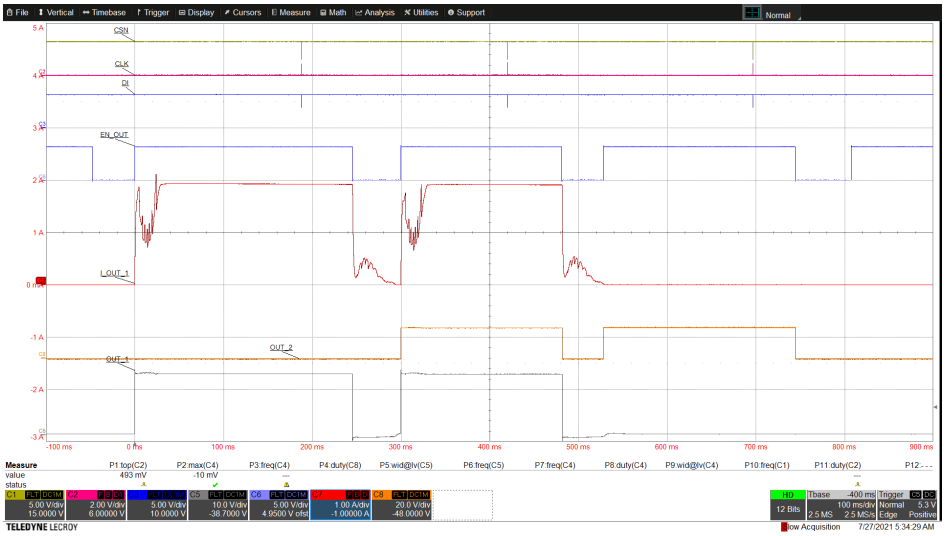
In the figure above the timing involved in the independent channel control procedure is highlighted by detailing the timing required for a single actuation (as the one described in the previous example: SPI configuration -> EN_OUT toggling -> OUT1 switch ON).

From the rising edge of the EN_OUT signal to the activation of the OUT1 signal there is another delay which can be evaluated roughly in around 70 µs.

Adding this delay with the t_{EN} time limiting the EN_OUT toggling interval it is evident that a total interval of around 150 µs is needed to complete the procedure.

It is important to notice that only during the EN_OUT toggling interval (i.e. when the EN_OUT signal is low, around 80 µs) all the outputs are switched OFF.

Figure 5. Test with a real motor connected to OUT1



In the figure above the waveforms when a real motor is connected to OUT1 are reported. In this specific case the OUT1 is set in current mode at 4A, but a load requiring approximately 2A in its inrush and stall phases is connected. Waveform C7 shows the behavior of the current on OUT1 during the different phases of the independent channel control mechanism.

3 Conclusion

The six half bridge drivers integrated in L99UDL01 can be independently controlled.

In this document the procedure for the independent control of the L99UDL01 integrated half bridges has been described, detailing the delays introduced at each channel actuation.

4 Document references

- L99UDL01 datasheet
- EVAL-L99UDL01 data brief
- STSW-L99UDL01 user manual

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
14-Sep-2021	1	Initial release.

Contents