SPC58xx System Integration Unit Lite 2 pin multiplexing and port configuration

Introduction

The SPC58xx is a family of Power Architecture® based microcontrollers that targets automotive vehicle body and gateway applications such as central body controller, smart junction box, mid and high end gateway.

This document explains the SPC58xx I/O pad and pin muxing configuration which is implemented by means of MSCRs registers in the System Integration Unit Lite SIUL2.

All the information needed for correct MSCR register configuration is available in the Microsoft Excel® workbook files available in the technical note specific for each family device, whose title is: "SPC58XXx I/O definition: signal description and input multiplexing tables".

1 SIUL2 – System Integration Unit Lite 2

The System Integration Unit Lite 2 (SIUL2) is a SPC58xx module that controls the MCU pad configuration, ports, general-purpose input and output signals and external interrupts with trigger event configuration.

This document focuses on the pad and pin muxing configuration. In particular, it explains the correct configuration of the SIUL2 Multiplexed Signal Configuration Register (SIUL2_MSCR), getting the required information from the SPC58xx_IO_Definition spreadsheet Microsoft Excel® file available in the technical note "SPC58XXx IO definition: signal description and input multiplexing tables".

In the rest of this document, this SPC58xx_IO_Definition excel file is referred to as *I/O spreadsheet*.

The SIUL2_MSCR registers control the I/O pin function and electrical properties for each pin on the device and are used to select the input signal for IP blocks on the device that have multiple input sources.

There is a dedicated SIUL2_MSCR register for each I/O pin on the device.

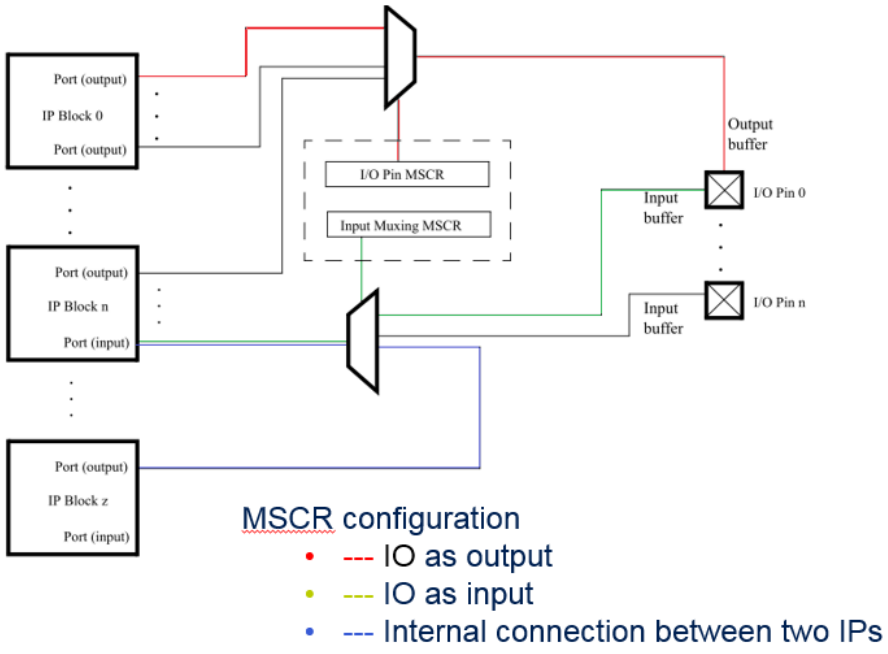
1.1 I/O pin configuration and IPs block source selection

Each pin of an SPC58XX device is connected to port control logic. The signal data flow from device IP blocks to I/O pins and the signal data flow from IP block to another IP block are shown in Figure 1. The SIUL2_MSCR registers control the above mentioned connections.

The SIUL2_MSCRs are divided in two sets of registers:

- SIUL2_MSCR_IO_n with n from 0 to 511 (I/O pin control registers) are used to configure a device pin as input or output. It is possible to set:
  - pad electrical properties controlling the drive strength, output drive circuit, pullup/down, input buffer enable, input level selection, and safe-mode operation of the associated I/O pin;
  - the output function on the associated output pin;
  - the pin as general purpose input.
- SIUL2_MSCR_MUX_n with "n" = 512… 1023 (Multiplexed input selection registers) are used to configure input for IP blocks. It is possible to select:
  - the input source for IP blocks that have input from multiple sources; the sources can be either IP blocks or I/O pins.

Figure 1. Signal data flow from device IP blocks to IO pins and from IP block to IP block



1.2 Pad electrical characteristics and output pin function configuration

The I/O pad electric configuration for input/output signals and output function configuration is done via the SIUL2_MSCR_IO_n registers.

The Figure 2 shows the SIUL2_MSCR_IO_n register bit fields. The Table 1 shows SIUL2_MSCR_IO_n fields description.

Figure 2. SIUL2_MSCR_IO_n register

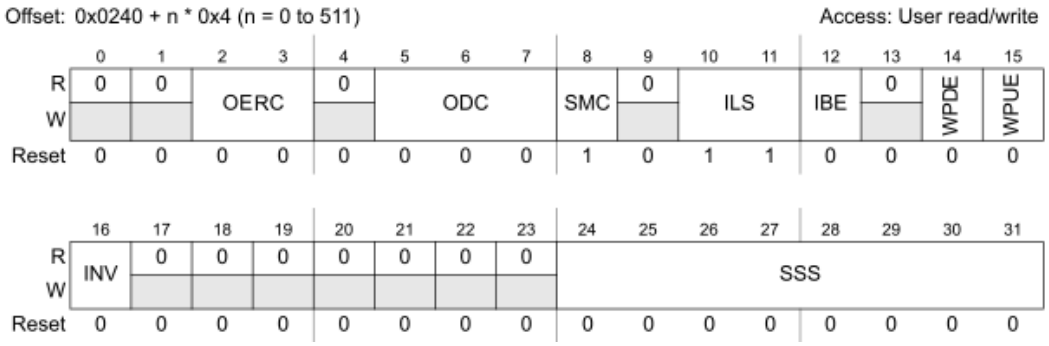


Table 1. SIUL2_MSCR_IO_n fields description

Bit Field	SIUL2_MSCR_IO_n fields description
OERC Bit 2:3	Output Edge Rate Control Specifies the output impedance, drive strength and slew rate of the associated pin. Refer to Output Impedance columns **I** in the excel spreadsheet for the applicable edge rates for each I/O pin on the device. See the device data sheet for the electrical characteristics of the weak, medium, strong and very strong pad types: • 00 - Weak drive • 01 - Medium drive • 10 - Strong drive • 11 - Very Strong drive
ODC Bit 5:7	Output Drive Control Specifies the type of output drive control for the associated pin: • 000 - Output buffer disabled • 001 - Open-drain • 010 - Push-pull • 011 - Open-source • 100 - Microsecond Channel LVDS • 101 - LFAST LVDS • 110 - Reserved • 111 - Reserved
SMC Bit 8	Safe Mode Control Specifies whether the chip disables the pin's output buffer when the chip enters: • 0 - Disable (the output buffer returns to its previous state when the chip leaves Safe mode). • 1 - Don't disableSafe mode. Resets to 0 except for PB[11] ERROR0 pin which resets to 1.
ILS Bit 10:11	Input Level Selection Specifies the logic family for the associated pin, which determines its logic switching levels. See the device data sheet for the electrical characteristics of the I/O pad input buffer types: • 00 - Reserved • 01 - TTL (CMOS for LP pads) • 10 - LVDS • 11 - CMOS

Bit Field	SIUL2_MSCR_IO_n fields description
IBE Bit 12	Input Buffer Enable Enables the associated pin's input buffer: • 0 - Disabled • 1 - Enabled When an I/O pin is configured as a single-ended input, the input buffer must be enabled for the pin using the MSCR[IBE] bit. This enables the input to all input destinations connected to the pin, including the GPIO input. In this way, the GPIO can be read at any time, regardless of the pin function. For IP blocks that have multiple input sources, the input source is selected in the multiplexed input selection MSCRs, SIUL2_MSCR_MUX_n, and the associated I/O pin MSCR for the selected input must have the MSCR[IBE] bit enabled.
WPDE Bit 14	Weak Pulldown Enable Used only when the associated destination is a chip pin. Enables the associated pin's weak pulldown resistor. It is OK for both WPDE and WPUE to be enabled, if they are on analog input pads, that pad is configured with Strong pulldown. On digital pads this configuration means neither a pullup nor a pulldown: • 0 - Disabled • 1 - Enabled
WPUE Bit 15	Weak Pullup Enable Used only when the associated destination is a chip pin. Enables the associated pin's weak pulldown resistor. It is OK for both WPDE and WPUE to be enabled, if they are on analog input pads, that pad is configured with Strong pulldown. On digital pads this configuration means neither a pullup nor a pulldown: • 0 - Disabled • 1 - Enabled
INV Bit 16	Invert The output selected by the corresponding MSCR SSS field can be inverted before it is driven on the I/O pin with the INV bit: • 0 - The output selected by the SSS field is not inverted before being driven to the pin. • 1 - The output selected by the SSS field is inverted before being driven to the pin. *Note: Use of the INV bit is not supported when the ODC is configured for open-drain or open-source modes, and the output data will not be as expected for an inverted open-drain or open-source connection.*
SSS Bit 24:31	Source Signal Select Selects which source signal is connected to the associated destination (chip pin or module port). For a chip pin, the source signals are outputs from module ports. For a module port, the source signals are either outputs from module ports or inputs from chip pins.

Note: Not all pads have all bits, not all pads have all possible output drive control (ODC) or input level selection (ILS) configuration.

All the bitfields in the I/O SIUL2_MSCR_IO_n registers described above are applicable for all the GPIO ports on the device. This includes all ports on the device with digital output function.

For ADC input ports, the OERC, ODC, SMC, INV and SSS bits/fields do not apply. The SSS is always 8b0 for input only ports, enabling the general purpose input function. The analog input path is enabled in the ADC logic when the channel is selected for conversion.

1.3 Input source for SPC58x IP blocks

The input sources for IP blocks coming from others IP blocks or from I/O pins are selected by SIUL2_MSCR_MUX_n registers shown in the Figure 3. The Table 2 shows SIUL2_MSCR_MUX_n bit filed description.

Figure 3. SIUL2_MSCR_MUXn registers

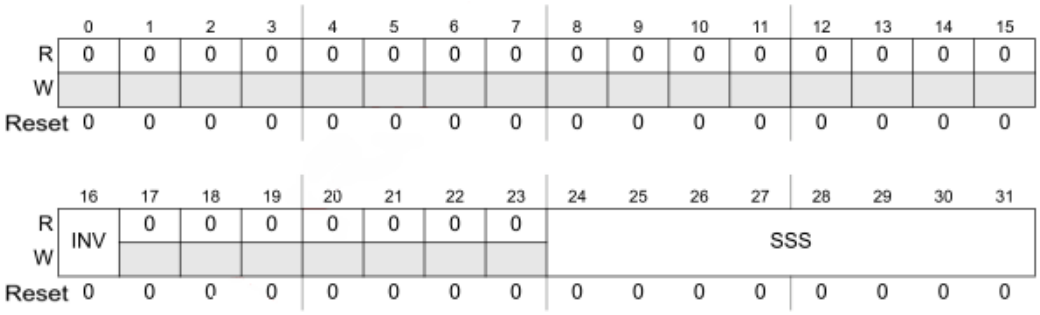


Table 2. SIUL2_MSCR_MUX_n bit fileds description

Bit Fields	SIUL2_MSCR_MUX_n bit filed description
INV Bit 16	Invert The input source signal selected by the corresponding SSS field for this MSCR can be inverted before it connects to the destination input with the INV bit: • 0 - SSS selected input signal is connected directly to the destination input. • 1 - SSS selected input signal is inverted before it is connected to the destination input.
SSS Bit 24:31	Source Signal Select Selects which source signal is connected to the associated destination (chip pin or module port). For a chip pin, the source signals are outputs from module ports. For a module port, the source signals are either outputs from module ports or inputs from chip pins. The meaning of each value depends on the destination.

2 Pad and pin muxing configuration

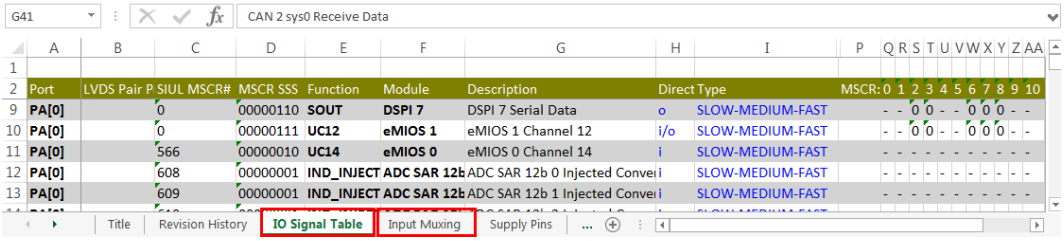
2.1 I/O spreadsheet

I/O spreadsheet file, attached to *SPC58xx I/O definition: signal description and input multiplexing Tables* technical note, is composed of several tabs.

For pad and pin muxing configuration purposes, the following two Tabs, highlighted in the Figure 4, has to be considered:

- *I/O Signal Table Tab*
- *Input Muxing Tab*

Figure 4. I/O spreadsheet Tabs: I/O Signal Table and Input Muxing



2.2 Output pin configuration

The output from an IP block to an external IO pin of device is controlled configuring *SIUL2_MSCR_IO_n* registers (n = 0 to 511) and getting the needed information from I/O Signal Table Tab in the I/O spreadsheet

The columns of I/O Signal Table Tab to be used for the port pad and I/O pin configuration are highlighted with a red square in the Figure 5:

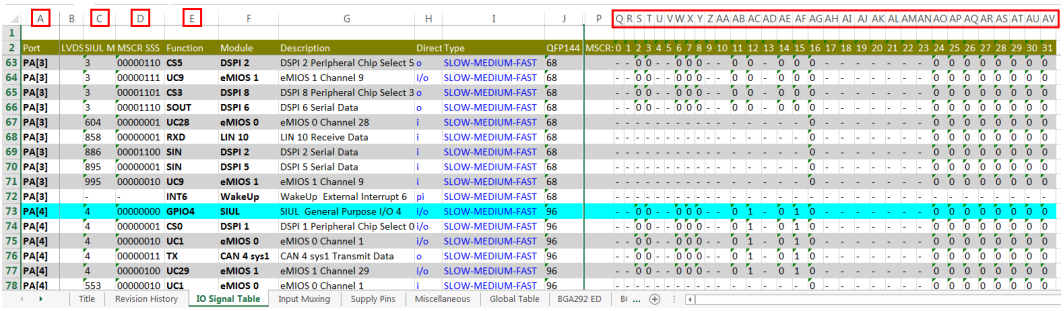
- Column **E**: there is the list of functions that can be assigned to port PX[Y].

  The selected function chosen in column **E** is set in SIUL2_MSCR_IO_n register using the correspondent SSS field available in column **D**.
- Column **C**: The specific SIUL2_MSCR_IO_n register to be set (in other words the n to be chosen) for the selected function and port has to be taken from column **C**.

  If in column C the read value is between 0 to 511 (SIUL MSCR# = 0..511), the associated register to be configured is SIUL2_MSCR_IO_n; if the read value is between 512 to 1023 (SIUL MSCR# = 512..1023) the associated register is SIUL2_MSCR_MUX_n.
- The columns from **Q** to **AV** in the IO Signal Table Tab are the default values of the bit fields of the SIUL2_MSCR_IO_n. The default values are applied to all GPIO pins on the devices.

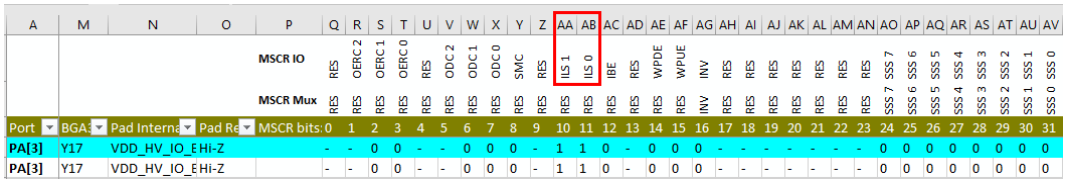
  Wherever in the spreadsheet there is the symbol "–", that functionality is non configurable. All bits not marked with the "–" symbol are applicable for all GPIO ports on the device.

Figure 5. Columns to be used for SIUL2_MSCR_n configuration



The Figure 6 shows the correspondence of columns from **Q** to **AV** in the I/O Signal Table Tab and the bitfields in SIUL2_MSCR registers. So for example the default value of the ILS field of SIUL2_MSCR_IO_n register is available in columns **AA** and **AB**.

Figure 6. SIUL2_MSCR_IO_n bit fields default values available in column Q to AV in the IO signal table Tab



In the following there are 2 examples of SIUL2_MSCR_IO configuration::

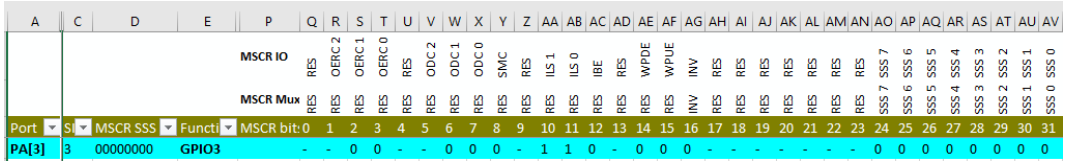
- Example 1: PA[3] configured as output with function chip select 5 on pin 68 of QFP144;

Example 1	Configure PIN 68, PA[3] port as Output. Associated function: chip select 5 for DSPI2.
Register configuration	SIUL2_MSCR_IO_ 3 = 0x02000006
	Details: SIUL2.MSCR_IO_3.ODC = 0x2 (0b010 - Output pin in Push-Pull configuration). SIUL2.MSCR_IO_3.SSS = 0X06 (0b0000_0110 - SPI_2_CS 5).

Port	LVDS Pair Port	SIUL MSCR#	MSCR SSS	Function	Module	Description	Direction	QFP144
PA[3]		3	00000110	**CS5**	**DSPI 2**	DSPI 2 Peripheral Chip Select 5	o	68

- Example 2: Reading SIUL2_MSCR_IOn register default values.

Example 2	Reading of the default value of *SIUL2_MSCR_IO_ 3* register from IO spreadsheet.
Register configuration	Columns S.T = 0.0 → **OERC** = 00 → weak drive. Columns V.W.X = -.0.0 → **ODC** = -00 output buffer is disabled. Columns Y = 0 → **SMC** = 0 the output buffer returns to its previous state when the chip leaves Safe mode). Columns AA.AB = 1.1 → **ILS**= Input Level Selection CMOS. Columns AC = 0 → **IBE** = 0 Input buffer disabled. Columns AE.AF = 0.0 → **WPUE** = 0 **WPDE** = 0, weak pull up/down disabled. Columns AG = 0 → **INV**=0 à The output selected by the SSS field is not inverted before being driven to the pin. From Column AO to AV = 0 → **SSS** = 0 GPIO function selected.



2.3 Input configuration

The Input signals to device IP blocks can be selected from external I/O pins or from other internal IP blocks, by properly configuring SIUL2_MSCR_MUX_n registers.

To configure SIUL2_MSCR_MUX_n (n = 512..1023) registers, the user gets the needed information from I/O Signal Table Tab and/or Muxing Tab if the input signal to IP block is from external I/O pin and from the Input Muxing Tab, if the input signal is from another IP block.

Input source from external pin

The column **H** of I/O Signal Table Tab indicates the direction, I/O or I, of the signal for the correspondent port. Setting IBE = 1, in SIUL2_MSCR_IO_n register, these signals are routed to the functions as inputs. In most cases, when the IBE is set, the signal will be routed to the input of an IP block and also the SIUL2_MSCR_MUX_n register has to be set.

Figure 7. I/O pin direction in column H - I/O Signal Table tab

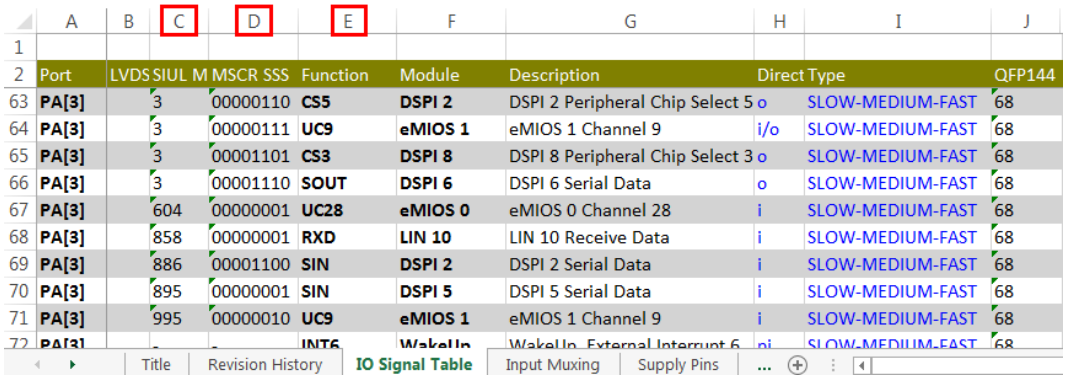
	A	G	H	I
1				
2	Port	Description	Direct	Type
57	**PA[3]**	SIUL General Purpose I/O 3	i/o	SLOW-MEDIUM-FAST
58	**PA[3]**	CAN 5 sys1 Transmit Data	o	SLOW-MEDIUM-FAST
59	**PA[3]**	LIN 1 Transmit Data	o	SLOW-MEDIUM-FAST
60	**PA[3]**	DSPI 5 Serial Data	o	SLOW-MEDIUM-FAST
61	**PA[3]**	DSPI 2 Serial Data	o	SLOW-MEDIUM-FAST
62	**PA[3]**	eMIOS 0 Channel 28	i/o	SLOW-MEDIUM-FAST
63	**PA[3]**	DSPI 2 Peripheral Chip Select 5	o	SLOW-MEDIUM-FAST
64	**PA[3]**	eMIOS 1 Channel 9	i/o	SLOW-MEDIUM-FAST
65	**PA[3]**	DSPI 8 Peripheral Chip Select 3	o	SLOW-MEDIUM-FAST
66	**PA[3]**	DSPI 6 Serial Data	o	SLOW-MEDIUM-FAST
67	**PA[3]**	eMIOS 0 Channel 28	i	SLOW-MEDIUM-FAST

SIUL2_MSCR_MUX_n registers with n from 512 to 1023 select which IP block function is connected to the associated input pin.

With reference to the Figure 8:

- the list of IPs block functions is available in the column E of IO Signal Table TAB.
- The selected function is set via the SSS field in SIUL2_MSCR_MUX_n, the value of the SSS field value is gotten from column D.
- The SIUL2_MSCR_MUX_n register to be set (in other words the n to choose) for the desired functionality has to be taken from column C.

Figure 8. **I/O Signal Table Tab in I/O spread sheet**



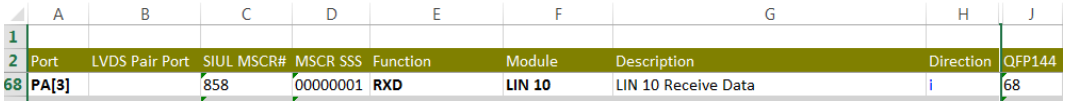
	A	B	C	D	E	F	G	H	I	J
1										
2	Port	LVDS	SIUL M	MSCR SSS	Function	Module	Description	Direct	Type	QFP144
63	PA[3]		3	00000110	CS5	DSPI 2	DSPI 2 Peripheral Chip Select 5	o	SLOW-MEDIUM-FAST	68
64	PA[3]		3	00000111	UC9	eMIOS 1	eMIOS 1 Channel 9	i/o	SLOW-MEDIUM-FAST	68
65	PA[3]		3	00001101	CS3	DSPI 8	DSPI 8 Peripheral Chip Select 3	o	SLOW-MEDIUM-FAST	68
66	PA[3]		3	00001110	SOUT	DSPI 6	DSPI 6 Serial Data	o	SLOW-MEDIUM-FAST	68
67	PA[3]		604	00000001	UC28	eMIOS 0	eMIOS 0 Channel 28	i	SLOW-MEDIUM-FAST	68
68	PA[3]		858	00000001	RXD	LIN 10	LIN 10 Receive Data	i	SLOW-MEDIUM-FAST	68
69	PA[3]		886	00001100	SIN	DSPI 2	DSPI 2 Serial Data	i	SLOW-MEDIUM-FAST	68
70	PA[3]		895	00000001	SIN	DSPI 5	DSPI 5 Serial Data	i	SLOW-MEDIUM-FAST	68
71	PA[3]		995	00000010	UC9	eMIOS 1	eMIOS 1 Channel 9	i	SLOW-MEDIUM-FAST	68
72	PA[3]		-	-	INT6	WakeUp	WakeUp_External Interrupt 6	pi	SLOW-MEDIUM-FAST	68

Title | Revision History | IO Signal Table | Input Muxing | Supply Pins | ...

In the following there are 2 examples of SIUL2_MSCR_MUX configuration:

- Example 3: port PA[3] configured as digital input with LIN RX function;

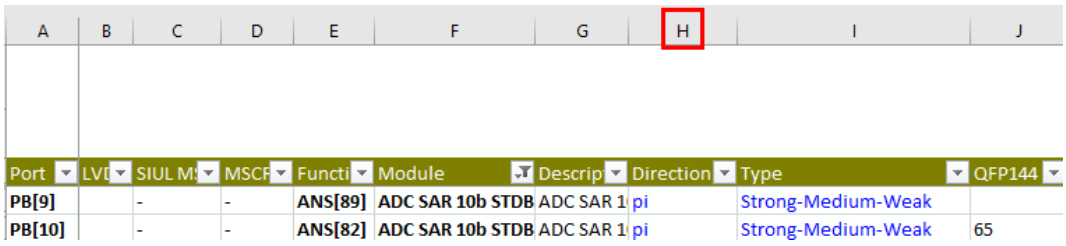
Example 3	Connect port PA[3], pin 68 of QFP144, to LIN10 Receive data, RXD.
Register configuration	SIUL2_MSCR_IO_3 = 0x0038_0000 SIUL2_MSCR_MUX_ 858 = 0x00000001
	Details of bit fields: SIUL2_MSCR_IO_3.ILS = 0b11 SIUL2_MSCR_IO_3.IBE = 0b1 SIUL2.MSCR_MUX_858.SSS = 0X01 (0b0000_0001 - LIN 10 RECEIVE DATA).



	A	B	C	D	E	F	G	H	J
1									
2	Port	LVDS Pair Port	SIUL MSCR#	MSCR SSS	Function	Module	Description	Direction	QFP144
68	PA[3]		858	00000001	RXD	LIN 10	LIN 10 Receive Data	i	68

- Example 4: port PB[0] configured as analogue input.

Example 4	Connect port PB[10], pin 65, to analogue input.
Register configuration	SIUL2_MSCR_IO_3.SSS = 0x0000_0000
	SIUL2 is not involved in the ADC analogue input, The analog input path is enabled in the ADC logic when the channel is selected for conversion. The SSS is always 8b0 for input only ports and this is the only constrain to be respected *Note: for analogue input the column **H**, Direction, is indicated with "pi".*



	A	B	C	D	E	F	G	H	I	J
	Port	LVD	SIUL M	MSCF	Functi	Module	Descrip	Direction	Type	QFP144
	PB[9]		-	-	ANS[89]	ADC SAR 10b STDB	ADC SAR 1	pi	Strong-Medium-Weak	
	PB[10]		-	-	ANS[82]	ADC SAR 10b STDB	ADC SAR 1	pi	Strong-Medium-Weak	65

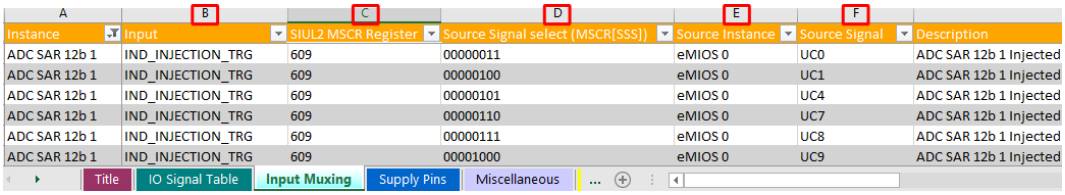
Input source from another IP block

If the input signal to IP block has to be selected from another IP blocks the needed information for SIUL2_MSCR_MUX_n (n = 512..1023) registers configuration are gotten from Input Muxing Tab:

- Each source instance in the column **E** of the Input Muxing Tab has the relative source signals available in the column **F**;
- Each source signal (available in column **F**) can be connected to the IP block Input available in the column **B**;

- The chosen source signal is set with SSS field of SIUL2_MSCR_MUX_n register, the value of SSS field is gotten from column **D**;
- The SIUL2_MSCR_MUX_ n register to be set (in other words the n to choose) for the chosen functionality has to be taken from column **C**.

Figure 9. Input Muxing Table Tab in I/O spread sheet



A	B	C	D	E	F	
Instance	Input	SIUL2 MSCR Register	Source Signal select (MSCR[SSS])	Source Instance	Source Signal	Description
ADC SAR 12b 1	IND_INJECTION_TRG	609	00000011	eMIOS 0	UC0	ADC SAR 12b 1 Injected
ADC SAR 12b 1	IND_INJECTION_TRG	609	00000100	eMIOS 0	UC1	ADC SAR 12b 1 Injected
ADC SAR 12b 1	IND_INJECTION_TRG	609	00000101	eMIOS 0	UC4	ADC SAR 12b 1 Injected
ADC SAR 12b 1	IND_INJECTION_TRG	609	00000110	eMIOS 0	UC7	ADC SAR 12b 1 Injected
ADC SAR 12b 1	IND_INJECTION_TRG	609	00000111	eMIOS 0	UC8	ADC SAR 12b 1 Injected
ADC SAR 12b 1	IND_INJECTION_TRG	609	00001000	eMIOS 0	UC9	ADC SAR 12b 1 Injected

Title | IO Signal Table | Input Muxing | Supply Pins | Miscellaneous

In the following there is one examples of SIUL2_MSCR_MUX configuration for an input source from another IP block:

- Example 5: connect UC1 signal from EMIOS 1 to ADC injection TRG.

Example 5	Connect UC1 source signal of EMIOS 1 to ADC SAR 2 IND_INJECTION_TRG input.
Register configuration	SIUL2_MSCR_MUX_609 = 0x00000047
	Details of bit fields:SIUL2.MSCR_MUX_609.SSS = 0X47 (0b0100_0111 - EMIOS UC1 connected to ADC SAR injection trigger).

	A	B	C	D	E	F
1	Instance	Input	SIUL2 MSCR Register	Source Signal select (MSCR[SSS])	Source Instance	Source Signal
128	ADC SAR 12b 1	IND_INJECTION_TRG	609	01000111	eMIOS 1	UC1

Finally In the following there are other 3 examples how to configure the pin as a GPIO, general purpose input or general purpose output and check its status:

- Example 6: configure PB[10] as general purpose input.

Example 6	Reading a digital input on PB[10] port.
Register configuration	SIUL2_MSCR_IO_26 = 0x0038_0000
	SIUL2_MSCR_IO_26.ILS = 0b11 SIUL2_MSCR_IO_26.IBE = 0b1 The status of port PB[10] can be read in the register SIUL2_GPDI26:PDI

Port	LVDS Pair Port	SIUL MSCR#	MSCR SSS	Function	Module	Description	Direction
PB[10]		26	00000000	GPIO26	SIUL	SIUL General Purpose I/O 26	i/o

- Example 7: configure PB[13] as general purpose output and set it to 1.

Example 7	Set to 1 the output, medium drive, on port PB[13].
Register configuration	SIUL2_MSCR_IO_29 = 0x1200_0000
	SIUL2_MSCR_IO_29.OERC = 0b1 SIUL2_MSCR_IO_29.ODC = 0b10 SIUL2_GPDI26.PDO = 0b1, sets the port PB[13] to 1 SIUL2_GPDI26.PDO = 0b0, sets the port PB[13] to 0

Port	LVDS Pair Port	SIUL MSCR#	MSCR SSS	Function	Module	Description	Direction
PB[13]		29	00000000	GPIO29	SIUL	SIUL General Purpose I/O 29	i/o

- Example 8: configure PB[13] as general purpose output and set it to 1 reading it back

Example 8	P[13] is configured as input and output, so that the pad value can be "read back".
Register configuration	SIUL2_MSCR_IO_29 = 0x1238_0000
	SIUL2_MSCR_IO_29.ILS = 0b11 SIUL2_MSCR_IO_29.IBE = 0b1 SIUL2_MSCR_IO_29.OERC = 0b1 SIUL2_MSCR_IO_29.ODC = 0b010 The "read back" configuration is a method of checking of the driven value on the associated I/O pad. Setting the logic level of pad by means of SIUL_GPDI29.PDI, its driven value can be read by the register SIUL_GPDI29.PDI.

Port	LVDS Pair Port	SIUL MSCR#	MSCR SSS	Function	Module	Description	Direction
PB[13]		29	00000000	GPIO29	SIUL	SIUL General Purpose I/O 29	i/o

Appendix A Other information

A.1 Reference documents

Table 3. **Reference documents**

Doc Name	ID	Title
AN4880	029356	SPC58xx hardware design guideline
TN1263	031450	SPC582Bx IO definition: signal description and input multiplexing tables
TN1264	031472	SPC584Gx, SPC58EGx, SPC58NGx IO definition: signal description and input multiplexing tables
TN1257	031245	SPC58EHx, SPC58NHx, IO definition: signal description and input multiplexing tables
TN1260	031389	SPC584Cx, SPC58ECx IO definition: signal description and input multiplexing tables
TN1265	031477	SPC584Bx IO definition: signal description and input multiplexing tables
TN1268	031648	SPC584Nx, SPC58ENx, SPC58NNx IO definition: signal description and input multiplexing tables
TN1298	033306	SPC58xEx IO definition: signal description and input multiplexing tables
RM0391	027214	SPC58 E/G Line - 32 bit Power Architecture automotive MCU Triple z4 cores 180 MHz, 6 MBytes Flash, HSM, ASIL-D
RM0403	027949	SPC58 2B Line - 32 bit Power Architecture automotive MCU z2 core 80 MHz, 1 MByte Flash, ASIL-B
RM0407	028117	SPC58 C Line - 32 bit Power Architecture automotive MCU Dual z4 cores 180 MHz, 4 MBytes Flash, HSM, ASIL-B – Reference Manual
RM0421	028528	SPC58xNx 32-bit Power Architecture microcontroller for automotive ASILD applications
RM0449	030699	SPC58 4B Line - 32 bit Power Architecture automotive MCU z4 core 120 MHz, 2 MBytes Flash, HSM, ASIL-B
RM0452	031241	SPC58 H Line - 32 bit Power Architecture automotive MCU Triple z4 cores 200 MHz, 10 MBytes Flash, HSM, ASIL-D

Revision history

Table 4. **Document revision history**

Date	Version	Changes
16-Jun-2021	1	Initial release.

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