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Technical note

SPC58x Ethernet filtering compatibility

Introduction

The SPC58x microcontroller family embeds the 10/100 and GiGa Ethernet controllers with flexible and advanced features to filter network traffic.

This document shows which filters are supported on each MCU, further details about filtering and related programming can be found in each device reference manual.

1 Ethernet overview

SPC58x automotive Micro-controllers features Quality-Of-Service 10/100/1000 Mbit/s Ethernet peripherals that implement the medium access control (MAC) layer plus several internal modules for standard and advanced network features that can be summarized into the following categories:

- MAC Core and MAC transaction layer (MTL)
- DMA engine
- SMA interface
- MAC management counters
- Power management block (PMT)
- Flexible and wide range of address filtering schemes

The following table shows the embedded Ethernet controllers available on the SPC58x family.

Table 1. SPC58x Ethernet controllers

MCU	Ethernet 0	Ethernet 1
SPC584B70	10/100	N/A
SPC58EC80	10/100	N/A
SPC58NG84	10/100	10/100
SPC58NH9X	10/100	10/100/1000

2 Filtering introduction

While developing efficient networking applications it is mandatory to consider the packet filtering, so the way to drop or pass the network traffic to the high protocol stacks according to the defined rules.

Packet filtering can be covered in software in many circumstances but paying a relevant cost in terms of performances and CPU usage.

The advanced Ethernet controllers available inside the SPC58x MCUs provide a wide selection of filter models designed to cover several configurations.

This document is focused on the difference from each micro-controller in terms of capabilities and number of available registers.

3 SPC58x Ethernet fixed filters

The Ethernet modules support the following types of fixed filters for rx packets:

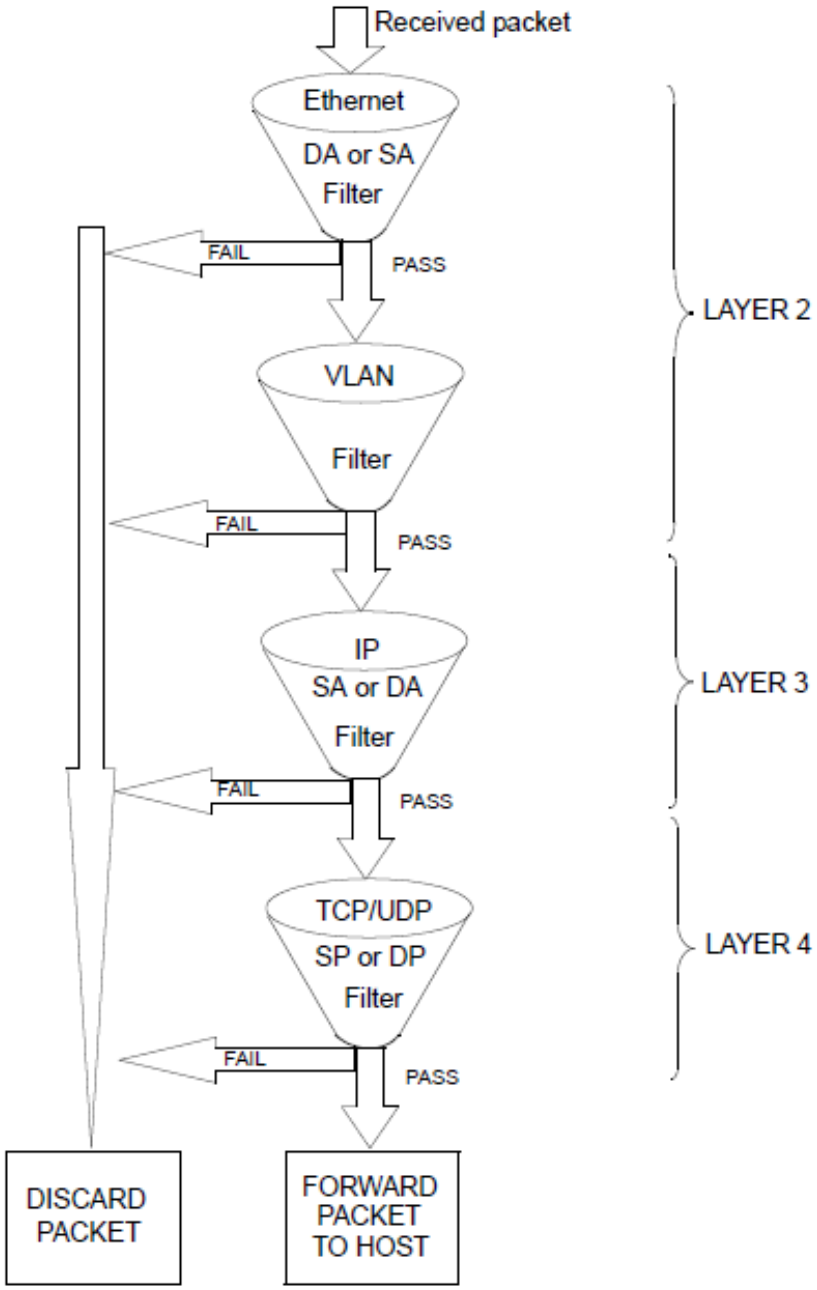
- Source address or destination address filtering
- VLAN filtering: the Ethernet module supports the VLAN tag based and VLAN hash filtering
- Layer 3 and layer 4 filtering: layer 3 filtering refers to source address and destination address filtering. Layer 4 filtering refers to source port and destination port filtering

The following figure shows how the internal filtering is done by the hardware. The device's reference manual reports how to program the MAC Packet Filter register (MAC_PACKET_FILTER) to select each filter mode.

Note: IEEE 802.1Q is the standard for Virtual LAN (VLAN).

For more information, user should refer to the packet filtering chapter inside the reference manual of each microcontroller.

Figure 1. Packet filter sequence



3.1 SA/DA layer 2 filtering

For Layer 2 filtering, MAC supports a specific set of MAC perfect filtering registers. The number of these registers for each MCU in the family is reported in the following table.

Note: When this mode is selected, the MAC compares all 48 bits of received address with the programmed MAC address for any match. The default Mac Address 0 is always enabled (used for the primary MAC address assigned to the interface).

Table 2. Perfect filter register set

MCU	Ethernet instance	Controller speed	MAC ADD0	MAC ADD 1… 31	MAC ADD 32… 63	MAC ADD 64… 127
SPC584B70	Eth0	10/100	yes	yes	yes	yes
SPC58EC80	Eth0	10/100	yes	yes	yes	yes
SPC58NG84	Eth0	10/100	yes	yes	yes	yes
	Eth1	10/100	yes	yes	yes	yes
SPC58NH9X	Eth0	10/100	yes	yes	N/A	N/A
	Eth1	10/100/1000	yes	yes	N/A	N/A

Note: the medium access control sublayer is the layer that controls the hardware responsible for interaction with the medium device.

Mac Address is a unique identifier assigned to a network interface: xx - xx - xx - xx - xx - xx

The following code shows how to program one of the MAC_PF_1_31 high and low registers with a software address (for DA or SA filtering).

```
data = (addr[5] << 8) | addr[4];
reg->MAC_PF_1_31->MAC_ADDRESS_HIGH31_1.B.ADDRHI = data;
data = (addr[3] << 24) | (addr[2] << 16) | (addr[1] << 8) | addr[0];reg-
>MAC_PF_1_31->MAC_ADDRESS_LOW31_1.B.ADDRLO = data;
reg->MAC_PF_1_31->MAC_ADDRESS_HIGH31_1.B.AE = 1;
```

For SPC584B70x, SPC58EC80x, SPC58NG84x Microcontrollers, it will be also possible to program the groups: 32…63 and 64…127 with a similar code shown above for DA filtering.

All the Ethernet controllers support the hash filtering mode: so, the MAC performs DA filtering using a 64-bit Hash table. The following registers are available for this support:

- Hash table register 0 (MAC_HASH_TABLE_REG0).
- Hash table register 1 (MAC_HASH_TABLE_REG1).

Note: all controllers also support all multicast filtering, inverse filtering, and the promiscuous mode. It causes the controller to pass all traffic it receives to the upper layer stack (e.g. TCP/IP).

3.2 VLAN filtering

All the SPC58x Ethernet modules support the following types of VLAN filtering:

- VLAN tag perfect filtering
- VLAN tag hash filtering

In a glance, in VLAN tag perfect filtering, the MAC compares the VLAN tag of received packet and provides the VLAN packet status to the application. In the latter mode, the MAC provides VLAN tag hash filtering with a 16-bit hash table.

3.2.1 Extended VLAN filtering and routing

Both Ethernet controllers embedded in the SPC58NH9x MCU also support the extended VLAN filtering and routing on receive path.

Thanks to this new feature, the MAC receiver can classify the received packets based on VLAN tag and steer them to a specific rx DMA channel.

3.2.2 VLAN registers

For SPC584B70x, SPC58EC80x, SPC58NG84x Microcontrollers, the following VLAN registers are available:

- **VLAN Tag register:** identifies the IEEE 802.1Q VLAN type packets.
- **VLAN hash table register:** hash table register is used for group address filtering based on the VLAN tag.
- **VLAN tag inclusion register:** it contains the VLAN tag for insertion or replacement in the Transmit packets. It also contains the VLAN tag insertion controls.
- **Inner VLAN tag inclusion register:** it contains the inner VLAN tag to be inserted or replaced in the transmit packet. It also contains the inner VLAN tag insertion controls.

The Ethernet controllers embedded in the SPC58NH9x MCU have the following registers:

- **VLAN Tag Control register:** it is the redefined format of the VLAN tag register; it contains extra fields to hold the address offset of the MAC VLAN tag filter register which the application is trying to access.
- **VLAN tag data register:** it holds the read/write data for Indirect Access of the Per VLAN tag registers, it programs the DMA channel used to route the frame.
- **VLAN tag filter <n> register:** a set of 16 registers to manage and route the tagged frames.
- **VLAN hash table register:** (same as above).
- **VLAN tag inclusion register:** (same as above).
- **VLAN tag inclusion <n> register (n = 0 to 15):** extended set of registers for the insertion in the transmit packets from Tx Queue <n>.
- **Inner VLAN tag inclusion register:** (same as above).

3.3 Layer 3 and layer 4 filtering

All the SPC58x Ethernet modules support both layer 3 and layer 4 based packet filtering. The layer 3 filtering refers to the IP source or destination address filtering in the IPv4 or IPv6 packets whereas layer 4 filtering refers to the source or destination port number filtering in TCP or UDP.

4 Flexible receive parsing based filtering

This is a new filter model only available in the Ethernet controller 1 (GiGa) on SPC58NH9x MCU. The MAC_HW_FEATURE3 shows if the module supports flexible receive parser features. This register also reports the maximum number of bytes of the packet data to be parsed by flexible receive (128 Bytes on this MCU).

The FRP is completely flexible and can do any of the register filter functions. The only difference is that, it can check for patterns sequentially unlike fixed filtering which can compare in parallel. This filter has the ability to re-direct the filtered traffic to the dedicated DMA channels.

Fixed filtering and FRP cannot be configured together on this MCU.

When the FRP feature is enabled then the application software must prepare a 96-bit programmable lookup table with all the flexible filters that can be applied to the incoming frames. The format of each entry in this table is detailed in the device's reference manual (flexible receive parser (FRP) chapter). By programming the table, it will be possible to accept or reject the frames or pass them to the DMA channel if the match is satisfied. There are 4-byte data, they are used for comparing with incoming packet data starting at the frame offset (always defined inside the table). The pattern match adopted by the FRP module gives the maximum flexibility parsing the incoming frames and taking also custom actions.

Appendix A Acronyms and abbreviations

Table 3. **Acronyms and abbreviations**

Terms	Meaning
SA	Source Address
DA	Destination Address
SP	Source Port
DP	Destination Port
UNI	Unicast Frames
MULTI	Multicast Frames
MAC	Media Access Control
MTL	Transaction Layer
VLAN	Virtual Local Area Network
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
IP	Internet Protocol
FRP	Flexible Receive Parser
N/A	Not Available

Appendix B Reference documents

- RM0452 reference manual

Revision history

Table 4. **Document revision history**

Date	Version	Changes
03-Nov-2020	1	Initial release.

Contents

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