SPC56EL54/SPC564L54 memory map

Introduction

The SPC56EL54 and the SPC564L54 are two microcontrollers belonging to the family of the SPC56EL60. All these devices have the same functionalities. The only difference is the dimension of the Flash and System RAM.

This document describes the memory map of the Flash and System RAM for the SPC56EL54 and SPC564L54.

For any other details about the functionality of the SPC56EL54 and SPC564L54 refer to the reference manual of SPC56EL60 (See Section Appendix A).

1 Memory map of SPC56EL54 memories

The SPC56EL54 is a dual-core microcontroller which can operate either in LSM (lock step mode) or DPM (decoupled parallel mode).

1.1 Memory map of the Flash

Table 1. Memory map of the SPC56EL54 Flash

Flash		
Start Address	**Size [KB]**	**Regions**
0x0000_0000	16	Flash-memory array partition 1 (low address) or test Flash memory(1)
0x0000_4000	48	Flash-memory array partition 1 (low address)
0x0001_0000	48	Flash-memory array partition 1 (low address)
0x0001_C000	16	Flash-memory array partition 1 (low address)
0x0002_0000	64	Flash-memory array partition 2 (low address)
0x0003_0000	64	Flash-memory array partition 2 (low address)
0x0004_0000	128	Flash-memory array partition 3 (mid address)
0x0006_0000	128	Flash-memory array partition 3 (mid address)
0x0008_0000	256	Flash-memory array partition 4 (high address)
-	-	-
0x00F0_0000	16	Shadow block
-	-	-
0x0100_0000	507904	Flash-memory emulation mapping

1. *Test Flash memory is mapped to this address if the SCTR[TFE] bit in the SSCM is set.*

1.2 Memory map of the SRAM

The memory map of the RAM depends on the operating mode of the device.

Table 2. Memory map of the SPC56EL54 RAM working in LSM

RAM		
Start Address	**Size [KB]**	**Regions**
0x4000_0000	96	SRAM

Table 3. Memory map of the SPC56EL54 RAM working in DPM

RAM		
Start Address	**Size [KB]**	**Regions**
0x4000_0000	48	SRAM
0x5000_0000	48	SRAM(1)

1. *This range cannot be accessed by DMA_0.*

2 Memory map of SPC564L54 memories

The SPC564L54 is a single-core microcontroller which has the same functionality of the SPC56EL54 configured in DPM. The main difference is that the SPC56EL54 in DPM contains two independent cores.

2.1 Memory map of the Flash

Table 4. Memory map of the SPC564L54 Flash

Flash		
Start Address	**Size [KB]**	**Regions**
0x0000_0000	16	Flash-memory array partition 1 (low address) or test Flash memory(1)
0x0000_4000	48	Flash-memory array partition 1 (low address)
0x0001_0000	48	Flash-memory array partition 1 (low address)
0x0001_C000	16	Flash-memory array partition 1 (low address)
0x0002_0000	64	Flash-memory array partition 2 (low address)
0x0003_0000	64	Flash-memory array partition 2 (low address)
0x0004_0000	128	Flash-memory array partition 3 (mid address)
0x0006_0000	128	Flash-memory array partition 3 (mid address)
0x0008_0000	256	Flash-memory array partition 4 (high address)
-	-	-
0x00F0_0000	16	Shadow block
-	-	-
0x0100_0000	507904	Flash-memory emulation mapping

1. *Test Flash memory is mapped to this address if the SCTR[TFE] bit in the SSCM is set.*

2.2 Memory map of the SRAM

Table 5. Memory map of the SPC564L54 RAM

SRAM		
Start Address	**Size [KB]**	**Regions**
0x4000_0000	48	SRAM
0x5000_0000	48	SRAM(1)

1. *This range cannot be accessed by DMA_0.*

2.3 Lockstep or decoupled mode

This device can work only as a single core, but the default configuration that ST uses when delivering samples to the user is the lockstep mode. The users must change this configuration from lockstep (LSM) to decoupled (DPM) mode before running their application. Besides, users must not enable the second core once the device is in decoupled mode.

The users must configure the User option bit to switch from LSM to DPM. The related reference manual (See Section Appendix A) describes this process in the "User option bits" and "Selecting LSM or DPM" sections.

Appendix A Reference documents

Table 6. **Reference documents**

Doc Name	ID	Title
RM0032	015265	SPC56EL60 32-bit MCU family built on the embedded Power Architecture®

Revision history

Table 7. **Document revision history**

Date	Version	Changes
22-Jan-2020	1	Initial release.

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