Migration differences between SPC582Bx and SPC560B5x

## Introduction

The 32-bit SPC56xB/C automotive microcontrollers (also known as SPC560B5X) are a family of System-on-Chip (SoC) devices designed to be central to the development of the next generation of central vehicle body controller, smart junction box, front module, peripheral body, door control and seat control applications.

The SPC56xB/C car body family is a series of automotive microcontrollers based on the Power Architecture® technology and designed specifically for embedded automotive applications.

The SPC56xB/C family is a highly scalable and compatible family of devices.

However, designing an application that can be easily ported across different members requires knowledge of the features of the devices and any significant differences between them.

The SPC582Bx is a family of 32-bit Power Architecture® microcontrollers that targets automotive vehicle body and gateway applications such as standalone gateway, simple body control module and satellite body application like door or lighting module. The SPC582Bx is the entry product of an automotive microcontroller family which offers the scalability needed to implement platform approaches and delivers the performance and features required by increasingly sophisticated body applications.

This document focuses between the differences across the SPC582Bx family, and SPC560B5x family.

For the latter, we will refer to the best so far product to highlight the differences with SPC582Bx family.

Both devices are ASIL-B compliant.

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# 1 Block diagrams

## 1.1 Comparison between block diagrams

In *Figure 1* and *Figure 2* are reported the two block diagrams of the SPC560B5x and SPC582Bx.

**Figure 1. SPC560B5x block diagram**

Legend:

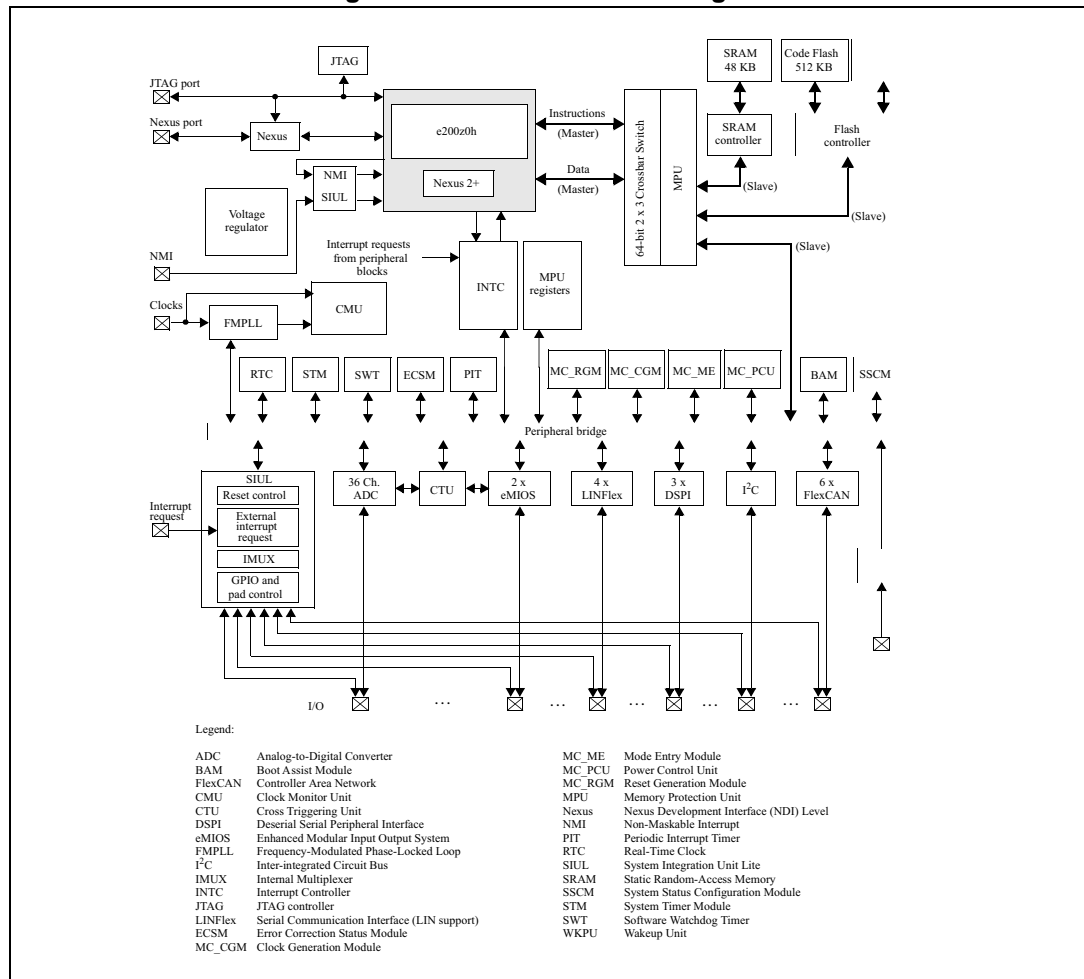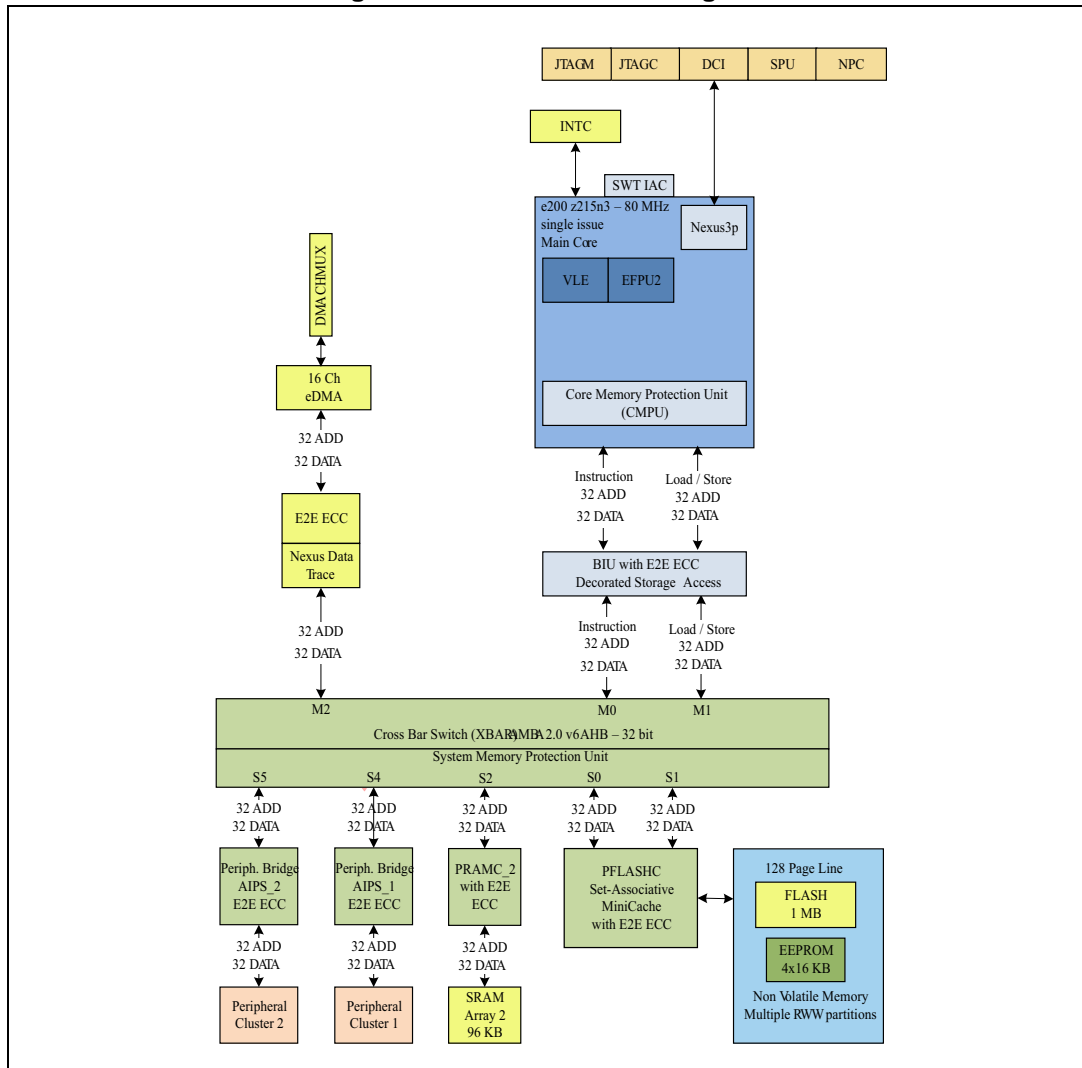| | | | |
|---|---|---|---|
| ADC | Analog-to-Digital Converter | MC_ME | Mode Entry Module |
| BAM | Boot Assist Module | MC_PCU | Power Control Unit |
| FlexCAN | Controller Area Network | MC_RGM | Reset Generation Module |
| CMU | Clock Monitor Unit | MPU | Memory Protection Unit |
| CTU | Cross Triggering Unit | Nexus | Nexus Development Interface (NDI) Level |
| DSPI | Deserial Serial Peripheral Interface | NMI | Non-Maskable Interrupt |
| eMIOS | Enhanced Modular Input Output System | PIT | Periodic Interrupt Timer |
| FMPLL | Frequency-Modulated Phase-Locked Loop | RTC | Real-Time Clock |
| $I^2C$ | Inter-integrated Circuit Bus | SIUL | System Integration Unit Lite |
| IMUX | Internal Multiplexer | SRAM | Static Random-Access Memory |
| INTC | Interrupt Controller | SSCM | System Status Configuration Module |
| JTAG | JTAG controller | STM | System Timer Module |
| LINFlex | Serial Communication Interface (LIN support) | SWT | Software Watchdog Timer |
| ECSM | Error Correction Status Module | WKPU | Wakeup Unit |
| MC_CGM | Clock Generation Module | | |

**Figure 2. SPC582Bx block diagram**

# 2 Overview

## 2.1 Features

Table 1 shows an overview of the features set of the two products. A more detailed description of the differences between the two devices and of the migration from SPC560B5x to SPC582Bx is given in the next sections.

**Table 1. Overview of main features and differences**

| Features | SPC582BX | SPC560B5x |
|---|---|---|
| Core/Platform | | |
| Core number | 1xz2 | 1xz0 |
| Core o | Z215 | Z0 |
| Core MPU | 28 regions/core | 8 regions/core |
| System MPU | 12 regions | 8 regions |
| Memory | | |
| RAM size | 96 K | 48 K |
| Standby ram (max/min) | 64K/8K | 32K/8K |
| Code Flash | 1M (1 x RWW partition) | 512K |
| Data Flash | 64K (4x16K) | 64K (4x16K) |
| I/O | | |
| I/O state during and out of reset | High-Z | High-Z |
| Debug | | |
| I Fast | 1 x JTAG | 1 x JTAG |
| Trace interface | Nexus | Nexus |
| Class | 3+ | 1 (2+ for LBGA208) |
| Clock | | |
| Max Freq. | 80 MHz | 64 MHz |
| Clock source (fast) | IRCOSC / XOSC / PLLx | IRCOSC / XOSC / PLLx |
| Clock source (slow) | SIRC | SIRC/SXOSC |
| System | | |
| INT_CTLR | 1 x INTC | 1 x INTC |
| DMA | 1 x 16ch | NO |
| STM | 1 | 1 |
| PIT | 6 | 6 |
| Communication I/F | | |
| LIN | 6 x LinFlex | 6 x LinFlex |
| CAN | 7 x ISOMCAN-FD | 6 x FlexCAN |

**Table 1. Overview of main features and differences (continued)**

| Features | SPC582BX | SPC560B5x |
|---|---|---|
| I2C | Yes | Yes |
| DSPI | 4 | |
| Timed I/O | | |
| eMIOS | 1 X 32 ch | 2 x 28 Ch |
| CTU | 32ch | 49ch |
| ADC | | |
| SARADC (12bit) | 64ch (1x 12-bit /1x 12-bit supervisor / 1x 10-bit STBY) | 36 ADC |
| Low Power | | |
| Low Power Modes | HALT/STOP/STANDBY | HALT/STOP/STANDBY |
| RTC/API | 1 | 1 |
| Asil level | ASIL-B | ASIL-B |
| FCCU | 1 | No |
| CRC | 2x4 ch | No |
| MBIST | on RAM and FLASH | No |

## 2.2     Supply and packages

**Table 2. Overview of main features and differences**

| Features | SPC582BX | SPC560B5x |
|---|---|---|
| Package | QFN32 / eTQFP64 / eLQFP100 | eLQFP64 / 100 / 144 / LBGA208(emulation package) |
| Temperature | -40°C +105°C/+125°C | -40°C +105°C/+125°C |
| Supply | | |
| High voltage | 3.3 or 5V | 3.3 or 5V |
| Low voltage | Internal | Internal |
| Ballast | Internal | Internal |

# 3 Core/Platform

## 3.1 Cores

The SPC582Bx has a High performance 80 MHz e200z2 single core with:

- 32-bit Power Architecture technology CPU
- Core frequency as high as 80 MHz
- Variable Length Encoding (VLE)
- Floating Point, End-to-End Error Correction

The SPC560B5x has a High-performance 64 MHz e200z0h CPU with:

- 32-bit Power Architecture® technology
- UP to 60 DMIPs operation
- Variable lenght encoding

## 3.2 MPU (Memory Protection Unit)

The MPU sits on the slave side of the XBAR and allows highly configurable control over all master accesses to the memory.

SPC582Bx has 12 regions per core, SPC560B5x has 8 regions.

## 3.3 Interrupt controller (INTC)

Both devices furnishes one INTC.

**INTC for SPC582Bx has the following features**:

- Each peripheral interrupt source is software-steeerable to processor 0
- 32 Software-settable interrupt request sources
- 10 bit vector
    - Unique vector for each interrupt request source
    - Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 64 priorities
- Each nterrupt source can be triggered by software
- Preemption
    - Preemptive prioritized interrupt requests to processor
    - ISR with higher priority preempts ISRs or tasks with lower priorities
    - Automatic pushing or popping of preempted priority to or from a LIFO
    - Ability to modify the ISR or task priority; modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources
    - 3 INTC clock cycles from interrupt request into interrupt request to CPU Low latency
    - 3 INTC clock cycles from receipt of interrupt request from peripheral to interrupt request to processor; four clock cycles from receipt of software request

**INTC for SPC560B5x has the following features**:

- Supporting 134 peripheral and 8 software
- configurable interrupt request sources
- Unique 9-bit vector per interrupt source
- Each interrupt source can be programmed to one of 16 Ppriorities
- Preemption
    – Preemptive prioritized interrupt requests to processor
    – ISR at a higher priority preempts ISRs or tasks at lower priorities
    – Automatic pushing or popping of preempted priority to or from a LIFO
    – Ability to modify the ISR or task priority; modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- Low latency
    – 3 clocks from receipt of interrupt request from peripheral to interrupt request to processor

## 3.4    DMA

SPC582Bx provides a 1x16ch DMA controller, SPC560B5x has no DMA

**Figure 3. SPC582Bx DMA controller structure**
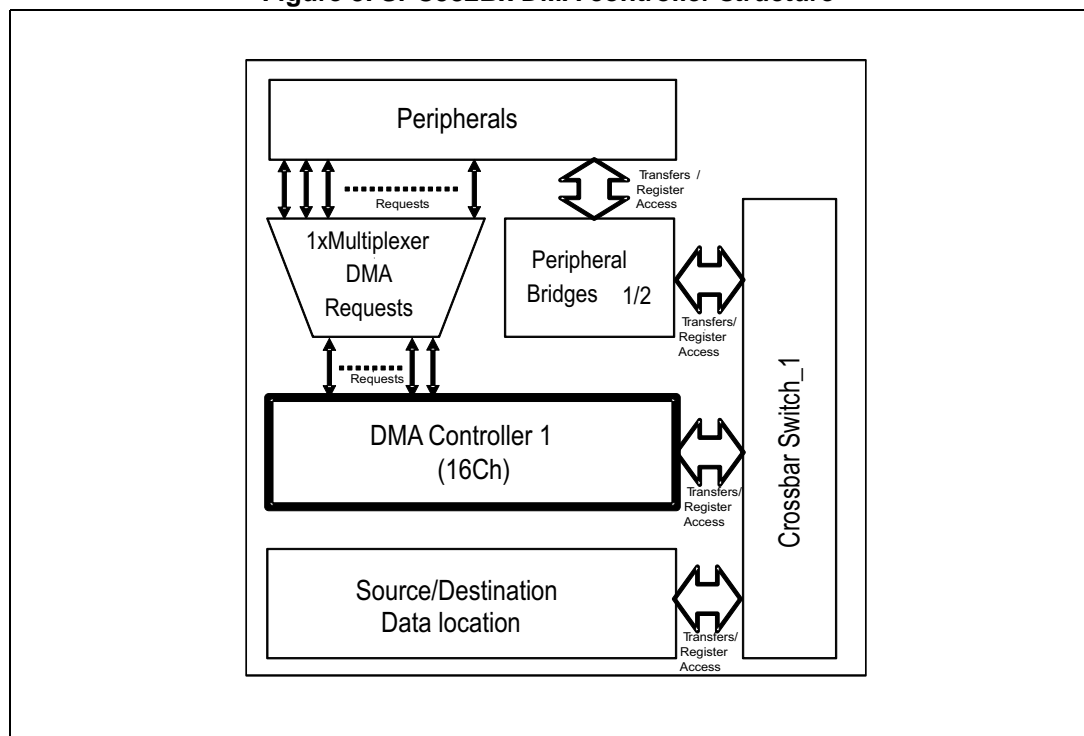
# 4 Memory

## 4.1 RAM controller

Both devices have one ram controller, the SPC582Bx one has size 96K (1XPRAM control), the SPC560B5x one has size 48K.

The difference between the two is that the SPC582Bx provides End-to-end Error Correction Code (e2eECC), instead the SPC560B5x provides traditional ECC.

This e2eECC is structurally different to traditional "ECC at memory" functionality because it provides robust error detection capabilities from one endpoint of an information transfer to another endpoint, with temporary information storage in one or more intermediate components. Memory protected by ECC/EDC traditionally generates and checks additional error parity information local to the memory unit to detect or correct errors that have occurred on data stored in the memory, or both. On the other hand, e2eECC generates error protection codes at the source of data generation.

## 4.2 RAM size

Both devices have one ram controller, the SPC582Bx one has size 96K (1XPRAM control), the SPC560B5x one has size 48K.

Standby RAM (Max/Min) is 64K/8K for SPC582Bx series and 32K/8K for SPC560B5x series.

## 4.3 Flash Controller

Below *Table 3* summarizes the differences between flash controllers available in SPC582Bx and SPC560B5x.

Table 3. Flash controller comparison between SPC582Bx and SPC560B5x

| Parameter/Feature | SPC582BX | SPC560B5x |
|---|---|---|
| N. of flash controller ports connected to the XBAR slave ports | 2 | 1 |
| AHB data bus width | 32 | 32 |
| Flash write data bus width | 128 | 32 |

**Table 3. Flash controller comparison between SPC582Bx and SPC560B5x (continued)**

| Parameter/Feature | SPC582BX | SPC560B5x |
|---|---|---|
| Flash read data bus width | 64 | 128 |
| Buffer | Read buffering and line prefetching support via 4-entry, 4-way setassociative mini-cache plus prefetch controller per AHB port to provide single-cycle "buffer hit" read response | Four-entry "page" buffer, each entry containing 128 bits of data plus an associated controller which prefetches sequential lines of data from the flash memory array into the buffer (code flash) + 128-bit register which serves as a temporary page holding register and does not support any prefetching (data flash) |

## 4.4 Code and Data Flash

Both device provide 64k of data flash, 4x16K banks.

**Table 4. Main difference between SPC582Bx and SPC560B5x**

| Features | SPC582BX | SPC560B5x |
|---|---|---|
| Code Flash size | 1M | 512 K |
| Error correction code | Double Error Correction, Triple Error Detection | Single error correction (SEC) Double error detection |
| Red-while-modify | Yes | NO |
| Programming during erase suspend | Yes | NO |
| Utest mode | Yes | NO |
| Protection strategy | Test mode disable | Censored mode against piracy |

# 5 Reset and boot modes

## 5.1 MC_RGM (Reset Generation Module)

The reset generation module (MC_RGM) centralizes the different reset sources and manages the reset sequence of the device. It provides a register interface and the reset sequencer.
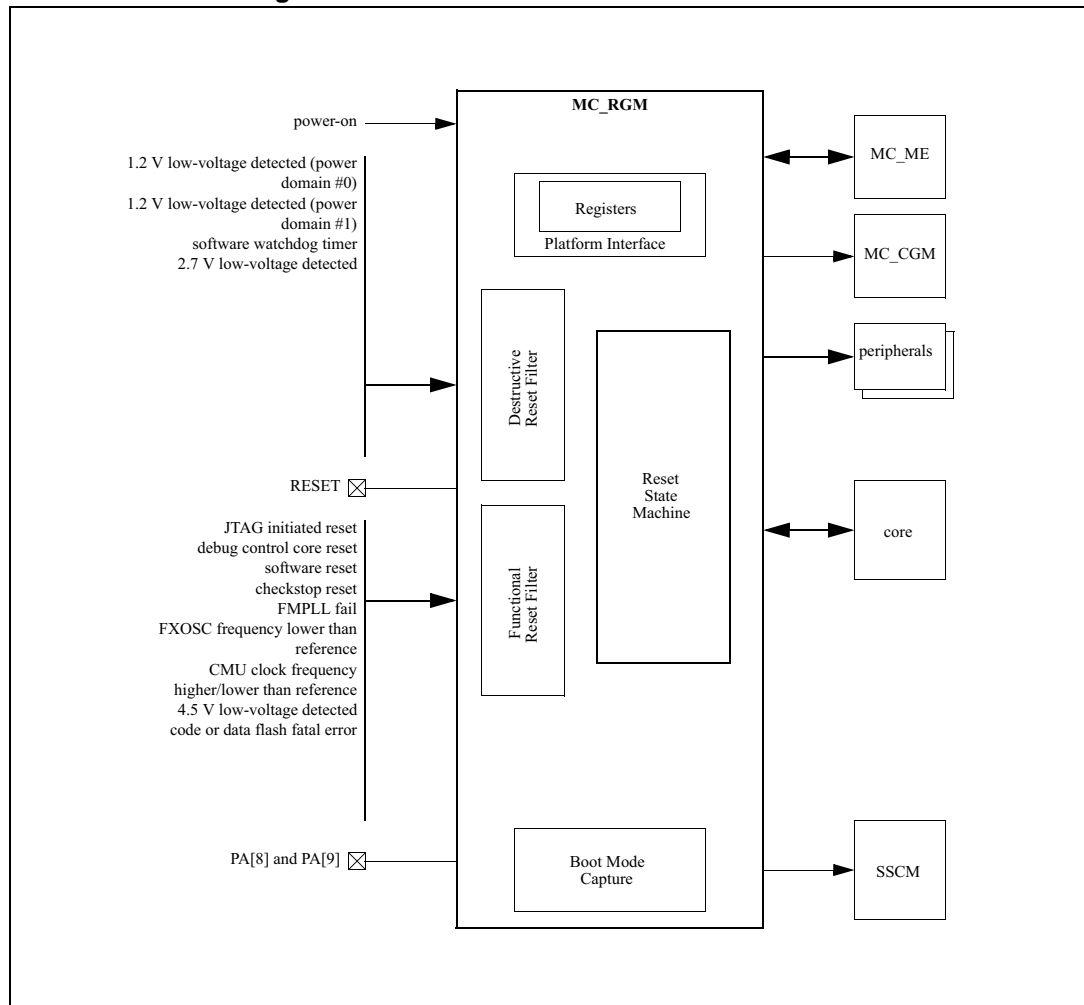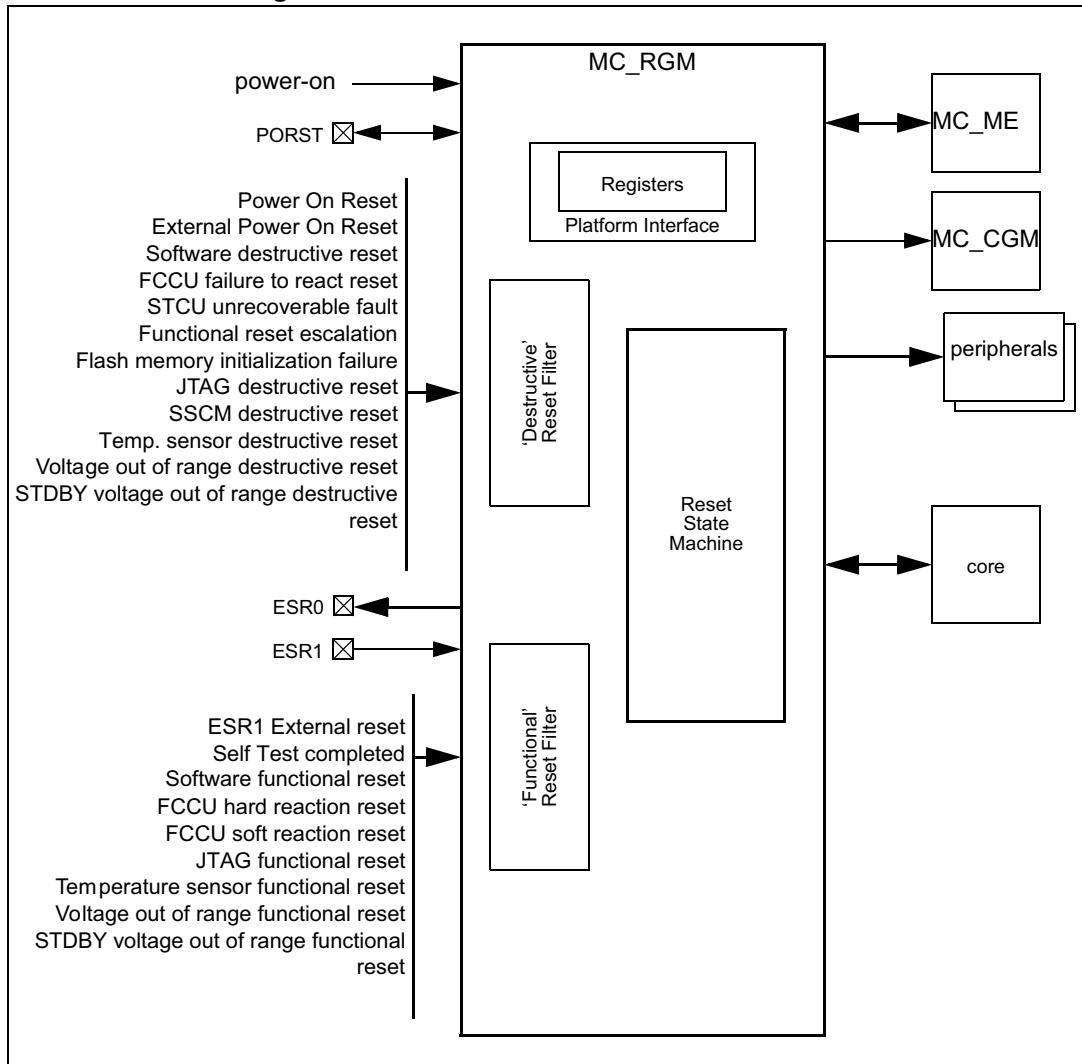
**Figure 4. SPC560B5x Reset Generation Module**

### Figure 5. SPC582B5x Reset Generation Module



MC_RMG common features:

- Destructive resets management
- Functional reset management
- Signaling of reset events after each reset sequence (reset status flags)
- Conversion of reset events to SAFE mode or interrupt request events (for further mode details please see the MC-ME chapter)
- Short reset sequence configuration
- Bidirectional reset behavior configuration

SPC560B5x MC_RGM provides also:

- Selection of alternate boot via the backup SRAM on STANDBY mode exit (for further mode details, please see the MC_ME chapter)
- Boot mode capture on RESET deassertion

## 5.2 BAM (Boot assist module) for SPC560B5x

The BAM consists of a block of ROM at address 0xFFFF_C000 containing VLE firmware. The BAM provides two main functions:

- Manages the serial download (FlexCAN or LINFlexD protocols supported) including support for a serial password if censorship is enabled
- Places the microcontroller into static mode if flash memory boot mode is selected and a valid BOOT_ID is not located in one of the boot sectors by the SSCM

**Figure 6. SPC560B5x BAM logic flow**
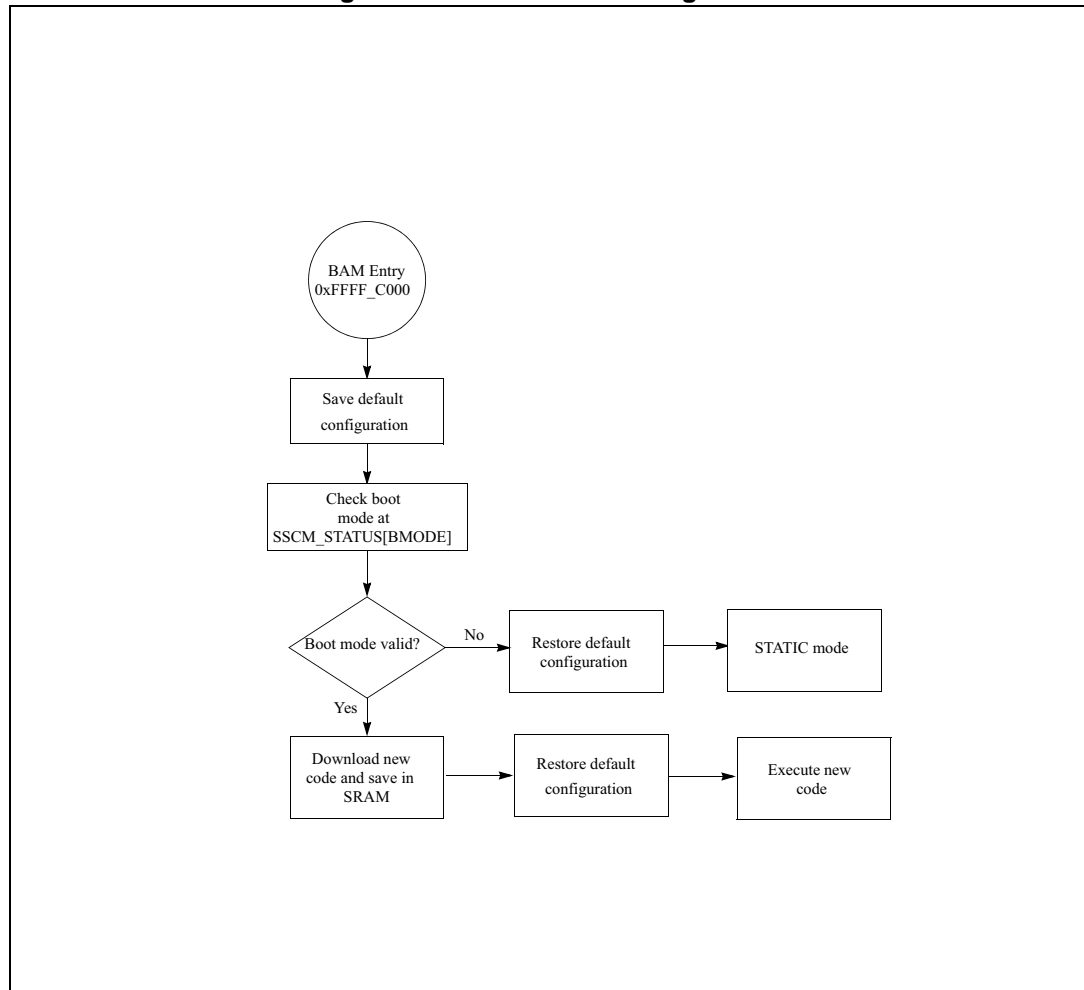


The initial (reset) device configuration is saved including the mode and clock configuration. This means that the serial download software running in the BAM can change to the modes and clocking, than restore these to the default values before running the newly downloaded application code from the SRAM.

The SSCM_STATUS[BMODE] field indicates which boot mode is to be executed. This field is only updated during reset.

There are two conditions where the boot mode is not considered valid and the BAM pushes the microcontroller into static mode after restoring the default configuration:

- BMODE = 011 (flash memory boot mode). This means that the SSCM has been unable to find a valid BOOT_ID in the boot sectors so has called the BAM
- BMODE = reserved

In static mode a wait instruction is executed to halt the core.

For the FlexCAN and LINFlexD serial boot modes, the respective area of BAM code is executed to download the code to SRAM.

## 5.3 BAF (Boot Assist FLash) for SPC582Bx

The BAF code is programmed by ST. The two main tasks of BAF are to provide a serial bootloader feature and to search for the application entry point. The BAF is executed using the IRCOSC as clock source.

The MCU is booted through a collaboration of several blocks, hardware and firmware. The first boot phases are performed by a state machine inside the System Status and Configuration Module (SSCM). Once completed, the SSCM sends a reset vector to the HW boot core of the device pointing into the Boot Assist Flash (BAF). The BAF code then checks the life cycle of the device. If it is FAIL_ANALYSIS, the BAF enters a loop in which it services the watchdog. Otherwise, it searches for a boot header and boots the application code in internal flash memory.

**Figure 7. SPC582B2x BAF logic flow**
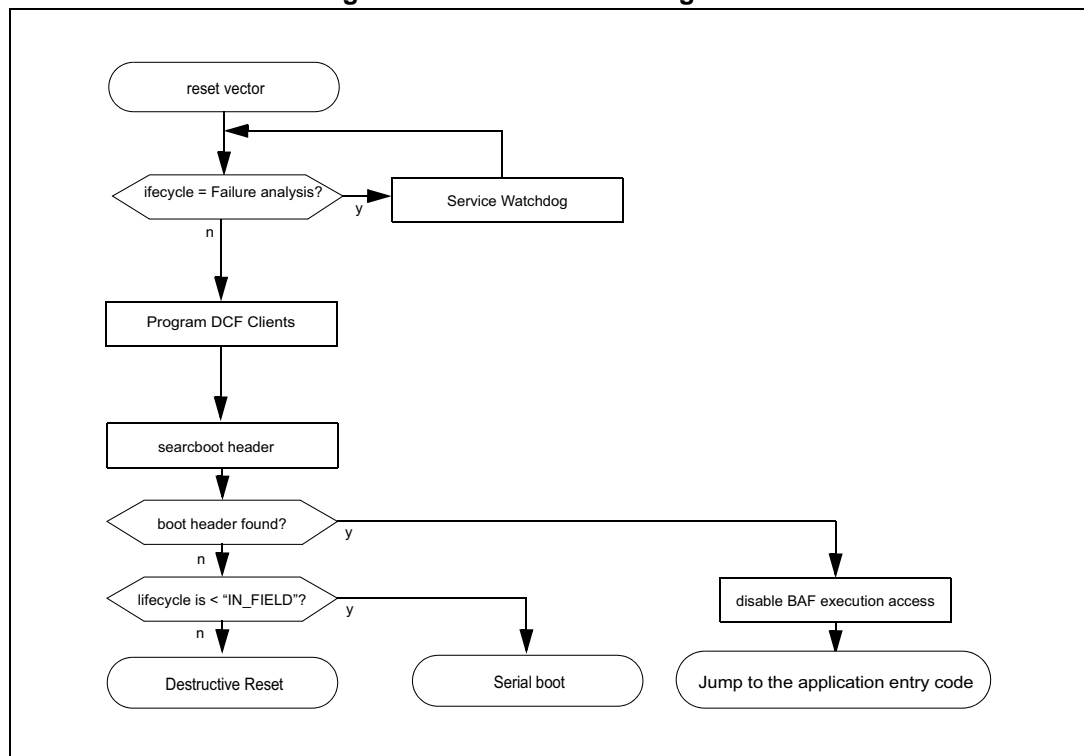
# 6 Clocking

## 6.1 Clock architecture

System clock for SPC560B5x is generated from three sources:

- Fast external crystal oscillator 4-16 MHz (FXOSC)
- Fast internal RC oscillator 16 MHz (FIRC)
- Frequency modulated phase locked loop (FMPLL)

Addionally, there are two low power (slow) oscillators:

- Slow internal RC oscillator 128 kHz (SIRC)
- Slow external crystal oscillator 32Khz (SXOSC)
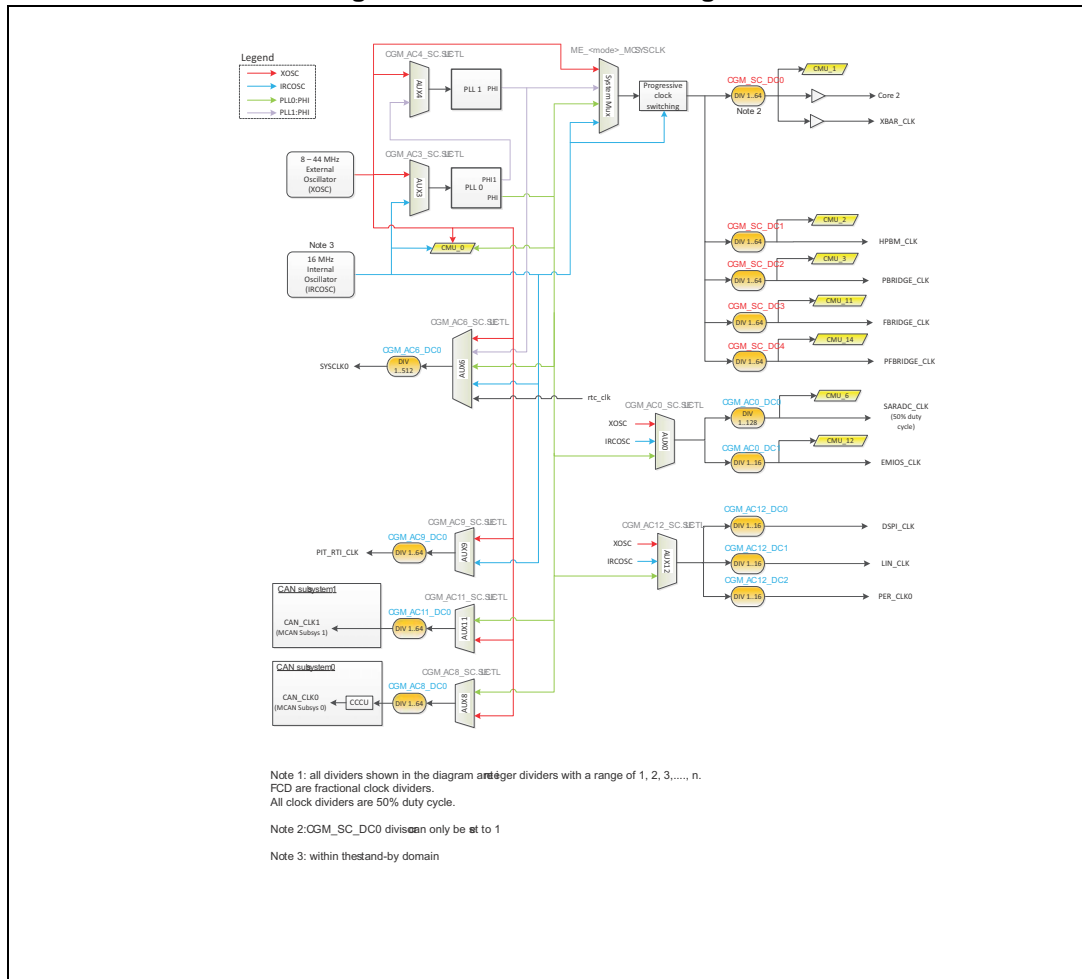
**Figure 8. SPC560B5x clock diagram**
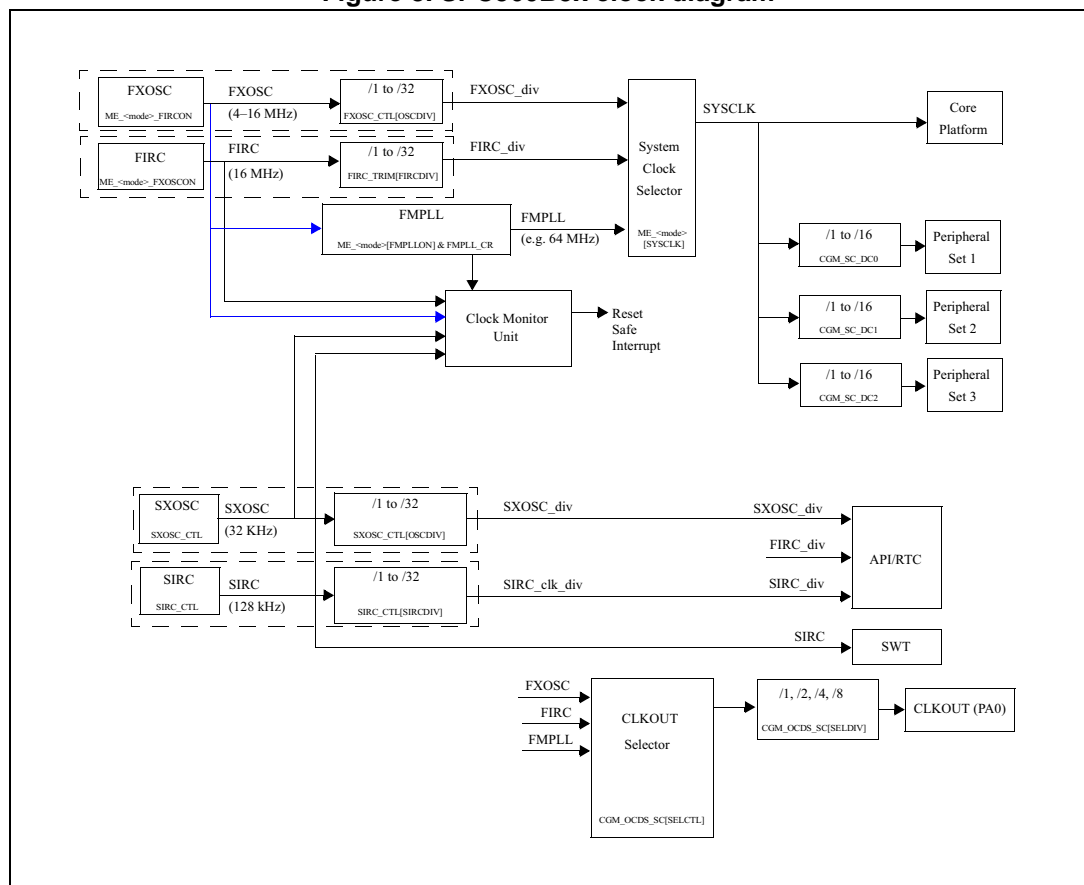


System clock for SPC582Bx is generated from three sources also:

- External oscillator/crystal (XOSC)
- Internal 16 MHz RC oscillator (IRCOSC)
- Frequency modulated phase locked loop (FMPLL)

Additionally there is the Slow internal RC oscillator 128 Khz (SIRC) as low power (slow) clock source.

**Figure 9. SPC582Bx clock diagram**



## 6.2 RTC/API (real time clock/autonomous periodic interrupt)

The RTC is a free running counter used for time keeping applications. The RTC may be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low power mode). The RTC also supports an autonomous periodic interrupt (API) function which can be used to generate a periodic event to the wakeup unit or an interrupt request. Both devices have one RTC/API, with the following different features in terms of counter clock sources.

**Table 5. Main difference between SPC582Bx and SPC560B5x**

|                                | SPC582BX                        | SPC560B5x                                        |
|--------------------------------|---------------------------------|--------------------------------------------------|
| Code Flash size                | 2                               | 2                                                |
| Type of counter clock sources  | LPRC prescaled by 8 (128 kHz)   | SIRC (128 KHz)<br>SXOC(32 KHz)<br>FIRC (16 MHz)  |

# 7 System

## 7.1 STM

Both devices provide one System Timer Module, with a difference regarding the clock source in charge to drive it.

SPC582Bx STM is driven by FBRIDGE clock divided by an 8bit prescale value; SPC560B5x STM is driver by the system clock divided by an 8bit prescale clock.

Here are the full feature, common to both:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode.

## 7.2 PIT (Periodic interrupt Timer)

Both devices have 6 channel PIT, the SPC582Bx PIT is also able to trigger DMA channels.

# 8 Debug

## 8.1 Nexus interface

Both devices support Nexus interface.

SPC582Bx has a Nexus Class 3+, the SPC560B5x has a Class 1 except for LBGA208 (emulation package) which provides the Class 2+

# 9 Communication I/F

## 9.1 LIN

SPC582Bx contains 6 Linflex, SPC560B5x contains 4 LinFlex.

The first one is DMA capable, the second one is not DMA capable.

**Table 6. Lin difference between SPC582Bx and SPC560B5x devices**

| Features | SPC582BX | SPC560B5x |
|---|---|---|
| N. of Linflex | 6 | 4 |
| Protocol version | version 1.3, 2.0, and 2.1 | Versions 1.3, 2.0, 2.1, and J2602 |
| Timeout management | Yes | No |
| DMA interface | Yes | No |
| Separate clock for baud rate calculation | Yes | N0 |

## 9.2 CAN

SPC582Bx has two CAN subsystem implemented

- CAN subsystem
- CAN subsystem

**Figure 10. CAN subsytem for SPC582Bx**
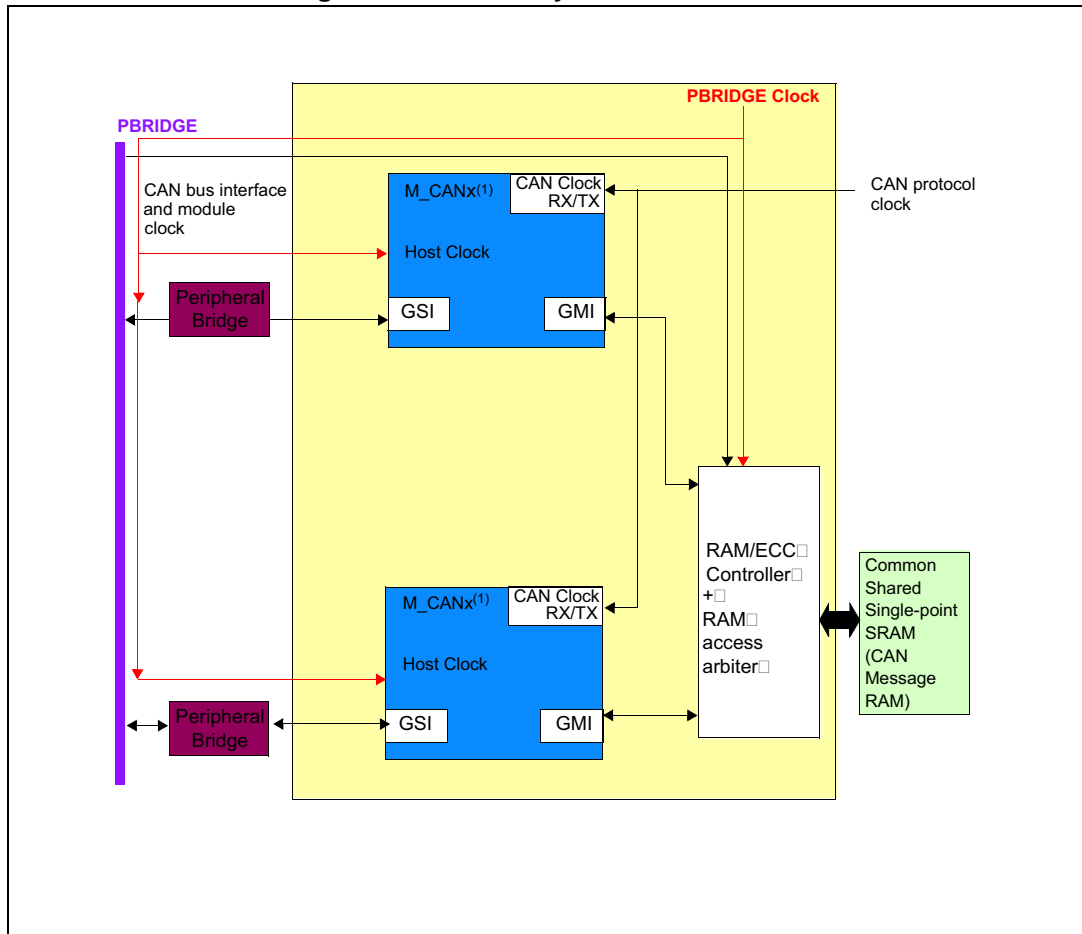


1.  Number of M_CAN nodes( M_CANx) varies per device.Please refer to RM0403 "SPC582Bx 32-bit Power
    Architecture® microcontroller for automotive vehicle body and gateway applications" Chapter 7 Device
    configuration to see the number of M_CAN nodes used in the device.

Features:

The can subsystem consists of the following major blocks:

•   Modular CAN cores: The registers of the CAN module can be accessed using the
    Generic Slave Interface (GSI)

•   CAN-RAM arbiter

•   SRAM interface and memory organization

•   ECC controller

SPC560B5x has the FlexCAN implemented.

The FlexCAN module is a communication controller implementing the CAN protocol
Specification.

**Figure 11. FlexCAN subsystem for SPC560B5x**
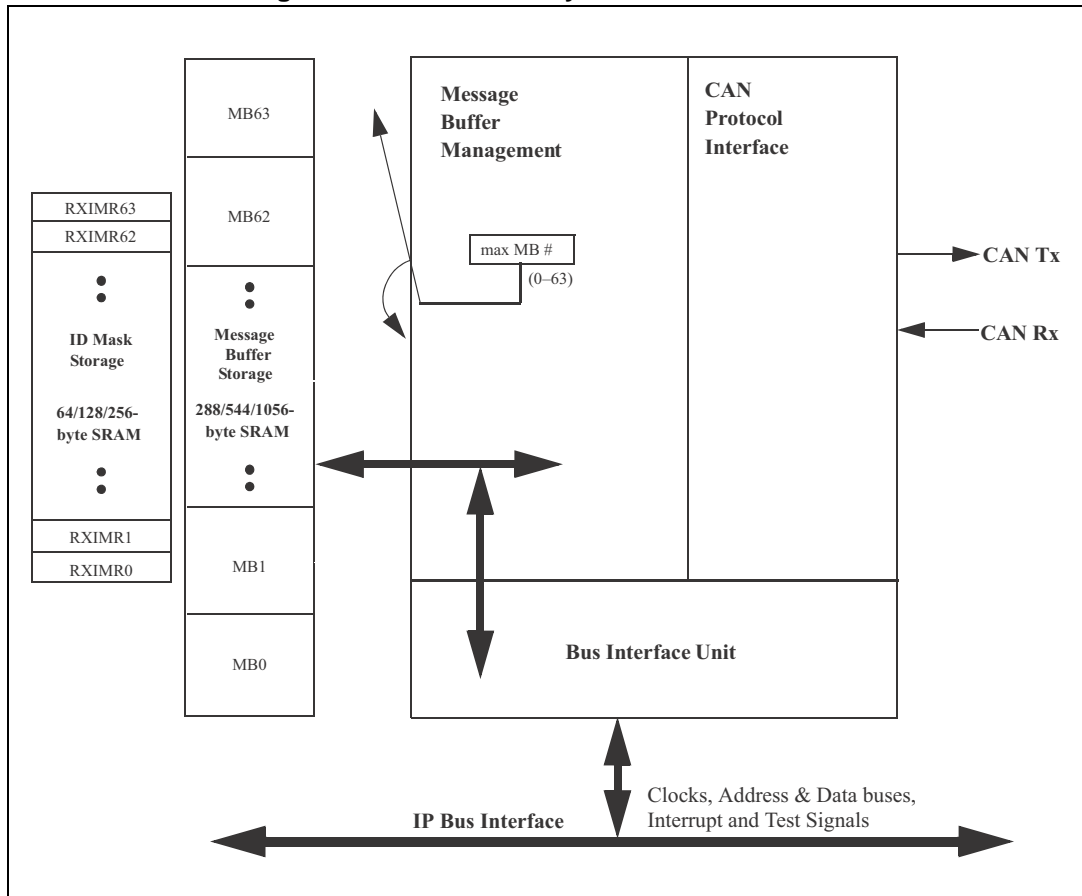
Features:

- Full implementation of the CAN protocol specification, version 2.0B
    - Standard data and remote frames
    - Extended data and remote frames
    - 0-8 bytes data lenght
    - Programmable bit rate up to 1 Mbit/s
    - Content-related addressing
- Flexible message buffers (up to 64) of zero to eight bytes data length
- Each MB configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per message buffer
- Includes either 1056 bytes (64 MBs) of SRAM used for MB storage
- Includes either 256 bytes (64 MBs) of SRAM used for individual Rx Mask Registers
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN version
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode
- Hardware cancellation on tx mesage buffers

## 9.3 I$^2$C

Both devices provide I2C interface, with some difference showed below by looking at the features.

- Maximum communication lenght and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF (SPC582Bx)
- No support for general call address (SPC560B5x)
- Not compliant to ten-bit addressing (SPC560B5x)

## 9.4 DSPI

For both devices, DSPI can operate in SPI configuration.

SPC582Bx has 4 DSPI, SPC560B5x has 3 DSPI.

Here the main differences:

- Type of transfer
  - Full-duplex, for wine synchronous transfers (SPC582Bx)
  - Full-duplex, three -wire synchronous transfers (SPC560B5x)
- Programmable transfer attributes on a per-frame basis
- **SPC582Bx**
  - 8 transfer attribute registers along with 8 extended transfer attribute registers
  - serial clock with programmable polarity and phase
  - various programmable delays
  - programmable serial frame size of 4 to 64 bits, expandable by software control. SPI frames longer than 32 bits are supported using the continuous selection format
  - Continuosly held chip select capability
  - parity control
- **SPC560B5x**
  - 6 clock and transfer attribute registers
  - Serial clock with programmable polarity and phase
- Programmable delays
  - CS to SCK delay
  - SCK to CS delay
  - Delay between frames
- Deglitching support
  - up to 128 Peripheral Chip Selects with external demultiplexer (SPC582Bx)
  - for up to 32 peripheral chip selects with external demultiplexer (SPC560B5x)
- DMA support for adding entries to TX FIFO and removing entries from RX FIFO **(SPC582Bx)**:
  - TX FIFO is not full (TFFF)
  - RX FIFO is not empty (RFDF)
  - CMD FIFO is not full (CMDFFF)
- SPC582Bx
  - End of Queue reached (EOQF)
  - TX FIFO is not full (TFFF)
  - CMD FIFO is not full (CMDFFF)
  - Transfer of current frame Complete (TCF)
  - Transfers due from current Command frame Complete (CMDTCF)
  - Transfer of current SPI frame Complete (SPITCF)
  - Transfer of current SPI frame complete (SPITCF)
  - attempt to transmith with an empity Transmith FIFO (TFUF)
  - RX FIFO is not empty (RFDF)
  - frame received while Receive FIFO is full (RFOF)
  - SPI parity error(SPEF)
  - data present in TX FIFO while CMD FIFO is empity (TFIWF)
- SPC560B5x

- End of queque reached (EOQF)
- TX FIFO is not full (TFFF)
- Transfer of current frame complete(TCF)
- RX FIFO is not empity(RFDF)
- FIFO overrun (attempt to transmit with an empity TX FIFO or serial frame received while RX FIFO is full) (RFOF) or (TFUF)
- Power-saving architectural features: support for stop mode (SPC582BX)

# 10 Timed I/O

## 10.1 eMIOS

The eMIOS provides functionality to generate or measure time events.

Here are the main differences:

- Number of blocks
  - 1 eMIOS block with 32 channels (SPC582Bx)
  - 2 eMIOS blocks with 28 channels each (SPC560B5x)
  - 50 chanenels with OPWMT, which can be connected to the CTU
  - 6 channels with single action IC/OC
  - Both eMIOS blocks can be synchronized
- eMIOS block can be synchronized from outside (SPC582Bx)
- Flag outputs of channels 8-11 of eMIOSs are used to disable the outputs of other channels. They form the ODIS bits **(**SPC582Bx)

## 10.2 SCTU (Self Test Contrl Unit)

To handle safety features, the SPC582Bx implements a STCU (for instance memory Buily-In Self test - MBIST). SPC560B5x does not implement the STCU module.

# 11 Analog modules

## 11.1 ADC/SARADC

SPC582Bx provides 64 ADC channels distributed between 10bit, 12bit, stdby ADC and an independent 12 bit SARADC.

SPC560B5x provides 36 ADC channels with 10bit resolution.

SPC560B5x ADC features:

- 10-bit resolution
- 36 channels (depending on package type), expandable to 64 channels via external multiplexing)
  - As many as 16 precision channels
  - As many as 20 standard channels, 4 being expandable to as many as 32 external channels
- Address decoder signal generation (alternate functions MA[2:0]) to control external multiplexers
- Individual conversion registers for each channel (internal and external)
- 3 different sampling and conversion time registers CTR[0:2] (internal precision channels, standard channels, external channels)
- As many as 64 data registers for storing converted data. Conversion information, such as mode of operation (normal, injected or CTU), is associated to data value
- Conversion triggering sources:
  - Software
  - CTU
  - PIT channel 2(for inject conversion)
- 4 analog whatchdogs
  - Interrupt capability
  - Allow continuous hardware monitoring of 4 analog input channels
- Presampling (VSS and VDD)
- Conversation on external channels managed in the same way as internal channels, making it transparent to the application
- One shot/Scan Modes
- Chain Injection Mode
- Power-down mode
- 2 different abort functions allow to abort either single-channel conversation
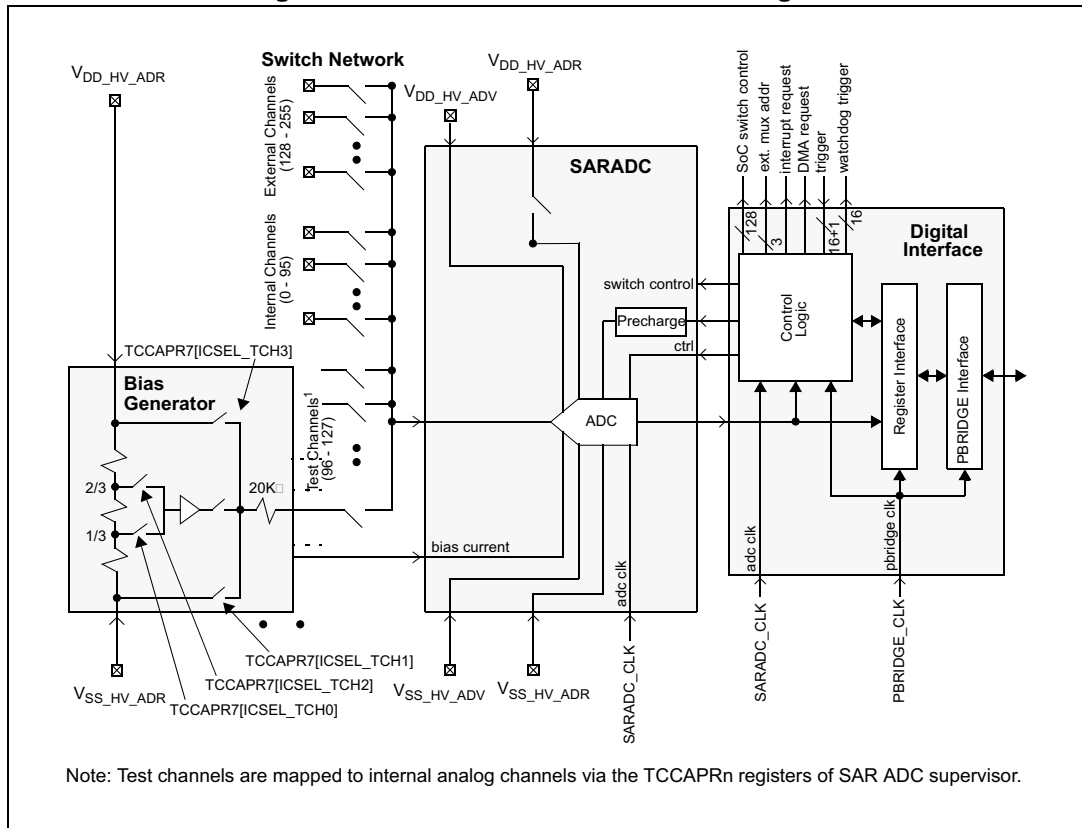- Auto-clock-off

**Figure 12. SPC560B5x ADC implementation**
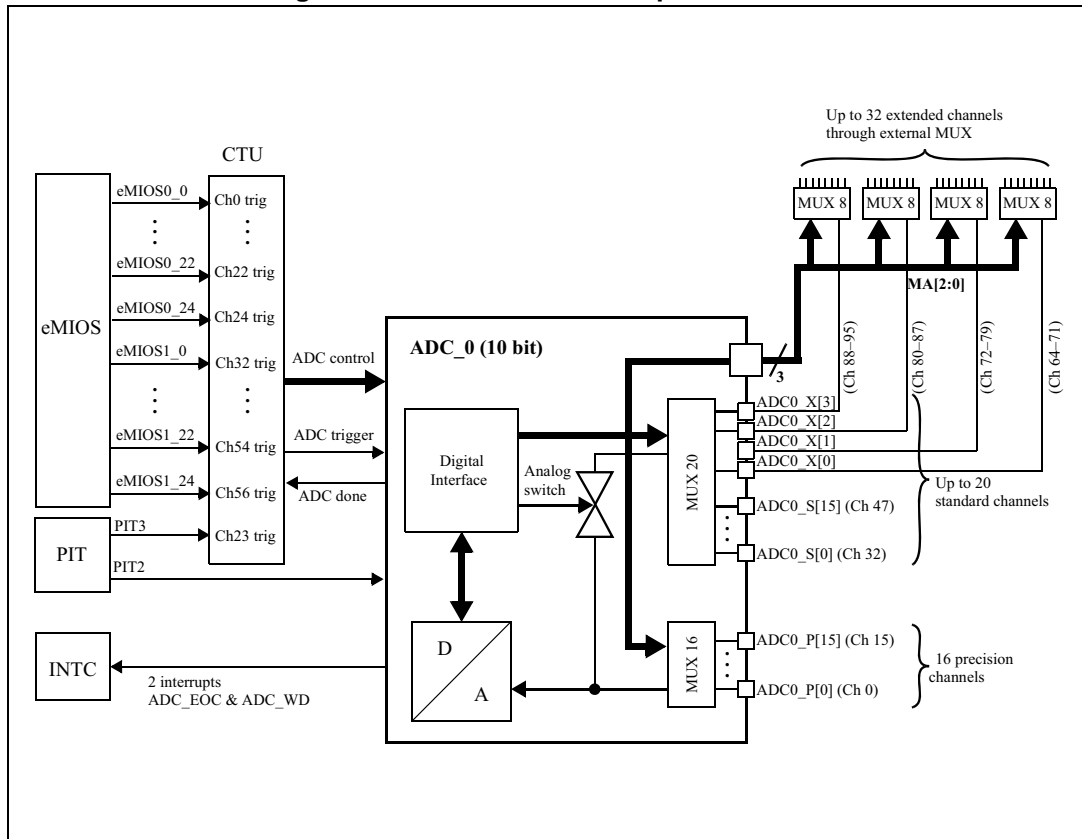
There are instead the list of the features about SPC582Bx SARADC, not available in SPC560B5x series:

- Selectable 10-bit or 12-bit data resolution output for 12-bit SARADC
- Selectable 8-bit or 10-bit data resolution output for 10-bit SARADC
- Up to 96 internal channels, 32 test channels, 128 external channels supported; variable number of analog channels of each type controlled by parameters
- 4 different conversion timing registers selectable for any channel
- Mapping of external channel to any internal channel through static programming by software
- Shorting of test channel with internal channel through static programming by software
- External decode signals (3 signals) for selection of external analog mux inputs
- Normal conversion with One Shot/Scan modes
- Injected conversion with dedicated trigger input
- 2 different abort features that allow to abort either a single channel conversion or chain conversion
- Reference selection for each channel
- Power Down Mode
- Dedicated data register for each channel, containing the following information regarding to the conversion result in one half-word:
  - 10-bit or 12-bit for 12-bit SARADC
  - 8-bit or 10 bit for 10-bit SARADC
- Status byte which provides some conversion information such as mode of operation (Normal, Injected, or CTU), data valid, data overwritten status
- Control byte for reference selection, conversion timing parameter selection
- Configurable number of analog watchdogs.Trigger outputs on watchdog threshold crossover events
- 2 different CTU modes (CTU Control mode and CTU Trigger mode) available when CTU feature is present in SARADC instance
- Interrupt/DMA support for the following conditions
  - End of conversion of single channel for both normal, injected conversions
  - End of conversion chain for both normal, injected conversions
  - End of CTU conversion
  - Watchdog Thresholds crossover

### Figure 13. SPC560B5x SARADC block diagram



Note: Test channels are mapped to internal analog channels via the TCCAPRn registers of SAR ADC supervisor.

# 12 Safety

## 12.1 FCCU/CRC/MBIST

These features are available on SPC582Bx only.

# 13 Appendix A

## 13.1 Reference document

1. SPC582B60x, SPC582B64x, SPC582B50x Datasheet – target specification
2. SPC582Bx Reference Manual – RM0403
3. SPC582Bx Reference Manual – RM0403
4. SPC560B5x Reference Manual - RM0017

# Revision history

**Table 7. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-May-2018 | 1 | Initial release. |

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**