Digital multi-phase constant-on-time regulator based on voltage controlled oscillator

Introduction

Digital controllers require few external components compared to analog solutions and so they could be very appreciated in very compact and high density designs like server power management. Moreover, the available area dedicated to the output filter is very small and also full ceramic capacitors design and high frequency operation are mandatory in this field.

As known, ceramic capacitors have very low ESR, so system stability could be compromised if a proper compensation network is not well designed or if control topology suffers at a very small output voltage ripple.

In this condition, voltage mode topology is usually preferred because it guarantees good stability with very low ESR by introducing additional zero in the compensation network but it finds its major weak points in the dynamic performances under load transient activity (see *1* in *Section 5: Literature and references on page 13*).

In fact, voltage mode controllers are clocked systems with fixed switching frequency and for this reason suffer of action delay (see *2* in *Section 5*). Because of this delay the entire system cannot respond to a load transient event with its theoretical closed loop bandwidth and the output voltage drop depends on when the load is applied during the switching period.

To improve this weakness and minimize the action delay, various solutions, like non-linear controls, are added to classic voltage mode architectures (see *3* and *4* in *Section 5*), but these features are often resulting on a trade-off between sensitivity to detect a load transient and noise immunity from switching activity. Moreover these techniques give "on/off" behavior and the response could be out of specification if the non-linear sensor was not triggered correctly.

It is known (see *5* in *Section 5*) that a constant-on-time (COT) controller has more linear response than the voltage mode. However this topology has different weaknesses. It has poor noise immunity and the system stability depends on the shape of the output voltage ripple.

This last characteristic doesn't enable this controller to full ceramic design where the ESR is very small and the system stability could be compromised.

Some analog and digital solutions have been proposed to enable COT to high frequency and ceramic output capacitors design (see *6* in *Section 5*) by adding to the error voltage a compensation ramp depending on the current inductor. Furthermore this controller would also require a very fast and accurate inductor current A/D to get the loop stability when ceramic capacitors are used. This could require an expensive A/D especially in a multi-phase controller. The solution referenced in *Section 5*, no. *7* "Digital hybrid ripple-based constant on-time control for voltage regulator modules", relieves the cost of this requirement with an inductor current estimator together with an average current inductor A/D but the risk of instability would require anyway some guidelines and the transient response could be slow.

Moreover another issue of the COT is the dependence of loop stability from input and output voltage. In fact, it's known that the output voltage ripple is a function of both V_{IN} and V_{OUT} in a buck controller.

Contents

1 Abstract

During the last decade, the technology's evolution of modern microprocessors required better computing performance and more efficient power management platforms. A faster processor in a less power envelope has led to lower supply voltages down to 1.2 V according to the used thinner gate oxides and higher currents even up to 200 A. Power systems are becoming increasingly complex; the classical concept of control has gradually evolved into the more general problem of power management, demanding functionalities that are hardly achievable in analog controllers.

The high flexibility offered by digital controllers and their capability to implement sophisticated control strategies, together with the programmability of controller parameters, make digital control very attractive for improving the features of DC-DC converters. By using of PC-based design tools, the digital controller can be fully configured and the power supply parameters can be monitored as well in order to optimize the total system efficiency.

In this document an innovative digital control technique is proposed for multi-phase buck topologies, but it could be applied also to the only one-phase system. This new digital modulator is derived from the analog STVCOT® (see *1* in *Section 5: Literature and references on page 13*) and combines advantages of both - the voltage mode and constant-on-time techniques.

2   Digital STVCOT®

To get advantages from both - the voltage mode and constant-on-time controllers, new analog control architecture has been introduced (see *1* in *Section 5: Literature and references on page 13*).

The main advantage of this topology is the full linearity of response, typical of the COT controllers. In fact, the system will respond to any load transient event with the real bandwidth set by the application, canceling the typical action delay of voltage mode controllers without using any non-linear response. Moreover, by introducing a compensation network, it's possible to add an additional zero to guarantee the system stability when low ESR design is required without adding any compensation ramp, typical of the COT regulators that could slow the transient response.

Analyzing this topology it's clear as the STVCOT controller, proprietary of STMicroelectronics, can be digitalized easily simplifying the board tuning and reducing the total bill of material (BOM) cost. System linearity and fast response are mandatory and for these reasons an oversampled controller is required not to compromise the transient response action.

Figure 1. Analog STVCOT multi-phase architecture
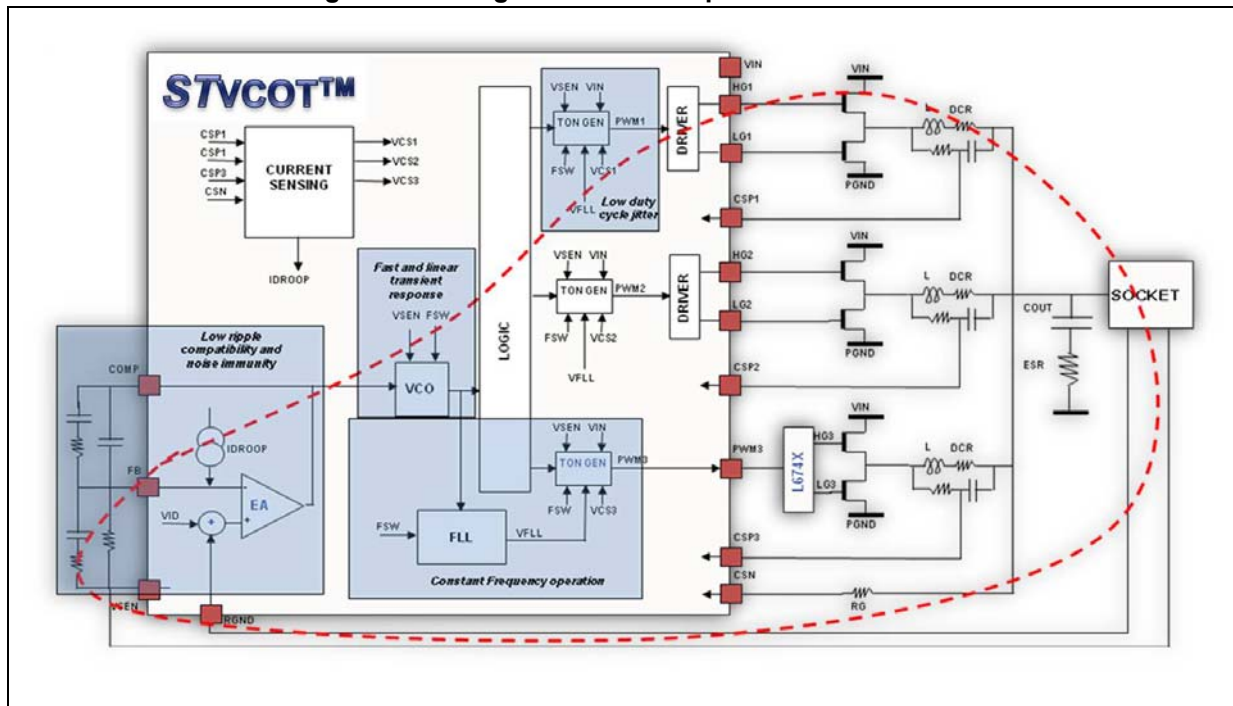
2.1 Digital error generation

Many times programmable output resistance (i.e. droop function) is required. To do this it's necessary to read the total output current information. In order to minimize the number of analog to digital converters (ADC), saving the area and current consumption, the current information is added to the error voltage and V_{ERR} is generated.

Equation 1

$$V_{ERR} = V_{CM} + V_{REG} - V_{DROOP} - V_{OUT}$$

Where V_{CM} is a common mode voltage and V_{DROOP} is the product between the programmed R_{DROOP} and output current. High accuracy requirements need high resolution ADC design to get to the accuracy level required. In this case it has been chosen to have 2 mV as the resolution in order to guarantee a quantization error of ± 0.2% with a minimum output voltage of 0.5 V.

The low conversion time and high throughput rate are fundamental requirements for quick transient response. For this reason we have chosen a very fast 7-bit pipeline A/D converter with a full scale range equal to 256 mV (± 128 mV on V_{CM}), 40 Msps and a latency of 62.5 ns.

2.2 Compensation filters

To guarantee good stability for every output filter, the Type II or Type III compensation is needed. It's known as digital PID controllers, by derivative, proportional and integrative actions, can implement a filter with two zeros and an integrative action. Low pass filters are needed at the input and output of the PID in order to filter high frequency spectral components and limit the gain at high frequency. The digital relationship of the PID can be written as:

Equation 2

$$PID(n) = PID(n - 1) + C_1 \bullet ERR_{FILT}(n) - C_2 \bullet ERR_{FILT}(n-1) + C_3 \bullet ERR_{FILT}(n-2)$$

Where:

Equation 3

$$C_1 = K_P + \frac{K_1}{f_{CK}} + K_D \bullet f_{CK}$$

$$C_2 = K_P + 2K_D \bullet f_{CK}$$

$$C_3 = K_D \bullet f_{CK}$$

and f_{CK} is the system clock frequency.

2.3   Full linear response

In order to make the controller response linear and cancel the action delay, it's needed to pass from the constant switching to the variable switching controller and to have the duty cycle linearly dependent from the COMP. The main concept of the STVCOT controller is to anticipate or delay the PWM firing according to the COMP voltage. If the COMP increases, also the switching frequency will increase. If the COMP decreases, the controller will decrease its frequency. To do this it's easy to think to correlate switching frequency to the COMP signal by a well-known component, the Digital VCO (DVCO). The insertion of the DVCO between the PID and the duty cycle generation generates a new pulse width modulator that inherits the error amplifier from the classic voltage mode and the on-time from COT controllers. The general transfer gain from the input to output of the DVCO can be written as:

Equation 4

$$G_{VCO} = \frac{F_{VCO}}{COMP}$$

At this point the DVCO will produce a clock signal at F_{VCO} frequency. This clock signal will be multiplexed to each phase by a simple shift register.

The gain of this new PWM modulator is:

Equation 5

$$\frac{duty_{PWM}}{COMP} = \frac{V_{OUT}}{V_{IN} \bullet F_{SW}} \bullet \frac{G_{VCO}}{N}$$

N represents the phase number to be multiplexed from the shift register. From this formula it is clear how the gain between the COMP and the duty cycle is proportional to the output voltage, whereas the input voltage dependence represents the feed forward compensation. The dependence from the output voltage is a weakness for the system stability because the total gain, the phase margin and the system bandwidth could not be under control at different regulated output voltages.

To eliminate this dependence it is necessary to make G_{VCO} dependent from output voltage and from the nominal F_{SW} in order to have:

Equation 6

$$\frac{duty_{PWM}}{COMP} = \frac{K}{v_{in}}$$

Then G_{VCO} has to be:

Equation 7

$$G_{VCO} = \frac{N \bullet K \bullet F_{SW}}{V_{OUT}}$$

2.4 Digital PWM (DPWM)

To avoid the limit cycle it's necessary to choose a proper DPWM resolution according to LSB of ADC (LSB_{ADC}). In fact, it's known (see *10* in *Section 5: Literature and references on page 13*) that to avoid the limit cycle LSB of the DPWM (LSB_{PWM}) has not to generate more than LSB_{ADC} of variation on the output voltage.

Moreover, it's useful to remember that for the constant-on-time controller, the control variable is T_{SW} instead of T_{ON} like a voltage mode.

Equation 8

$$V_{OUT} = \frac{T_{ON}}{t_{SW}} \bullet V_{IN}$$

V_{IN} is the input voltage, t_{SW} is the switching period and T_{ON} is the constant-on-time. For one LSB_{DPWM} of variation on t_{SW}, a variation on V_{OUT} is generated:

Equation 9

$$\Delta V_{OUT} = \frac{T_{ON}}{t_{SW-NOM}^2} \bullet V_{IN} \bullet LSB_{DPWM} = \frac{V_{OUT}}{T_{SW-NOM}} \bullet LSB_{DPWM}$$

In this case T_{SW_NOM} represents the steady state switching period. The variation on V_{OUT} must be less than LSB_{ADC}, then:

Equation 10

$$LSB_{DPWM} \leq LSB_{ADC} \bullet \frac{1}{F_{SW-NOM} \bullet V_{OUT}}$$

For 2.3 V as maximum output voltage and 1 MHz as maximum switching frequency, 870 ps as DPWM resolution is obtained. By using a clock frequency of 40 MHz and 5 bits of the DPWM, the resolution will be 781 ps, which is enough to avoid any possible limit cycle due to DPWM resolution.

2.5 Constant frequency operation and current sharing

Thermal design constraints and EMI rejection requires a modulator with a fixed switching frequency at least during the steady state condition. In this case, voltage mode structure has inherently a constant frequency embedded in the PWM saw-tooth signal.

The nominal output frequency of the DVCO will be N times the nominal F_{SW} (where *N* is the number of phases), but the constant-on-time architecture cannot guarantee constant F_{SW} if it keeps the constant-on-time of the PWM. In fact the controller has to be able to change it to compensate the system losses at load current variation and increases the F_{SW} (see *11* in *Section 5*). To solve this issue, the analog STVCOT modulator (see *1* in *Section 5*) embeds another system, called the digital frequency locked loop (FLL).

Also in the digital controller this function can be implemented easily. The digital FLL (DFLL) measures the DVCO frequency and compares it to the nominal switching frequency set by the board designer, multiplied by N. If the real frequency is higher than nominal frequency, the on time will be increased and vice versa, if the real frequency is less then nominal frequency, the on time will be decreased (see *12* in *Section 5*). The main requirements for

the DFLL is that its bandwidth has to be very slow not to interact with the main loop, but this constraint is easily reachable for digital signal processing.

The DFLL is not the only mechanism that changes the on-time. In multi-phase converters another feature is required to keep the phase currents under control. In fact, due to components and layout mismatches and parasitic resistances, the unbalancing current could occur and the system reliability could be compromised.

In order to control the balancing phase current, a current reading circuit reads the current of each phase and each current is compared to the average current of the system.

One ADC per phase converts this error to the digital word that will be processed to adjust the on-time at each switching cycle. If the phase current is higher than the average current then the on-time will be decreased and at the same manner, if the phase current is less than the average current then the on-time will be increased.

The DFLL and current sharing features require fine adjusting of on-time per each phase. This requirement brings to have the DPWM also for on-time and not only for off-time as the classic constant-on-time would need.

It's useful to check that 781 ps of DPWM resolution does not generate limit cycles on frequency and current sharing regulations.

If the DFLL and current sharing loops are designed to have their loop bandwidth much lower than main loop bandwidth, output voltage can be assumed like a virtual ground from the DFLL and the current sharing loops point of view.

For frequency regulation it's possible to write:

Equation 11

$$\Delta t_{SW} = \frac{\Delta T_{ON}}{V_{OUT}} \bullet V_{IN}$$

The frequency can be measured easily with the system clock (f_{CK}), in this case equal to 40 MHz. The resolution of frequency measurement will be 25 ns (T_{CK}).

To avoid the limit cycle on the frequency regulation, switching period variation due to the on-time variation has to be less then measurement resolution.

Then:

Equation 12

$$\Delta T_{ON} < \frac{V_{OUT}}{V_{IN}} \bullet T_{CK}$$

With 0.5 V as minimum V_{OUT} and 19 V as maximum input voltage, a minimum resolution of 658 ps has to be implemented. This means that we will need to add a bit to our DPWM resolution: with 6 bits, 390 ps of DPWM resolution avoid any possible limit cycle on frequency regulation. Note that this resolution is only needed on the Ton duration, so it is still possible to save some area and calculation power using a 5-bit resolution to generate the PWM start time (and that's enough to avoid limit cycles on the main control loop) and a 6-bit resolution for the Ton duration (necessary to avoid limit cycles in the DFLL).

For current sharing control, it's possible to define:

Equation 13

$$\Delta I_{PHASE} = \frac{V_{IN} - V_{OUT}}{L} \bullet \Delta T_{ON}$$

Maximum variation is obtained with maximum V_{IN}, minimum V_{OUT} and minimum inductance. By using an ADC for each current sharing error with 200 mA as resolution, it's possible to guarantee 0.5% of quantization error at 20 A of the load.

In this case, by choosing 19 V as maximum V_{IN}, 0.5 V and 100 nH as minimum output voltage and inductance respectively, the maximum current variation due to DPWM resolution is equal to 72 mA, much lower than current ADC resolution.

Figure 2 shows the full digital STVCOT architecture.

Figure 2. Digital STVCOT controller
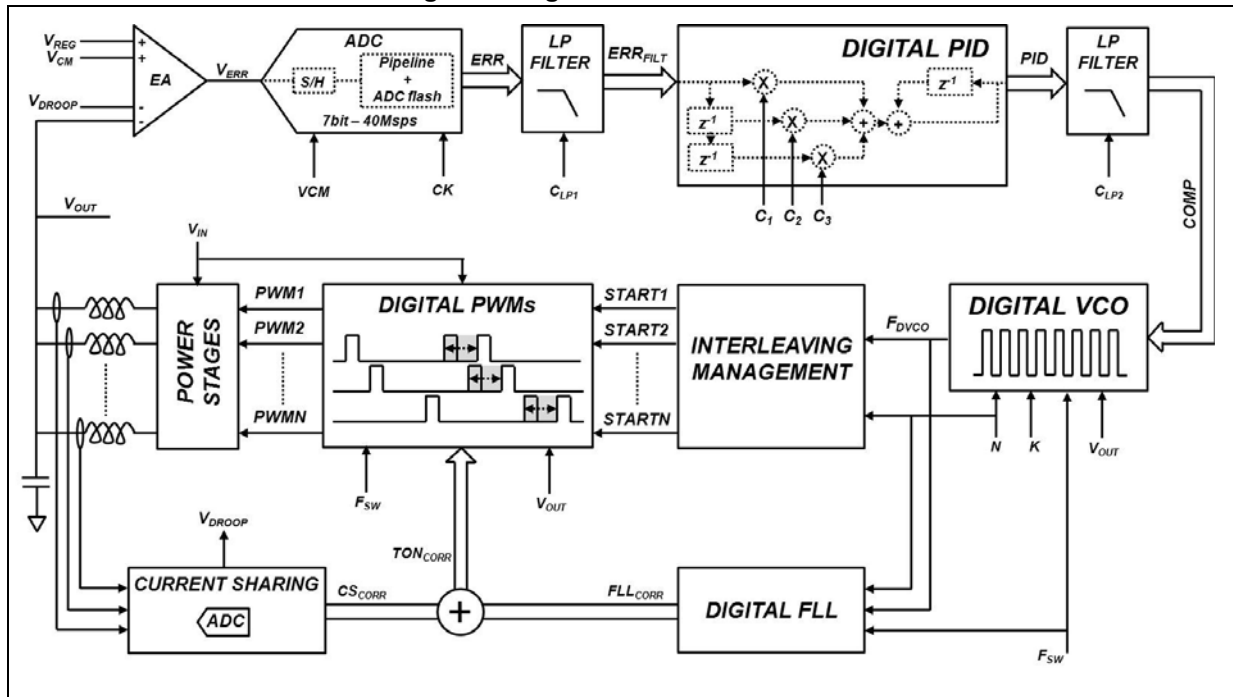
3 Results

The following measurements comes from a server processor multi-phase application running at 1 MHz, 6 phases, 1.8 V, 1 mΩ as droop resistance, 150 nH inductors and only ceramic capacitors at the output voltage.

Figure 3 shows the typical load transient response of the STVCOT controller. In this figure it's possible to see the controller ability to overlap the phases linearly in order to react to the voltage drop.

Figure 3. 6-phase load transient response 160 A/260 ns
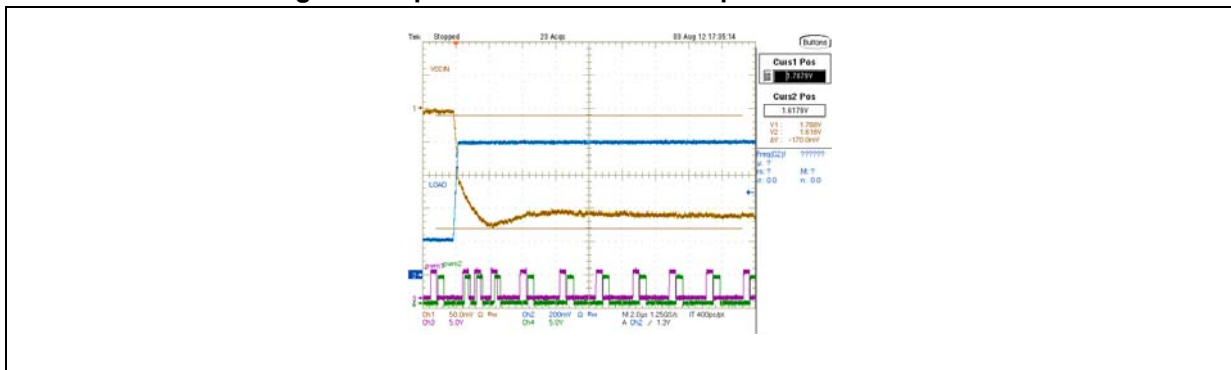
Figure 4 demonstrates the exceptional adaptability of the STVCOT control loop architecture to very severe and unknown behavior of the digital load. The output voltage is always properly regulated within the designed voltage window. This behavior demonstrates that the STVCOT control loop is able to respond with its real bandwidth to any load transient in spite of a very different load change rate spreading for order of the magnitude 150 A/µs up to 1750 A/µs without any action delay due to sampling effects.

**Figure 4. Different load transient rise time**
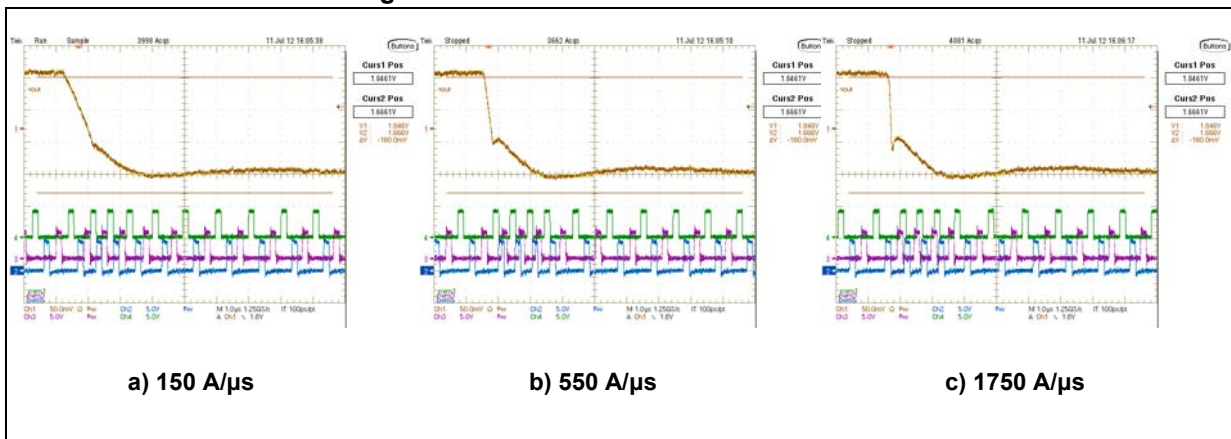
| a) 150 A/µs | b) 550 A/µs | c) 1750 A/µs |

Figure 5 shows jitter on PWMs in a 6-phase system at 700 kHz of the switching frequency operation and 60 A of the load current. The jitter amount demonstrates that there is not any limit cycle on regulation; it's principally due to the different system bandwidth.

Figure 5. PWM1-3 jitter for low and high bandwidth in 6-phase system

a) Low bandwidth   b) High bandwidth
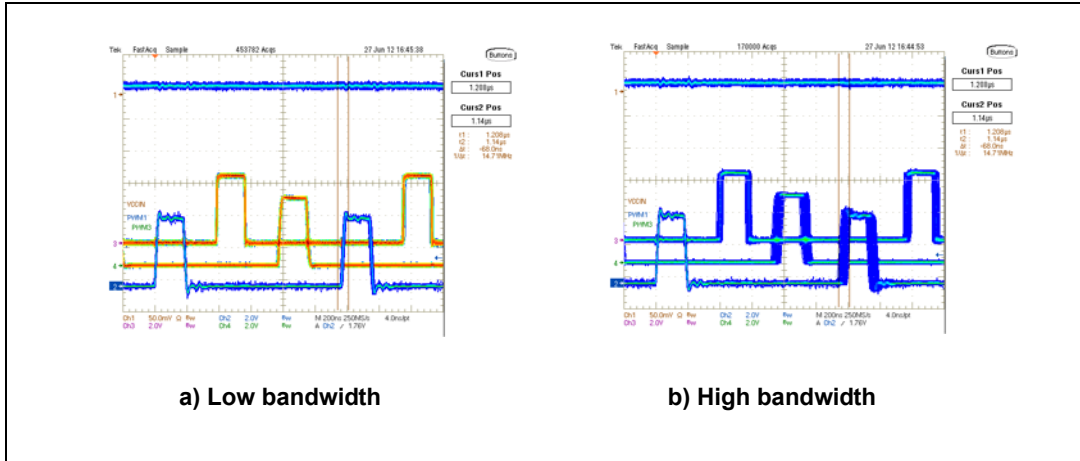
4 Conclusion

An innovative digital multi-phase controller has been shown. New topology shows a really cost optimized digital controller based on the constant-on-time controller implemented with a Digital VCO in the PWM modulator. This digital control loop architecture (STVCOT) allows achieving more than 1 MHz per phase using ceramic capacitors without any kind of the slope or virtual ESR compensation. Moreover it is done with very low jitter and no limit cycles. The new architecture allows a no-dithering DPWM, in this case implemented with 390 ps resolution and a very fast A/D with the 2 mV step, 7 bits and 40 Msps. The result has been obtained without the non-linear control thanks to the Digital VCO, so making the application design fast and easy experience.

The new controller allows canceling the typical action delay of voltage mode controllers by using oversampled digital control and linearizing the response by using a Digital VCO with a variable gain, making the system stability independent from both input and output voltage values.

5 Literature and references

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10. Peterchev, A; Sanders, S: Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters. Department of Electrical Engineering and Computer Science University of California, Berkeley.

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12. LTC®3770 - Fast No R$_{SENSE}$^{TM} Step-Down Synchronous Controller with Margining, Tracking and PLL.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
28-Mar-2017	1	Initial release.

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