TN1230
Technical note

Increase SPC563Mxx ADC accuracy

Introduction

This document indicates how to improve ADC performance in the SPC563Mxx microcontroller family.

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1 Layout recommendations

Getting the expected performance out of a high-performance ADC, is often a challenging task, because it gets affected by several factors.The proper choice of the external components, their placement and the routing can strongly influence the linearity, gain and offset. Additional noise can be induced to the ADC and even the input signal can become distorted. Several steps can be taken to prevent the ADC conversion results becoming corrupted. Any active element inside a microcontroller has direct or indirect connections to the power supply system; thus, any switching inside the microcontroller causes current to flow.

There are different noise sources that have to be taken into account:

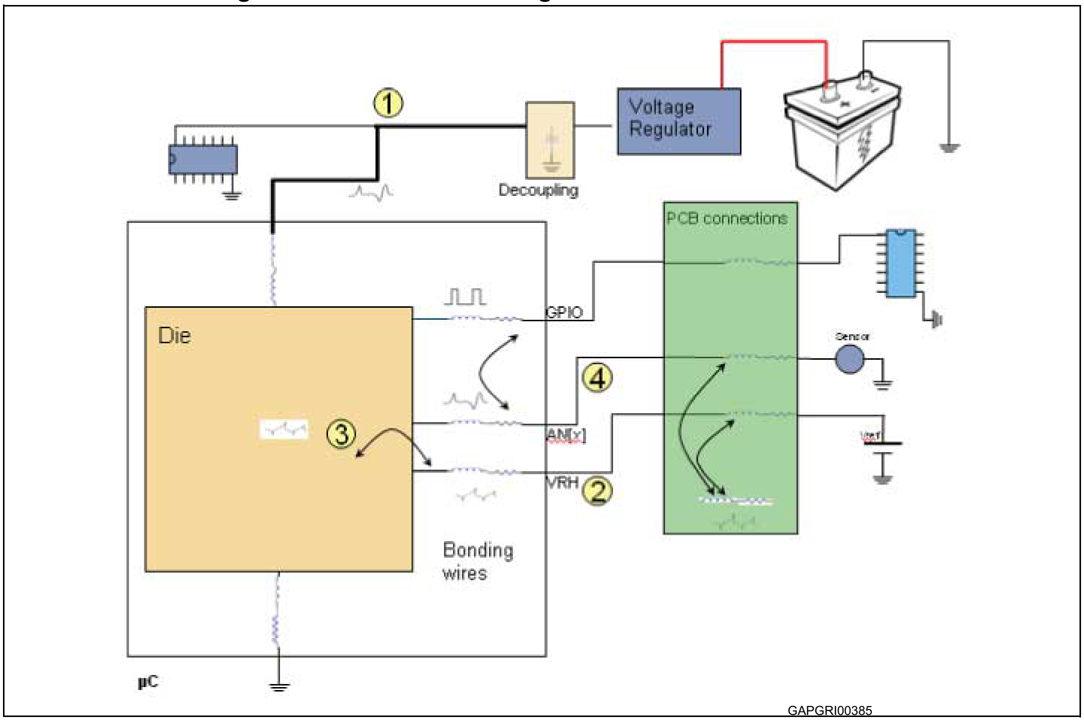
The conducted noise:

1. the noise generated by any other ICs on the board and transmitted through the power supply rail
2. the current inducted on ADC voltage reference, coupled via PCB parasitic inductance, coming from activities of other ICs
3. Noise generated inside the microcontroller due to internal logic; this can be coupled through the package impedance
4. Current inducted on ADC input pins, coupled with PCB parasitic inductance, coming from digital IO activity.

The radiated noise:

- PCB layout is analyzed in order to remove/minimize loops and wires that act as antennas.

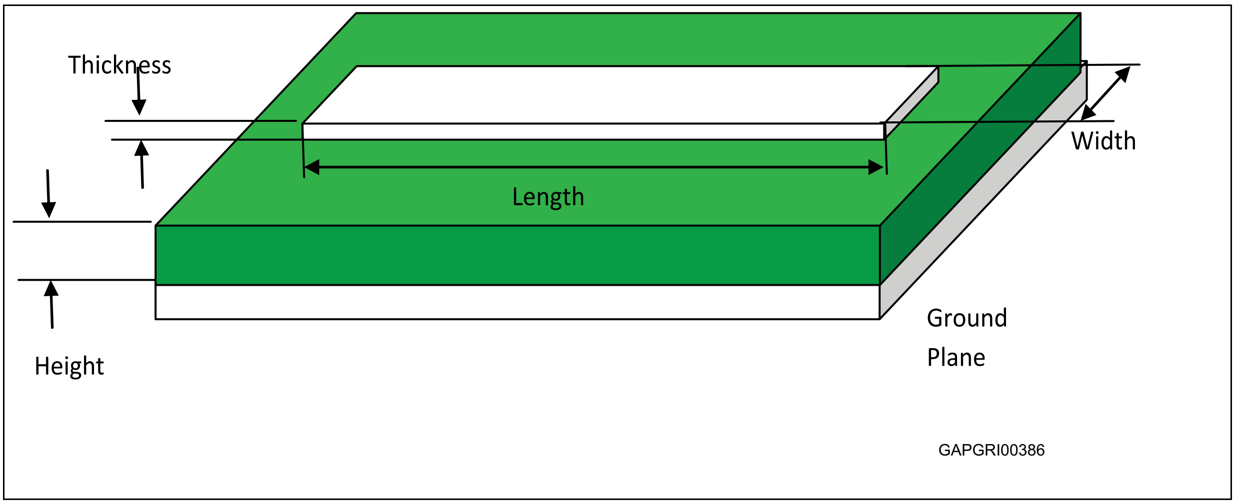
Figure 1. Noise influencing ADC conversion on PCB



In order to maximize ADC resolution, it is important to analyze power supply network, minimizing its impedance in the frequency range where the device works. Reducing both coupling mechanism and reducing connection impedence.

PCB connection can be modeled as RL; at low frequency impedance is purely resistive, while at high frequency it is an inductance.

Figure 2. PCB wire



The resistance and the inductance, in case of microstrip placed on ground plane, are calculated as follow:

Equation 1

$$Resistance = Copper\_Resistivity * \frac{Length}{Width * Thickness} * (1 + Temp\_Co * (Temp - 25))$$

where

Copper Resistivity	1.70E-06	ohm-cm
Copper Temp_Co	3.90E-03	ohm/ohm/C

Equation 2

$$Inductance = 2.64 * 87^2 * 10^{-11} * \ln\left(5.98 * \frac{Height}{0.8 * Width + Thickness}\right) * Length$$

Both inductance and resistance are inversely proportional to track width, thus, in order to reduce impedance, track width is increased.

If the inductance is still too large, a double plane is used. The inductance for both Vss and Vdd plane is pH/cm (inductance with single plane in the range of tens of nH/cm).

The noise from this current loop is proportional to the area of the loop(s); therefore, it is necessary to design these loops as small as possible.

One such loop, is the current loop between the microcontroller and the decoupling capacitors (including VCR33 capacitor). Ceramic capacitors are used next to the power pins of the microcontroller, connected if possible directly through small island (micro - plane) or with thicker or wider traces that lower inductive impedance of the line.

Moreover, in order to further reduce the inductance contribution on VCR33, the key point for reducing noise on ADC, two capacitors of 1uF in parallel are used on VCR33 to get the 2uF in order to half capacitor series inductance.

This technique that uses two capacitors in parallel can be used in any other loop.

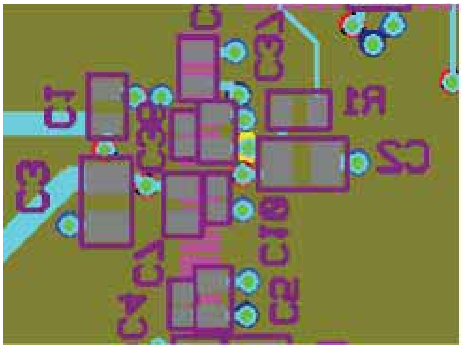
A small ceramic capacitor, very close to micro pin, 1 nF, in parallel to 2uF can help to suppress HF noise.

If possible, keep digital pins away from analog pins when this is not possible, using extra shielding between digital and the analog tracks is recommended.

For improving decoupling, two vias can be used to connect the capacitor to the ground plane.

A layout that tries to divert digital return current away from the ADC supply/inputs is recommended.

Figure 3. Decoupling capacitors close to micro pin



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To preserve the accuracy of the A/D converter, it is also necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite (100 nF is already a good value). This capacitor contributes to attenuating the noise present on the input pin; furthermore, it charges during the sampling phase, when the analog signal source is a high-impedance source.

A real filter, can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC Filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

2 Reducing Flash coupling effects

Experimental results conclude that noise coming from Flash supply coupling externally with ADC supply can be reduced.

When the internal 3.3 V voltage regulator is enabled, VCR33 pin must be connected to an external bypass capacitor of 600 nF - 2 μF with low ESR (max 50 mΩ).

Using a capacitor value on VCR33 pin, closer to upper limit as described in the Reference Manual (C = 2μF) brings significant reduction of code spread.

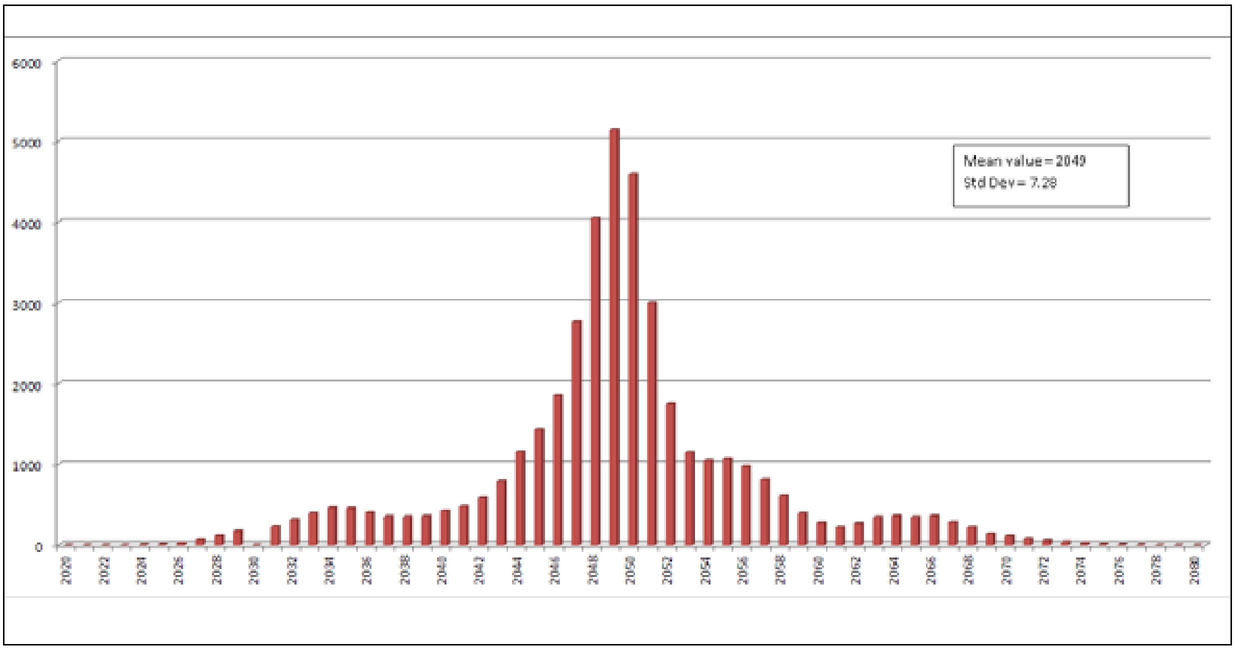
3 Determine noise on the system

To determine the noise on the system, it is required to take multiple readings on the selected ADC channel, where a constant voltage is applied, and analyzing the data.

Figure 3 shows an example set of results obtained by about 40,000 reads on the AIN1 channel fixed at 2.5V.

It is seen that a single read might lead to poor data: the span of results is 56 codes (from 2021 to 2077).

Figure 4. Distribution with fixed ADC input voltage



Important parameters to be calculated are mean and standard deviation; in particular standard deviation gives a figure of how much code changes around the mean value.

In order to take into account process and temperature variation, bench results have to be degraded to 40% process variation and 40% more for temperature, in case data has not been taken at lower temperature of interest (for example at -40°C).

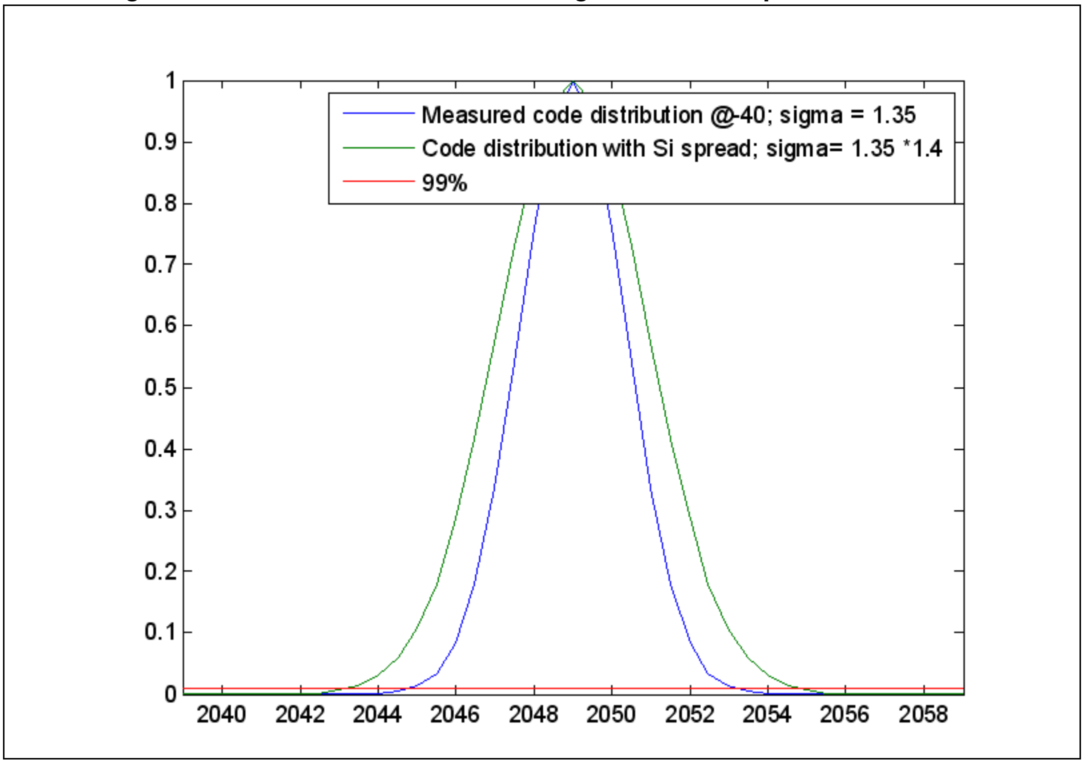
Example 1

Assuming to have performed measurement at -40°C, obtaining certain number of samples with stdv = 1.35 (blue line), it is important to add the contribution of process variation.

For this reason, new stdv is calculated as stdv *1.4 (green line).

Red line shown in *Figure 5* represents 99% probability to get samples inside Gaussian region; looking at intersection between red and green line, spread can be foreseen.

Figure 5. Code distribution after taking into account process variation



4 Averaging

Averaging is achieved using multiple reads, then calculating an average in software. There are two items to be decided: the number of samples and the average to use.

With this distribution, closer to a Gaussian, typical of persistent noise, as the one coming from Flash, it is seen that a mean average is a good choice.

Different noise level is found in different application board.

For this reason running an experiment to determine the level of noise on the target system generate data to allow an averaging scheme to be determined.

According to Nyquist theorem, a signal must be sampled at least twice as fast as the bandwidth of the signal to accurately reconstruct the waveform. Thus, the minimum required sampling frequency, in accordance to the Nyquist Theorem, is the Nyquist Frequency.

Equation 3

$$f_{nyquist} = 2 \cdot f_{signal}$$

where f_{signal} is the highest frequency of interest in the input signal. Sampling frequencies above $f_{nyquist}$ are called ‘oversampling’.

This sampling frequency, however, is just a theoretical absolute minimum sampling frequency. In practice the user usually wishes the highest possible sampling frequency, to give the best possible representation of the measured signal, in time domain. One could say that in most cases the input signal is already oversampled.

Adding *m* samples and dividing the result by *m* is usually called normal averaging.

Averaging data from an ADC measurement is equivalent to a low-pass filter and has the advantage of attenuating signal fluctuation or noise, and flatten out peaks in the input signal. The Moving Average method is very often used to do this. It means taking m readings, place them in a cyclic queue and average the most recent m. It gives a slight time delay, because each sample is a representation of the last m samples. This can be done with or without overlapping windows.

Figure 6. Moving averaging without overlapping window

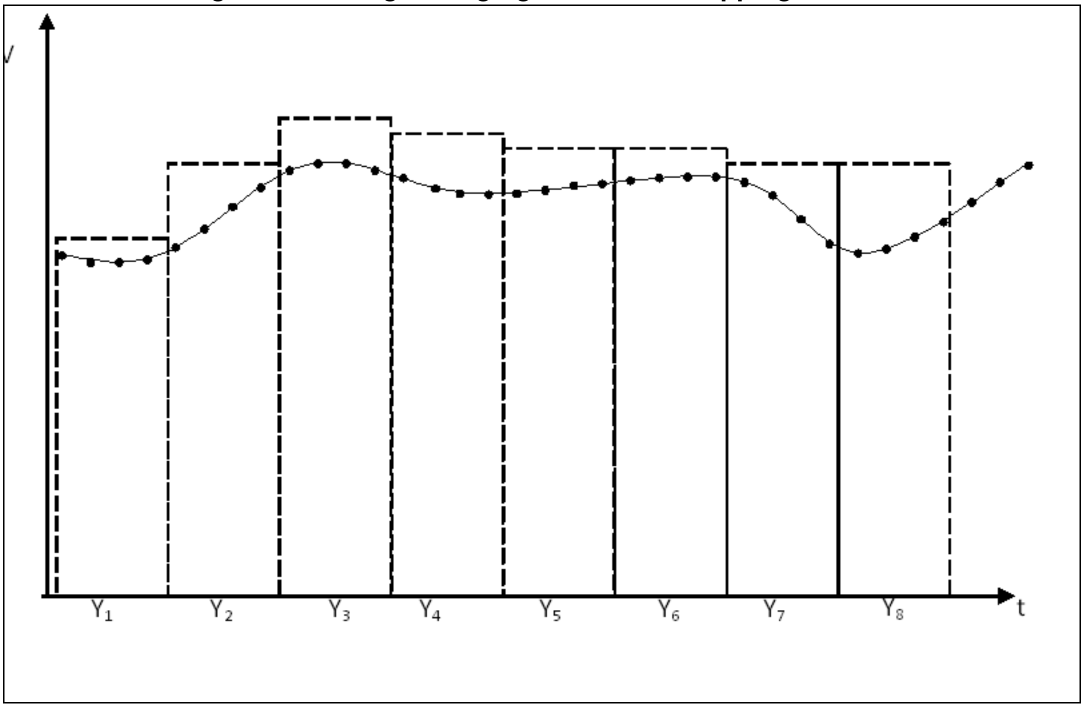


Figure 6 shows eight (y1-y8), independently Moving Average results without overlapping.

It is possible to implement moving average in recursive way. In *Equation 4* x[] is the input signal, y[ ] is the output signal, M is the number of points in the moving average (an odd number). In the *Equation 4* the first point to be calculated is the signal using a standard summation.

Equation 4

$$y[i] = y[i-1] + x[i+p] - x[i-q] \quad where \;\; p = \frac{M-1}{2} \quad and \quad q = p+1$$

This method increases the Signal to Noise Ratio. Doubling the sample number lowers the in-band noise by 3dB, and increases the resolution of the measurement by 0.5 bits.

4.1 Oversampling

In case the application cannot sustain the drawback of normal sampling (signal delaying and attenuation), oversampling is used.

This technique requires a higher amount of samples. These extra samples can be achieved by oversampling the signal. The oversampling ratio is defined as

Equation 5

$$\beta = \frac{f_{oversampling}}{f_{nyquist}}$$

For each additional bit of resolution, n, the signal must be oversampled four times. The frequency required to sample the input signal with, is given by *Equation 6*.

Equation 6

$$f_{oversampling} = 4^n \cdot f_{nyquist}$$

To get the best possible representation of an analog input signal, it is necessary to oversample the signal, because a larger amount of samples give a better representation of the input signal, when averaged.

If multiple samples are taken of the same quantity with uncorrelated noise added to each sample, then averaging N samples reduces the noise power by a factor of 1/N.[1] If, for example, we oversample by a factor of 4, the signal-to-noise ratio in terms of power improves by factor of 4 which corresponds to factor of 2 improvements in terms of voltage.

Oversampling and averaging improve the SNR and measurement resolution at the cost of increased CPU utilization and reduced throughput.

5 Experimental results

Test setup:

Xtal = 8 MHz,
PLL = 80 MHz
ADCclock = 10 MHz
Sample time 64 clocks
Vin (AN1) = 2.5 V
Temperature: ambient
2 µF VRC33

ADC calibration using Vref 25 % and Vref75 % is always performed during ADC initialization. ADC data are captured without averaging. Each test consists of 40960 codes.

Device used for all tests is SPC53M64 revision 2.1, identified with JTAG_ID = 0x2AE01041.

5.1 Generic board

Table 1. 2 uF on VRC33 - Vin= 2,5 V

2uF AVG1 - STEP=40960 - Vin=2.5 V **DIFFERENCE BETWEEN EXPECTED AND OBTAINED VALUE**	
Test 1-2 uF	23.43
Test 2-2 uF	26.46
Test 3-2 uF	25.44
Test 4-2 uF	25.45
Test 5-2 uF	24.44
Mean -2 uF	25.045

Shown below is distribution of Test 2 -2 uF codes. Histogram approximates a Gaussian probability distribution function, thus the noise approximates a white noise and the measurement can benefit from averaging and oversampling techniques.

Figure 7. Typical code distribution with fixed ADC input voltage (at 2.5 V) and VCR33 capacitor = 2 uF

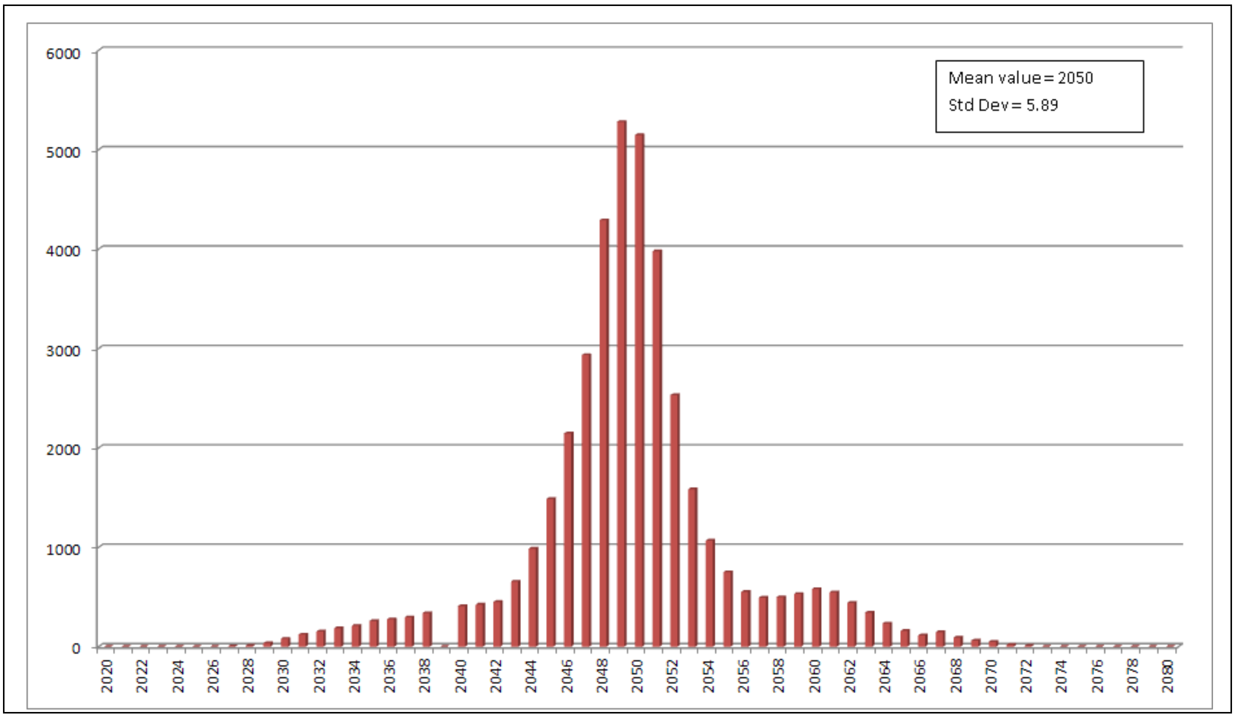
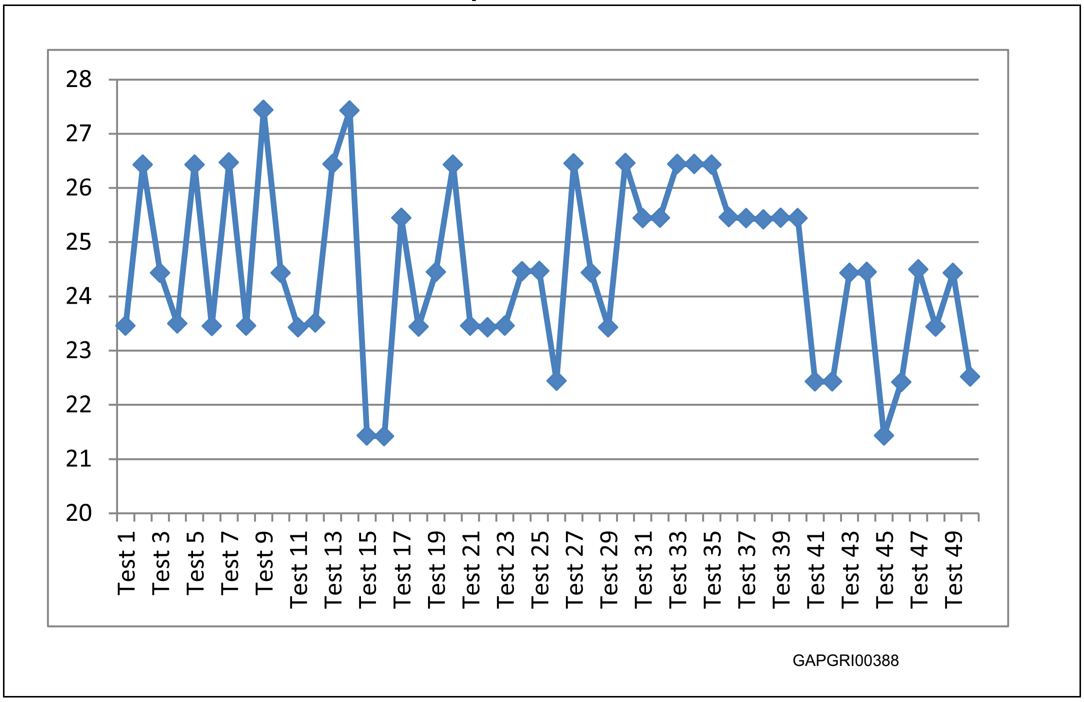


Figure 8. Max code spread, fixed ADC input voltage (at 2.5 V) and VCR33 capacitor = 2 uF



Using a generic board with soldered microcontroller in noiseless environment, results in difference between samples and expected value without averaging is:

- Max difference between Expected and Obtained value without averaging is
  - 27.5 LSB (typical)
  - 31 LSB (max)[a]

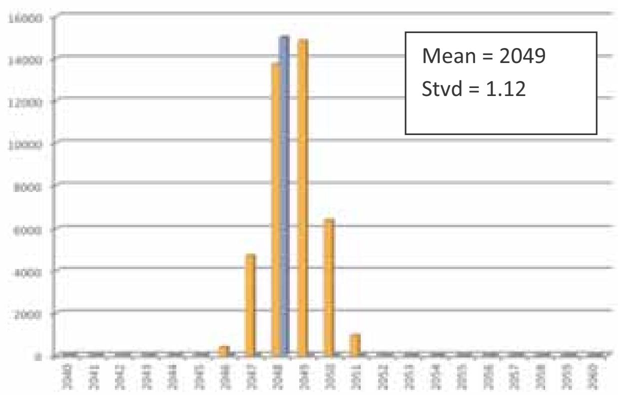
This can be guaranteed for all ADC channels; AIN38 and AIN39 show an offset of about 2 LSB of mean value.

5.2 Board designed with good layout

In case of well designed board, that takes into account all layout recommendations listed in *Section 1: Layout recommendations*, minimizing wire inductances (using both V_{ss} and V_{dd} ground planes) and adding capacitors on ADC inputs, better results are obtained, showing that the greater part of noise power figure showed in the previous chapter was coming from external coupling rather than microcontroller internal one.

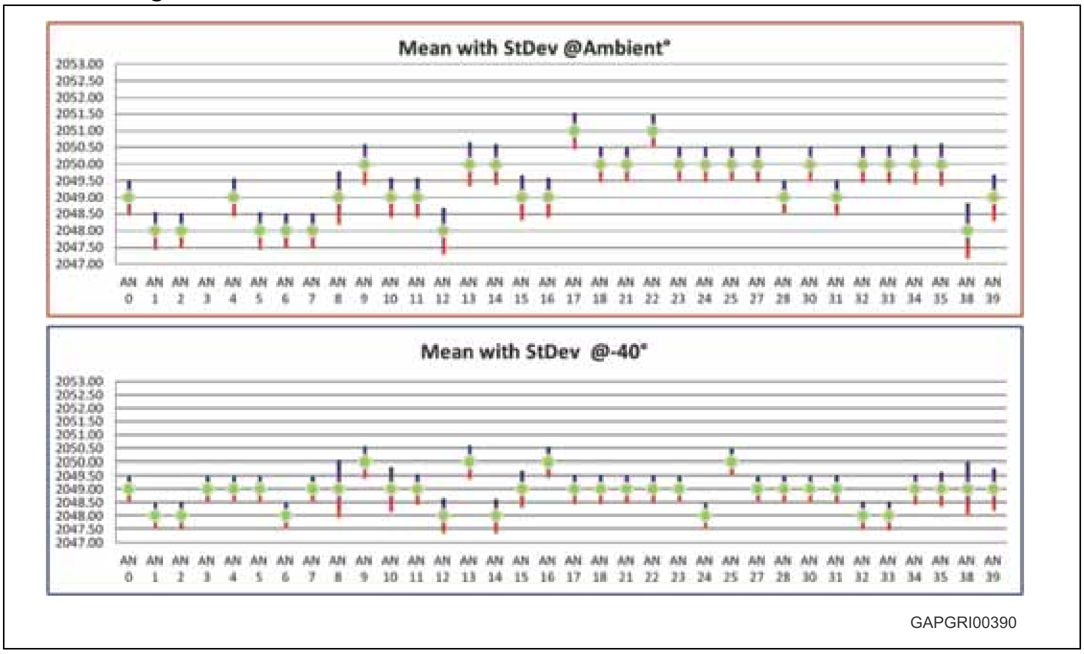
Figure 9 shows Ch1 distribution (yellow) and mean value (blue); in this case, there is difference between Expected and Obtained value of 4 LSB, thus a spread of 8 counts.

Figure 9. Code distribution with fixed ADC input voltage (at 2.5 V)



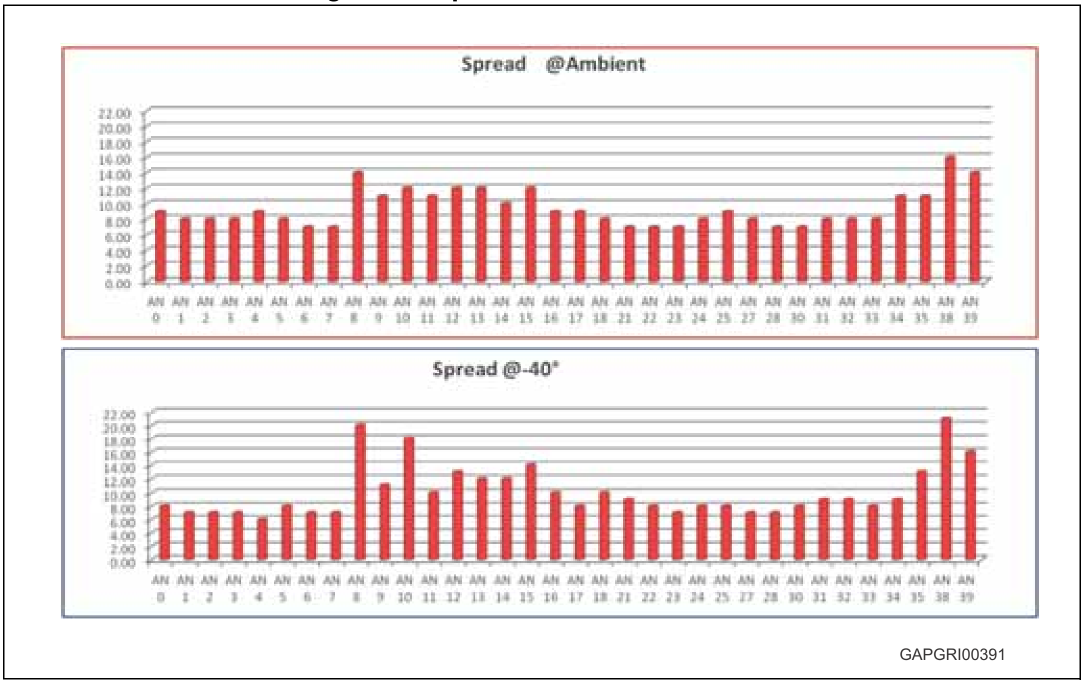
a. This parameter is achieved by characterization on a small sample size, taken across process variations.

Figure 10. Mean value and standard deviation of all ADC channels



All channels are evaluated and channels performances (mean and standard deviation, but also spread) with such board are shown in *Figure 11* and *12*.

Figure 11. Spread of all ADC channels



All the channels have a standard deviation in the range of 1-1.2LSB (it means a code spread of less than 14 LSB), except AN38 and AN39 (AN8 and AN9 sharing AN38 and 39 pins) that shows a standard deviation spread of 2LSB, thus a code spread of about 20 counts.

Results shown in *Figure 11* were achieved using LQFP144 pin package; anyway similar results are expected with LQFP176 pin, as they have the same range of pin impedance.

5.3 Averaging examples

Recursive average (see *Section 4: Averaging*) has been applied to data related to *Section 5* that shows improvement obtained averaging 2, 4, 6 and 8 samples.

For most of the channels already after only 2 samples averaging, the standard deviation goes well below 1, with related spread in the range of 8-9 counts.

Figure 12. Mean value and standard deviation of all ADC channels after averaging

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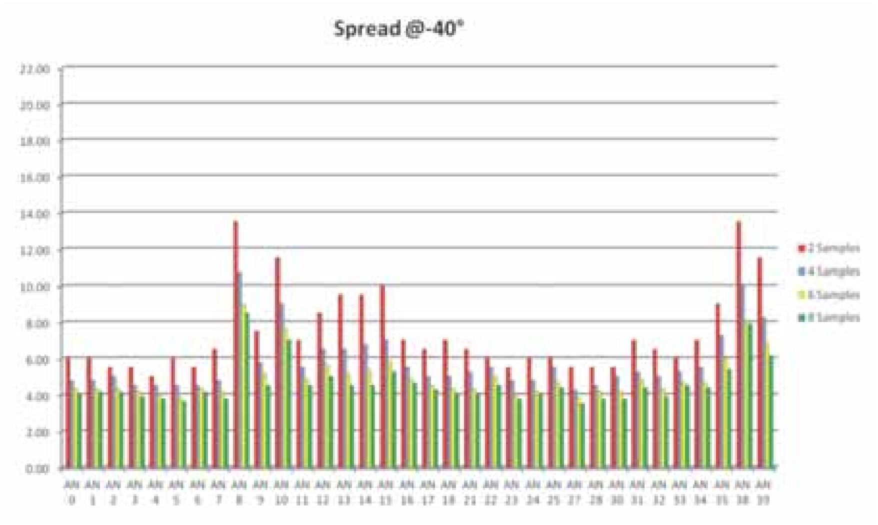
Figure 13. Spread of all ADC channels after averaging



6 Conclusions

Different noise sources can influence microcontroller ADC acquisition, both internal to the micro and external. Some layout suggestions have been described here in order to reduce external coupling mechanisms. In order to determine noise level of application board, a method has been shown. Based on number obtained, with the aim to further decrease noise level, averaging (with or without oversampling) can be applied.

Appendix A Further information

Table 2. Measurement data related to *Section 5.2* (part 1)

Value @Ambient					
	StDev	Spread	Mean	Positive	Negative
AN 0	1.06	9	2049	2053	2044
AN 1	1.12	8	2049	2052	2044
AN 2	1.05	8	2049	2052	2044
AN 3	1.05	8	2049	2054	2046
AN 4	1.13	9	2049	2053	2044
AN 5	1.13	8	2049	2050	2042
AN 6	1.03	7	2049	2052	2045
AN 7	1.06	7	2049	2052	2045
AN 8	1.59	14	2049	2055	2041
AN 9	1.20	11	2049	2054	2043
AN 10	1.40	12	2049	2054	2042
AN 11	1.17	11	2049	2055	2044
AN 12	1.39	12	2049	2055	2043
AN 13	1.30	12	2049	2055	2043
AN 14	1.22	10	2049	2056	2046
AN 15	1.35	12	2049	2057	2045
AN 16	1.18	9	2049	2054	2045
AN 17	1.07	9	2049	2056	2047
AN 18	1.05	8	2049	2053	2045
AN 21	1.01	7	2049	2054	2047
AN 22	0.98	7	2049	2055	2048
AN 23	1.02	7	2049	2053	2046
AN 24	1.04	8	2049	2054	2046
AN 25	0.97	9	2049	2055	2046
AN 27	1.07	8	2049	2054	2046
AN 28	0.98	7	2049	2052	2045
AN 30	1.03	7	2049	2054	2047
AN 31	1.05	8	2049	2053	2045
AN 32	1.09	8	2049	2054	2046
AN 33	1.12	8	2049	2055	2047
AN 34	1.17	11	2049	2057	2046

Table 2. Measurement data related to *Section 5.2* (part 1)

Value @Ambient					
	StDev	**Spread**	**Mean**	**Positive**	**Negative**
AN 35	1.25	11	2049	2056	2045
AN 38	1.64	16	2049	2055	2039
AN 39	1.40	14	2049	2055	2041

Table 3. Measurement data related to *Section 5.2* (part 2)

Value @-40°					
	StDev	**Spread**	**Mean**	**Positive**	**Negative**
AN 0	0.98	8.00	2049.00	2053.00	2045.00
AN 1	0.99	7.00	2049.00	2052.00	2045.00
AN 2	1.01	7.00	2049.00	2052.00	2045.00
AN 3	0.97	7.00	2049.00	2052.00	2045.00
AN 4	0.95	6.00	2049.00	2053.00	2047.00
AN 5	0.97	8.00	2049.00	2052.00	2044.00
AN 6	0.95	7.00	2049.00	2052.00	2045.00
AN 7	0.97	7.00	2049.00	2053.00	2046.00
AN 8	2.13	20.00	2049.00	2058.00	2038.00
AN 9	1.17	11.00	2049.00	2055.00	2044.00
AN 10	1.70	18.00	2049.00	2057.00	2039.00
AN 11	1.13	10.00	2049.00	2054.00	2044.00
AN 12	1.30	13.00	2049.00	2056.00	2043.00
AN 13	1.22	12.00	2049.00	2056.00	2044.00
AN 14	1.27	12.00	2049.00	2055.00	2043.00
AN 15	1.37	14.00	2049.00	2055.00	2041.00
AN 16	1.10	10.00	2049.00	2054.00	2044.00
AN 17	1.09	8.00	2049.00	2053.00	2045.00
AN 18	1.06	10.00	2049.00	2054.00	2044.00
AN 21	1.02	9.00	2049.00	2054.00	2045.00
AN 22	1.01	8.00	2049.00	2053.00	2045.00
AN 23	0.95	7.00	2049.00	2052.00	2045.00
AN 24	0.96	8.00	2049.00	2053.00	2045.00
AN 25	0.98	8.00	2049.00	2053.00	2045.00
AN 27	0.96	7.00	2049.00	2052.00	2045.00
AN 28	0.97	7.00	2049.00	2052.00	2045.00

Table 3. Measurement data related to *Section 5.2* (part 2)

Value @-40°					
	StDev	Spread	Mean	Positive	Negative
AN 30	1.00	8.00	2049.00	2054.00	2046.00
AN 31	1.02	9.00	2049.00	2053.00	2044.00
AN 32	1.05	9.00	2049.00	2053.00	2044.00
AN 33	1.09	8.00	2049.00	2053.00	2045.00
AN 34	1.14	9.00	2049.00	2054.00	2045.00
AN 35	1.30	13.00	2049.00	2056.00	2043.00
AN 38	1.99	21.00	2049.00	2057.00	2036.00
AN 39	1.59	16.00	2049.00	2056.00	2040.00

Figure 14. Average results related to *Section 5.3*

StDev	N. Sample averaging			
	2	4	6	8
AN 0	0.98	0.83	0.74	0.70
AN 1	0.84	0.76	0.73	0.71
AN 2	0.86	0.78	0.75	0.73
AN 3	0.83	0.75	0.72	0.70
AN 4	0.81	0.73	0.70	0.68
AN 5	0.83	0.74	0.71	0.70
AN 6	0.81	0.73	0.70	0.68
AN 7	0.84	0.76	0.73	0.71
AN 8	1.55	1.22	1.08	1.02
AN 9	0.93	0.79	0.73	0.70
AN 10	1.26	1.00	0.89	0.84
AN 11	0.92	0.80	0.75	0.73
AN 12	1.02	0.83	0.76	0.73
AN 13	0.96	0.78	0.71	0.68
AN 14	1.00	0.83	0.77	0.73
AN 15	1.06	0.87	0.80	0.76
AN 16	0.91	0.80	0.76	0.74
AN 17	0.91	0.81	0.77	0.75
AN 18	0.87	0.77	0.73	0.71
AN 21	0.86	0.77	0.74	0.72
AN 22	0.87	0.80	0.77	0.75
AN 23	0.81	0.72	0.69	0.68
AN 24	0.81	0.73	0.70	0.68
AN 25	0.83	0.75	0.72	0.70
AN 27	0.80	0.72	0.69	0.67
AN 28	0.81	0.73	0.69	0.68
AN 30	0.84	0.75	0.72	0.70
AN 31	0.85	0.76	0.72	0.70
AN 32	0.87	0.76	0.73	0.71
AN 33	0.90	0.80	0.76	0.74
AN 34	0.92	0.80	0.76	0.74
AN 35	1.00	0.84	0.78	0.75

Spread	N. Sample averaging				
	1	2	4	6	8
AN 0	8.00	6.00	4.75	4.33	4.00
AN 1	7.00	6.00	4.75	4.33	4.13
AN 2	7.00	5.50	5.00	4.33	4.13
AN 3	7.00	5.50	4.50	4.17	3.88
AN 4	6.00	5.00	4.50	4.00	3.75
AN 5	8.00	6.00	4.50	3.83	3.63
AN 6	7.00	5.50	4.50	4.33	4.13
AN 7	7.00	6.50	4.75	4.17	3.75
AN 8	20.00	13.50	10.75	9.00	8.50
AN 9	11.00	7.50	5.75	5.17	4.50
AN 10	18.00	11.50	9.00	7.67	7.00
AN 11	10.00	7.00	5.50	4.83	4.50
AN 12	13.00	8.50	6.50	5.67	5.00
AN 13	12.00	9.50	6.50	5.17	4.50
AN 14	12.00	9.50	6.75	5.33	4.50
AN 15	14.00	10.00	7.00	5.83	5.25
AN 16	10.00	7.00	5.50	4.83	4.63
AN 17	8.00	6.50	5.00	4.50	4.25
AN 18	10.00	7.00	5.00	4.33	4.00
AN 21	9.00	6.50	5.25	4.33	4.00
AN 22	8.00	6.00	5.50	5.00	4.50
AN 23	7.00	5.50	4.75	4.00	3.75
AN 24	8.00	6.00	4.75	4.17	4.00
AN 25	8.00	6.00	5.50	4.67	4.38
AN 27	7.00	5.50	4.25	3.83	3.50
AN 28	7.00	5.50	4.50	4.17	3.75
AN 30	8.00	5.50	5.00	4.17	3.75
AN 31	9.00	7.00	5.25	4.83	4.38
AN 32	9.00	6.50	5.00	4.33	3.88
AN 33	8.00	6.00	5.25	4.67	4.50
AN 34	9.00	7.00	5.50	4.67	4.38
AN 35	13.00	9.00	7.25	6.00	5.38

Revision history

Table 4. Revision history

Date	Revision	Changes
01-Dec-2015	1	Initial release.