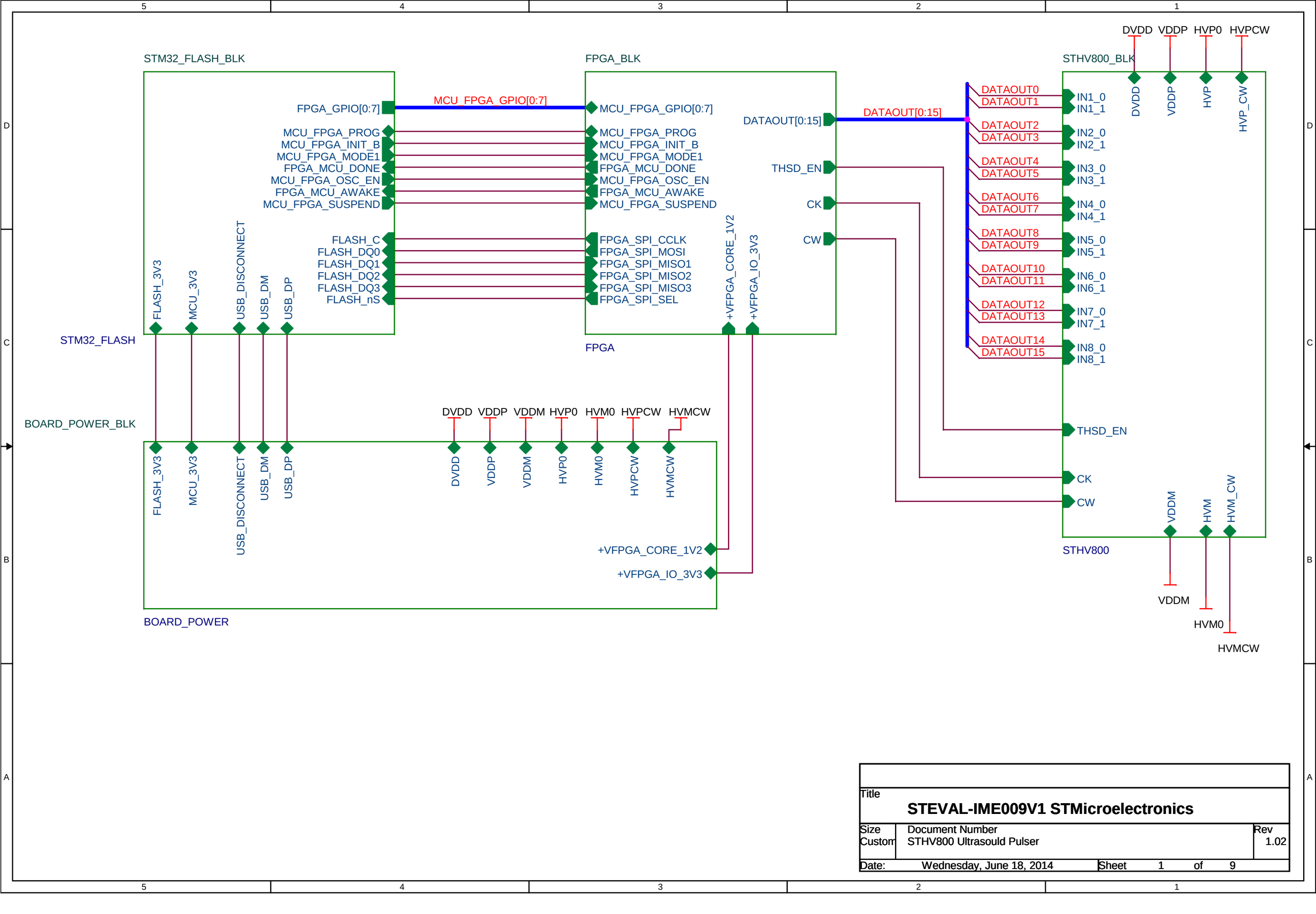

Title	**STEVAL-IME009V1 STMicroelectronics**	
Size: Custom	Document Number: STHV800 Ultrasould Pulser	Rev: 1.02
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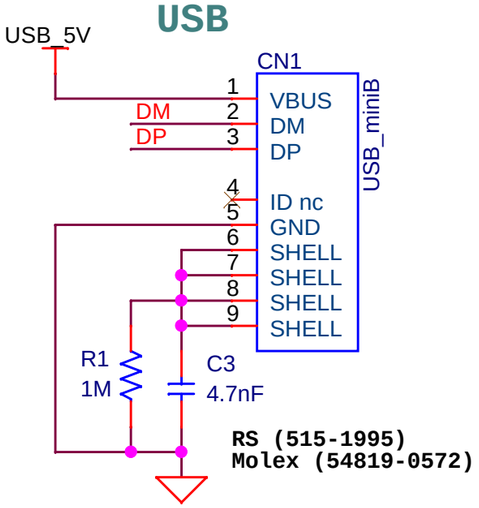
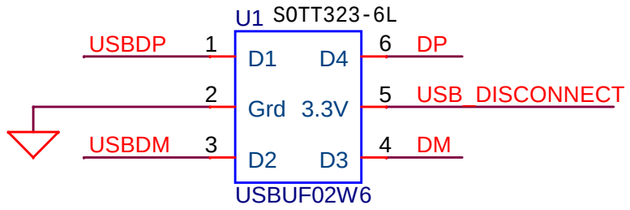
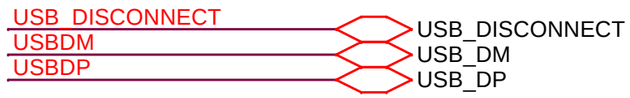
USB



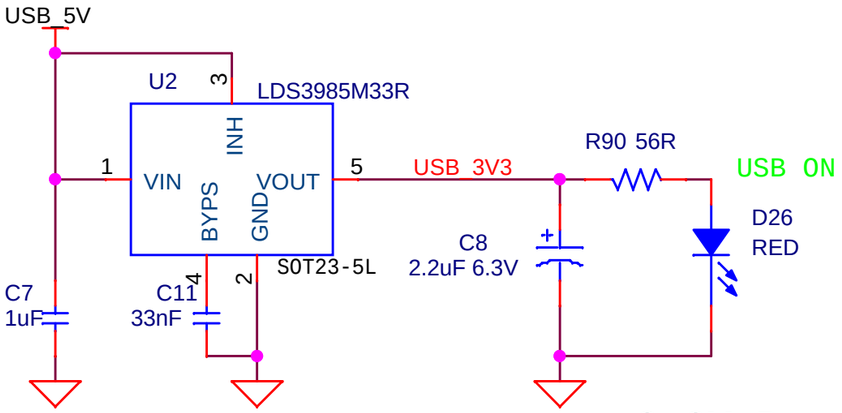
RS (515-1995)
Molex (54819-0572)





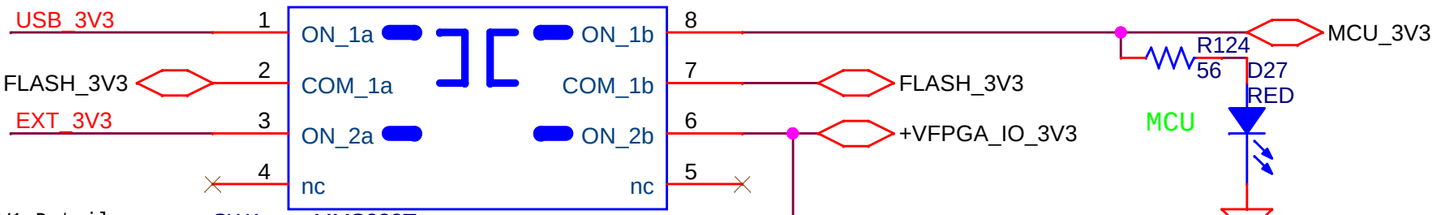
C7 Details:
Digikey (445-4998-2-ND) - TDK (C1005X5R0J105K)
Package 0402

C8 Details:
DigiKey (478-2552-2-ND) - AVX (TACL225M006XTA)
Package 0603

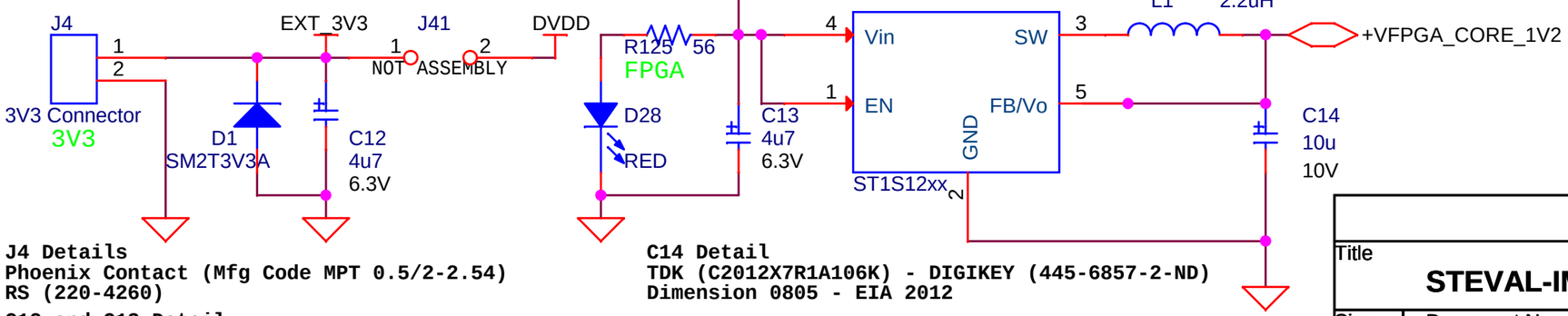


Kingbright KP2012SURC
RS: 466-3829
Farnell: 8529930
LED 0805

3.3V Power Management



SW1 Details:
RS 711-8329
KNITTER-SWITCH (MMS228T)



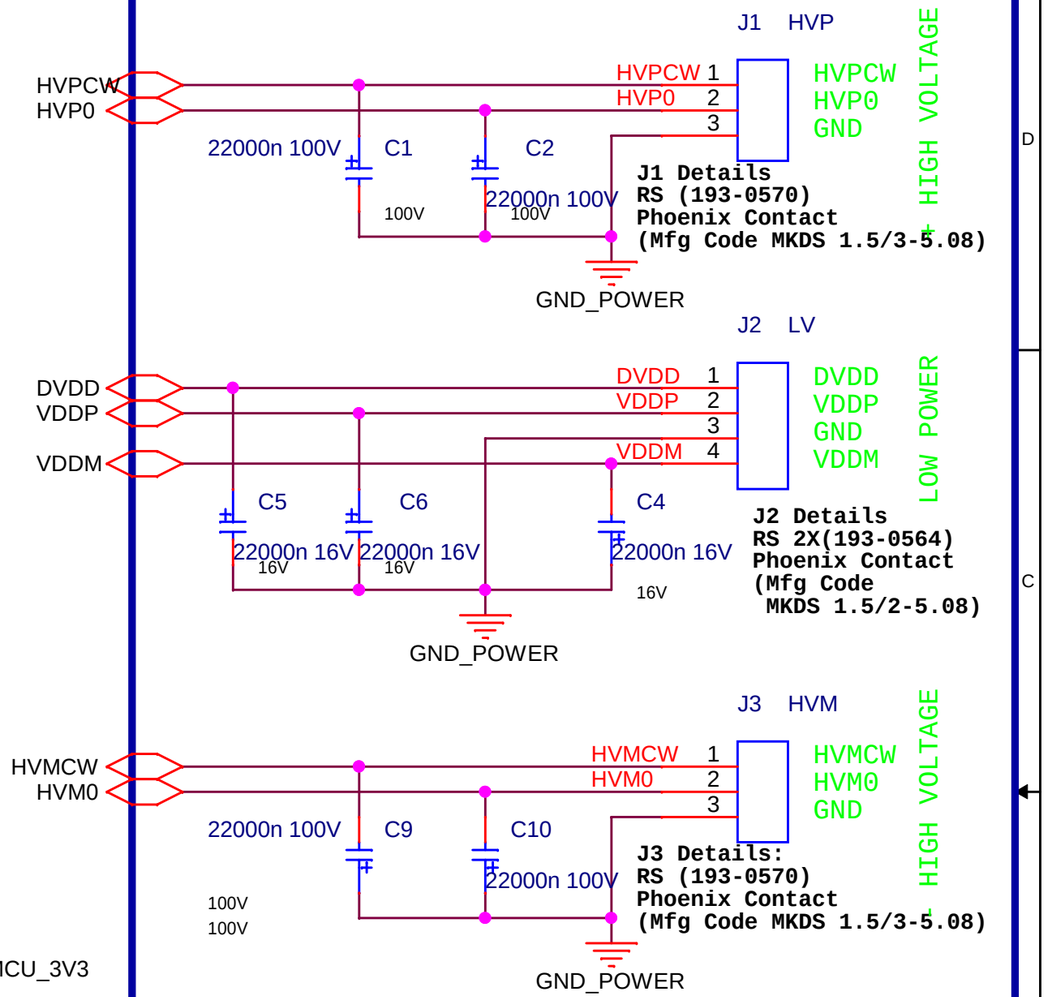
J4 Details
Phoenix Contact (Mfg Code MPT 0.5/2-2.54)
RS (220-4260)

C12 and C13 Detail
TDK (C1608X5R0J475K) - Digikey (445-5178-2-ND)
Dimension 0603 - EIA 1608

C14 Detail
TDK (C2012X7R1A106K) - DIGIKEY (445-6857-2-ND)
Dimension 0805 - EIA 2012

L1 Detail
TDK (VLF4012AT-2R2M1R5) - RS (614-3147)

STHV800 Power Management



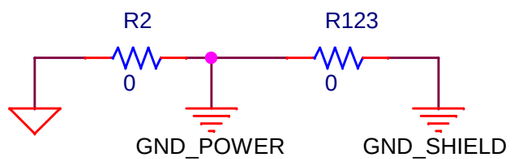
J1 Details
RS (193-0570)
Phoenix Contact
(Mfg Code MKDS 1.5/3-5.08)

J2 Details
RS 2X(193-0564)
Phoenix Contact
(Mfg Code
MKDS 1.5/2-5.08)

J3 Details:
RS (193-0570)
Phoenix Contact
(Mfg Code MKDS 1.5/3-5.08)

C1, C2, C9, C10 Details:
Digikey (445-5217-2-ND) - TDK (CKG57NX7S2A226M)
Package 6.5mm x 5.5 mm

C4, C5, C6 Details:
Digikey (445-1436-2-ND) - TDK (C3225X5R1C226M)
Package 1210 - EIA 3225



Title
STEVAL-IME009V1 STMicroelectronics

Size	Document Number	Rev
A	STHV800 Demonstration Board	1.02
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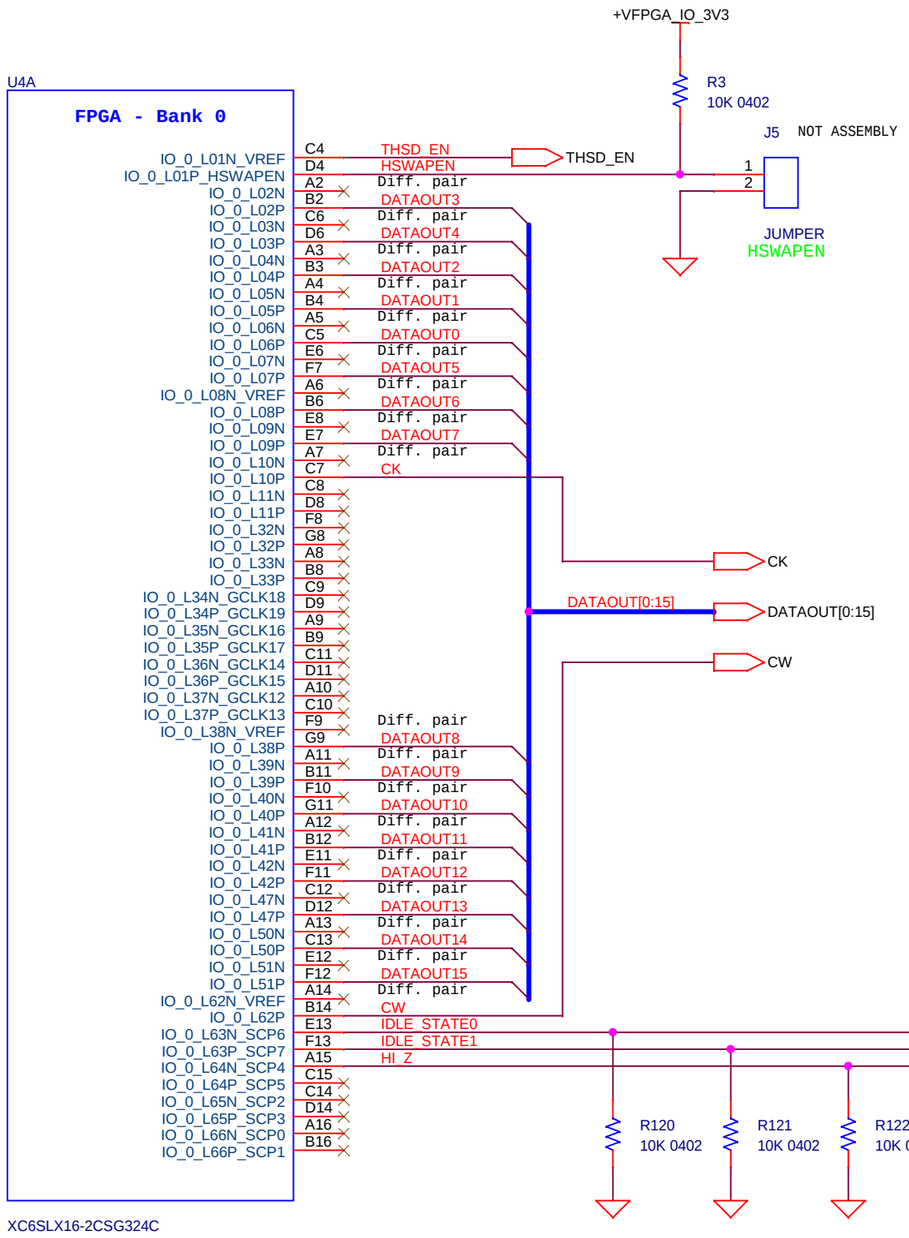
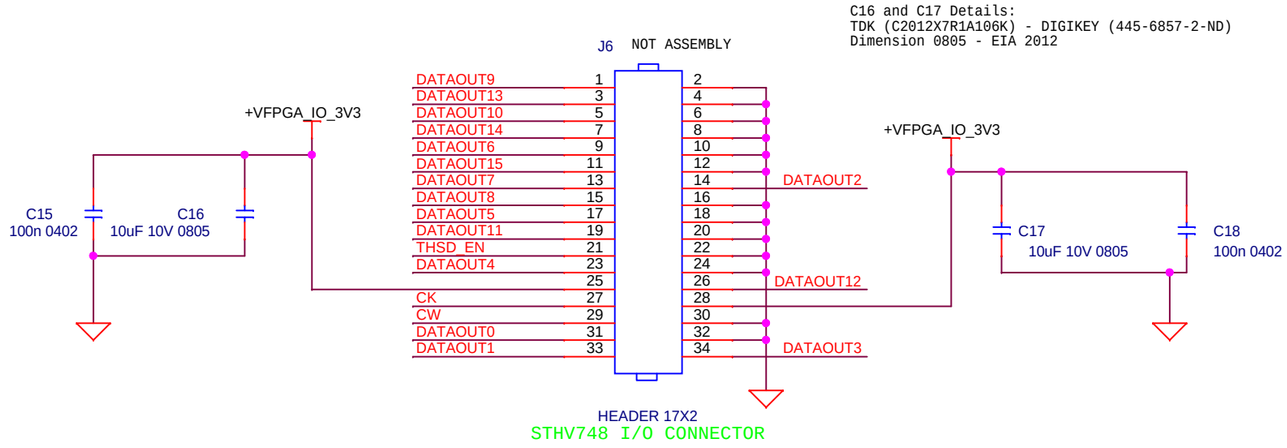


Jumper J5 is used to control I/O pullups during FPGA configuration.

Open (default) to float I/O output during FPGA configuration.
Set jumper 1:2 to enable I/O pullups during FPGA configuration.



Jumpers J35, J36 and J37 are used to set dataout output state.

Configure J35 and J36 to setup outputs idle state as follows:
00 - (J35 and J36 open) --> High-Z (default)
01 - (J35 closed and J36 open) --> Clamp/HVR_SW
11 - (J35 and J36 closed) --> High-Z
10 - (J35 open and J36 closed) --> Clamp

Open J37 (default) to connect FPGA outputs
Close J37 to disconnect outputs (High-Z)

Title	**STEVAL-IME0009V1 STMicroelectronics**	
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66MHZ EXTERNAL OSCILLATOR

When using backup oscillator X1, R126 have to be unmounted and R6 must be placed.

+VFPGA_IO_3V3

R126 10k

C19 100nF

C20 10nF

BACKUP OF U5

MCU_FPGA_OSC_EN

X1: OE ST, VCC, GND, OUT

U5: VCC, VCC, n/c, n/c, PDN, GND, GND, OUT

MCU_FPGA_OSC_EN

R6 10K NM

FPGA_CLK_66MHZ

R7 33R2

Place R7 (1%) close to the clock source DS1088LU-66 device

DS1088LU-66

66MHZ OSC

PUSHBUTTONS

+VFPGA_IO_3V3

R4 10K 0402

SEL_PROG_PB — SW PUSHBUTTON-DPST — C21 100nF — SW2 — PROGRAM

+VFPGA_IO_3V3

R5 10K 0402

START_PB — SW PUSHBUTTON-DPST — C22 100nF — SW3 — START

+VFPGA_IO_3V3

R8 10K 0402

STOP_PB — SW PUSHBUTTON-DPST — C23 100nF — SW4 — STOP

+VFPGA_IO_3V3

SW PUSHBUTTON-DPST — SW5 — FPGA RESET

FPGA_RESET — C24 100nF — R9 10K 0402

SW2, SW3, SW4, Details RS (378-6527)

PERIPHERRAL MODULE (PMOD)

+VFPGA_IO_3V3

C25 100nF

C26 10uF 10V 0805

C27 10uF 10V 0805

C28 100nF

PMOD1

J8 NOT ASSEMBLY

SX

FPGA_PMOD1_P1, FPGA_PMOD1_P3, FPGA_PMOD1_P7, FPGA_PMOD1_P9 — FPGA_PMOD1_P2, FPGA_PMOD1_P4, FPGA_PMOD1_P8, FPGA_PMOD1_P10

HEADER 6X2

C26, C27, C30 and C31 Detail
TDK (C2012X7R1A106K) - DIGIKEY (445-6857-2-ND)
Dimension 0805 - EIA 2012

+VFPGA_IO_3V3

C29 100nF

C30 10uF 10V 0805

C31 10uF 10V 0805

C32 100nF

PMOD2

J9 NOT ASSEMBLY

DX

FPGA_PMOD2_P1, FPGA_PMOD2_P3, FPGA_PMOD2_P7, FPGA_PMOD2_P9 — FPGA_PMOD2_P2, FPGA_PMOD2_P4, FPGA_PMOD2_P8, FPGA_PMOD2_P10

HEADER 6X2

CTRL LED

CTRL_LED0 — R10 56R 0402 — D2 GREEN — Near START button

CTRL_LED1 — R11 56R 0402 — D3 GREEN — Near STOP button

CTRL_LED2 — R12 56R 0402 — D4 GREEN — IDLE state signal — IDLE

CTRL_LED3 — R13 56R 0402 — D5 RED — ERROR signal — ERROR

RED LED
Kingbright KP2012SURC
RS: 466-3829
Farnell: 8529930
LED 0805

GREEN LED
Kingbright KP2012SURC
RS: 466-3778
Farnell: 8529906
LED 0805

U4B

FPGA - Bank 1

IO_1_L01N_A24_VREF	F16	FPGA_PMOD1_P2
IO_1_L01P_A25	F15	FPGA_PMOD1_P1
IO_1_L29N_A22_M1A14	C18	FPGA_PMOD1_P4
IO_1_L29P_A23_M1A13	C17	FPGA_PMOD1_P3
IO_1_L30N_A20_M1A11	G14	FPGA_PMOD1_P8
IO_1_L30P_A21_M1RESET	F14	FPGA_PMOD1_P7
IO_1_L31N_A18_M1A12	D18	FPGA_PMOD1_P10
IO_1_L31P_A19_M1CKE	D17	FPGA_PMOD1_P9
IO_1_L32N_A16_M1A9	G13	FPGA_PMOD2_P2
IO_1_L32P_A17_M1A8	H12	FPGA_PMOD2_P1
IO_1_L33N_A14_M1A4	E18	FPGA_PMOD2_P4
IO_1_L33P_A15_M1A10	E16	FPGA_PMOD2_P3
IO_1_L34N_A12_M1BA2	K13	FPGA_PMOD2_P8
IO_1_L34P_A13_M1WE	K12	FPGA_PMOD2_P7
IO_1_L35N_A10_M1A2	F18	FPGA_PMOD2_P10
IO_1_L35P_A11_M1A7	F17	FPGA_PMOD2_P9
IO_1_L36N_A8_M1BA1	H14	
IO_1_L36P_A9_M1BA0	H13	
IO_1_L37N_A6_M1A1	H16	
IO_1_L37P_A7_M1A0	H15	
IO_1_L38N_A4_M1CLKN	G18	
IO_1_L38P_A5_M1CLK	G16	
IO_1_L39N_M1ODT	K14	CTRL_LED1
IO_1_L39P_M1A3	J13	CTRL_LED0
IO_1_L40N_GCLK10_M1A6	L13	SEL_PROG_PB
IO_1_L40P_GCLK11_M1A5	L12	FPGA_CLK_66MHZ
IO_1_L41N_GCLK8_M1CASN	K16	START_PB
IO_1_L41P_GCLK9_IRDY1_M1RASN	K15	
IO_1_L42N_GCLK6_TRDY1_M1LDM	L16	STOP_PB
IO_1_L42P_GCLK7_M1UDM	L15	
IO_1_L43N_GCLK4_M1DQ5	H18	FPGA_RESET
IO_1_L43P_GCLK5_M1DQ4	H17	
IO_1_L44N_A2_M1DQ7	J18	FPGA_USER_IO_0
IO_1_L44P_A3_M1DQ6	J16	FPGA_USER_IO_1
IO_1_L45N_A0_M1LDQSN	K18	FPGA_USER_IO_2
IO_1_L45P_A1_M1LDQS	K17	FPGA_USER_IO_3
IO_1_L46N_FOE_B_M1DQ3	L18	FPGA_USER_IO_4
IO_1_L46P_FCS_B_M1DQ2	L17	FPGA_USER_IO_5
IO_1_L47N_LDC_M1DQ1	M18	FPGA_USER_IO_6
IO_1_L47P_FWE_B_M1DQ0	M16	FPGA_USER_IO_7
IO_1_L48N_M1DQ9	N18	FPGA_USER_IO_8
IO_1_L48P_HDC_M1DQ8	N17	FPGA_USER_IO_9
IO_1_L49N_M1DQ11	P18	FPGA_USER_IO_10
IO_1_L49P_M1DQ10	P17	FPGA_USER_IO_11
IO_1_L50N_M1UDQSN	N16	FPGA_USER_IO_12
IO_1_L50P_M1UDQS	N15	FPGA_USER_IO_13
IO_1_L51N_M1DQ13	T18	FPGA_USER_IO_14
IO_1_L51P_M1DQ12	T17	FPGA_USER_IO_15
IO_1_L52N_M1DQ15	U18	CTRL_LED3
IO_1_L52P_M1DQ14	U17	CTRL_LED2
IO_1_L53N_VREF	N14	
IO_1_L53P	M14	
IO_1_L61N	M13	
IO_1_L61P	L14	
IO_1_L74N_DOUT_BUSY	P16	FPGA_DOUT_BUSY
IO_1_L74P_AWAKE	P15	FPGA_AWAKE

XC6SLX16-2CSG324C

FPGA USER I/O

J7 NOT ASSEMBLY

HEADER 16X2

TP1 TEST POINT

FPGA_MCU_AWAKE

Two right-angle, 12-pin (2 x 6 female) Peripheral Module (PMOD) headers (J8, J9) are interfaced to the FPGA, with each header providing 3.3 V power, ground, and eight I/O's. These headers may be utilized as general-purpose I/Os or may be used to interface to PMODs. J6 and J8 are placed in close proximity (0'9" -centers) on the PCB in order to support dual PMODs.

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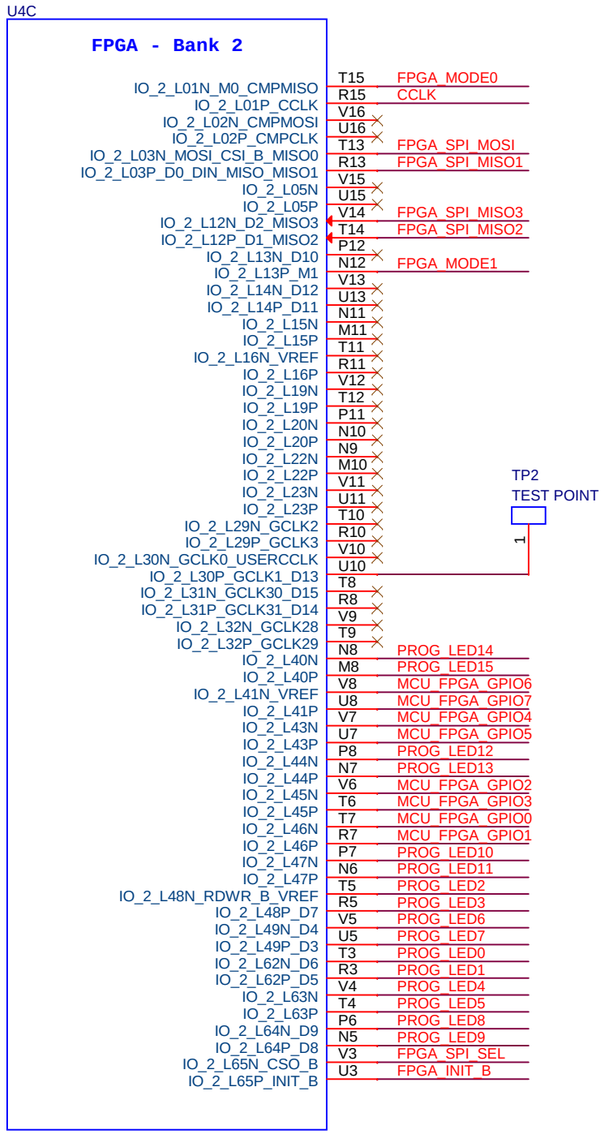
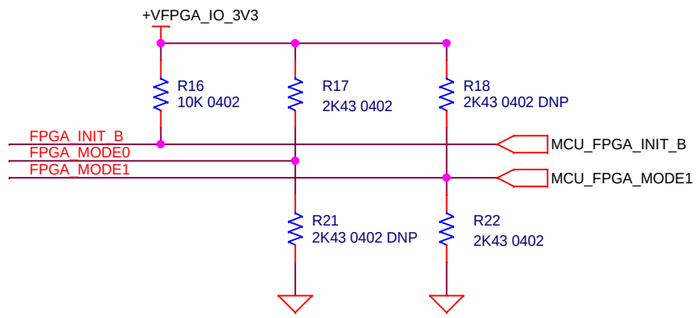


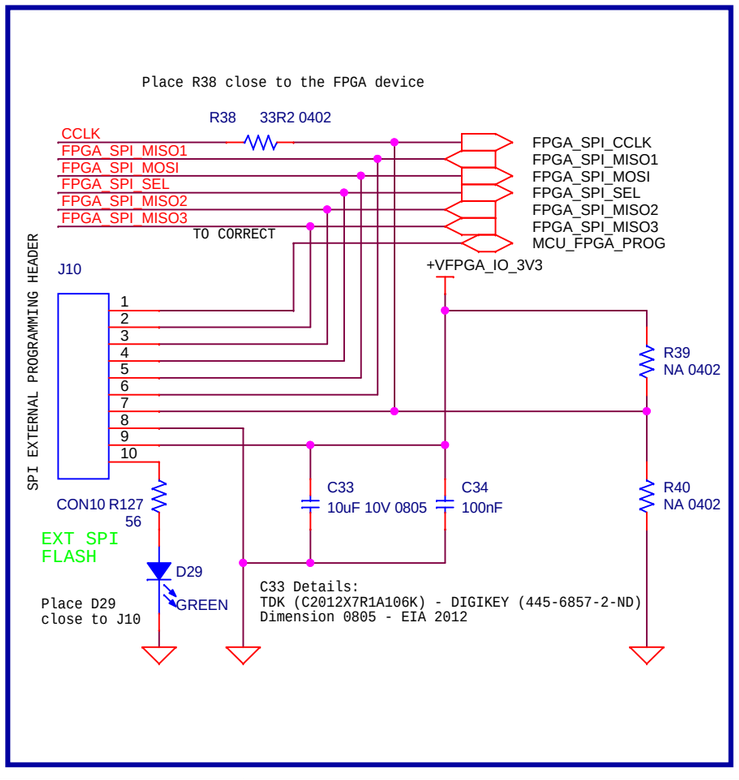
FPGA CONFIGURATION



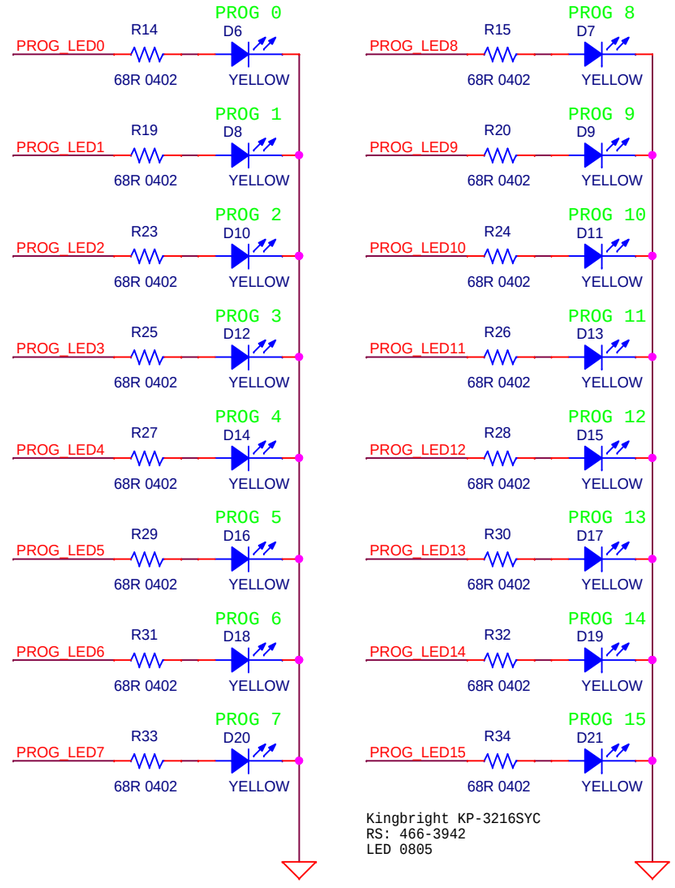
Configuration mode selection:
FPGA_MODE0 = Parallel (Low) or Serial (High)
FPGA_MODE1 = Master (Low) or Slave (High)

When FPGA_INIT_B (bidirectional open-drain) is Low the configuration memory is being cleared.
When held Low, the start of configuration is delayed.
During configuration, a Low on this output indicates that a configuration data error has occurred.

SPI FLASH CTRL SIGNALS



PROGRAM SELECTOR LEDS



Title	**STEVAL-IME009V1 STMicroelectronics**	
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U4D

FPGA - Bank 3

IO_3_L01N_VREF	N3
IO_3_L01P	N4
IO_3_L02N	P3
IO_3_L02P	P4
IO_3_L31N_VREF	M5
IO_3_L31P	L6
IO_3_L32N_M3DQ15	U1
IO_3_L32P_M3DQ14	U2
IO_3_L33N_M3DQ13	T1
IO_3_L33P_M3DQ12	T2
IO_3_L34N_M3UDQSN	P1
IO_3_L34P_M3UDQS	P2
IO_3_L35N_M3DQ11	N1
IO_3_L35P_M3DQ10	N2
IO_3_L36N_M3DQ9	M1
IO_3_L36P_M3DQ8	M3
IO_3_L37N_M3DQ1	L1
IO_3_L37P_M3DQ0	L2
IO_3_L38N_M3DQ3	K1
IO_3_L38P_M3DQ2	K2
IO_3_L39N_M3LDQSN	L3
IO_3_L39P_M3LDQS	L4
IO_3_L40N_M3DQ7	J1
IO_3_L40P_M3DQ6	J3
IO_3_L41N_GCLK26_M3DQ5	H1
IO_3_L41P_GCLK27_M3DQ4	H2
IO_3_L42N_GCLK24_M3LDM	K3
IO_3_L42P_GCLK25_TRDY2_M3UDM	K4
IO_3_L43N_GCLK22_IRDY2_M3CASN	K5
IO_3_L43P_GCLK23_M3RASN	L5
IO_3_L44N_GCLK20_M3A6	H3
IO_3_L44P_GCLK21_M3A5	H4
IO_3_L45N_M3ODT	K6
IO_3_L45P_M3A3	L7
IO_3_L46N_M3CLKN	G1
IO_3_L46P_M3CLK	G3
IO_3_L47N_M3A1	J6
IO_3_L47P_M3A0	J7
IO_3_L48N_M3BA1	F1
IO_3_L48P_M3BA0	F2
IO_3_L49N_M3A2	H5
IO_3_L49P_M3A7	H6
IO_3_L50N_M3BA2	E1
IO_3_L50P_M3WE	E3
IO_3_L51N_M3A4	F3
IO_3_L51P_M3A10	F4
IO_3_L52N_M3A9	D1
IO_3_L52P_M3A8	D2
IO_3_L53N_M3A12	G6
IO_3_L53P_M3CKE	H7
IO_3_L54N_M3A11	D3
IO_3_L54P_M3RESET	E4
IO_3_L55N_M3A14	F5
IO_3_L55P_M3A13	F6
IO_3_L83N_VREF	C1
IO_3_L83P	C2

XC6SLX16-2CSG324C

FPGA BANK 3 NOT USED

Title	STEVAL-IME0009V1 STMicroelectronics		
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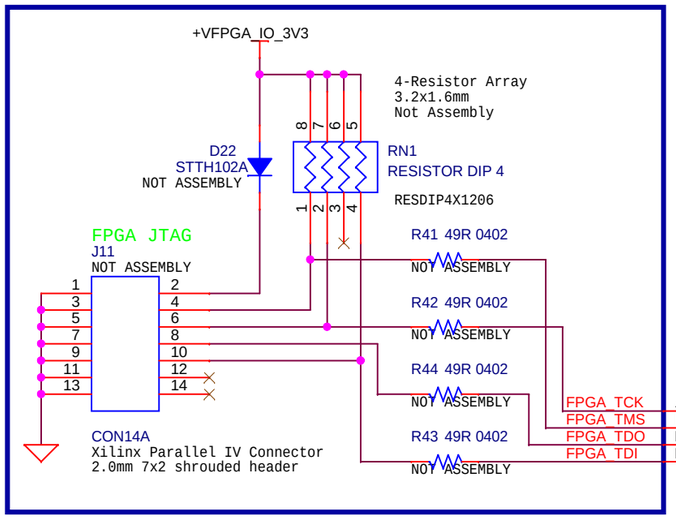
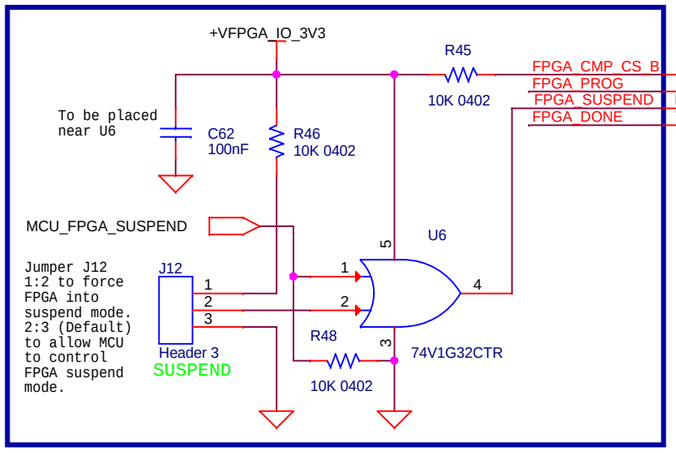
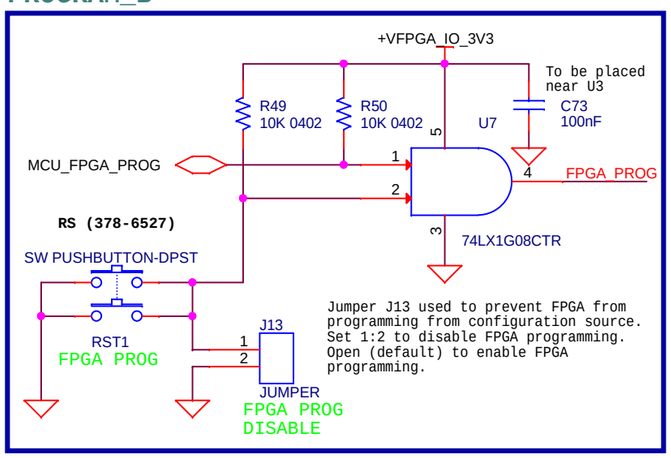
FPGA JTAG



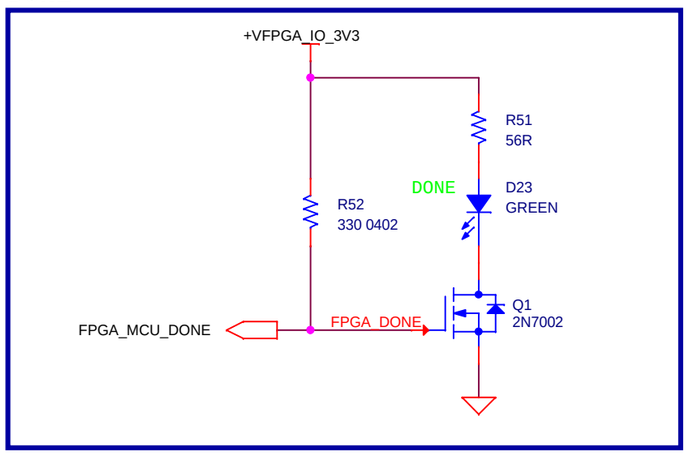
SUSPEND & CMPCS_B

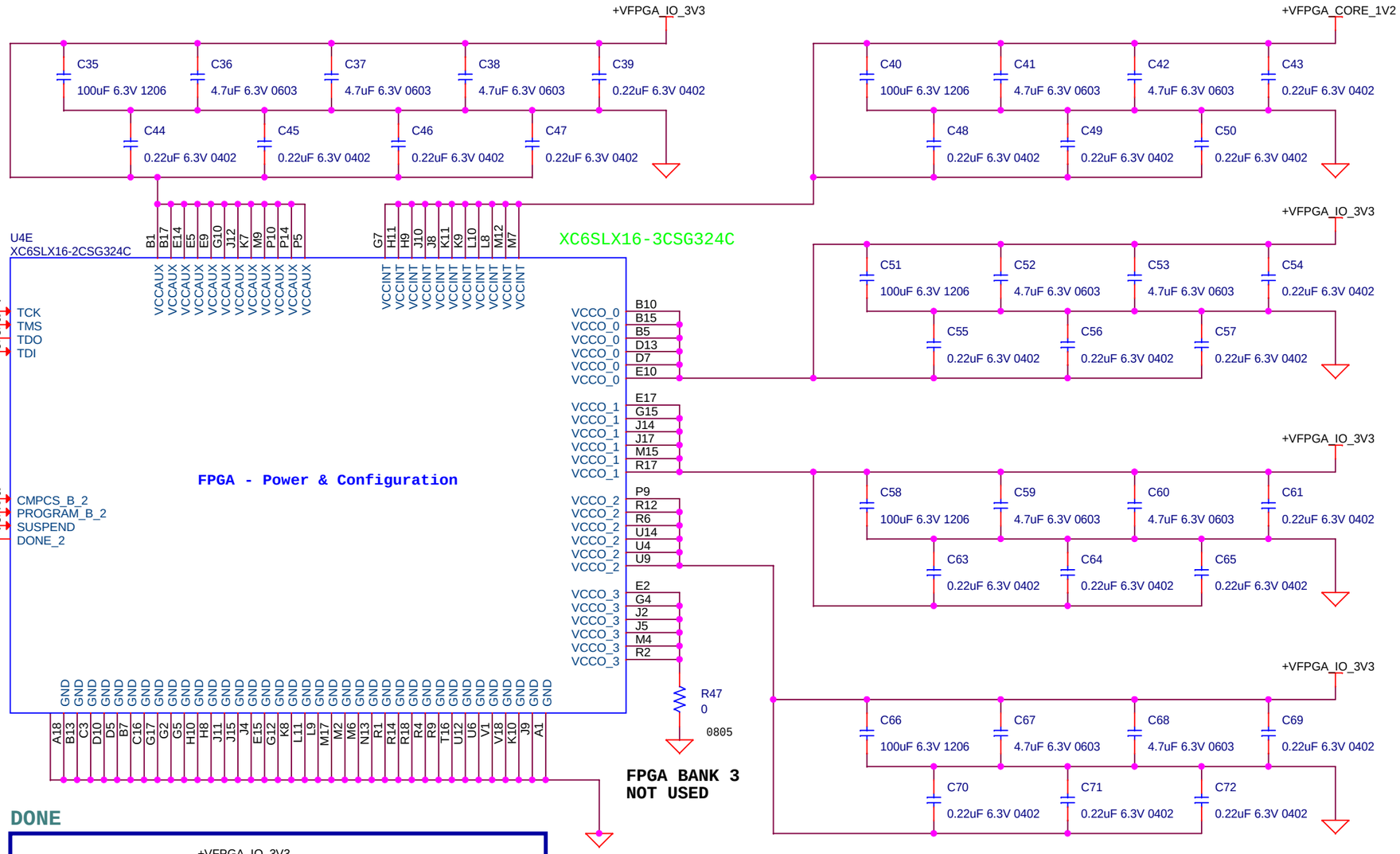


PROGRAM_B



DONE





FPGA - Power & Configuration

C35, C40, C51, C58, C66 Details
Murata (GRM31CR60J107ME39L) - Digikey (490-4539-1-ND)
Dimension 1206 - EIA 3216

C36, C37, C38, C41, C42, C52, C53, C59, C60, C67, C68 Details
TDK (C1608X5R0J475K) - Digikey (445-5178-2-ND)
Dimension 0603 - EIA 1608

Title: **STEVAL-IME009V1 STMicroelectronics**		
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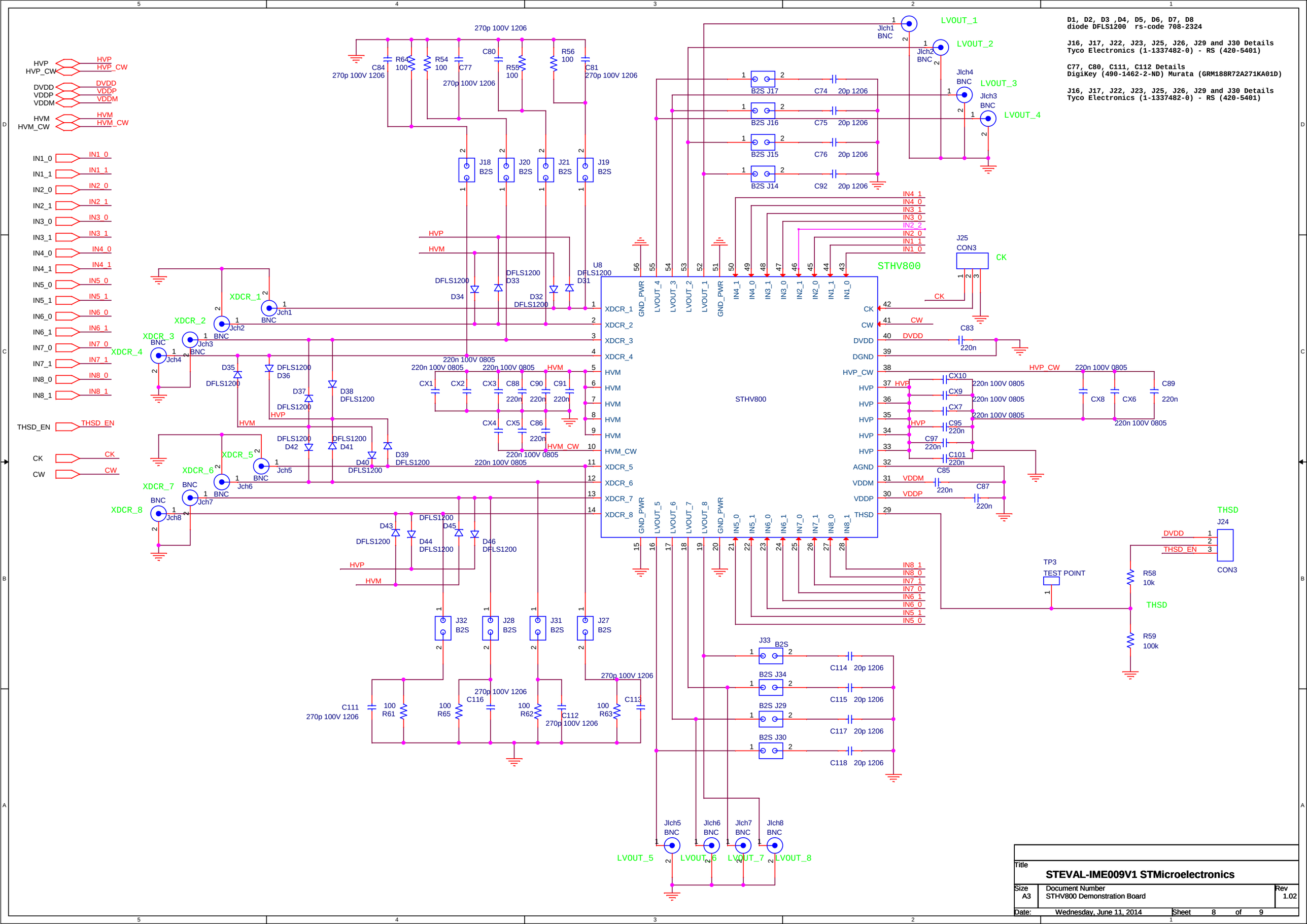
D1, D2, D3 ,D4, D5, D6, D7, D8
diode DFLS1200 rs-code 708-2324
J16, J17, J22, J23, J25, J26, J29 and J30 Details
Tyco Electronics (1-1337482-0) - RS (420-5401)
C77, C80, C111, C112 Details
DigiKey (490-1462-2-ND) Murata (GRM188R72A271KA01D)
J16, J17, J22, J23, J25, J26, J29 and J30 Details
Tyco Electronics (1-1337482-0) - RS (420-5401)
HVP
HVP_CW
DVDD
VDDP
VDDM
HVM
HVM_CW
IN1_0
IN1_1
IN2_0
IN2_1
IN3_0
IN3_1
IN4_0
IN4_1
IN5_0
IN5_1
IN6_0
IN6_1
IN7_0
IN7_1
IN8_0
IN8_1
THSD_EN
CK
CW
270p 100V 1206
C84
R64 100
R54 100
C77
C80
R55 100
R56 100
C81
J18 B2S
J20 B2S
J21 B2S
J19 B2S
XDCR_1
XDCR_2
XDCR_3
XDCR_4
XDCR_5
XDCR_6
XDCR_7
XDCR_8
Jch1 BNC
Jch2 BNC
Jch3 BNC
Jch4 BNC
Jch5 BNC
Jch6 BNC
Jch7 BNC
Jch8 BNC
DFLS1200
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
D42
D43
D44
D45
D46
220n 100V 0805
CX1
CX2
CX3
CX4
CX5
C86
C88
C90
C91
U8
STHV800
XDCR_1
XDCR_2
XDCR_3
XDCR_4
HVM
HVM_CW
XDCR_5
XDCR_6
XDCR_7
XDCR_8
GND_PWR
LVOUT_1
LVOUT_2
LVOUT_3
LVOUT_4
LVOUT_5
LVOUT_6
LVOUT_7
LVOUT_8
IN4_1
IN4_0
IN3_1
IN3_0
IN2_2
IN2_0
IN1_1
IN1_0
IN5_0
IN5_1
IN6_0
IN6_1
IN7_0
IN7_1
IN8_0
IN8_1
THSD
Jlch1 BNC
Jlch2 BNC
Jlch4 BNC
Jlch3 BNC
B2S J17
B2S J16
B2S J15
B2S J14
C74 20p 1206
C75 20p 1206
C76 20p 1206
C92 20p 1206
J25 CON3
CK
CW
DVDD
DGND
HVP_CW
HVP
VDDM
VDDP
AGND
C83 220n
CX10
CX9
CX7
C95 220n
C97 220n
C101 220n
C85
C87
C89
CX8
CX6
J33 B2S
B2S J34
B2S J29
B2S J30
C114 20p 1206
C115 20p 1206
C117 20p 1206
C118 20p 1206
C111 270p 100V 1206
C116 270p 100V 1206
C112 270p 100V 1206
C113 270p 100V 1206
100 R61
100 R65
100 R62
100 R63
J32 B2S
J28 B2S
J31 B2S
J27 B2S
TP3
TEST POINT
J24 CON3
R58 10k
R59 100k
Title
STEVAL-IME009V1 STMicroelectronics
Size A3
Document Number
STHV800 Demonstration Board
Rev 1.02
Date: Wednesday, June 11, 2014
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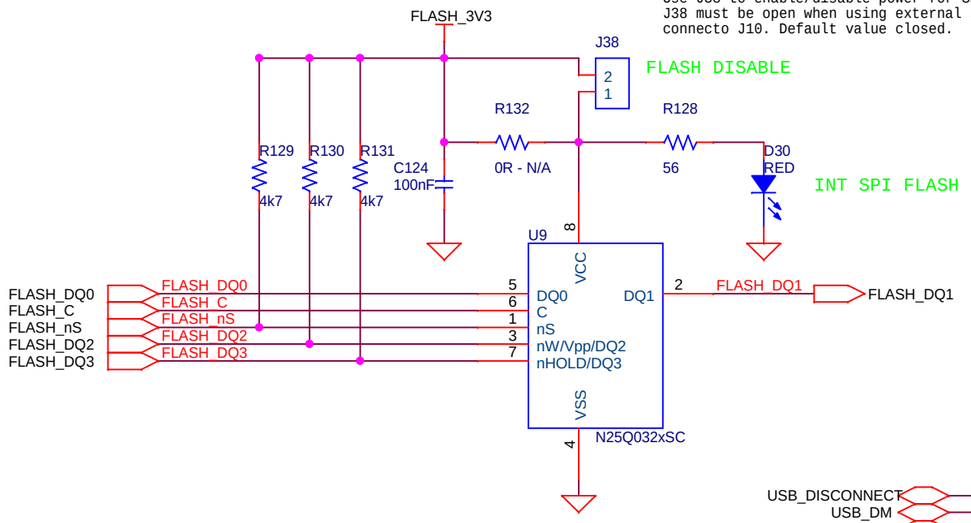
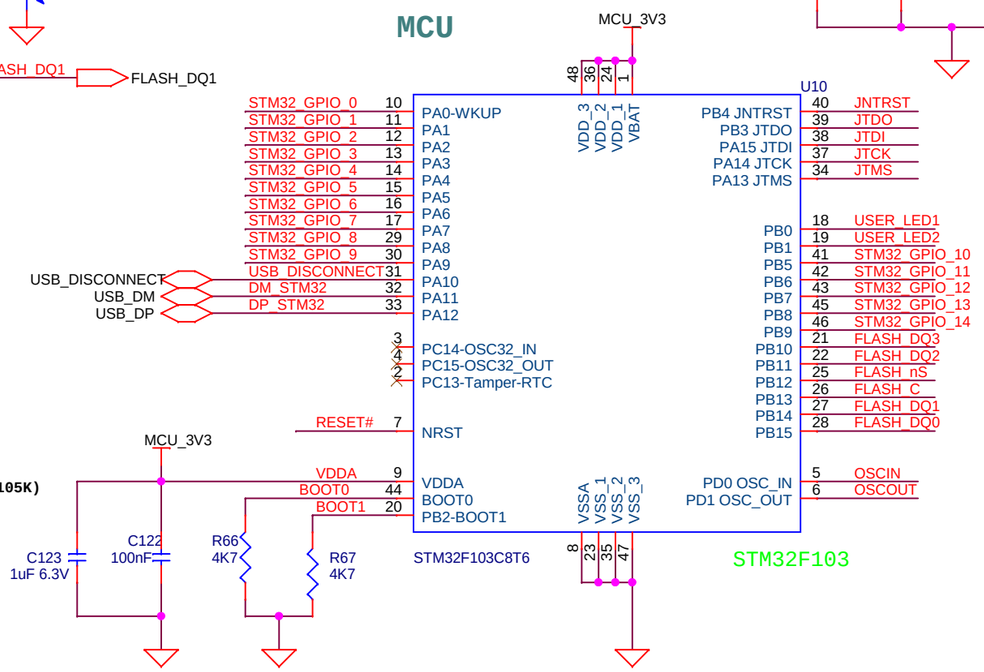
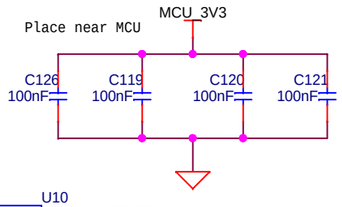
SPI FLASH

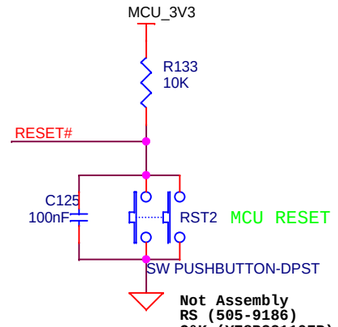
Use J38 to enable/disable power for SPI flash device.
J38 must be open when using external spi flash device on
connecto J10. Default value closed.



MCU

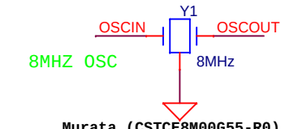






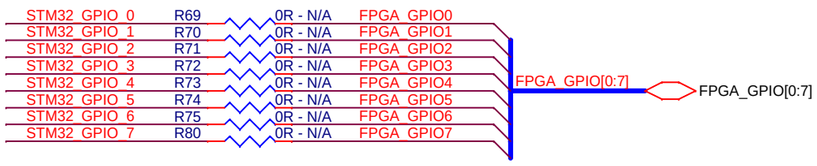
C123 Details:
Digikey (445-4998-2-ND) - TDK (C1005X5R0J105K)
Package 0402

OSCILLATOR

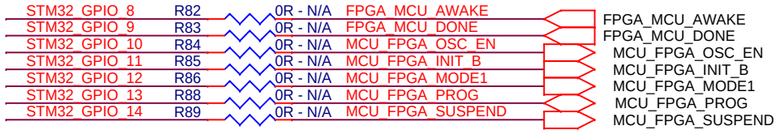


Murata (CSTCE8M00G55-R0)
DigiKey (490-1195-1-ND)
RS: 283-961
Farnell: 1615352

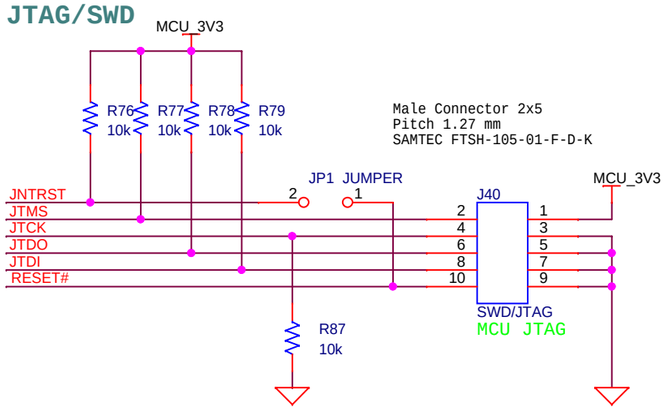
OPTIONAL FPGA I/O



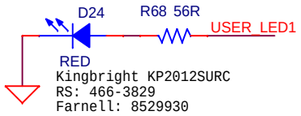
OPTIONAL FPGA CONFIGURATION SIGNALS



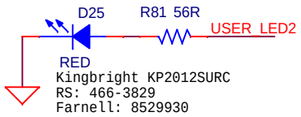
JTAG/SWD



DOWNLOAD



FLASH READY



Title	**STEVAL-IME009V1 STMicroelectronics**	
Size B	Document Number STHV800 Demonstration Board	Rev 1.02
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