NUCLEO-144 STM32C5 series

MB2310 C5A3ZG

Table of contents

U_Top
Top.SchDoc

HW1
STICKER PRODUCT
N/A

HW2
PCB
MB2310

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

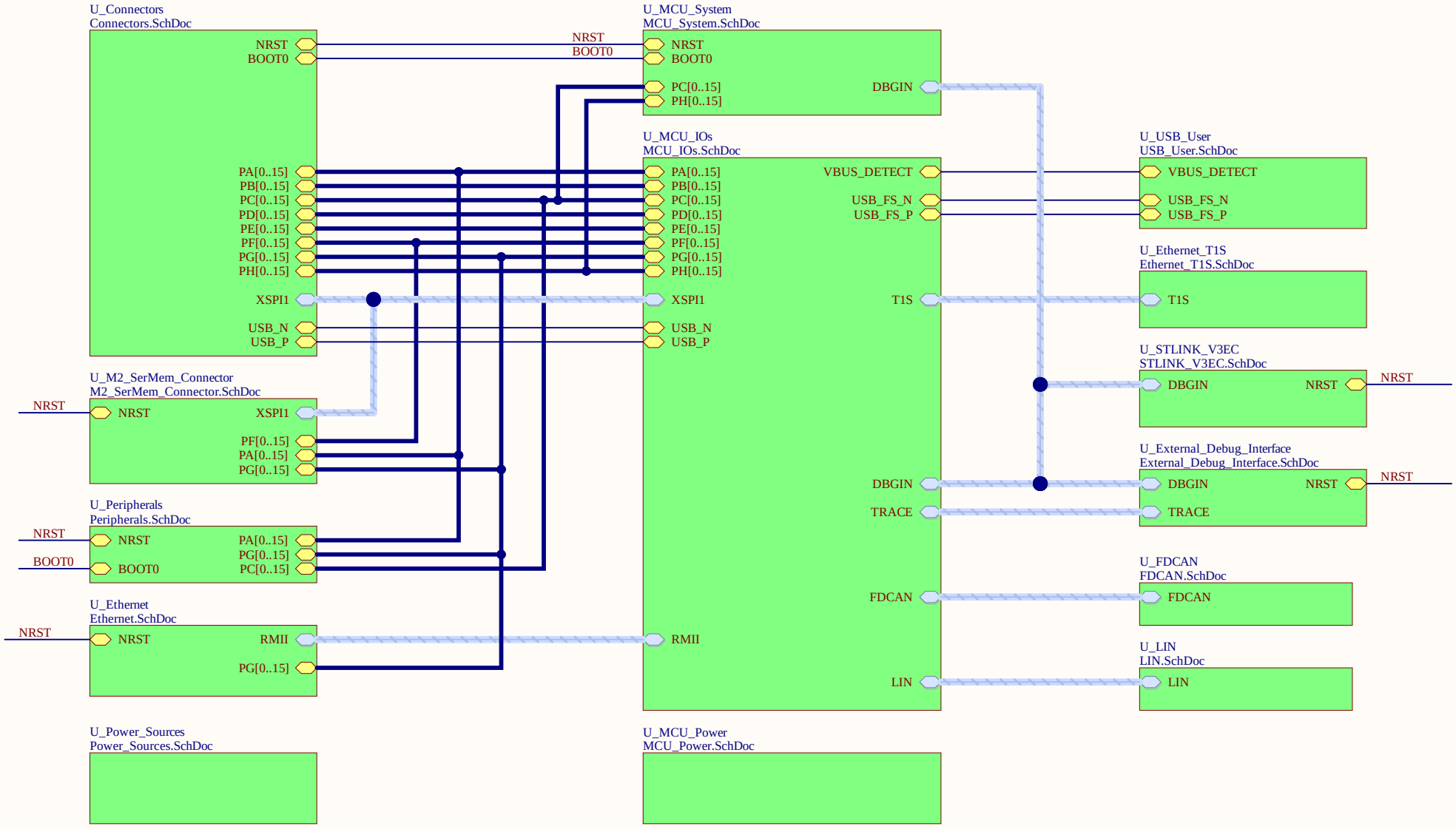
OPEN PLATFORM LICENSE AGREEMENT

The Open Platform License Agreement (“Agreement”) is a binding legal contract between you ("You") and STMicroelectronics International N.V. (“ST”), a company incorporated under the laws of the Netherlands acting for the purpose of this Agreement through its Swiss branch 39, Chemin du Champ des Filles, 1228 Plan-les-Ouates, Geneva, Switzerland.

By using the enclosed reference designs, schematics, PC board layouts, and documentation, in hardcopy or CAD tool file format (collectively, the “Reference Material”), You are agreeing to be bound by the terms and conditions of this Agreement. Do not use the Reference Material until You have read and agreed to this Agreement terms and conditions. The use of the Reference Material automatically implies the acceptance of the Agreement terms and conditions.

The complete Open Platform License Agreement can be found on www.st.com/opla.

Title: **Project Overview**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 1 of 16



FID HW10 FID HW11
FID HW12 FID HW13

Title: **Top**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 2 of 16

MCU_System

PC[0..15]
PH[0..15]

DBGIN

MCO	DBGIN.MCO	PH0
SWDIO	DBGIN.SWDIO	PA13
SWO	DBGIN.SWO	PB3
SWCLK	DBGIN.SWCLK	PA14
JTDI	DBGIN.JTDI	PA15
VCP_TX	DBGIN.VCP_TX	PA2
VCP_RX	DBGIN.VCP_RX	PA3

U1A
MCU CLK & RST

NRST — 25 NRST
BOOT0-PH2 138 — BOOT0

EXTERNAL LSE CLK

C60 8.2pF OSC32_IN R1 0R PC14-OSC32_IN
X2 32.768kHz
C61 8.2pF OSC32_OUT R2 0R PC15-OSC32_OUT

8 PC14-OSC32_IN
9 PC15-OSC32_OUT

EXTERNAL HSE CLK

PH0-OSC_IN R3 0R OSC_IN C62 1.8pF
X3 48MHz
PH1-OSC_OUT R4 0R OSC_OUT C59 1.8pF

23 PH0-OSC_IN
24 PH1-OSC_OUT

STM32C5A3ZGT6

TO CONNECT IOs ON MORPHO CONNECTOR

SB should be close to MCU pad

PC14 SB1 DNF 0R PC14-OSC32_IN
PC15 SB2 DNF 0R PC15-OSC32_OUT

TO CONNECT IOs ON MORPHO CONNECTOR

SB should be close to MCU pad

0R DNF SB5 DBGIN.MCO
PH0-OSC_IN 0R DNF SB3 PH0
PH1-OSC_OUT 0R DNF SB4 PH1

HW3 LQFP144_socket
DNF

Title: **MCU_System**			
Project: **NUCLEO-144 STM32C5 series**			
Variant: C5A3ZG			
Revision: B-02		Reference: MB2310	
Size: A4	Date: 2025-Dec-11	Sheet: 3 of 16	

MCU IOs

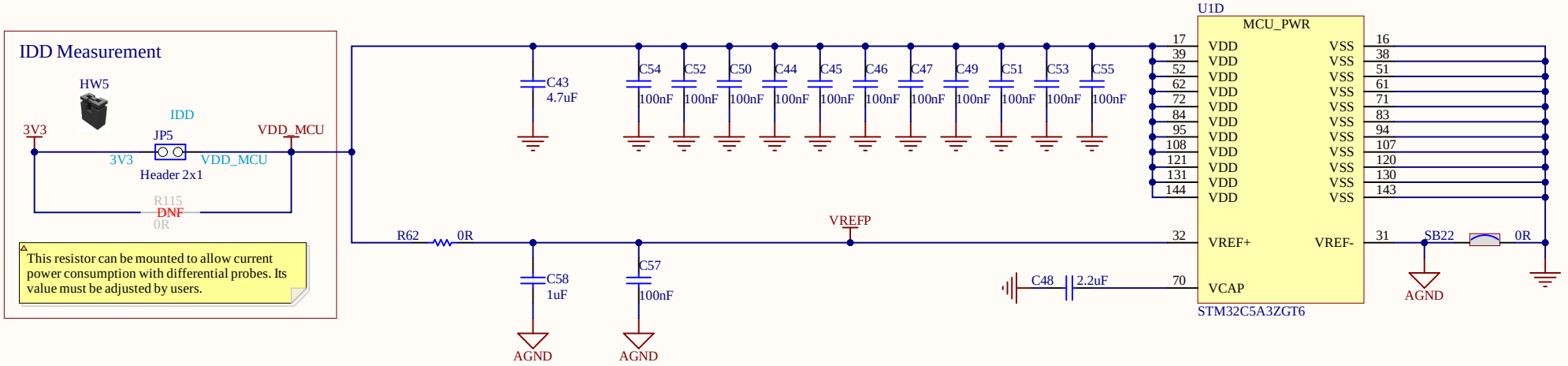
SB CONFIGURATION

DEBUG, TRACE and USB ARE CONNECTED BY DEFAULT, THEN SB FOR OPTIONAL CONFIGURATION ON MORPHO
ETHERNET, FDCAN: SB ON THE IOs INTERFACE TO BE ABLE TO DISCONNECT THE FUNCTION TO USE THE IOs ON MORPHO.
XSPI INTERFACE DIRECTLY CONNECTED TO M2 MEMORY CONNECTOR WITH 0R FOR SIGNAL INTEGRITY. REMOVED M2 MEMORY MODULE TO USED THESE IOs ON THE MORPHO
ONLY MAIN NUCLEO FUNCTION ARE MENTIONED ON THIS SHEET
PLEASE REFER TO THE STM32 DATASHEET TO HAVE THE COMPLET VIEW OF ALL THE ALTERNATE FUNCTION

Title: **MCU IOs**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A3	Date: 2025-Dec-11	Sheet: 4 of 16

MCU Power

Operating range: VDD/VREF deped nof the STM32 supported



Title: **MCU Power**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 5 of 16

Connectors

COLOR LEGEND
- MORPHO SPECIFICATION
- ARDUINO SPECIFICATION
- STM32 ALTERNATE FUNCTION
- STM32 IO PORT
- ~~FUNCTION NOT AVAILABLE~~

PA[0..15] PB[0..15] PC[0..15] PD[0..15] PE[0..15] PF[0..15] PG[0..15] PH[0..15]

NRST BOOT0

USB_N USB_P

XSPI1

IO0	XSPI1.IO0	PF9
IO1	XSPI1.IO1	PF8
IO2	XSPI1.IO2	PF7
IO3	XSPI1.IO3	PF6
IO4	XSPI1.IO4	PE7
IO5	XSPI1.IO5	PE8
IO6	XSPI1.IO6	PE9
IO7	XSPI1.IO7	PE10
NCS1	XSPI1.NCS1	PE11
NCS2	XSPI1.NCS2	PE0
DQS0	XSPI1.DQS0	PB2
CLK	XSPI1.CLK	PF10
NCLK	XSPI1.NCLK	PF11

ARDUINO HOLES

H1 H2 H3

ST-MORPHO AND ARDUINO UNO-V3

Operating range: 3V < VCC < 3.6V
Max current budget 500mA

ST MORPHO CONNECTOR LEFT SIDE

CN7 — Header 19x2

PC10	SDIO_DAT2 / I2S_CK	1 2	SDIO_DAT3 / I2S_SDI	PC11
PC12	SDIO_CLK / I2S_SDO	3 4	SDIO_CMD	PD2
3V3	3V3	5 6	5V_EXT (2)	5V_EXT
BOOT0	BOOT0	7 8	GND	
PA2	GPIO	9 10	GPIO	PB8
PA3	GPIO	11 12	IOREF	
PA13	SWDIO	13 14	NRST	NRST
PA14	SWCLK	15 16	3V3 (3)	
PA15	JTDI/TIM2_CH1 (H1) /I2S_WS	17 18	5V	
	GND	19 20	GND	
PD0	GPIO / FDCAN_STBY	21 22	GND	
PC13	WKUP	23 24	VIN	
PC14	LSE_IN	25 26	GPIO	PB9
PC15	LSE_OUT	27 28	ADCx_INy	PH4
PH0	HSE_IN	29 30	ADCx_INy	PH5
PH1	HSE_OUT	31 32	ADCx_INy / DACx_OUTy	PA4
	~~VBAT~~	33 34	ADCx_INy	PB0
PC2	ADCx_INy / SPIB_MISO	35 36	ADCx_INy	PE13
PC3	ADCx_INy / SPIB_MOSI	37 38	ADCx_INy	PC0

3V3 3V3 5V 3V3 VIN 5V_VIN

R50 1K

CN6 — Socket 8x1 — POWER

1	NC
2	IOREF
3	NRST
4	3V3
5	5V
6	GND
7	GND
8	VIN

CN8 — Socket 6x1 — ANALOG

1	A0
2	A1
3	A2
4	A3
5	A4
6	A5

VREFP

SB6 DNF 0R

C38 100nF

ST MORPHO CONNECTOR RIGHT SIDE

CN5 — Socket 10x1 — DIGITAL ~ PWM

10	SCL
9	SDA
8	AREF
7	GND
6	SCK
5	MISO
4	~ MOSI
3	~ NSS
2	~ D9
1	D8

CN9 — Socket 8x1 — DIGITAL ~ PWM

8	D7
7	~ D6
6	~ D5
5	D4
4	~ D3
3	D2
2	TX
1	RX

CN10 — Header 19x2

PC9	SDIO_DAT1 / LINA_RX	1 2	SDIO_DAT0 / LINA_TX	PC8
PB6	I2C1/I3C1_SCL	3 4	GPIO	PC7
PB7	I2C1/I3C1_SDA	5 6	GPIO	PF15
	AREF (2)	7 8	5V_STLK (3)	5V_STLK
	GND	9 10	GPIO	PF14
PA5	SPI1_SCK	11 12	USB_DP / FDCANA_TX	USB_P PA12
PA6	SPI1_MISO	13 14	USB_DM / FDCANA_RX	USB_N PA11
PA7	SPI1_MOSI / TIM15_CH1	15 16	TIM1_BKIN / FDCANB_RX	PB12
PB5	SPI1_NSS / TIM8_CH3	17 18	ADCx_INy	PB1
PC6	TIM8_CH1	19 20	GND	
PA9		21 22	GPIO	PF13
PA8		23 24	GPIO	PF12
PB10		25 26	TIM1_CH3N (WL)	PB15
PB4	TIM8_CH2	27 28	TIM1_CH2N (VL)	PB14
PA0	WKUP1	29 30	TIM1_CH1N (UL) / SPIB_SCK / FDCANB_TX	PB13
PB3		31 32	AGND	AGND
PA10		33 34	ADCx_INy	PE14
PD5		35 36	UART_TX	PD4
PD6		37 38	UART_RX	PD3

CN11 — Header 16x2 — DNF

PG2	1 2	XSPI1.IO3	PF6
PG3	3 4	XSPI1.IO2	PF7
PE2	5 6	XSPI1.IO1	PF8
PE3	7 8	XSPI1.IO0	PF9
PE4	9 10	PE5	
	11 12	PE6	
PF1	13 14	PF2	
PF0	15 16	PH15	
PD1	17 18	PF3	
PF4	19 20	PG1	
PG0	21 22		
PE1	23 24	PD7	
PG9	25 26	PG15	
PG10	27 28	PG12	
PH3	29 30	PG13	
PD9	31 32	PG11	

CN12 — Header 16x2 — DNF

PE7	XSPI1.IO4	XSPI1.NCS1	PE11
PE8	XSPI1.IO5	XSPI1.NCS2	PE0
PE9	XSPI1.IO6	XSPI1.DQS0	PB2
PE10	XSPI1.IO7	XSPI1.CLK	PF10
PD12		XSPI1.NCLK	PF11
PD11		PD13	
PE15		PD14	
PE12			
PD8		PD15	
PC1		PF5	
PG14		PC4	
		PC5	
PD10		PA1	
PG7		PG8	
PG4		PG5	
		PG6	

CN15 — BOTTOM LEFT — GND

CN16 — BOTTOM RIGHT — GND

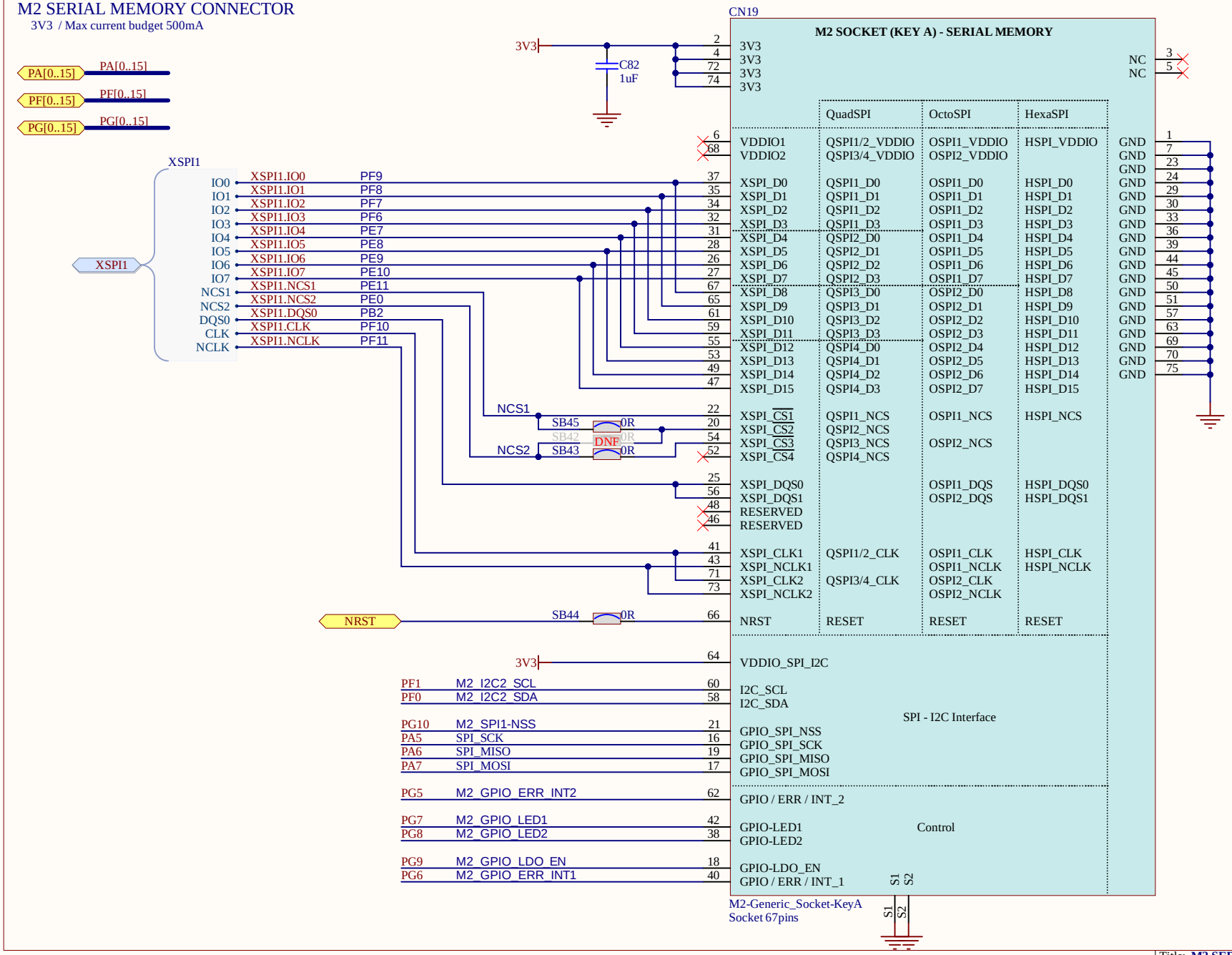
(1): VIN (NUCLEO INPUT) WARNING voltage applied to 7V < VIN <12V
(2): E5V, AREF (NUCLEO INPUT)
(3): 5V, 3V3, IOREF, VBUS_STLK (NUCLEO OUTPUT, SHIELD INPUT)

ST-MORPHO SHIELD COMPATIBLE:
X-NUCLEO_IHM16M1
X-NUCLEO-GFX01M2

Title: **Connectors**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A3	Date: 2025-Dec-11	Sheet: 6 of 16

M2 SERIAL MEMORY CONNECTOR

3V3 / Max current budget 500mA



HW6

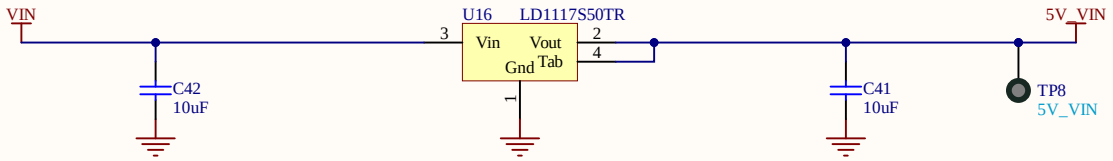
S001-00001-A42-R

Title: **M2 SERIAL MEMORY CONNECTOR**			
Project: **NUCLEO-144 STM32C5 series**			
Variant: C5A3ZG			
Revision: B-02		Reference: MB2310	
Size: A4	Date: 2025-Dec-11	Sheet: 7 of 16	

POWER SOURCES

VIN / 5V PWR / 800mA

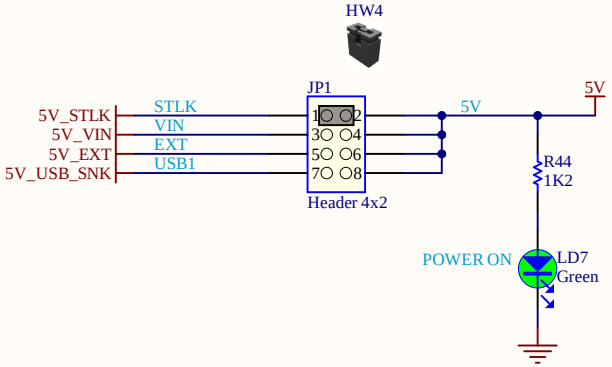
Operating range: 7V < VIN < 12V



5V PWR SELECTION

ONLY ONE POSITION SHOULD BE SELECTED

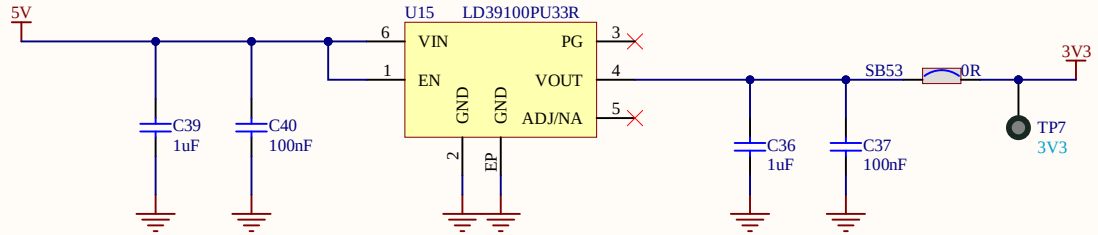
5V / 1A



STLK: 5V from USB STLINK
VIN: 5V from Arduino VIN + LDO_U16
EXT: 5V from Morpho connector
USB1: 5V from USB User connector CN13

3V3 PWR / 1A

Operating range: 4.5V < PVIN < 5.5V

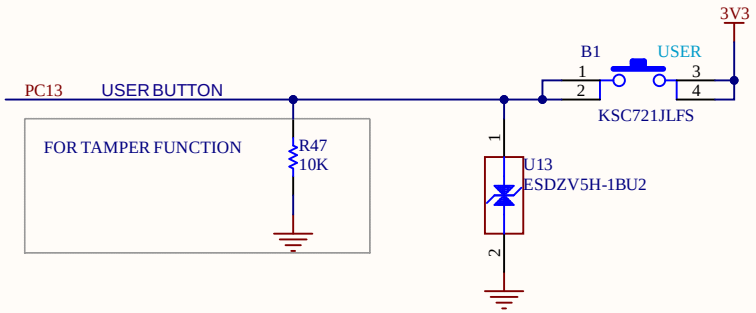


GND HEADERS

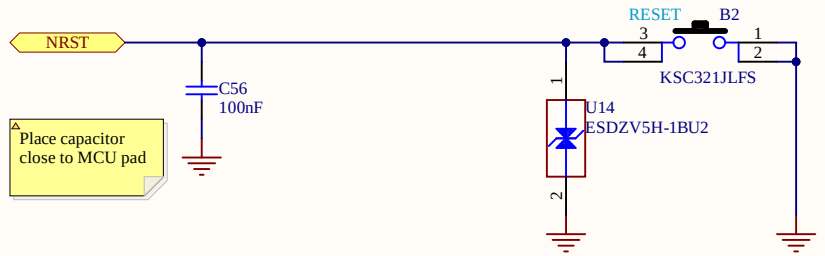
Title: **POWER SOURCES**			
Project: **NUCLEO-144 STM32C5 series**			
Variant: C5A3ZG			
Revision: B-02		Reference: MB2310	
Size: A4	Date: 2025-Dec-11	Sheet: 8 of 16	

PERIPHERALS

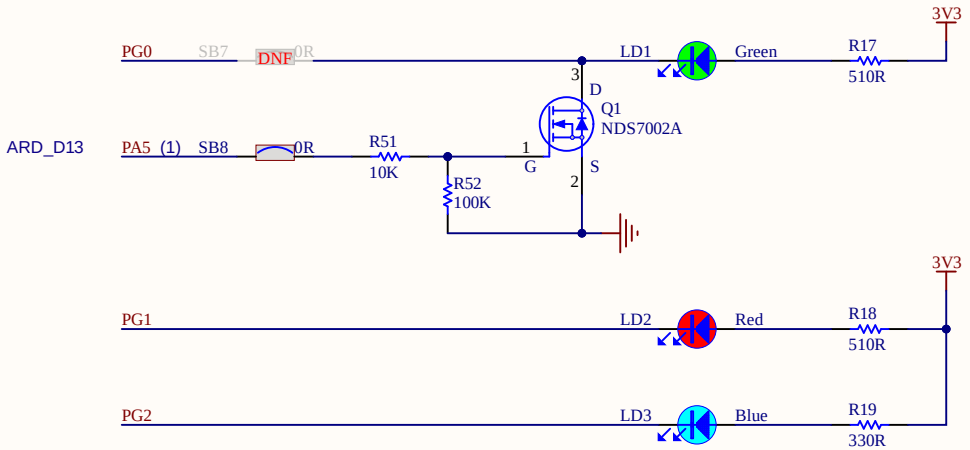
USER BUTTON



RESET BUTTON

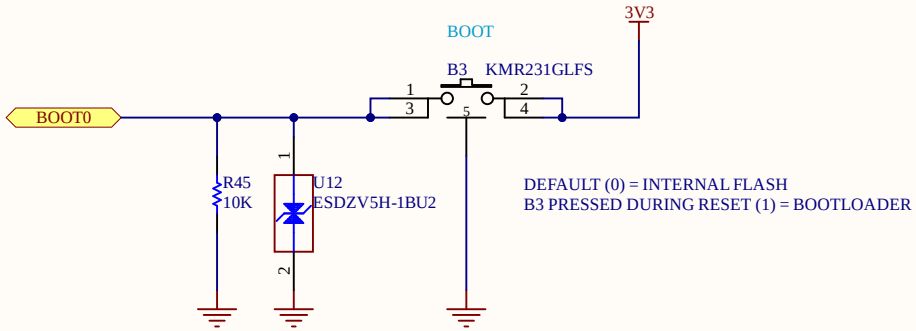


USER LED



(1): Removed this SB to isolate the LED1 to ARDUINO-D13 (SPI-SCK) (Arduino D13 driving is the main configuration)

BOOT MODE



PA[0..15] PA[0..15]

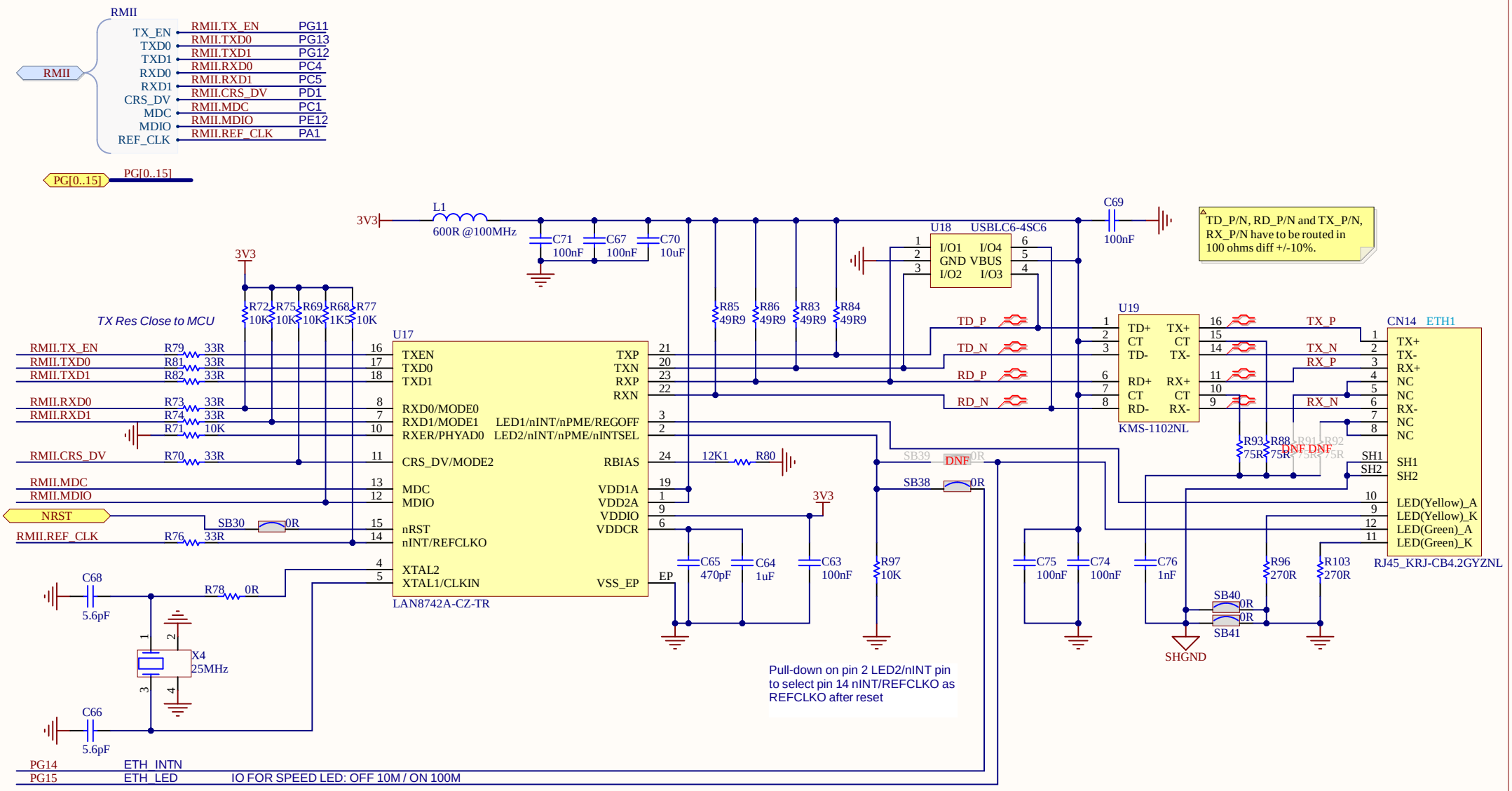
PC[0..15] PC[0..15]

PG[0..15] PG[0..15]

Title: **PERIPHERALS**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 9 of 16

ETHERNET 10/100Mbps

Operating range: 3V<VDDxA<3V6
Operating range: 1V62<VDDIO<3V6

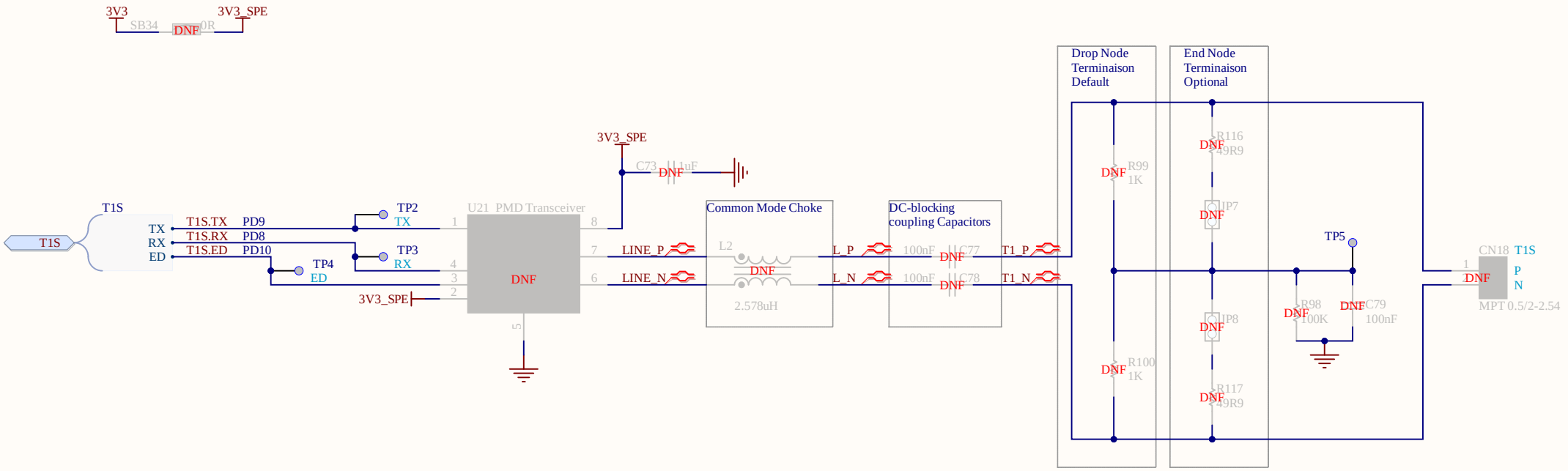


Title: **ETHERNET 10/100Mbps**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 10 of 16

ETHERNET - T1S

50 V COMPATIBLE

Operating range: xVx<VCC<xVx

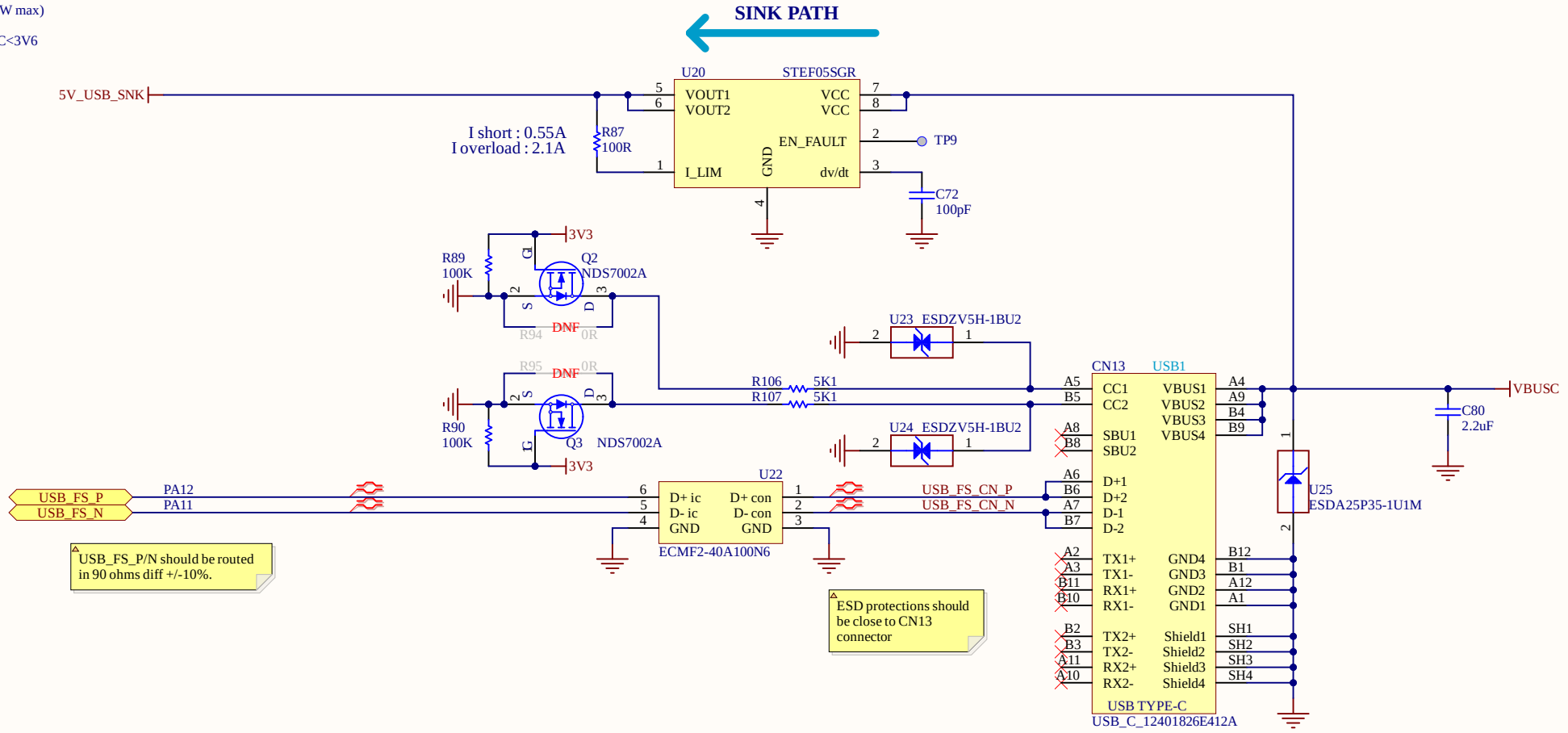


Title: **ETHERNET - T1S**			
Project: **NUCLEO-144 STM32C5 series**			
Variant: C5A3ZG			
Revision: B-02		Reference: MB2310	
Size: A4	Date: 2025-Dec-11	Sheet: 11 of 16	

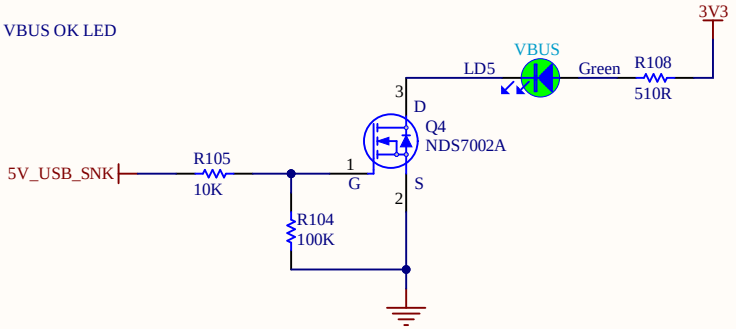
USB USER

USB-C SELF POWER MODE
VBUSC : 5V/500mA (2.5W max)

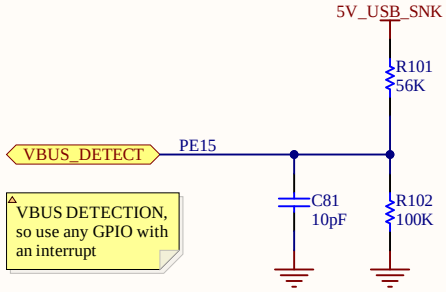
Operating range: 3V<VCC<3V6



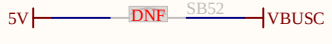
5V_USB_LED



VBUS SENSE



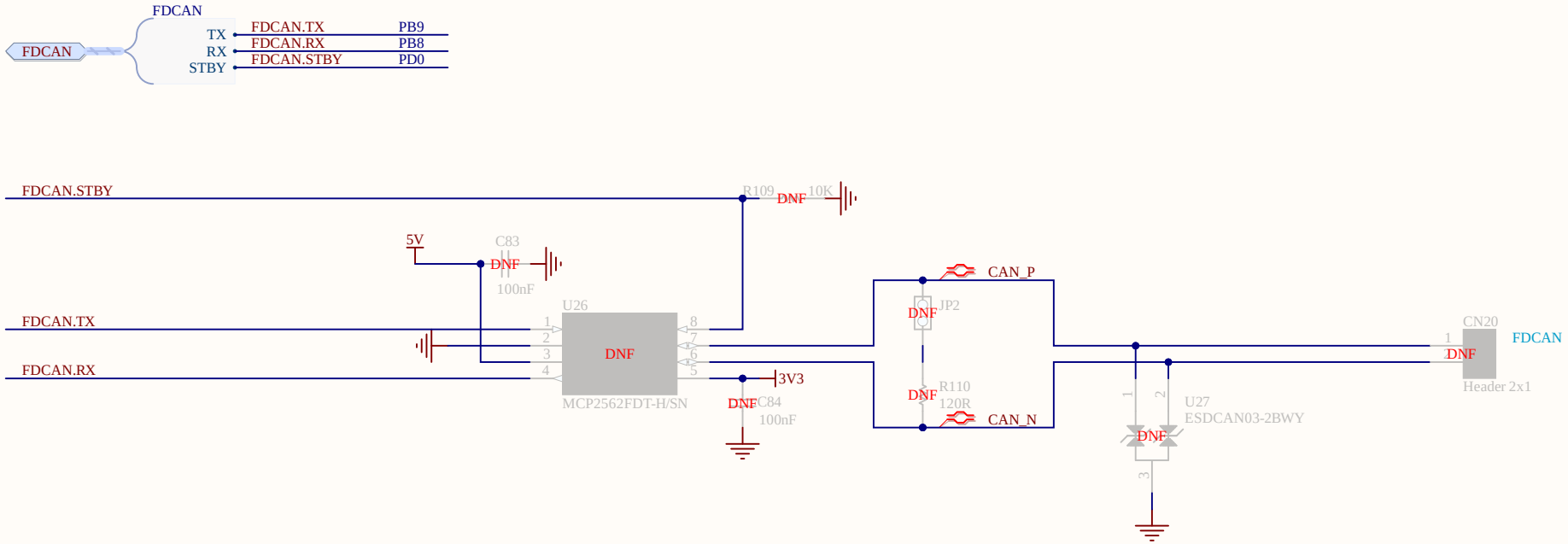
FOR DEBUG PURPOSE



Title: **USB USER**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 12 of 16

CAN FD

Operation Volatage: VDD: 4.5 ~ 5.5V; VIO: 1.8 ~ 5.5V

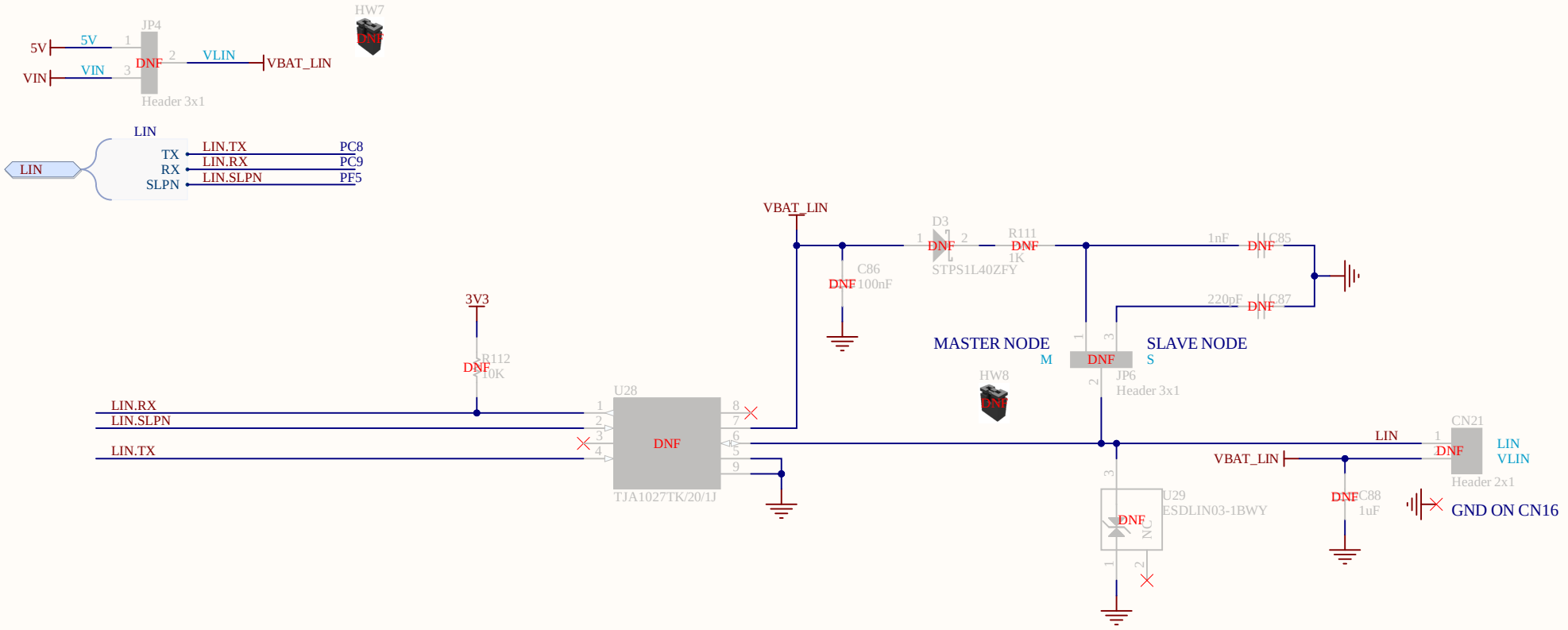


Title: **FDCAN**			
Project: **NUCLEO-144 STM32C5 series**			
Variant: C5A3ZG			
Revision: B-02		Reference: MB2310	
Size: A4	Date: 2025-Dec-11	Sheet: 13 of 16	

LIN

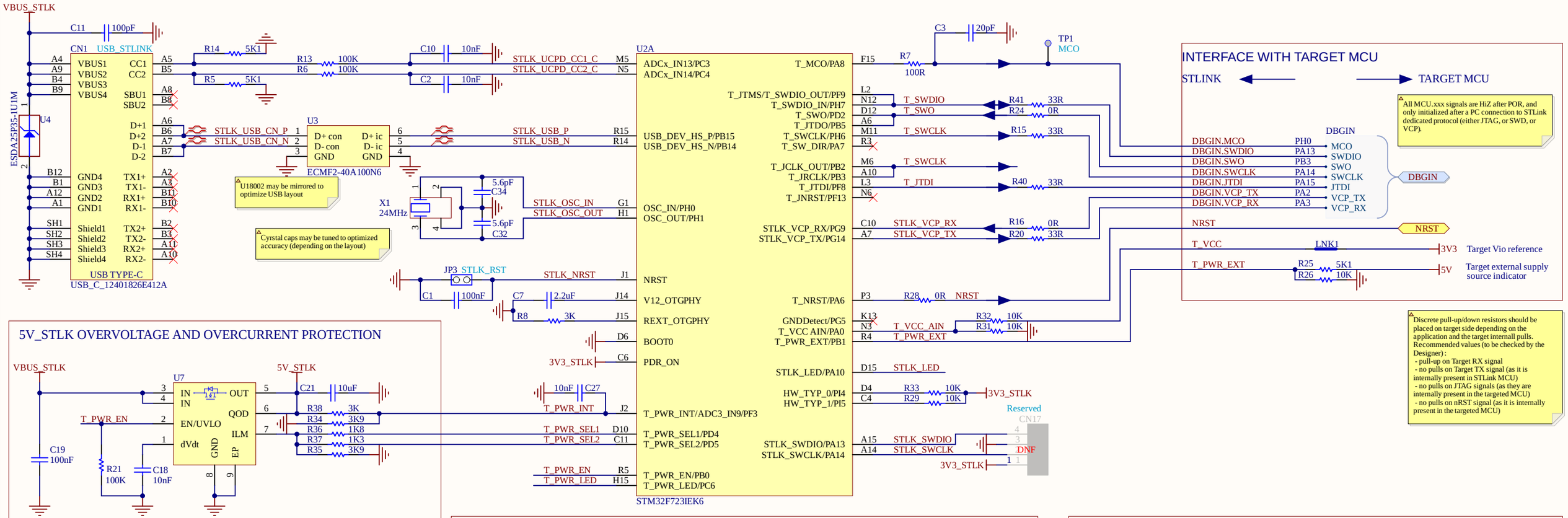
Operation Voltage: VBAT: 5 ~ 18V
Operation Voltage: VIN: 7 ~ 12V

If VBAT < 5 V, the TJA1027 may remain operational, but parameter values cannot be guaranteed to remain within the operation ranges specified in datasheet

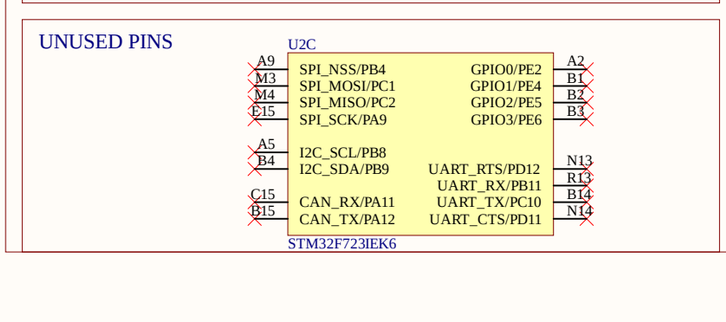


Title: **LIN**			
Project: **NUCLEO-144 STM32C5 series**			
Variant: C5A3ZG			
Revision: B-02		Reference: MB2310	
Size: A4	Date: 2025-Dec-11	Sheet: 14 of 16	

STLINK-V3EC



5V_STLK OVERVOLTAGE AND OVERCURRENT PROTECTION

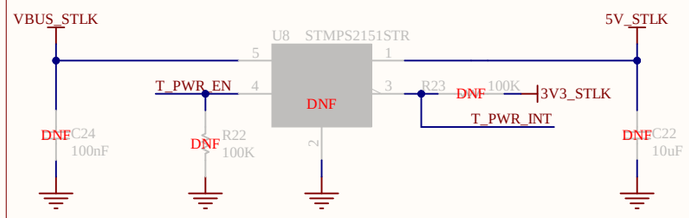


5V_STLK OVERCURRENT PROTECTION MANAGEMENT

	T_PWR_SEL2/PD5	T_PWR_SEL1/PD4
PowerDefault.SNK *(current limit: 550mA)*	Hi-Z	Hi-Z
Power1.5.SNK *(current limit: 1.66A)*	Hi-Z	0
Power3.0.SNK *(current limit: 3.2A)*	0	0

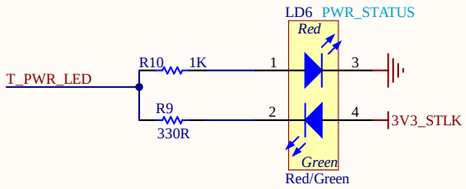
Hi-Z = IO set in high impedance

STMPS2151STR is backup of the TPS259535DSG

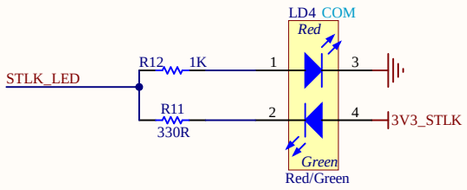


UNUSED PINS

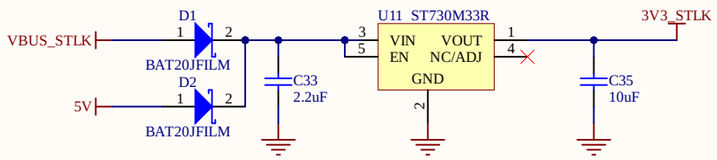
POWER STATUS



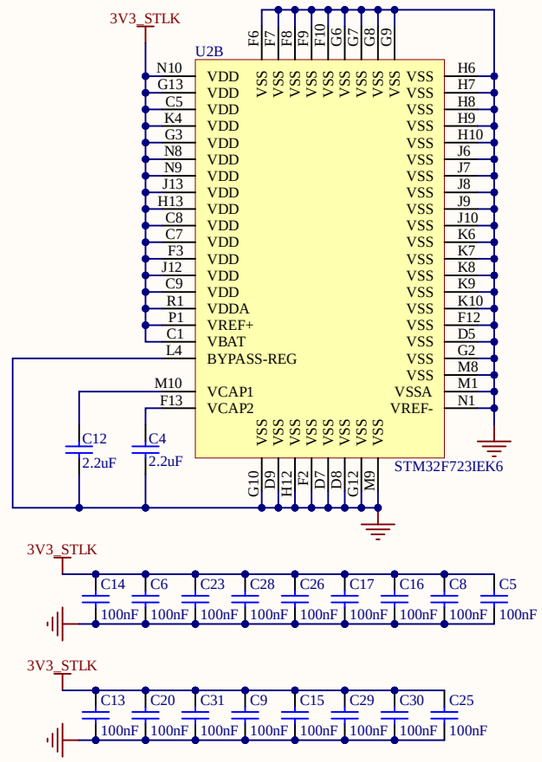
COM STATUS



ST-LINK POWER (3V3/300mA)

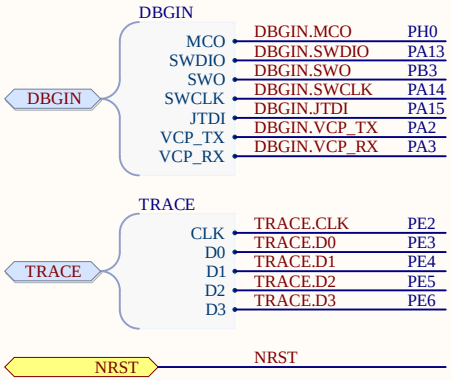


STLINK MCU POWER

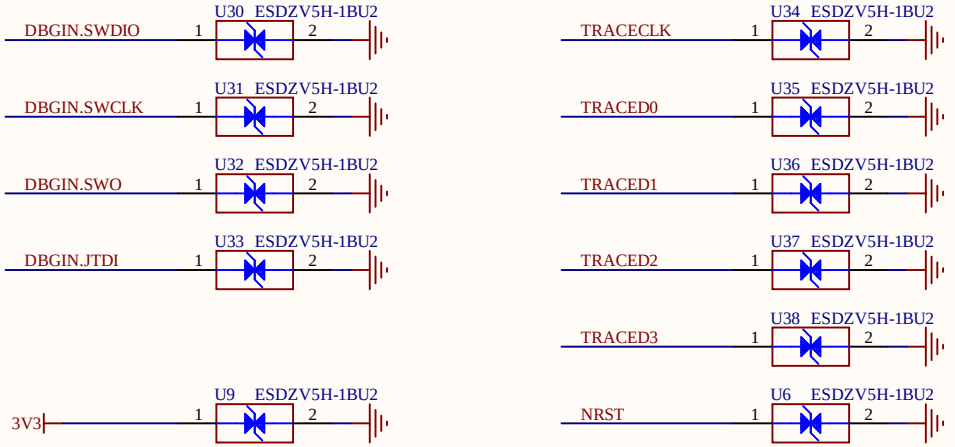


Title: **STLINK-V3EC**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A3	Date: 2025-Dec-11	Sheet: 15 of 16

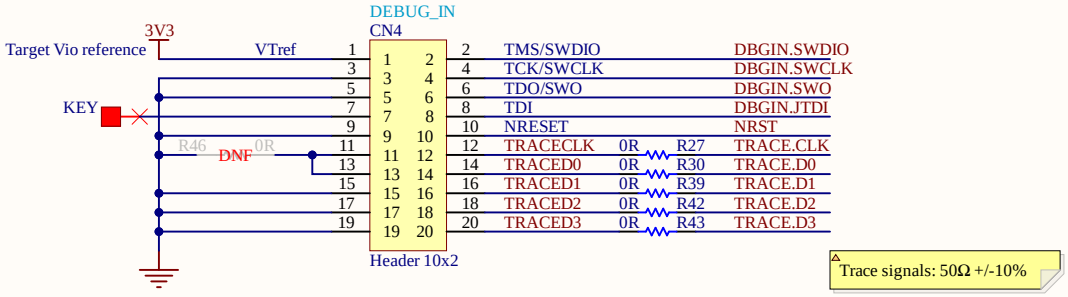
EXTERNAL DEBUG INTERFACES



ESD PROTECTIONS

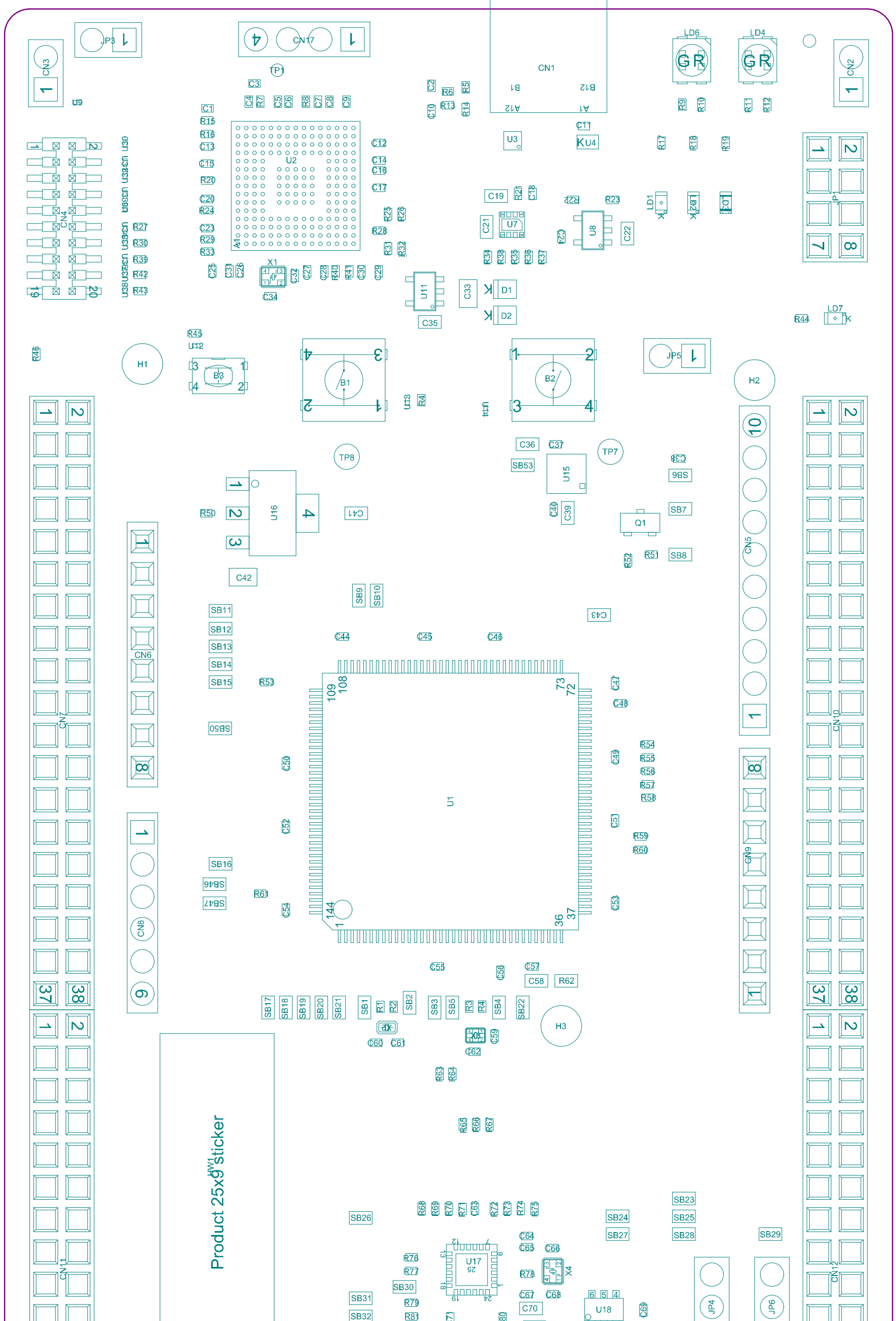


MIPI-20 CONNECTOR

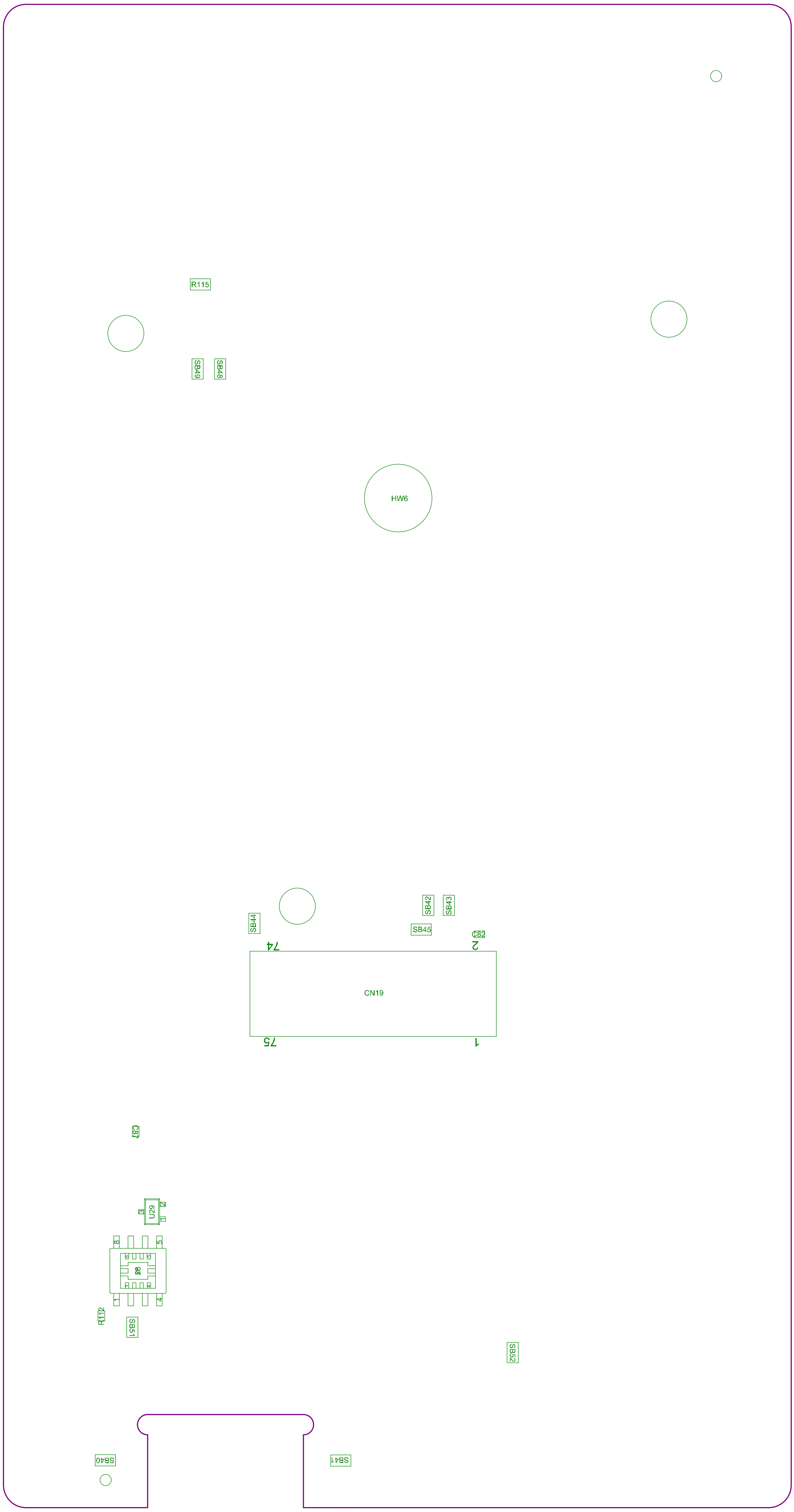


Specific constraints for MCU.SWDIO and MCU.SWCLK (must be same length and must be Shielded).

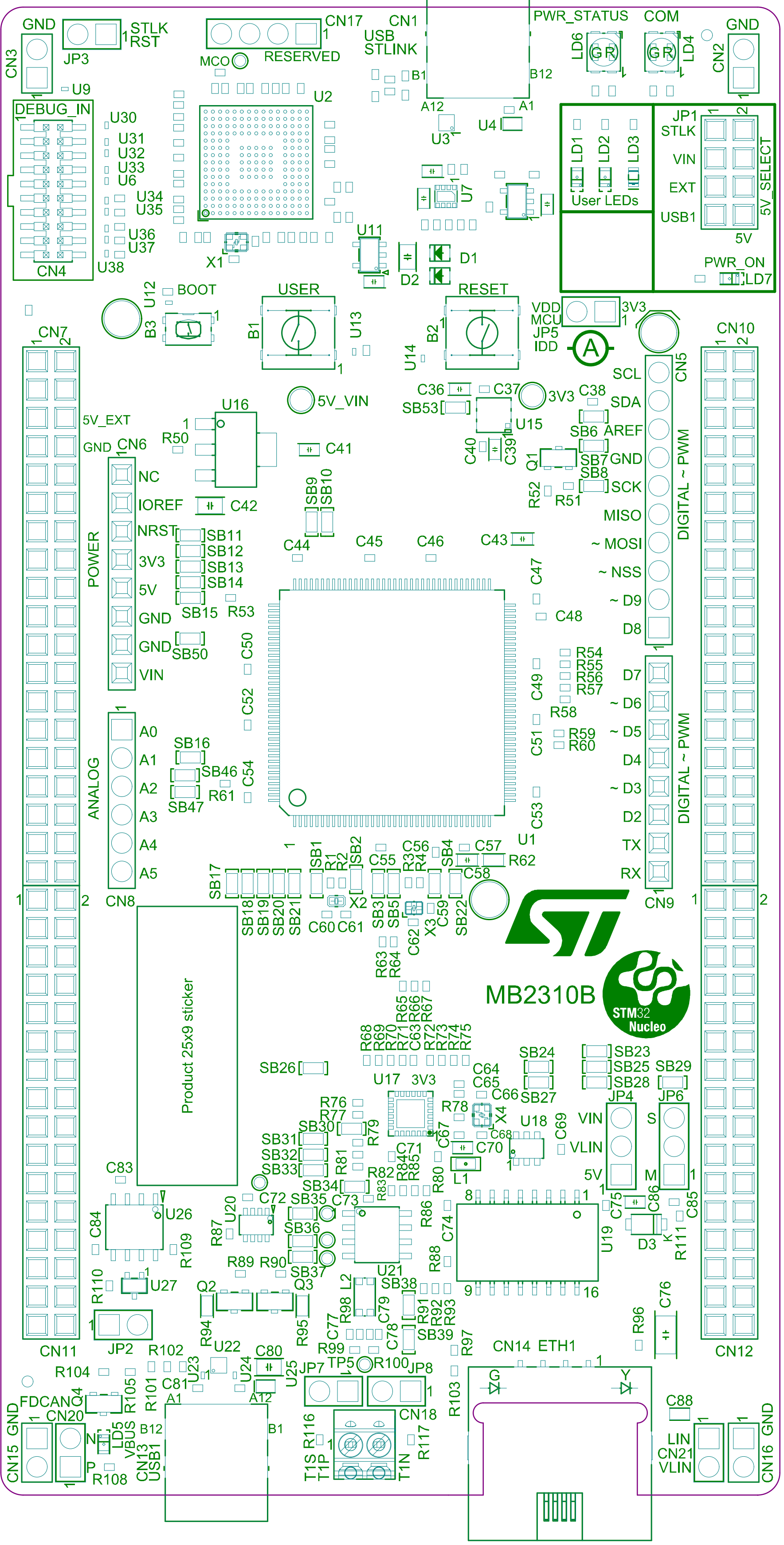
Title: **EXTERNAL DEBUG INTERFACES**		
Project: **NUCLEO-144 STM32C5 series**		
Variant: C5A3ZG		
Revision: B-02		Reference: MB2310
Size: A4	Date: 2025-Dec-11	Sheet: 16 of 16



Project: NUCLEO-144 STM32C5 series	
Layer: M14-Top Assembly	Gerber: .GM14
Variant: [No Variations]	MB2310
Date: 2025-Dec-11	Rev: B



Project: NUCLEO-144 STM32C5 series	
Layer: M15-Bottom Assembly	Gerber:.GM15
Variant: [No Variations]	MB2310
Date: 2025-Dec-11	Rev: B



Top Overlay

Top Assembly

.GTO

GND GND

R115

CN10 2 1

CN7 2 1

SCL
SDA
AREF
GND
SCK
MISO
MOSI ~
NSS ~
D9 ~
D8

DIGITAL ~ PWM

SB49 SB48

D7
D6 ~
D5 ~
D4
D3 ~
D2
TX
RX

DIGITAL ~ PWM

SB44 SB45 SB42 SB43

C82

CN19

1

M.2 Serial Memory

POWER

NC
IOREF
NRST
3V3
5V
GND
GND
VIN

ANALOG

A0
A1
A2
A3
A4
A5

C87

U29

U28

R112 SB51

SB52

CN12 ETH1 CN11

GND LIN SB40 SB41 T1S GND

USB1 FDCAN

M15-Bottom Assembly .GM15

Bottom Overlay