NUCLEO-64 STM32H5/STM32C5 series

MB2213 -C562RE

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U_Top
Top.SchDoc

HW1
STICKER PRODUCT
N/A

HW5
PCB
MB2213

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

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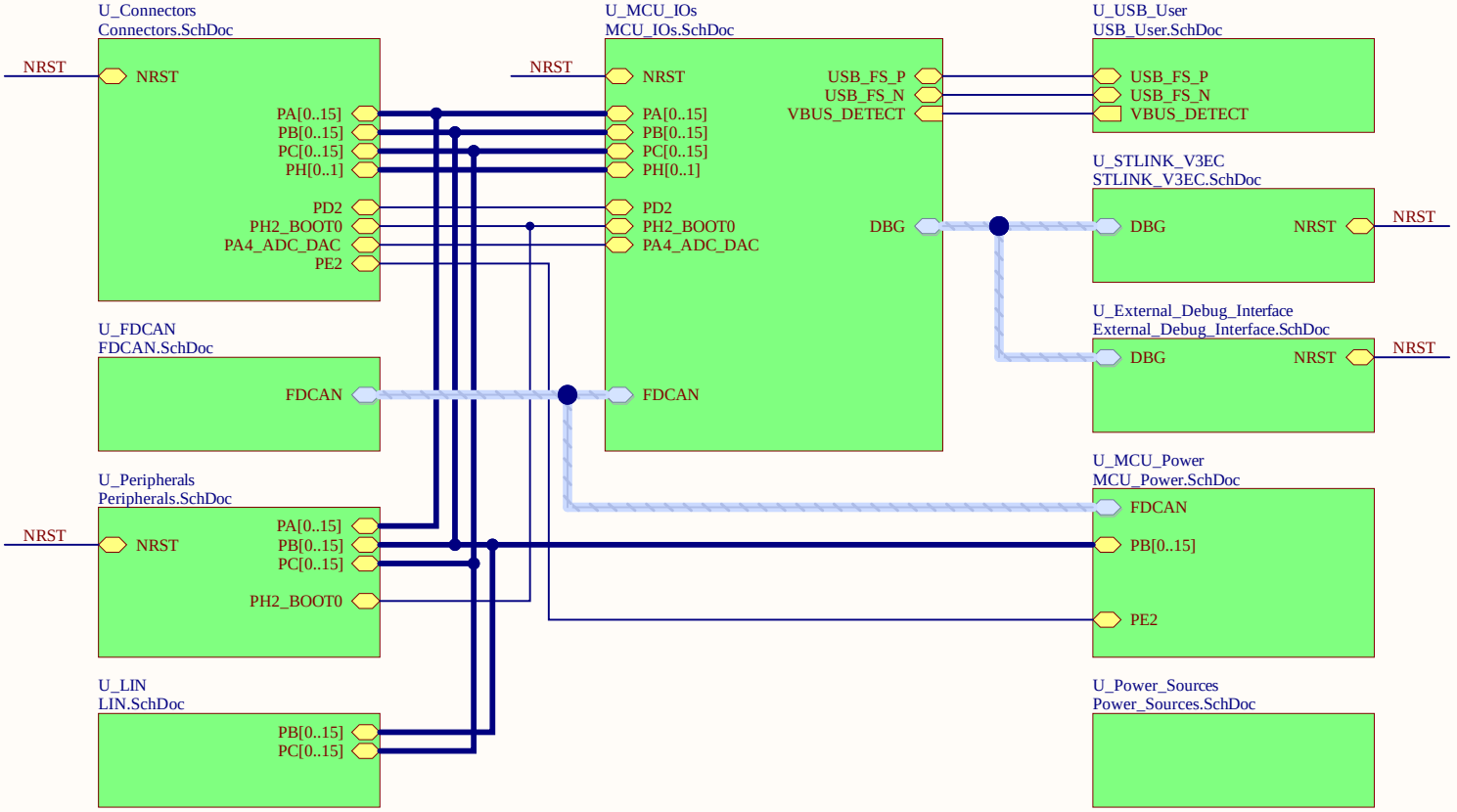
Title: **Project Overview**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
Variant: C562RE		
Revision: B-02		Reference: MB2213
Size: A4	Date: 2025-Nov-21	Sheet: 1 of 12



FID HW9 FID HW10
FID HW11 FID HW12

Title: **Top**		
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HARNESS

DBG

MCO	DBG.MCO	
SWDIO	DBG.SWDIO	PA13
SWO	DBG.SWO	PB3
SWCLK	DBG.SWCLK	PA14
JTDI	DBG.JTDI	PA15
VCP_TX	DBG.VCP_TX	PA2/PA4
VCP_RX	DBG.VCP_RX	PA3

FDCAN

TX	FDCAN.TX	PB9
RX	FDCAN.RX	PB8
STBY	FDCAN.STBY	PE2

32.768 KHz LSE

PC14 — DNF — SB1

C20 8.2pF — R1 0R — OSC32_IN

X2 32.768kHz

C19 8.2pF — R2 0R — OSC32_OUT

PC15 — DNF — SB2

24 MHz HSE

DBG.MCO — DNF — SB5

PH0 — DNF — SB3

C21 1.8pF — R3 0R — OSC_IN

X3 24MHz

C18 1.8pF — R4 0R — OSC_OUT

PH1 — DNF — SB4

MCU IOs

U1A

MCU_IOs

	PA0	14	PB0	26	PB0
	PA1	15	PB1	27	PB1
USART2_TX	PA2	16	PB2	28	PB2
USART2_RX/3_RX	PA3	17	(JTDO/TRACESWO) PB3	55	DBG.SWO — SB20 — PB3
USART3_TX / ADC / DAC	PA4	20	(NJTRST) PB4	56	PB4
	PA5	21	PB5	57	PB5
	PA6	22	PB6	58	PB6
	PA7	23	PB7	59	PB7
	PA8	41	PB8	61	PB8 — SB36 — FDCAN.RX
	PA9	42			
	PA10	43	PB10	29	PB10
PA11 — SB23	USB_FS_N	44			
PA12 — SB25	USB_FS_P	45	PB12	33	PB12
PA13 — SB14	DBG.SWDIO	46	PB13	34	PB13
PA14 — SB16	DBG.SWCLK	49	PB14	35	PB14
PA15 — SB18	DBG.JTDI R16 0R	50	PB15	36	PB15
	PC0	8			
	PC1	9			
	PC2	10	PD2	54	PD2
VBUS_DETECT — SB33	PC3	11			
	PC4	24			
	PC5	25			
	PC6	37			
	PC7	38			
	PC8	39			
	PC9	40			
	PC10	51			
	PC11	52			
	PC12	53			
	PC13	2			

MCU CLK & RST

3	PC14 - OSC32_IN	PH2-BOOT0	60 — PH2_BOOT0
4	PC15 - OSC32_OUT		
		NRST	7 — NRST
5	PH0 - OSC_IN		
6	PH1 - OSC_OUT		

STM32C562RET6

HW3 DNF Socket_LQFP64

VCP ON USART2 USED FOR H533 and C5xx configuration
VCP ON USART3 USED FOR H503 configuration

VCP on USART2 VCP on PA2/PA3

VCP on USART3 VCP on PA3/PA4

PA3 — SB12 — DBG.VCP_RX

PA2 — SB26 — DBG.VCP_TX

PA4 — DNF SB46 — DBG.VCP_TX

PA4 — SB24 — PA4_ADC_DAC

PA[0..15] PA[0..15]
PB[0..15] PB[0..15]
PC[0..15] PC[0..15]
PH[0..1] PH[0..1]

PD2 PD2
USB_FS_N USB_FS_N
USB_FS_P USB_FS_P
VBUS_DETECT VBUS_DETECT

PA4_ADC_DAC PA4_ADC_DAC
PH2_BOOT0 PH2_BOOT0
NRST NRST

Title: **MCU IOs**		
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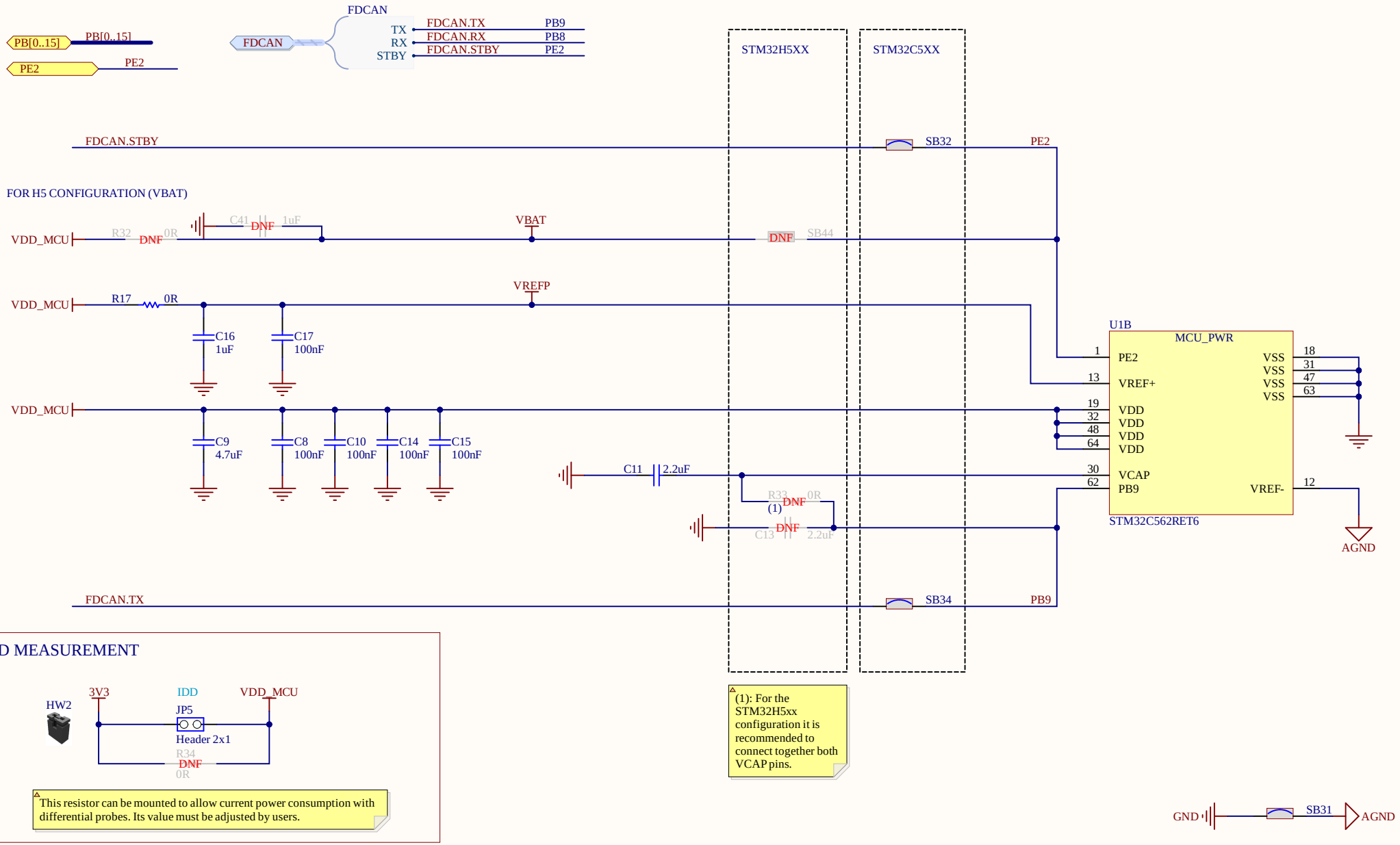
MCU POWER SUPPLY



(1): For the STM32H5xx configuration it is recommended to connect together both VCAP pins.

IDD MEASUREMENT

This resistor can be mounted to allow current power consumption with differential probes. Its value must be adjusted by users.

Title: **MCU Power**		
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CONNECTORS

PA[0..15] PB[0..15] PC[0..15] PD2 PE2 PH[0..1]

PH2_BOOT0 NRST

ST-MORPHO CONFIGURATION

UART 4 WIRES NOT SUPPORTED
SDIO INTERFACE DEPEND OF THE STM32 PROVIDED WITH THE NUCLEO
PC9: SPI_CS: BECAUSE OF MUXING IT IS NOT POSSIBLE TO HAVE THE SPI_NSS FUNCTION. SPI_CS IS AVAILABLE BY DRIVING A STANDARD GPIO

H5 CONFIGURATION: PB14 IS SHARED BETWEEN ARD_D1 (UART) AND TIM1_CH2N FOR MOTOR CONTROL
H5 CONFIGURATION: PB15 IS SHARED BETWEEN ARD_D0 (UART) AND TIM1_CH3N FOR MOTOR CONTROL
H5 CONFIGURATION: H5-512K: TIM_VH IS REPLACE BY TIM8_CH2
H5 CONFIGURATION: H5-512K: TIM_WH IS REPLACE BY TIM8_CH3

TIMx_CHy: x AND y DEPEND OF THE STM32 PROVIDED WITH THE NUCLEO
ADCx_INy: x AND y DEPEND OF THE STM32 PROVIDED WITH THE NUCLEO

COLOR LEGEND

ST-MORPHO SPECIFICATION
ARDUINO SPECIFICATION
STM32 ALTERNATE FUNCTION
STM32 IO PORT
~~FUNCTION NOT AVAILABLE~~

ARDUINO HOLES

H1 H2 H3

ARDUINO V3

Operating range: 3V < VCC < 3.6V

ST MORPHO CONNECTOR LEFT SIDE

CN7 — Header 19x2

PC10	SDIO_DAT2 / I2S_CK		1 2	4	SDIO_DAT3 / I2S_SDI	PC11
PC12	SDIO_CLK / I2S_SDO	3	3 4	6	SDIO_CMD	PD2
3V3	3V3	5	5 6	8	5V_EXT (2)	5V_EXT
PH2_BOOT0	BOOT0	7	7 8	10	~~GPIO~~	
PA2	GPIO	9	9 10	12	IOREF	
PA3	GPIO	11	11 12	14	NRST	NRST
PA13	SWDIO	13	13 14	16	3V3	
PA14	SWCLK	15	15 16	18	5V	
PA15	JTDI/TIM2_CH1 (H1) /I2S_WS	17	17 18	20	GND	
	GND	19	19 20	22	GND	
PE2	GPIO	21	21 22	24	VIN	
PC13	WKUPx	23	23 24	26	~~GPIO~~	
PC14	LSE_IN	25	25 26	28	ADCx_INy	PA0
PC15	LSE_OUT	27	27 28	30	ADCx_INy	PA1
PH0	HSE_IN	29	29 30	32	ADCx_INy / DACx_OUTy	PB1/PA4
PH1	HSE_OUT	31	31 32	34	ADCx_INy	PB0
	VBAT	33	33 34	36	ADCx_INy	PC1/PC5
VBAT	ADCx_INy / SPIB_MISO	35	35 36	38	ADCx_INy	PC0
PC2	ADCx_INy / SPIB_MOSI	37	37 38			

3V3 3V3 5V 3V3 VIN 5V_VIN

R5 1K

CN6 — Socket 8x1 — POWER

1	NC	
2	IOREF	
3	NRST	
4	3V3	(3)
5	5V	(3)
6	GND	
7	GND	
8	VIN	(1)

CN8 — Socket 6x1 — ANALOG

1	A0	ARD_A0
2	A1	ARD_A1
3	A2	ARD_A2
4	A3	ARD_A3
5	A4	ARD_A4
6	A5	ARD_A5

ST MORPHO CONNECTOR RIGHT SIDE

VREFP

DNF SB13

C12 100nF

CN5 — Socket 10x1 — DIGITAL ~ PWM

SCL	10	PB6	I2C/I3C_SCL	
SDA	9	PB7	I2C/I3C_SDA	
AREF	8	AREF		
GND	7			
SCK	6			
MISO	5			
~ MOSI	4	PA5	SPI1_SCK	SHARED WITH LED1
~ NSS	3	PA6	SPI1_MISO	
~ D9	2	PA7	SPI1_MOSI / TIMx_CHy	
D8	1	PC9	SPI1_CS / TIMx_CHy	ARD_D10

CN9 — Socket 8x1 — DIGITAL ~ PWM

D7	8	PC6	TIMx_CHy	
~ D6	7	PC7/PA9	TIM1_CH2	ARD_D8
~ D5	6	PA8	TIM1_CH1	
D4	5	PB10	TIM2_CH3	
~ D3	4	PB4	TIMx_CHy	ARD_D4
D2	3	PB3	TIM2_CH2 / SWO	ARD_D2
TX	2	PB5/PC1	WKUPx	ARD_D1
RX	1	PC8/PA10	TIM1_CH3	ARD_D0

CN10 — Header 19x2

CN10_1	SDIO_DAT1 / LINA_RX		1 2	4	SDIO_DAT0 / LINA_TX	PA9/PC8 CN10_2
	I2C_SCL	3	3 4	6	GPIO	PA10/PC7 CN10_4_GPIO
	I2C_SDA	5	5 6	8	GPIO	PC5/PB5 CN10_6_GPIO
	AREF (2)	7	7 8	10	5V_STLK (3)	5V_STLK
	GND	9	9 10	12	~~GPIO~~	
	SPIA_SCK	11	11 12	14	USB_DP / FDCANA_TX	PA12
	SPIA_MISO	13	13 14	16	USB_DM / FDCANA_RX	PA11
	SPIA_MOSI	15	15 16	18	TIM1_BKIN / FDCANB_RX	PB12
	SPIA_NSS	17	17 18	20	ADCx_INy	CN10_18_ADC
	GPIO	19	19 20	22	GND	
	TIM1_CH2 (VH)	21	21 22	24	GPIO	PB2
	TIM1_CH1 (UH)	23	23 24	26	~~GPIO~~	
	TIM2_CH3 (H3)	25	25 26	28	TIM1_CH3N (WL)	PB15
TIM_CUR-REF / LINB_RX		27	27 28	30	TIM1_CH2N (VL)	PB14
	GPIO	29	29 30	32	TIM1_CH1N (UL) / SPIB_SCK / FDCANB_TX	PB13
TIM2_CH2 (H2) / SWO / LINB_TX		31	31 32	34	AGND	AGND
	TIM1_CH3 (WH)	33	33 34	36	ADCx_INy	PC4
	UART_TX	35	35 36	38	GPIO / ~~UART2_RFS~~	CN10_36_GPIO
	UART_RX	37	37 38		~~GPIO / UART2_CTS~~	

H5 IO SETTING / C5 IO SETTING

PC1	DNF	SB47	SB30	ARD_A4	ARD_D4
PC5	DNF	SB43	SB27		CN10_6_GPIO
PB5	DNF	SB42	SB22		
PA4_ADC_DAC	NOT CONNECTED		SB28	ARD_A2	
PB1	DNF	SB45	SB29		CN10_18_ADC
PB15	SB49				ARD_D0 UART_RX
PB8 SHARED WITH FDCAN	DNF	SB50	SB37 DNF		CN10_36_GPIO
PB14	SB48				ARD_D1 UART_TX
PB9 SHARED WITH FDCAN			SB35 DNF		
PC7	DNF	SB41	SB21		ARD_D8
PC8	DNF	SB40	SB19		ARD_D2
PA9	DNF	SB39	SB17		CN10_4_GPIO
PA10	DNF	SB38	SB15		CN10_2
PC9			SB11		ARD_D10
			SB9 DNF		CN10_1

OPTIONAL CONFIGURATION FOR DESIGN SUPPORTING SDIO INTERFACE

(1): VIN (NUCLEO INPUT) WARNING voltage applied to 7V < VIN < 12V
(2): 5V_EXT, AREF (NUCLEO INPUT)
(3): 5V, 3V3, IOREF, 5V_STLK (NUCLEO OUTPUT, SHIELD INPUT)

Title: **Connectors**		
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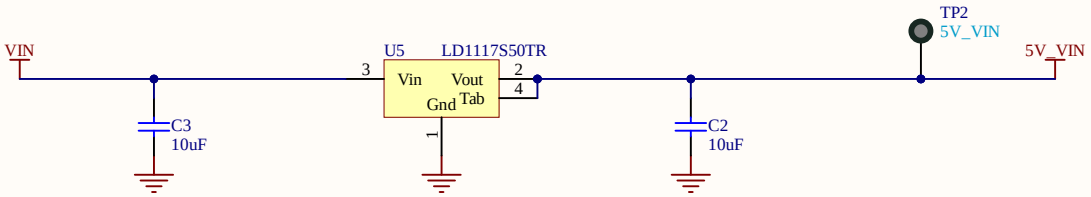
POWER SOURCES

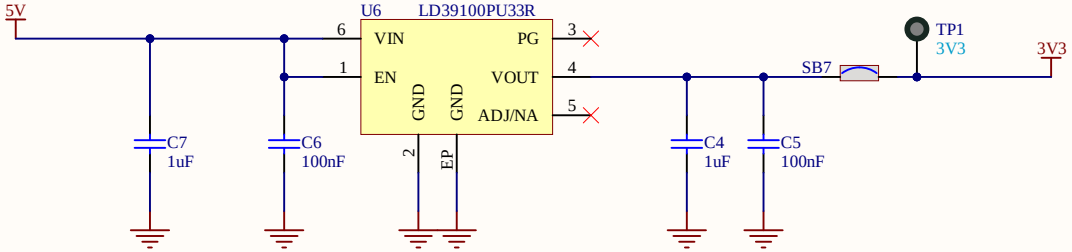
VIN / 5V PWR/ 800mA

Operating range: 7V < VIN < 12V

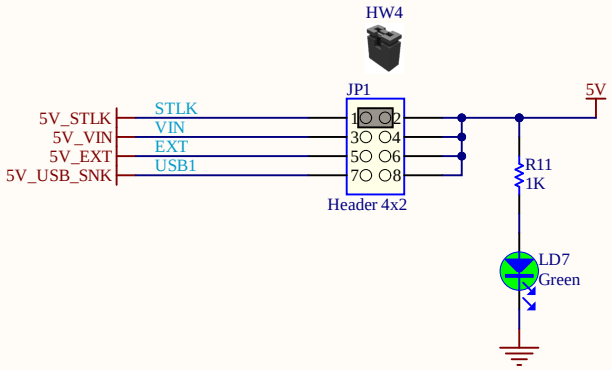


3V3 PWR/ 1A

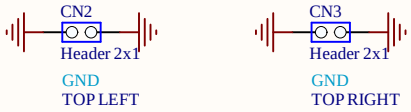
Operating range: 4.5V < VI < 5.5V



5V PWR SELECTION



GND HEADERS



Title: **Power Sources**		
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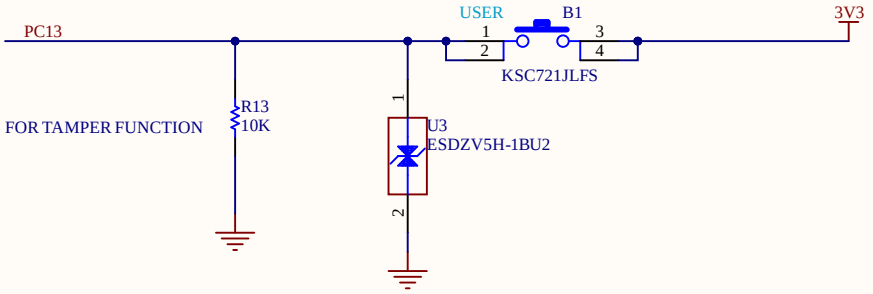
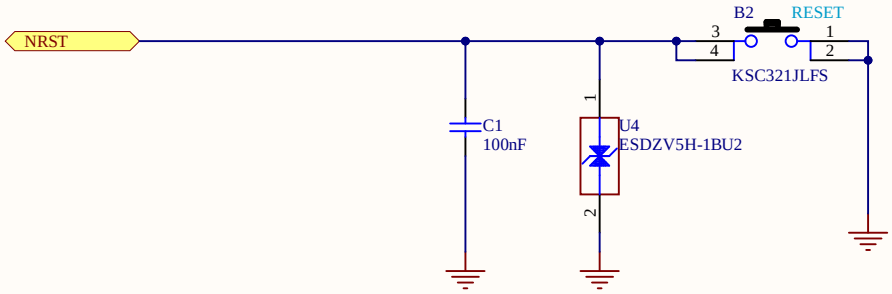
PERIPHERALS

PA[0..15] — PA[0..15]
PB[0..15] — PB[0..15]
PC[0..15] — PC[0..15]

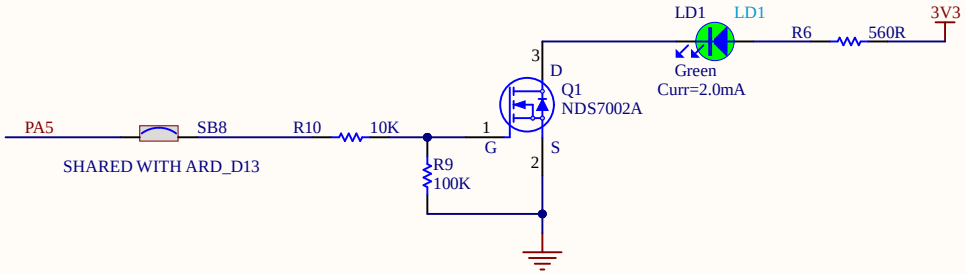
USER BUTTON



RESET



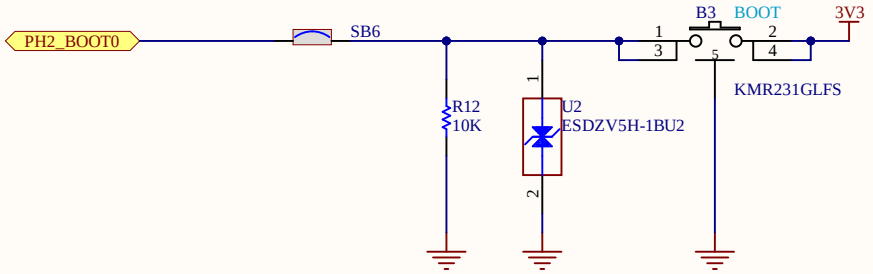
LED



BOOT SELECT

DEFAULT = INTERNAL FLASH

B3 PRESSED = BOOTLOADER



Title: **Peripherals**		
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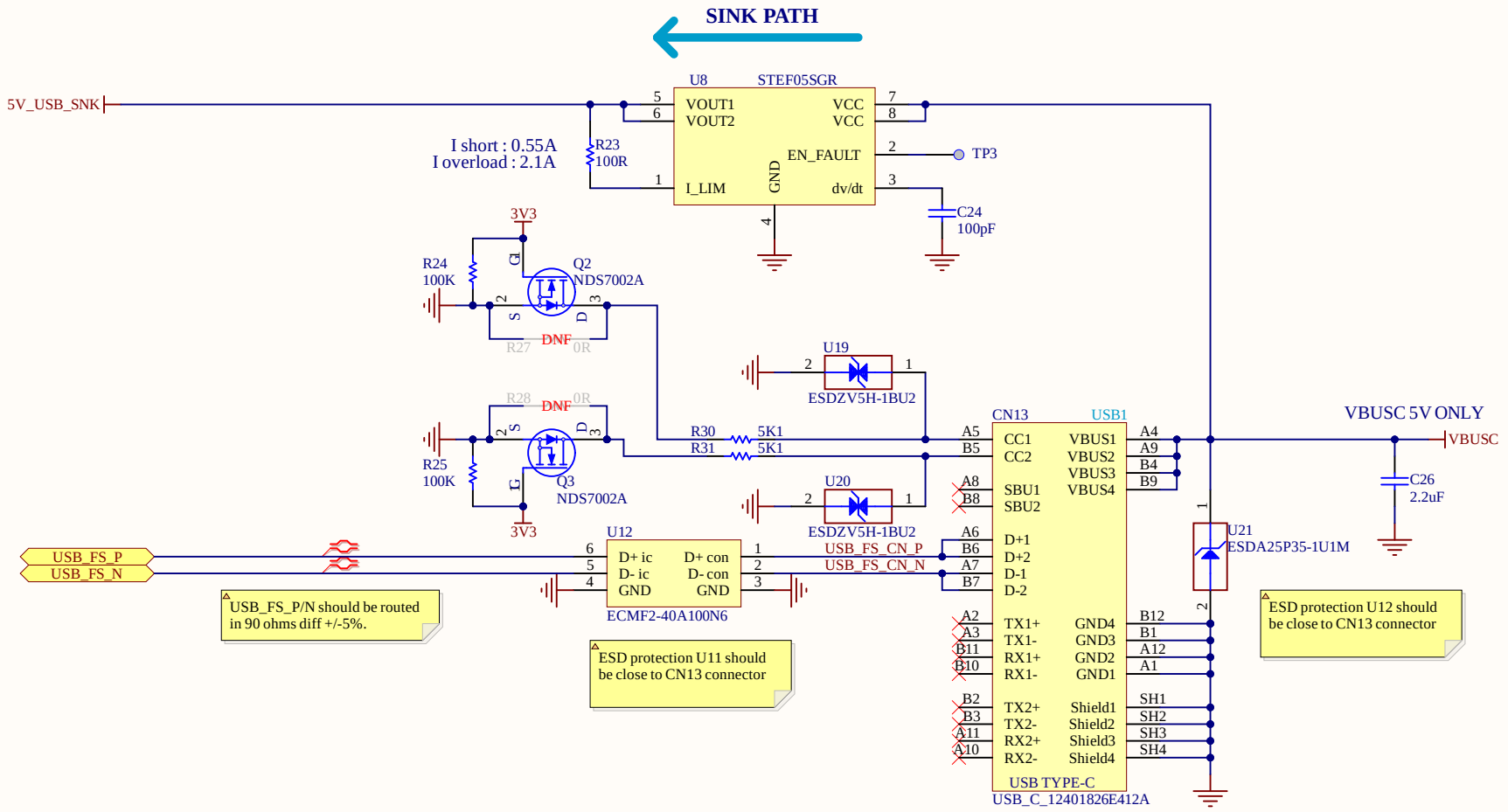
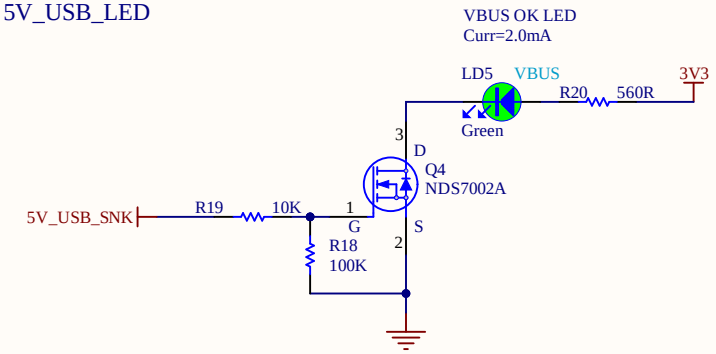
USB User

USB Type-C, SINK Only

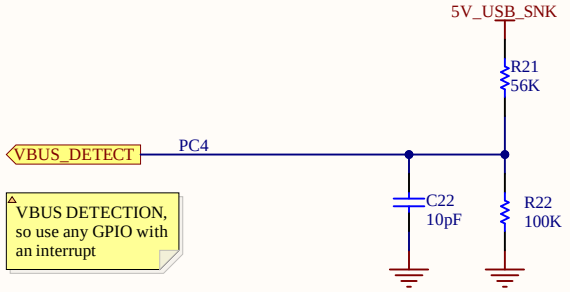
2.5W / 5V / 500mA



5V_USB_LED



VBUS_DETECTION



FOR DEBUG PURPOSE

Title: **USB User**		
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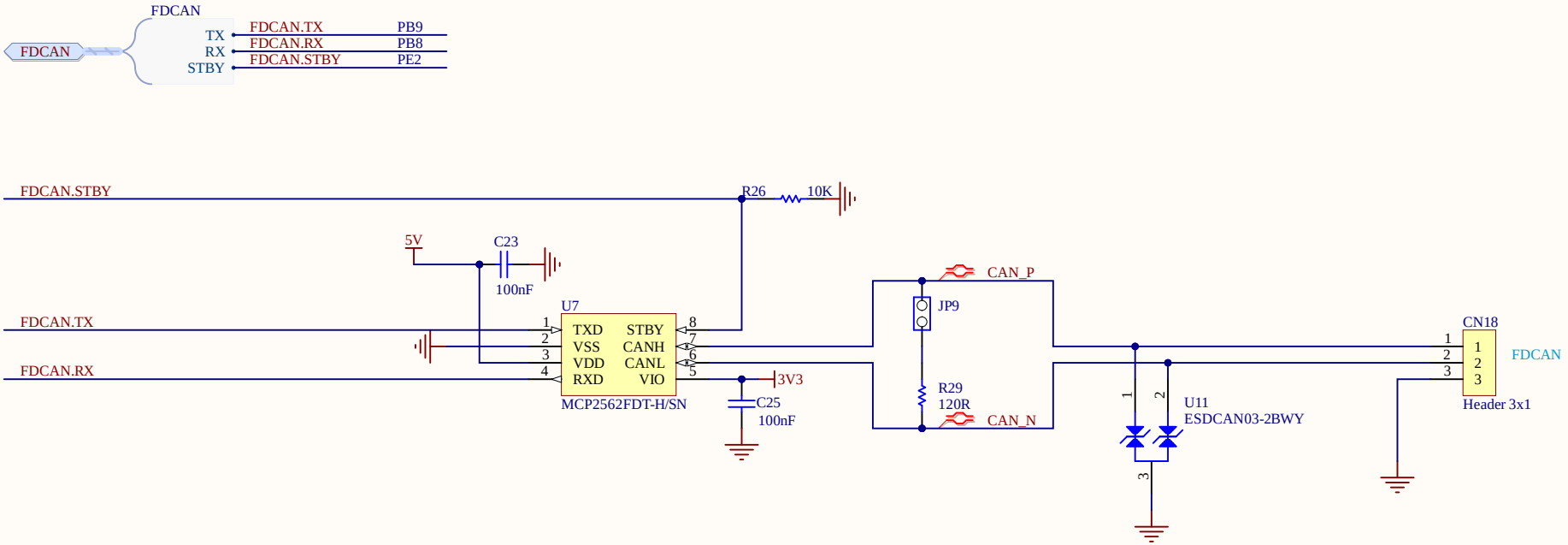
CAN FD

Operation Volatage: VDD: 4.5 ~ 5.5V; VIO: 1.8 ~ 5.5V



Title: **FDCAN**			
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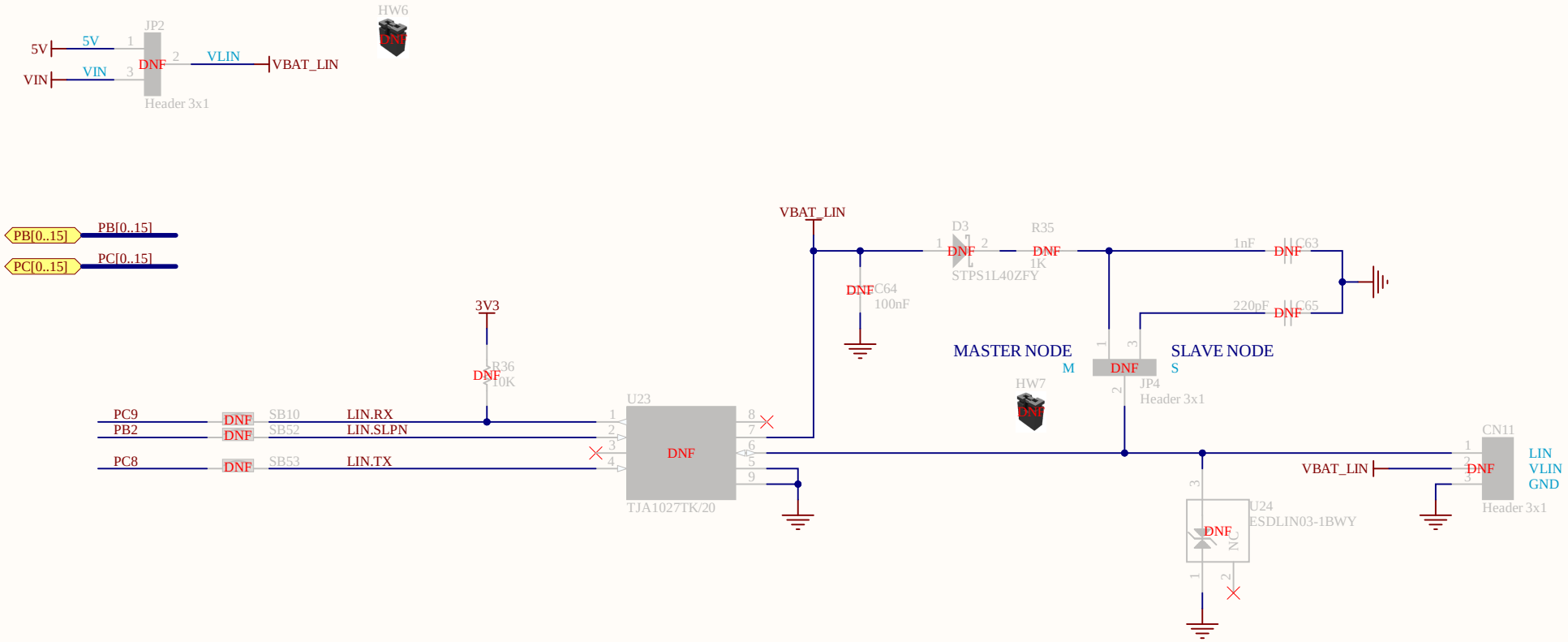
LIN

Operation Voltage: VBAT: 5 ~ 18V
Operation Voltage: VIN: 7 ~ 12V

If VBAT < 5 V, the TJA1027 may remain operational, but parameter values cannot be guaranteed to remain within the operation ranges specified in datasheet



Title: **LIN**			
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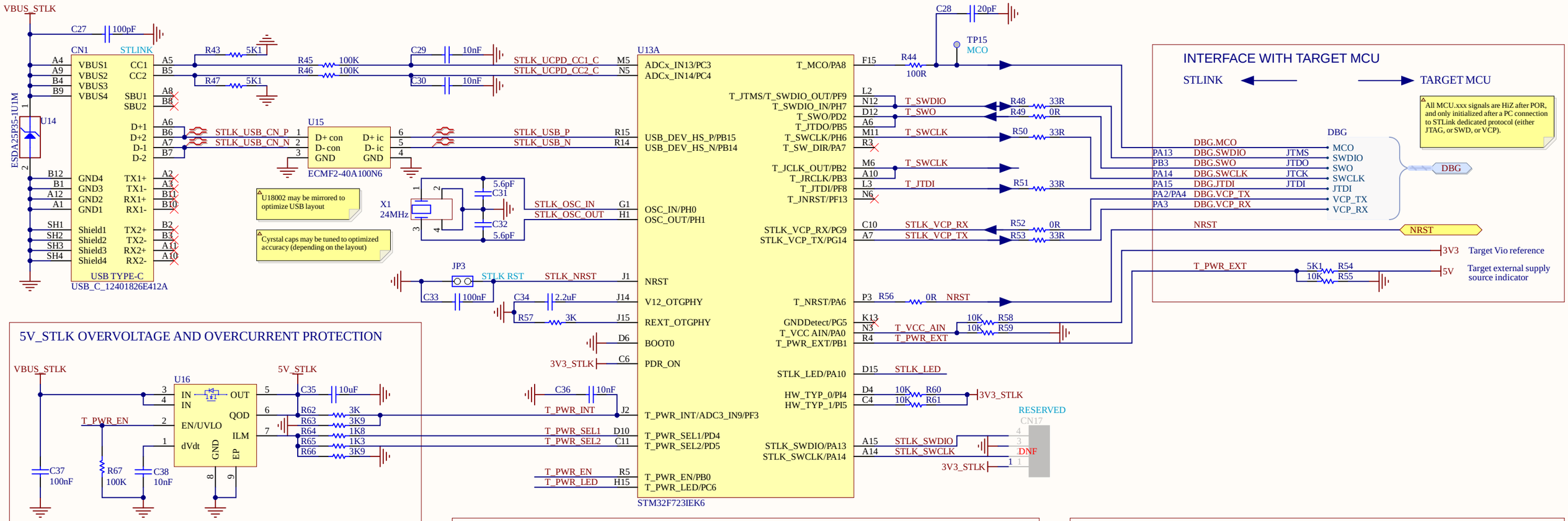
STLINK-V3EC



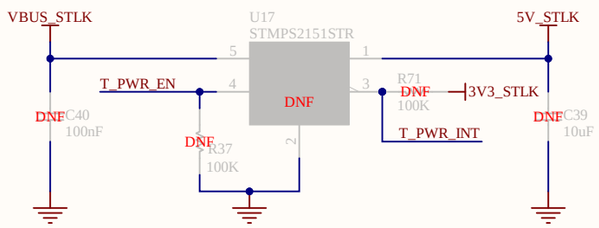
5V_STLK OVERVOLTAGE AND OVERCURRENT PROTECTION

5V_STLK OVERCURRENT PROTECTION MANAGEMENT

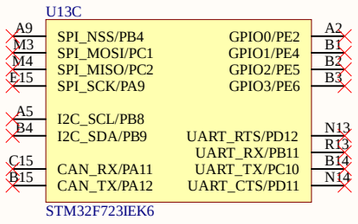
	T_PWR_SEL2/PD5	T_PWR_SEL1/PD4
PowerDefault.SNK *(current limit: 550mA)*	Hi-Z	Hi-Z
Power1.5.SNK *(current limit: 1.66A)*	Hi-Z	0
Power3.0.SNK *(current limit: 3.2A)*	0	0

Hi-Z = IO set in high impedance

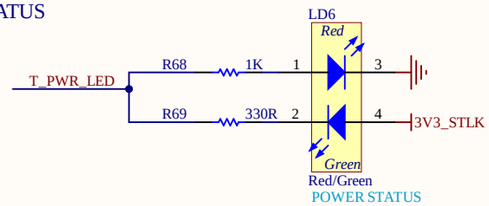
STMPS2151STR is backup of the TPS259535DSG



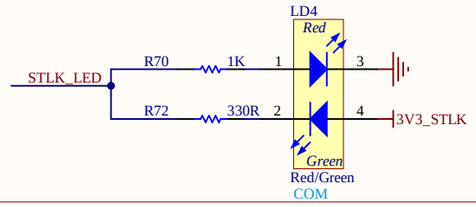
UNUSED PINS



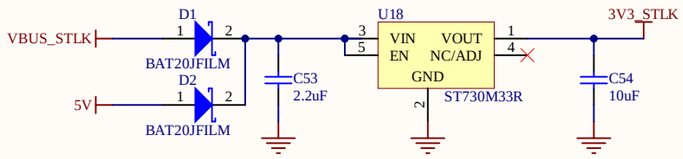
LED POWER STATUS



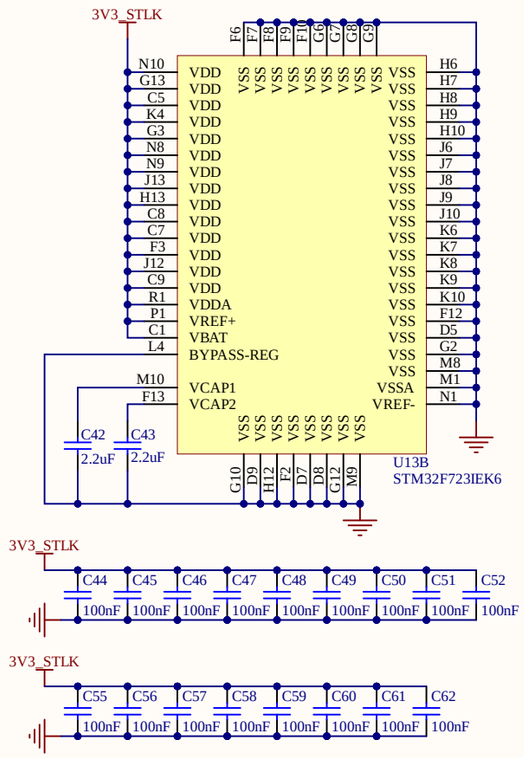
LED STLINK



ST-LINK POWER (3V3/300mA)



STLINK MCU POWER



Title: **STLINK-V3EC**		
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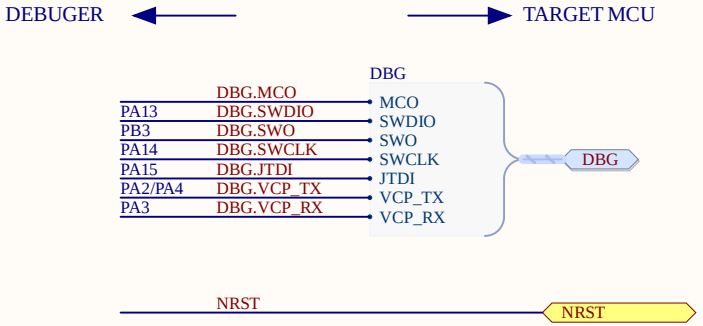
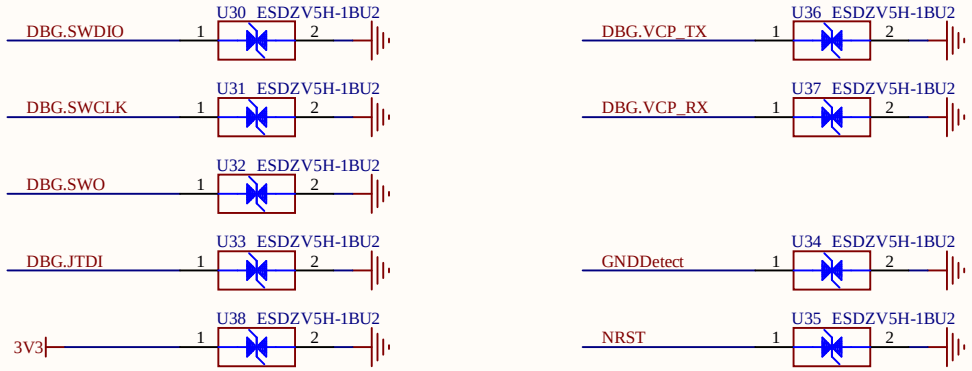
EXTERNAL DEBUGER INTERFACES

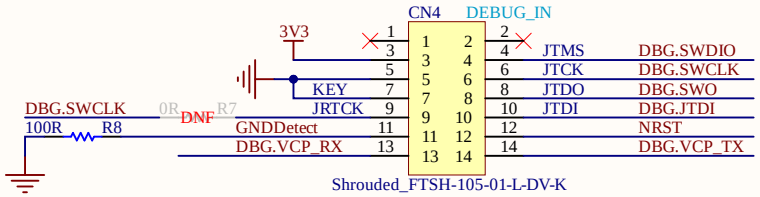
INTERFACE WITH TARGET MCU



ESD PROTECTIONS

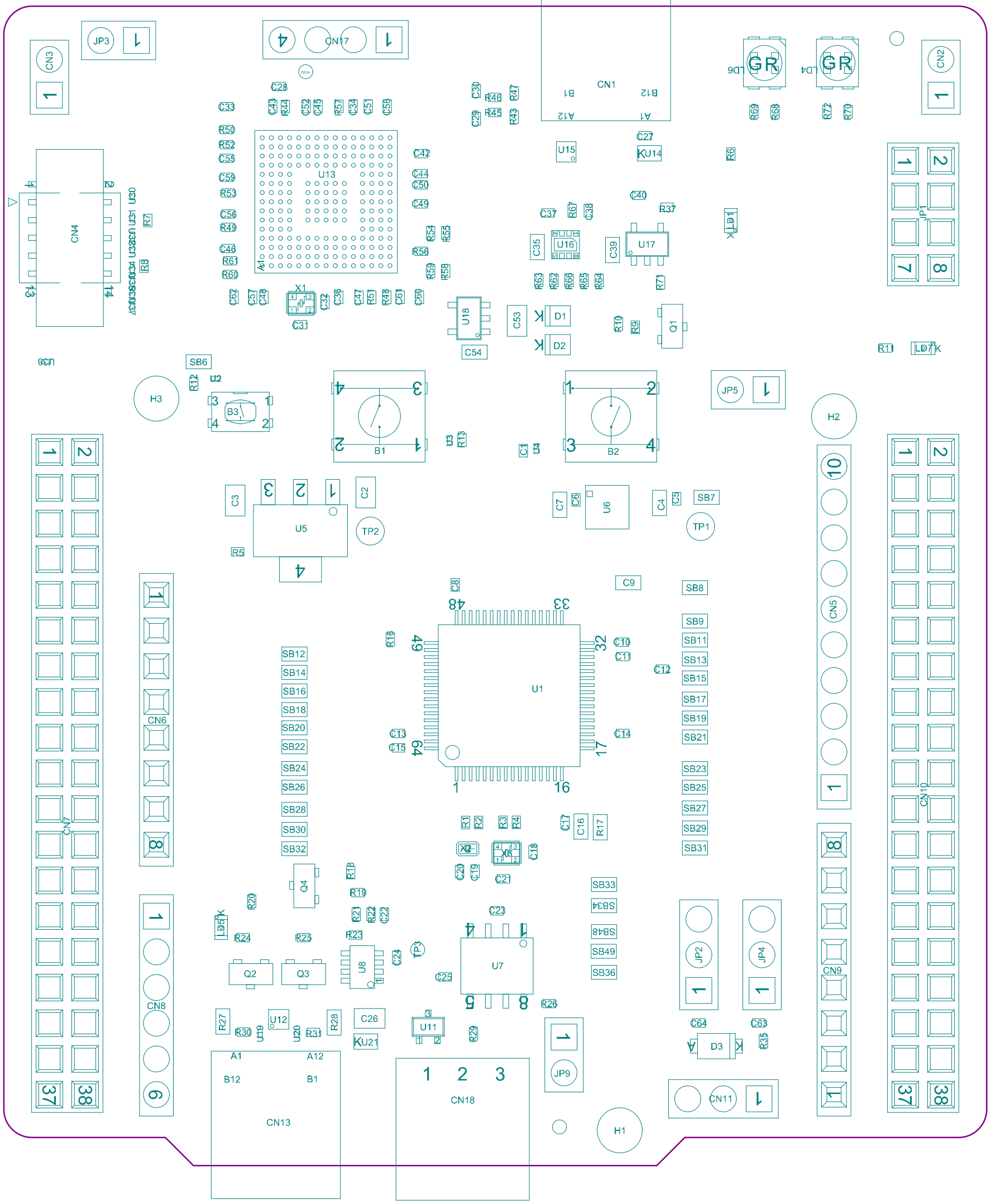


STDC14 RECEIVER

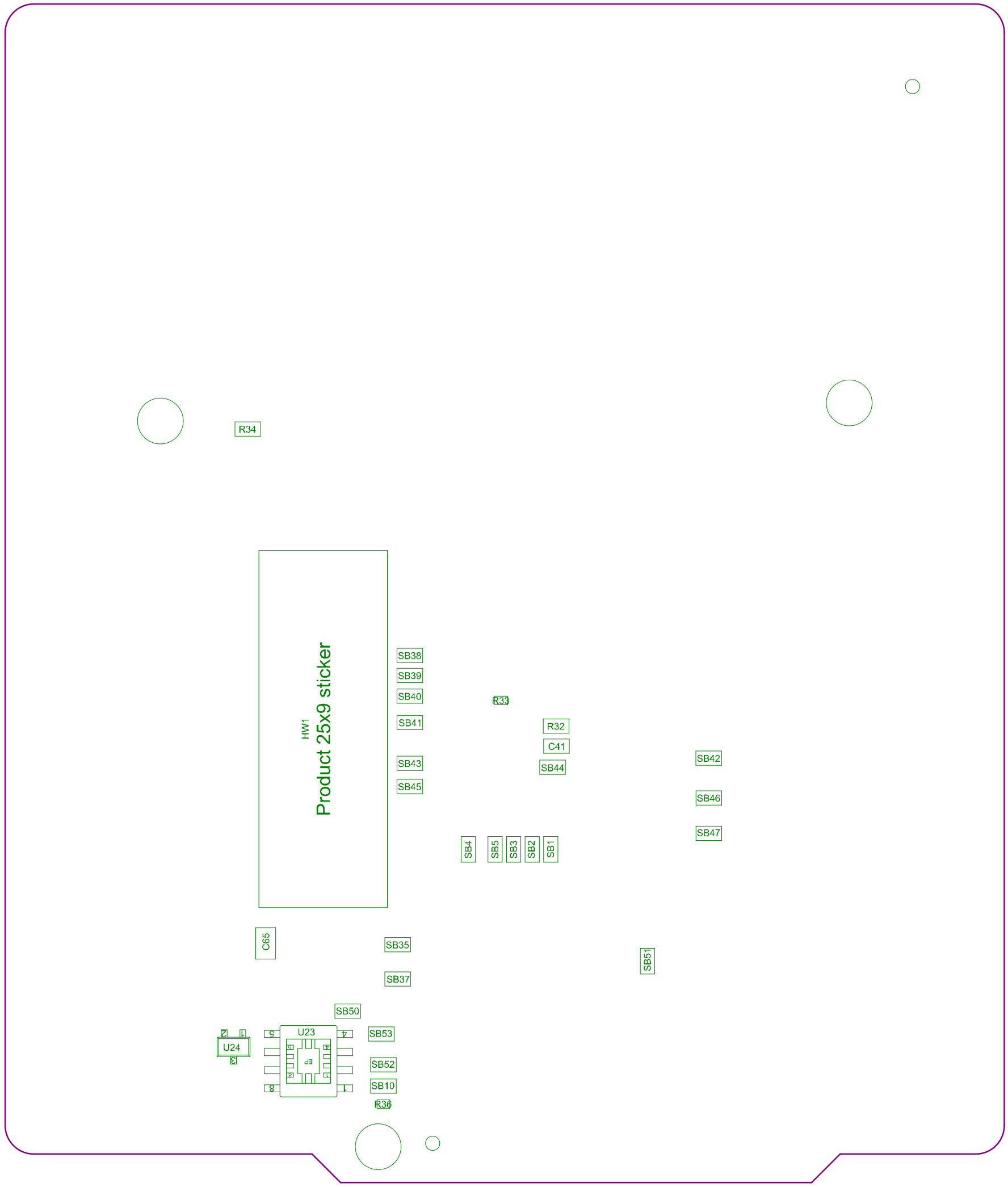


JRTCK is connected to MCU.SWCLK for compatibility with some debug probes

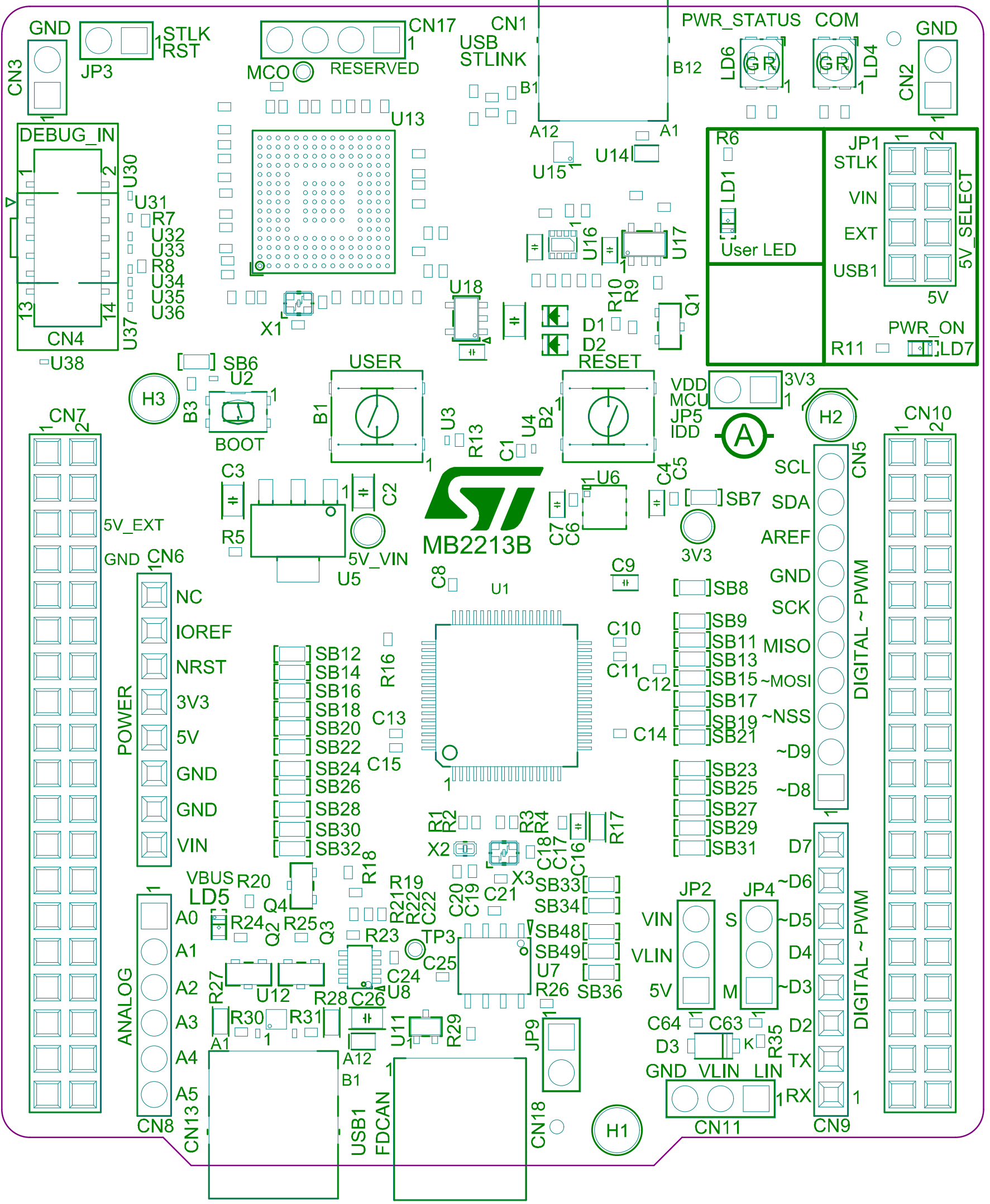
Title: **External_Debug_Interface**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
Variant: C562RE		
Revision: B-02		Reference: MB2213
Size: A4	Date: 2025-Nov-21	Sheet: 12 of 12



Project: NUCLEO-64 STM32H5/STM32C5 series	
Layer: M14-Top Assembly	Gerber: .GM14
Variant: [No Variations]	MB2213
Date: 2025-Nov-21	Rev: B



Project: NUCLEO-64 STM32H5/STM32C5 series	
Layer: M15-Bottom Assembly	Gerber:.GM15
Variant: [No Variations]	MB2213
Date: 2025-Nov-21	Rev: B



Top Overlay

Top Assembly

.GTO

GND GND

STM32 Nucleo

R34

SCL
SDA
AREF
GND
SCK
MISO
~MOSI
~NSS
~D9
~D8
D7
~D6
~D5
D4
~D3
D2
TX
RX

HW1

Product 25x9 sticker

SB38 SB39 SB40 SB41 R33
R32 C41
SB43 SB44 SB45
SB42 SB46 SB47
SB4 SB5 SB3 SB2 SB1
SB35 SB37
SB51
C65 U23 U24
SB50 SB53 SB52
R36 SB10

NC
IOREF
NRST
3V3
5V
GND
GND
VIN
A0
A1
A2
A3
A4
A5

LIN FDCAN USB1

PYx PYx PYx 5V STLK PYx PA12 PA11 PB12 PYx GND PB2 PYx PB15 PB14 PB13 AGND PC4 PYx PYx PYx

PYx PB6 PB7 AREF GND PA5 PA6 PA7 PYx PC6 PYx PA8 PB10 PB4 PYx PB3 PYx PYx PYx

PC11 PD2 5V_EXT GND PYx IOREF NRST 3V3 5V GND GND VIN PYx PA0 PA1 PYx PB0 PYx PC0

PC10 PC12 3V3 PH2 BOOT PA2 PA3 PA13 PA14 PA15 GND PE2 PC13 PC14 PC15 PH0 PH1 VBAT PC2 PC3

M15-Bottom Assembly

Board Layer Stack Bottom Overlay.GM15