NUCLEO-64 STM32H5/STM32C5 series

MB2213 -C542RC

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U_Top
Top.SchDoc

HW1
STICKER PRODUCT
N/A

HW5
PCB
MB2213

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

Notes to generate the board layout.

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Title: **Project Overview**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
Variant: C542RC		
Revision: B-02		Reference: MB2213
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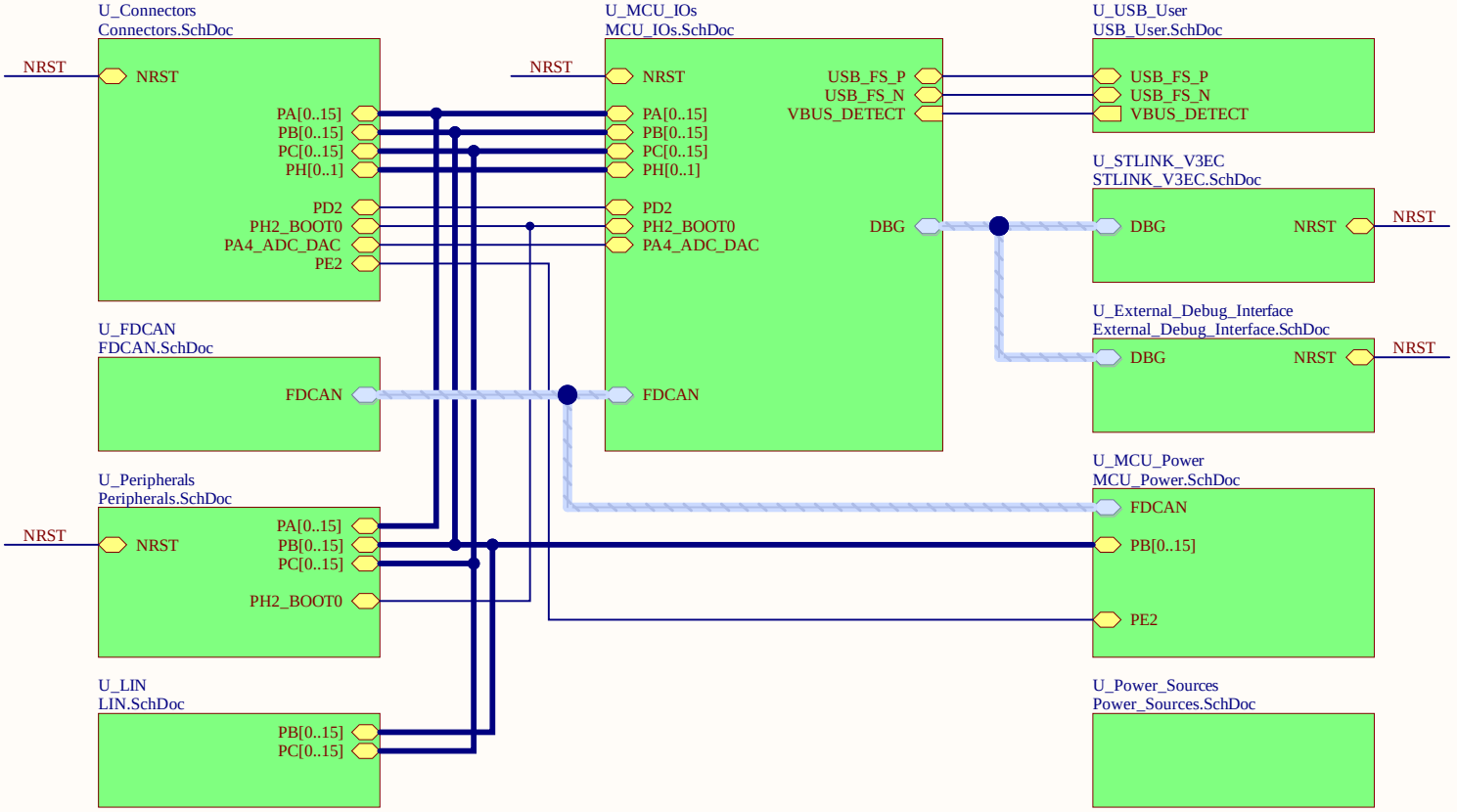

FID HW9
FID HW10
FID HW11
FID HW12

Title: **Top**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
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HARNESS

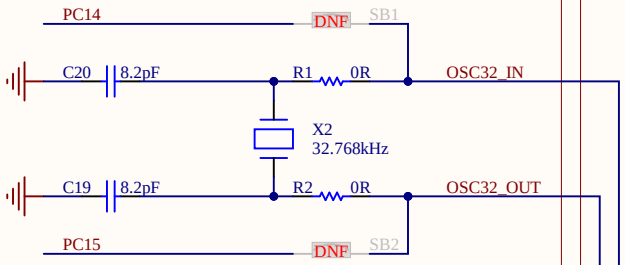
DBG

MCO	DBG.MCO	
SWDIO	DBG.SWDIO	PA13
SWO	DBG.SWO	PB3
SWCLK	DBG.SWCLK	PA14
JTDI	DBG.JTDI	PA15
VCP_TX	DBG.VCP_TX	PA2/PA4
VCP_RX	DBG.VCP_RX	PA3

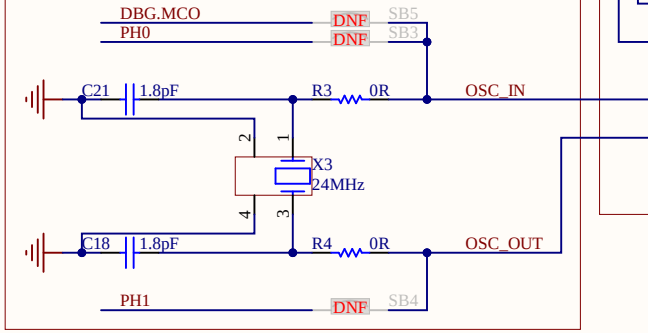
FDCAN

TX	FDCAN.TX	PB9
RX	FDCAN.RX	PB8
STBY	FDCAN.STBY	PE2

32.768 KHz LSE



24 MHz HSE



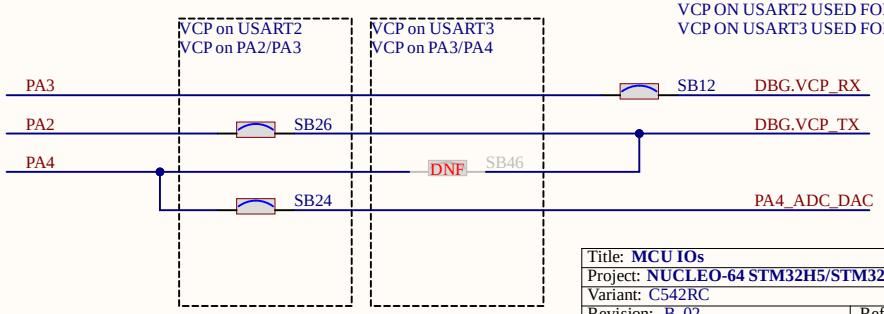
MCU IOs

U1A — STM32C542RCT6

		PA0	14		
		PA1	15		
USART2_TX		PA2	16		
USART2_RX/3_RX		PA3	17		
USART3_TX / ADC / DAC		PA4	20		
		PA5	21		
		PA6	22		
		PA7	23		
		PA8	41		
		PA9	42		
		PA10	43		
PA11	SB23	USB_FS_N	44		
PA12	SB25	USB_FS_P	45		
PA13	SB14	DBG.SWDIO	46		
PA14	SB16	DBG.SWCLK	49		
PA15	SB18	DBG.JTDI	R16 0R 50		
		PC0	8		
		PC1	9		
		PC2	10		
		PC3	11		
VBUS_DETECT	SB33	PC4	24		
		PC5	25		
		PC6	37		
		PC7	38		
		PC8	39		
		PC9	40		
		PC10	51		
		PC11	52		
		PC12	53		
		PC13	2		
		PC14 - OSC32_IN	3		
		PC15 - OSC32_OUT	4		
		PH0 - OSC_IN	5		
		PH1 - OSC_OUT	6		
		NRST	7		
		PB0	26	PB0	
		PB1	27	PB1	
		PB2	28	PB2	
		(JTDO/TRACESWO) PB3	55	DBG.SWO	SB20 PB3
		(NJTRST) PB4	56	PB4	
		PB5	57	PB5	
		PB6	58	PB6	
		PB7	59	PB7	
		PB8	61	PB8	SB36 FDCAN.RX
		PB10	29	PB10	
		PB12	33	PB12	
		PB13	34	PB13	
		PB14	35	PB14	
		PB15	36	PB15	
		PD2	54	PD2	
		PH2-BOOT0	60	PH2_BOOT0	

HW3 DNF Socket_LQFP64

VCP ON USART2 USED FOR H533 and C5xx configuration
VCP ON USART3 USED FOR H503 configuration



PA[0..15]	PA[0..15]	
PB[0..15]	PB[0..15]	
PC[0..15]	PC[0..15]	
PH[0..1]	PH[0..1]	
PD2	PD2	
USB_FS_N	USB_FS_N	
USB_FS_P	USB_FS_P	
VBUS_DETECT	VBUS_DETECT	
PA4_ADC_DAC	PA4_ADC_DAC	
PH2_BOOT0	PH2_BOOT0	
NRST	NRST	

Title: **MCU IOs**			
Project: **NUCLEO-64 STM32H5/STM32C5 series**			
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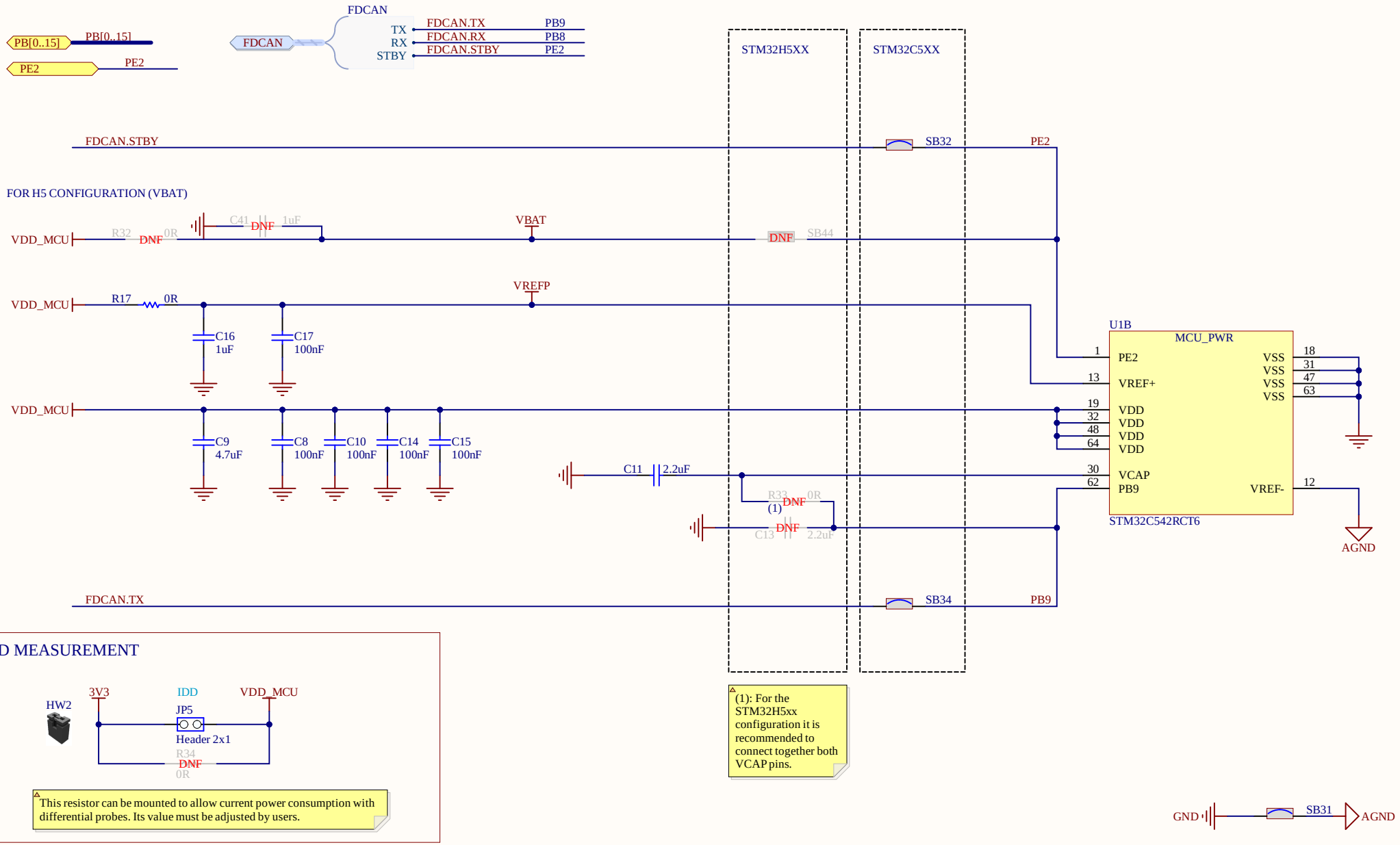
MCU POWER SUPPLY



IDD MEASUREMENT

This resistor can be mounted to allow current power consumption with differential probes. Its value must be adjusted by users.

(1): For the STM32H5xx configuration it is recommended to connect together both VCAP pins.

Title: **MCU Power**		
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CONNECTORS

PA[0..15] — PA[0..15]
PB[0..15] — PB[0..15]
PC[0..15] — PC[0..15]
PD2 — PD2
PE2 — PE2
PH[0..1] — PH[0..1]

PH2_BOOT0 — PH2_BOOT0
NRST — NRST

ST-MORPHO CONFIGURATION

UART 4 WIRES NOT SUPPORTED
SDIO INTERFACE DEPEND OF THE STM32 PROVIDED WITH THE NUCLEO
PC9: SPI_CS: BECAUSE OF MUXING IT IS NOT POSSIBLE TO HAVE THE SPI_NSS FUNCTION. SPI_CS IS AVAILABLE BY DRIVING A STANDARD GPIO

H5 CONFIGURATION: PB14 IS SHARED BETWEEN ARD_D1 (UART) AND TIM1_CH2N FOR MOTOR CONTROL
H5 CONFIGURATION: PB15 IS SHARED BETWEEN ARD_D0 (UART) AND TIM1_CH3N FOR MOTOR CONTROL
H5 CONFIGURATION: H5-512K: TIM_VH IS REPLACE BY TIM8_CH2
H5 CONFIGURATION: H5-512K: TIM_WH IS REPLACE BY TIM8_CH3

TIMx_CHy: x AND y DEPEND OF THE STM32 PROVIDED WITH THE NUCLEO
ADCx_INy: x AND y DEPEND OF THE STM32 PROVIDED WITH THE NUCLEO

COLOR LEGEND

ST-MORPHO SPECIFICATION
ARDUINO SPECIFICATION
STM32 ALTERNATE FUNCTION
STM32 IO PORT
~~FUNCTION NOT AVAILABLE~~

ARDUINO HOLES

H1 H2 H3

ARDUINO V3

Operating range: 3V < VCC < 3.6V

ST MORPHO CONNECTOR LEFT SIDE

CN7 — Header 19x2

PC10	SDIO_DAT2 / I2S_CK		1 2		SDIO_DAT3 / I2S_SDI	PC11
PC12	SDIO_CLK / I2S_SDO	3	3 4	4	SDIO_CMD	PD2
3V3	3V3	5	5 6	6	5V_EXT (2)	5V_EXT
PH2_BOOT0	BOOT0	7	7 8	8	GND	
PA2	GPIO	9	9 10	10	~~GPIO~~	
PA3	GPIO	11	11 12	12	IOREF	
PA13	SWDIO	13	13 14	14	NRST	NRST
PA14	SWCLK	15	15 16	16	3V3	
PA15	JTDI/TIM2_CH1 (H1) /I2S_WS	17	17 18	18	5V	
	GND	19	19 20	20	GND	
PE2	GPIO	21	21 22	22	GND	
PC13	WKUPx	23	23 24	24	VIN	
PC14	LSE_IN	25	25 26	26	~~GPIO~~	
PC15	LSE_OUT	27	27 28	28	ADCx_INy	PA0
PH0	HSE_IN	29	29 30	30	ADCx_INy	PA1
PH1	HSE_OUT	31	31 32	32	ADCx_INy / DACx_OUTy	PB1/PA4
VBAT	VBAT	33	33 34	34	ADCx_INy	PB0
PC2	ADCx_INy / SPIB_MISO	35	35 36	36	ADCx_INy	PC1/PC5
PC3	ADCx_INy / SPIB_MOSI	37	37 38	38	ADCx_INy	PC0

3V3 3V3 5V 3V3 VIN 5V_VIN

R5 1K

CN6 — Socket 8x1 — POWER

1	NC	
2	IOREF	
3	NRST	
4	3V3	(3)
5	5V	(3)
6	GND	
7	GND	
8	VIN	(1)

CN8 — Socket 6x1 — ANALOG

1	A0	ARD_A4
2	A1	
3	A2	ARD_A2
4	A3	
5	A4	
6	A5	

ST MORPHO CONNECTOR RIGHT SIDE

VREFP
DNF SB13
C12 100nF

CN5 — Socket 10x1 — DIGITAL ~ PWM

SCL	10	PB6	I2C/I3C_SCL	
SDA	9	PB7	I2C/I3C_SDA	
AREF	8	AREF		
GND	7			
SCK	6			
MISO	5			
~ MOSI	4	PA5	SPI1_SCK	SHARED WITH LED1
~ NSS	3	PA6	SPI1_MISO	
~ D9	2	PA7	SPI1_MOSI / TIMx_CHy	
D8	1	PC9	SPI1_CS / TIMx_CHy	ARD_D10

CN9 — Socket 8x1 — DIGITAL ~ PWM

D7	8	PC6	TIMx_CHy	
~ D6	7	PC7/PA9	TIM1_CH2	ARD_D8
~ D5	6	PA8	TIM1_CH1	
D4	5	PB10	TIM2_CH3	
~ D3	4	PB4	TIMx_CHy	
D2	3	PB5/PC1	WKUPx	ARD_D4
TX	2	PB3	TIM2_CH2 / SWO	
RX	1	PC8/PA10	TIM1_CH3	ARD_D2
		PB14/PB9		ARD_D1
		PB15/PB8		ARD_D0

CN10 — Header 19x2

CN10_1	SDIO_DAT1 / LINA_RX		1 2		SDIO_DAT0 / LINA_TX	PA9/PC8 CN10_2
	I2C_SCL	3	3 4		GPIO	PA10/PC7 CN10_4_GPIO
	I2C_SDA	5	5 6		GPIO	PC5/PB5 CN10_6_GPIO
	AREF (2)	7	7 8		5V_STLK (3)	5V_STLK
	GND	9	9 10		~~GPIO~~	
	SPIA_SCK	11	11 12		USB_DP / FDCANA_TX	PA12
	SPIA_MISO	13	13 14		USB_DM / FDCANA_RX	PA11
	SPIA_MOSI	15	15 16		TIM1_BKIN / FDCANB_RX	PB12
	SPIA_NSS	17	17 18		ADCx_INy	CN10_18_ADC
	GPIO	19	19 20		GND	
	TIM1_CH2 (VH)	21	21 22		GPIO	PB2
	TIM1_CH1 (UH)	23	23 24		~~GPIO~~	
	TIM2_CH3 (H3)	25	25 26		TIM1_CH3N (WL)	PB15
TIM_CUR-REF / LINB_RX		27	27 28		TIM1_CH2N (VL)	PB14
	GPIO	29	29 30		TIM1_CH1N (UL) / SPIB_SCK / FDCANB_TX	PB13
TIM2_CH2 (H2) / SWO / LINB_TX		31	31 32		AGND	AGND
	TIM1_CH3 (WH)	33	33 34		ADCx_INy	PC4
	UART_TX	35	35 36		GPIO / ~~UART2_RFS~~	CN10_36_GPIO
	UART_RX	37	37 38		~~GPIO / UART2_CTS~~	

H5 IO SETTING / C5 IO SETTING

PC1	DNF SB47	SB30	ARD_A4	ARD_D4
PC5	DNF SB43	SB27		CN10_6_GPIO
PB5	DNF SB42	SB22		
PA4_ADC_DAC	NOT CONNECTED	SB28	ARD_A2	
PB1	DNF SB45	SB29		CN10_18_ADC
PB15	SB49	DNF SB37		ARD_D0 UART_RX
PB8 SHARED WITH FDCAN	DNF SB50			CN10_36_GPIO
PB14	SB48	DNF SB35		ARD_D1 UART_TX
PB9 SHARED WITH FDCAN				
PC7	DNF SB41	SB21		ARD_D8
				CN10_4_GPIO
PC8	DNF SB40	SB19		ARD_D2
PA9	DNF SB39	SB17		CN10_2
PA10	DNF SB38	SB15		
PC9		SB11		ARD_D10
	DNF SB9			CN10_1

OPTIONAL CONFIGURATION FOR DESIGN SUPPORTING SDIO INTERFACE

(1): VIN (NUCLEO INPUT) WARNING voltage applied to 7V < VIN < 12V
(2): 5V_EXT, AREF (NUCLEO INPUT)
(3): 5V, 3V3, IOREF, 5V_STLK (NUCLEO OUTPUT, SHIELD INPUT)

Title: **Connectors**		
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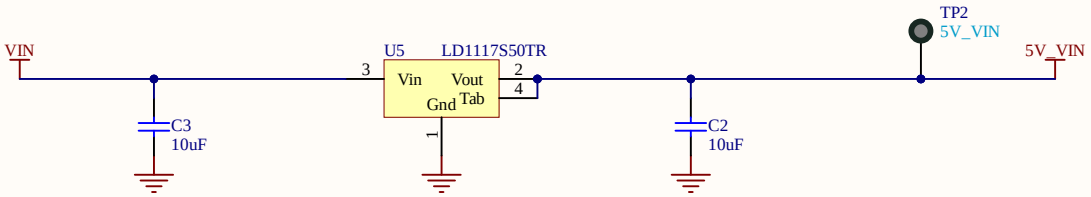
POWER SOURCES

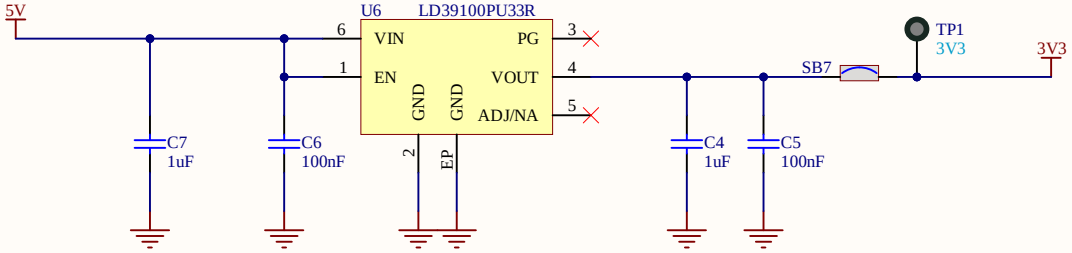
VIN / 5V PWR/ 800mA

Operating range: 7V < VIN < 12V

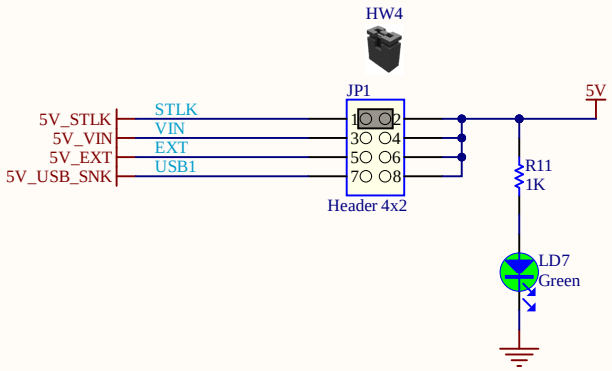


3V3 PWR/ 1A

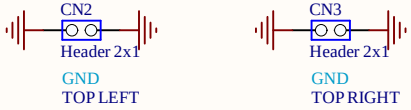
Operating range: 4.5V < VI < 5.5V



5V PWR SELECTION



GND HEADERS



Title: **Power Sources**		
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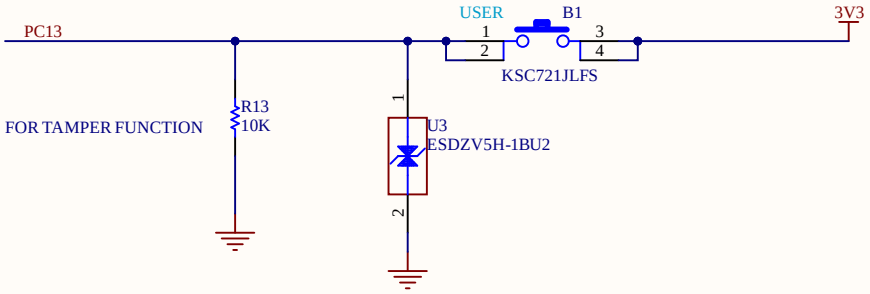
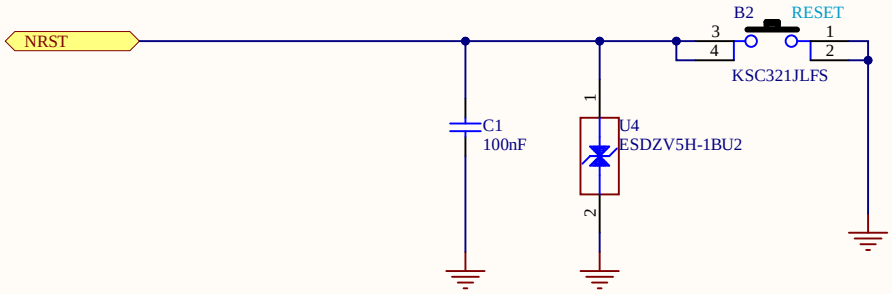
PERIPHERALS

PA[0..15] — PA[0..15]
PB[0..15] — PB[0..15]
PC[0..15] — PC[0..15]

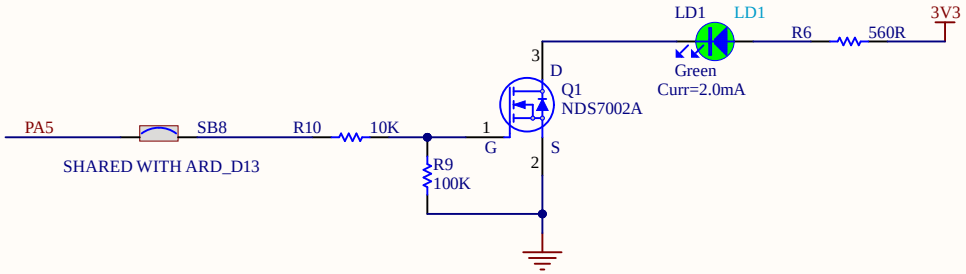
USER BUTTON



RESET



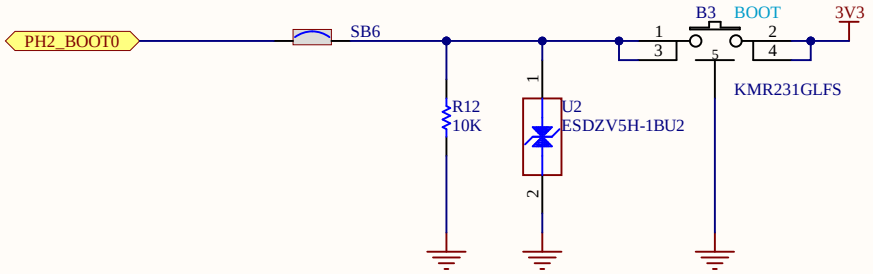
LED



BOOT SELECT

DEFAULT = INTERNAL FLASH

B3 PRESSED = BOOTLOADER



Title: **Peripherals**		
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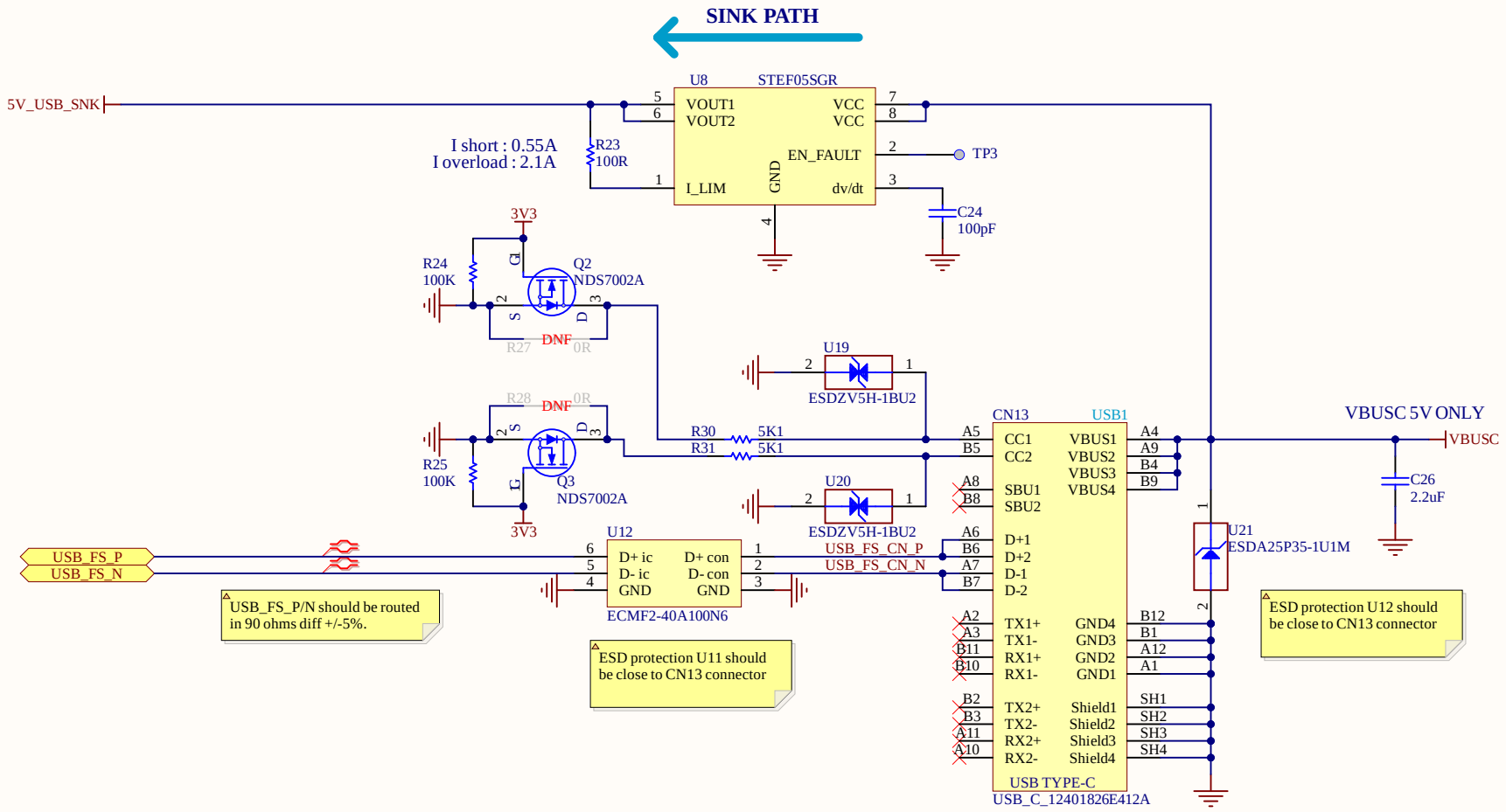
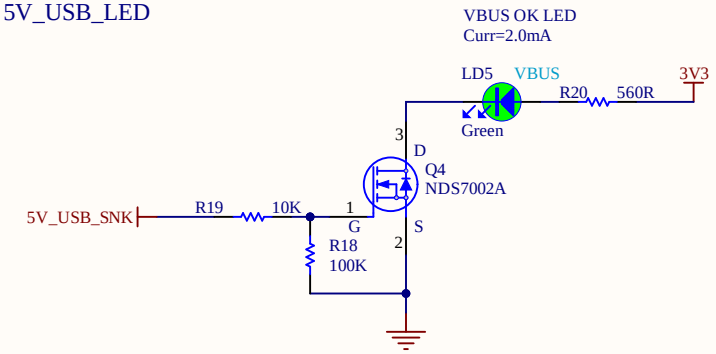
USB User

USB Type-C, SINK Only

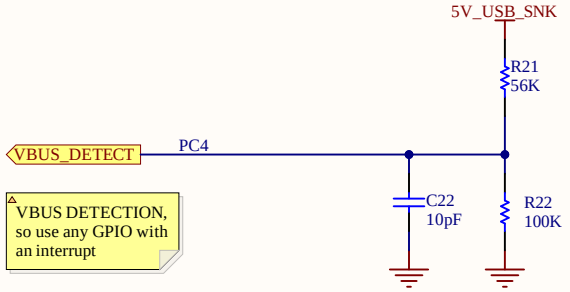
2.5W / 5V / 500mA



5V_USB_LED



VBUS_DETECTION



FOR DEBUG PURPOSE

Title: **USB User**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
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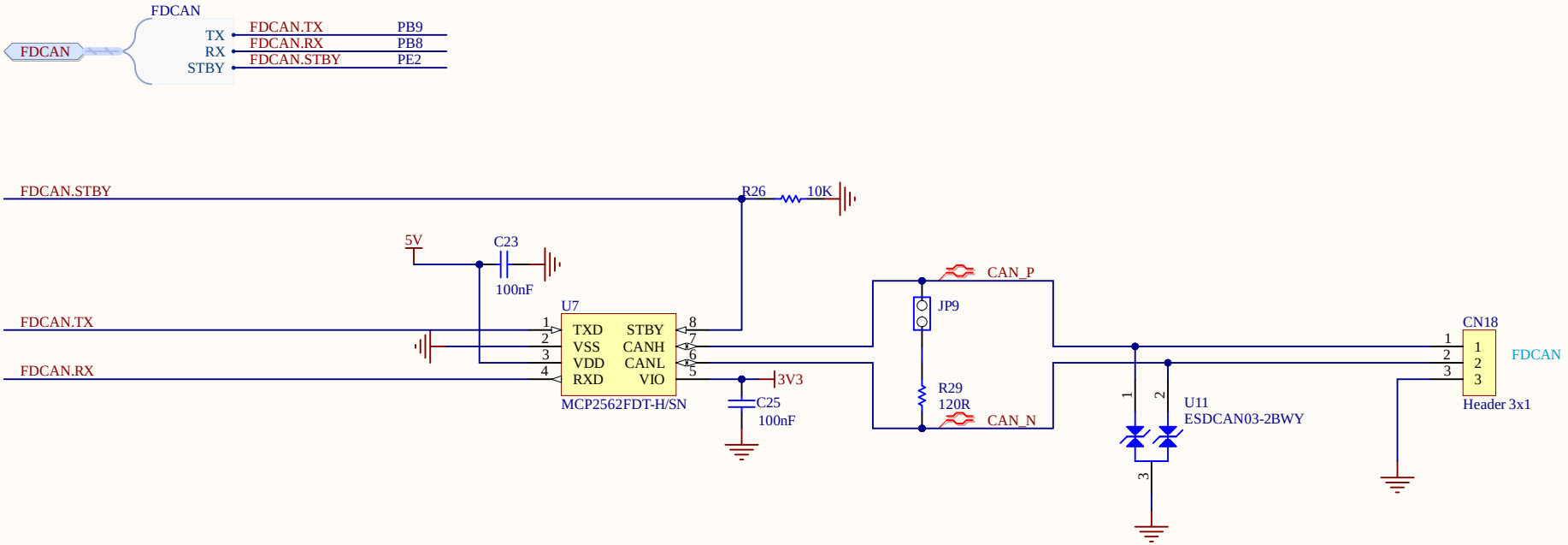
CAN FD

Operation Volatage: VDD: 4.5 ~ 5.5V; VIO: 1.8 ~ 5.5V



Title: **FDCAN**			
Project: **NUCLEO-64 STM32H5/STM32C5 series**			
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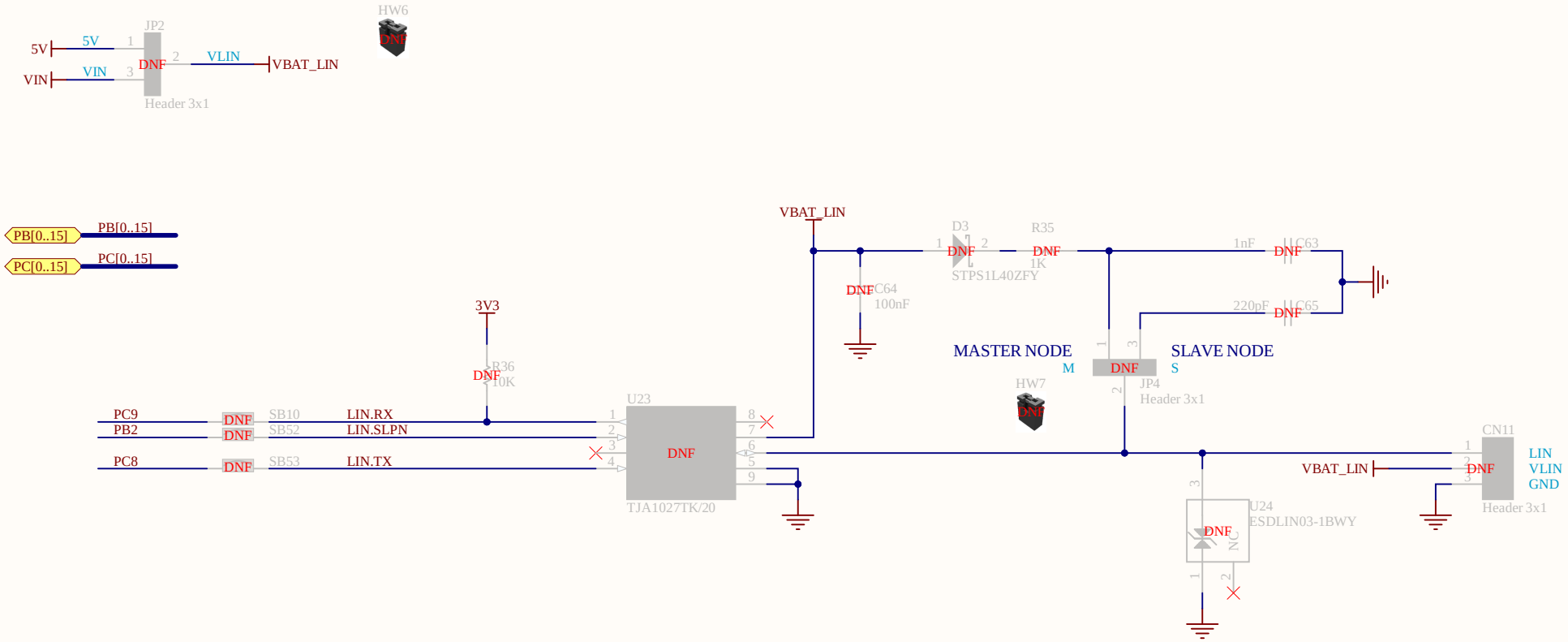
LIN

Operation Voltage: VBAT: 5 ~ 18V
Operation Voltage: VIN: 7 ~ 12V

If VBAT < 5 V, the TJA1027 may remain operational, but parameter values cannot be guaranteed to remain within the operation ranges specified in datasheet



Title: **LIN**		
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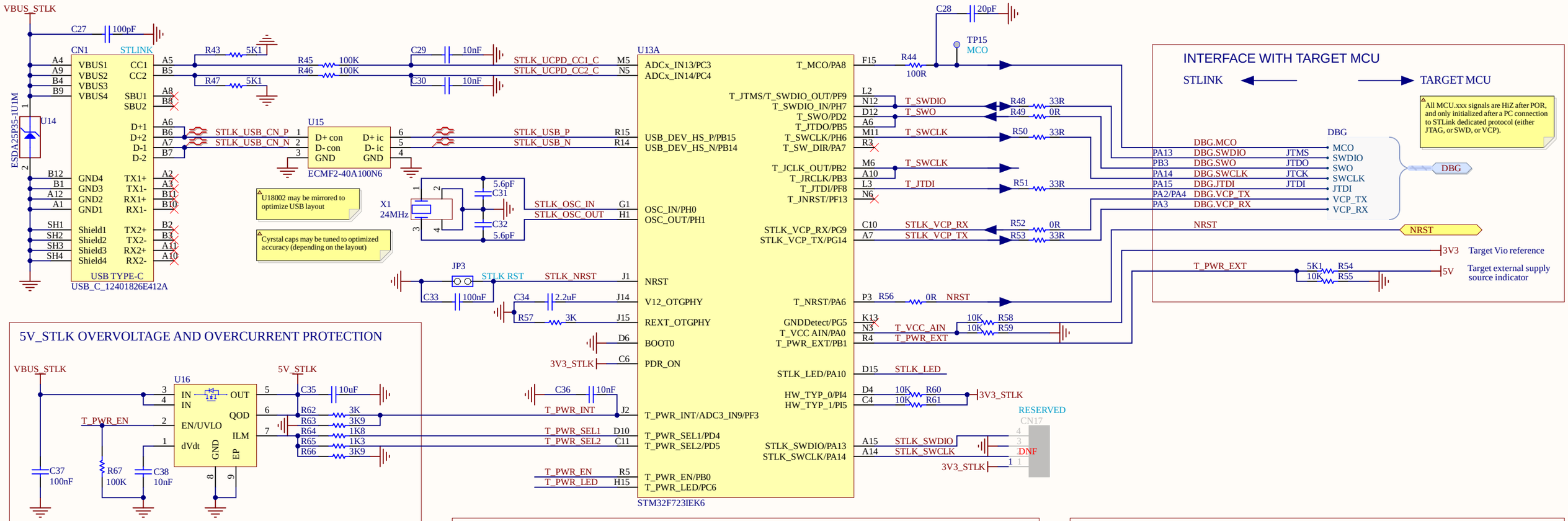
STLINK-V3EC



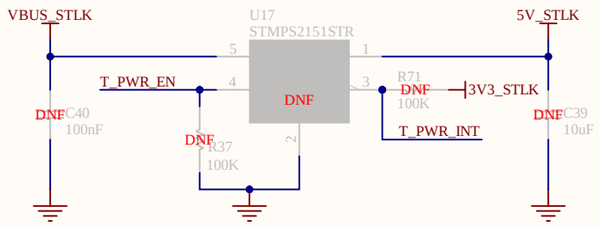
5V_STLK OVERVOLTAGE AND OVERCURRENT PROTECTION

5V_STLK OVERCURRENT PROTECTION MANAGEMENT

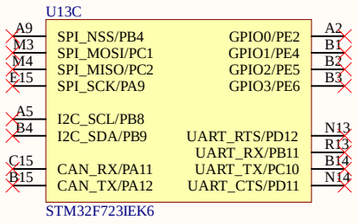
	T_PWR_SEL2/PD5	T_PWR_SEL1/PD4
PowerDefault.SNK *(current limit: 550mA)*	Hi-Z	Hi-Z
Power1.5.SNK *(current limit: 1.66A)*	Hi-Z	0
Power3.0.SNK *(current limit: 3.2A)*	0	0

Hi-Z = IO set in high impedance

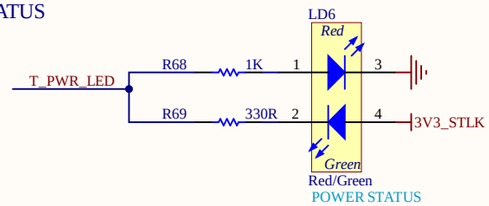
STMPS2151STR is backup of the TPS259535DSG



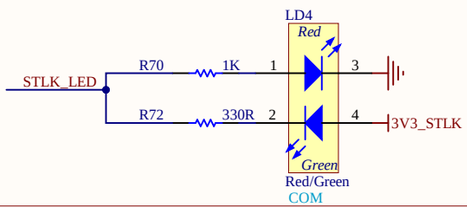
UNUSED PINS



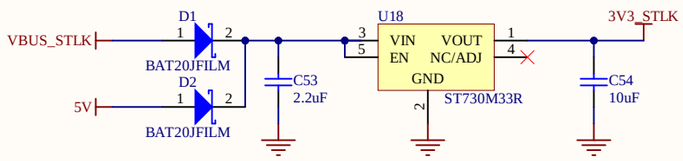
LED POWER STATUS



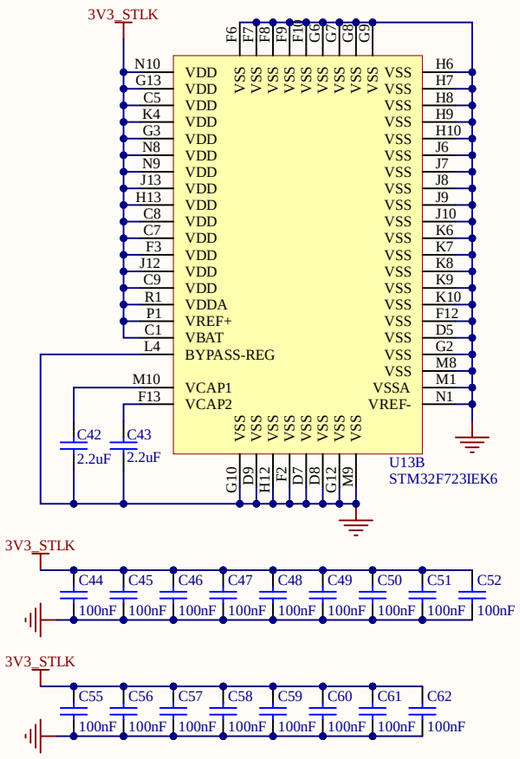
LED STLINK



ST-LINK POWER (3V3/300mA)



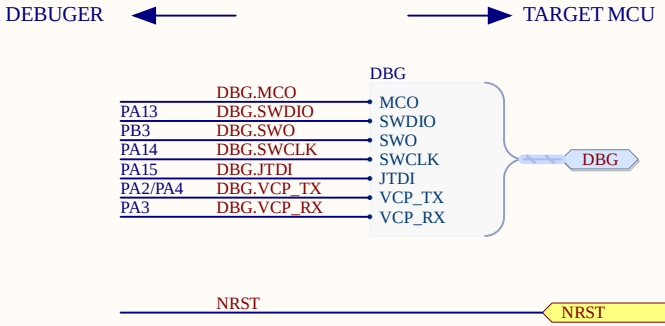
STLINK MCU POWER



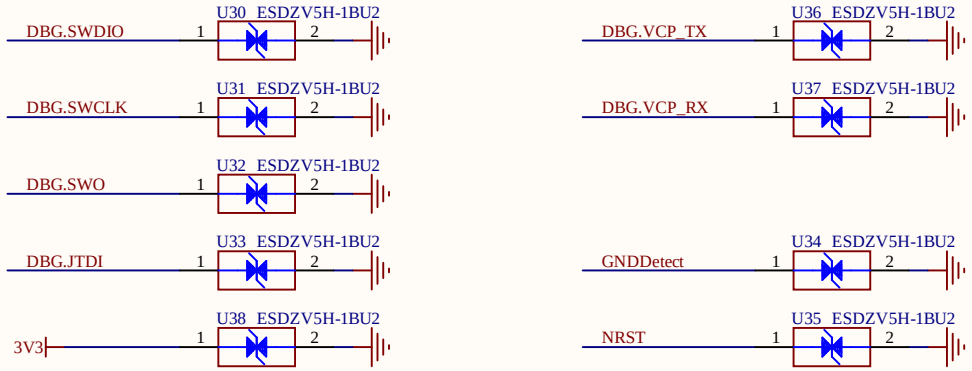
Title: **STLINK-V3EC**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
Variant: C542RC		
Revision: B-02		Reference: MB2213
Size: A3	Date: 2025-Nov-21	Sheet: 11 of 12

EXTERNAL DEBUGER INTERFACES

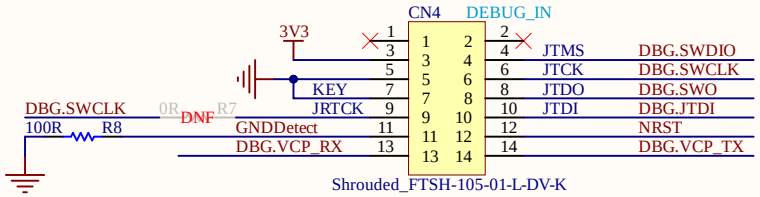
INTERFACE WITH TARGET MCU



ESD PROTECTIONS

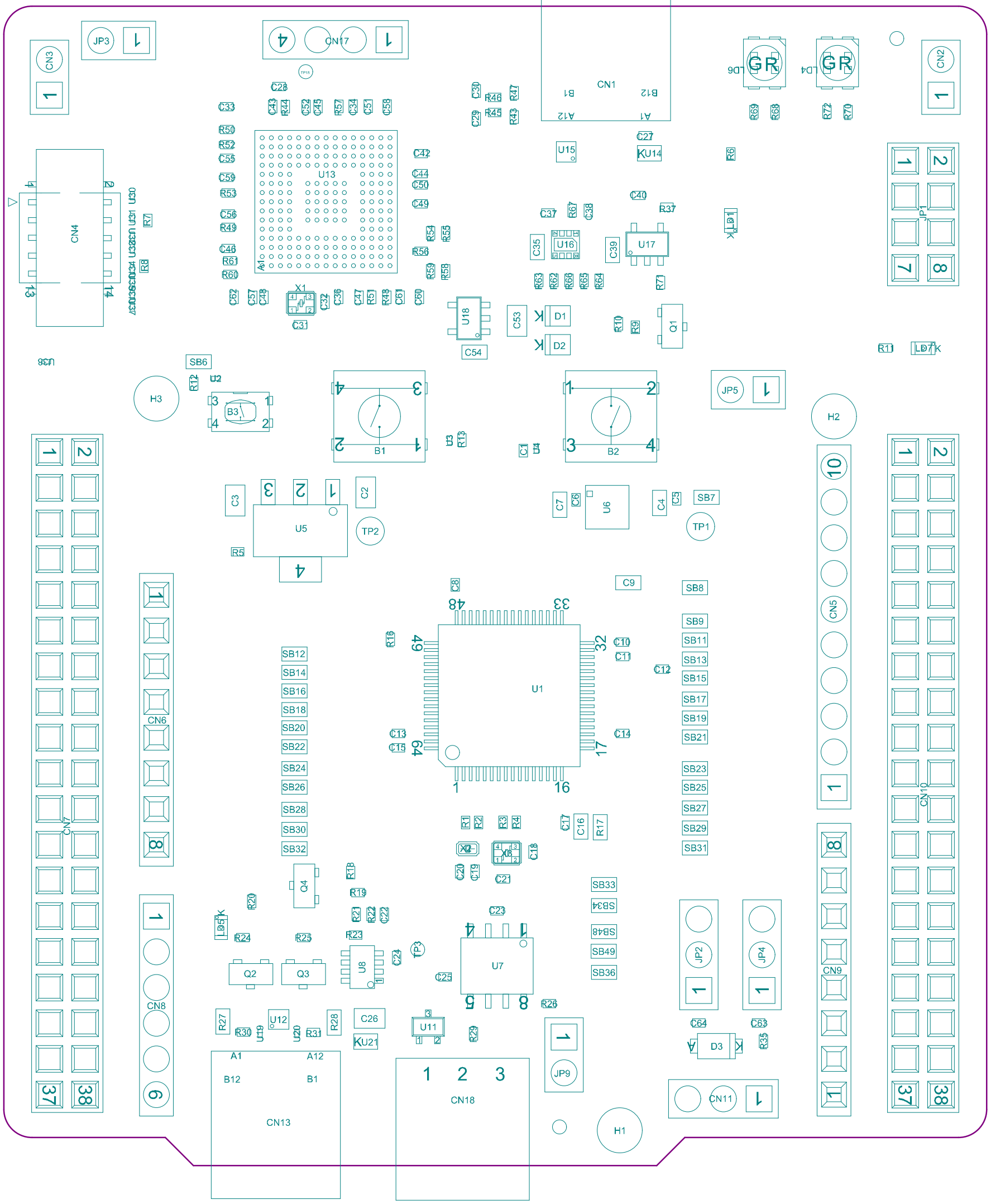


STDC14 RECEIVER

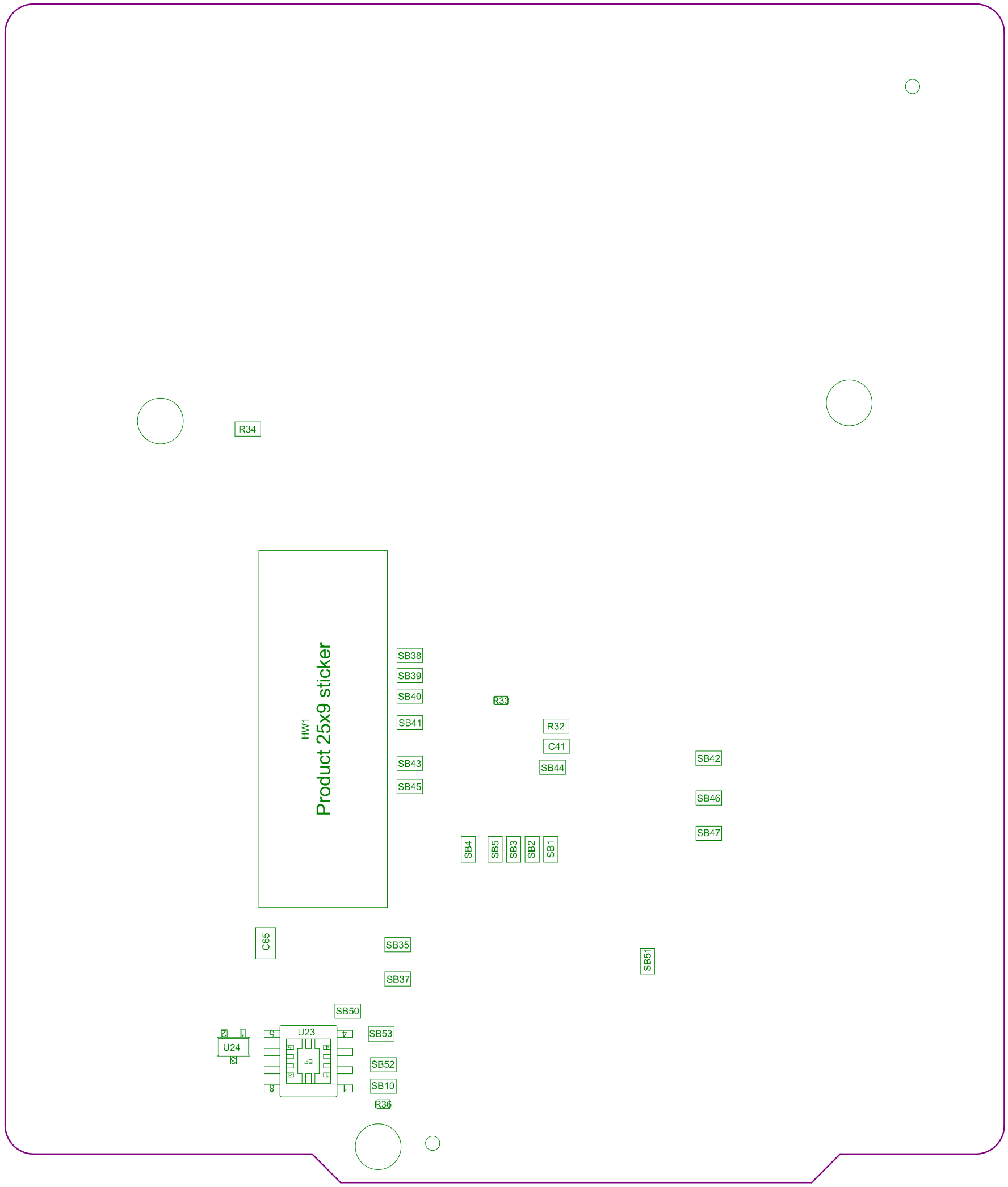


JRTCK is connected to MCU.SWCLK for compatibility with some debug probes

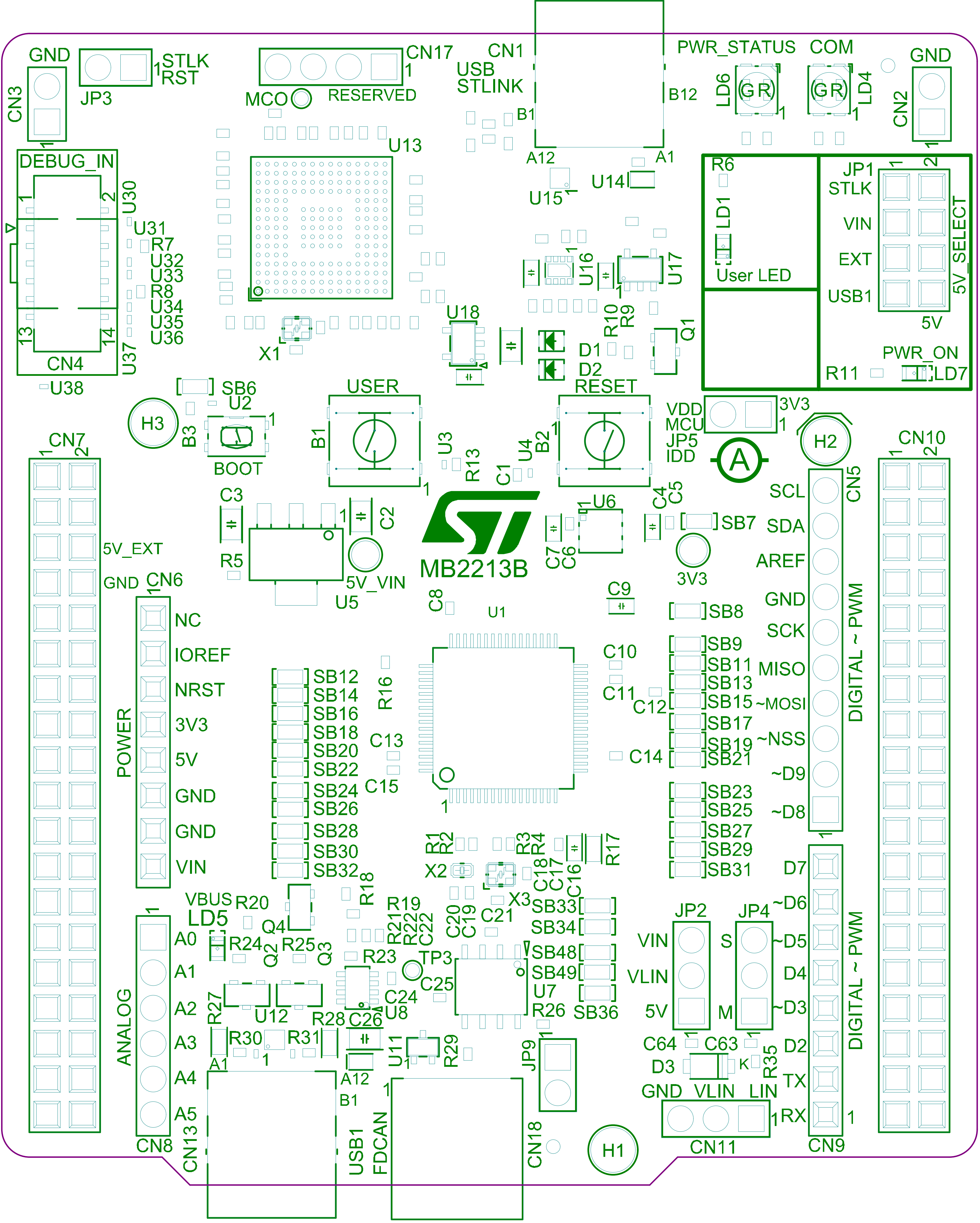
Title: **External_Debug_Interface**		
Project: **NUCLEO-64 STM32H5/STM32C5 series**		
Variant: C542RC		
Revision: B-02		Reference: MB2213
Size: A4	Date: 2025-Nov-21	Sheet: 12 of 12



Project: NUCLEO-64 STM32H5/STM32C5 series	
Layer: M14-Top Assembly	Gerber: .GM14
Variant: [No Variations]	MB2213
Date: 2025-Nov-21	Rev: B



Project: NUCLEO-64 STM32H5/STM32C5 series	
Layer: M15-Bottom Assembly	Gerber:.GM15
Variant: [No Variations]	MB2213
Date: 2025-Nov-21	Rev: B

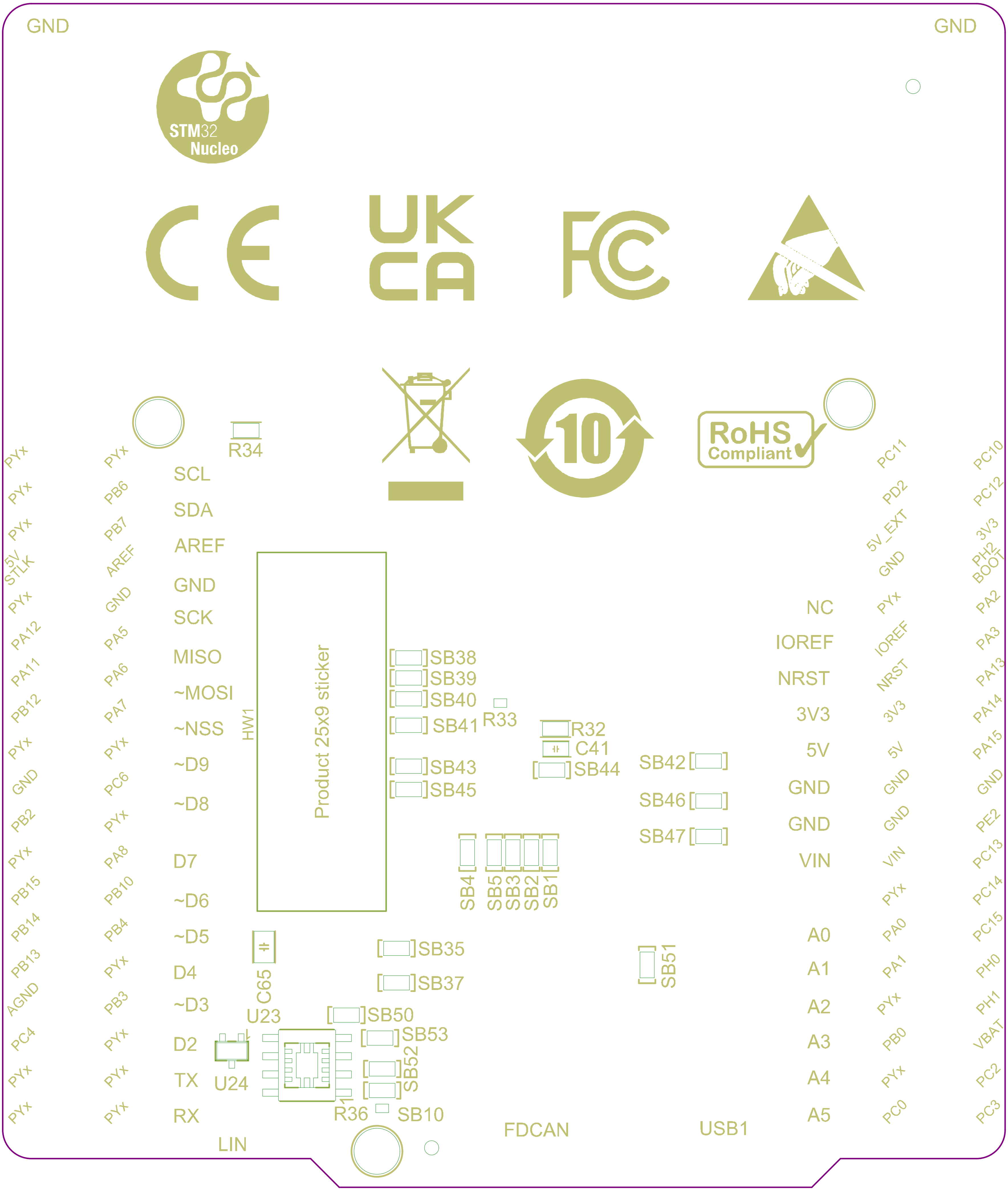


M14-Top Assembly

Top Overlay

.GM14

.GTO



GND
GND
STM32 Nucleo
UK CA
RoHS Compliant
R34
SCL
SDA
AREF
GND
SCK
MISO
~MOSI
~NSS
~D9
~D8
D7
~D6
~D5
D4
~D3
D2
TX
RX
HW1
Product 25x9 sticker
SB38
SB39
SB40
SB41
R33
R32
C41
SB44
SB43
SB45
SB42
SB46
SB47
SB4
SB5
SB3
SB2
SB1
SB35
SB37
SB51
C65
U23
SB50
SB53
SB52
U24
SB10
R36
LIN
FDCAN
USB1
NC
IOREF
NRST
3V3
5V
GND
GND
VIN
A0
A1
A2
A3
A4
A5
PYx
PYx
PYx
5V STLK
PYx
PA12
PA11
PB12
PYx
GND
PB2
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PB15
PB14
PB13
AGND
PC4
PYx
PYx
PYx
PB6
PB7
AREF
GND
PA5
PA6
PA7
PYx
PC6
PYx
PA8
PB10
PB4
PYx
PB3
PYx
PYx
PYx
PC11
PD2
5V_EXT
GND
PYx
IOREF
NRST
3V3
5V
GND
GND
VIN
PYx
PA0
PA1
PYx
PB0
PYx
PC0
PC10
PC12
3V3
PH2 BOOT
PA2
PA3
PA13
PA14
PA15
GND
PE2
PC13
PC14
PC15
PH0
PH1
VBAT
PC2
PC3

Board Layer Stack Bottom Overlay.GBO

M15-Bottom Assembly.GM15