

NUCLEO-WL5JC

MB1389

Table of contents

Sheet 1: Project overview (this page)

Sheet 2: mb1367_Top

Sheet 3: STM32 microcontroller I/Os

Sheet 4: STM32 microcontroller power & user buttons

Sheet 5: STM32 microcontroller RF

Sheet 6: Arduino & Morpho extension connectors

Sheet 7: ST-LINK/V3E-SWD Module

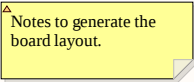
Sheet 8: ST-LINK/V3E-SWD Power Module

U_MB1389_Top
MB1389_Top.SchDoc



Legend

- General comment such as function title, configuration, ...
- Text to be added to silkscreen.
- Warning text.



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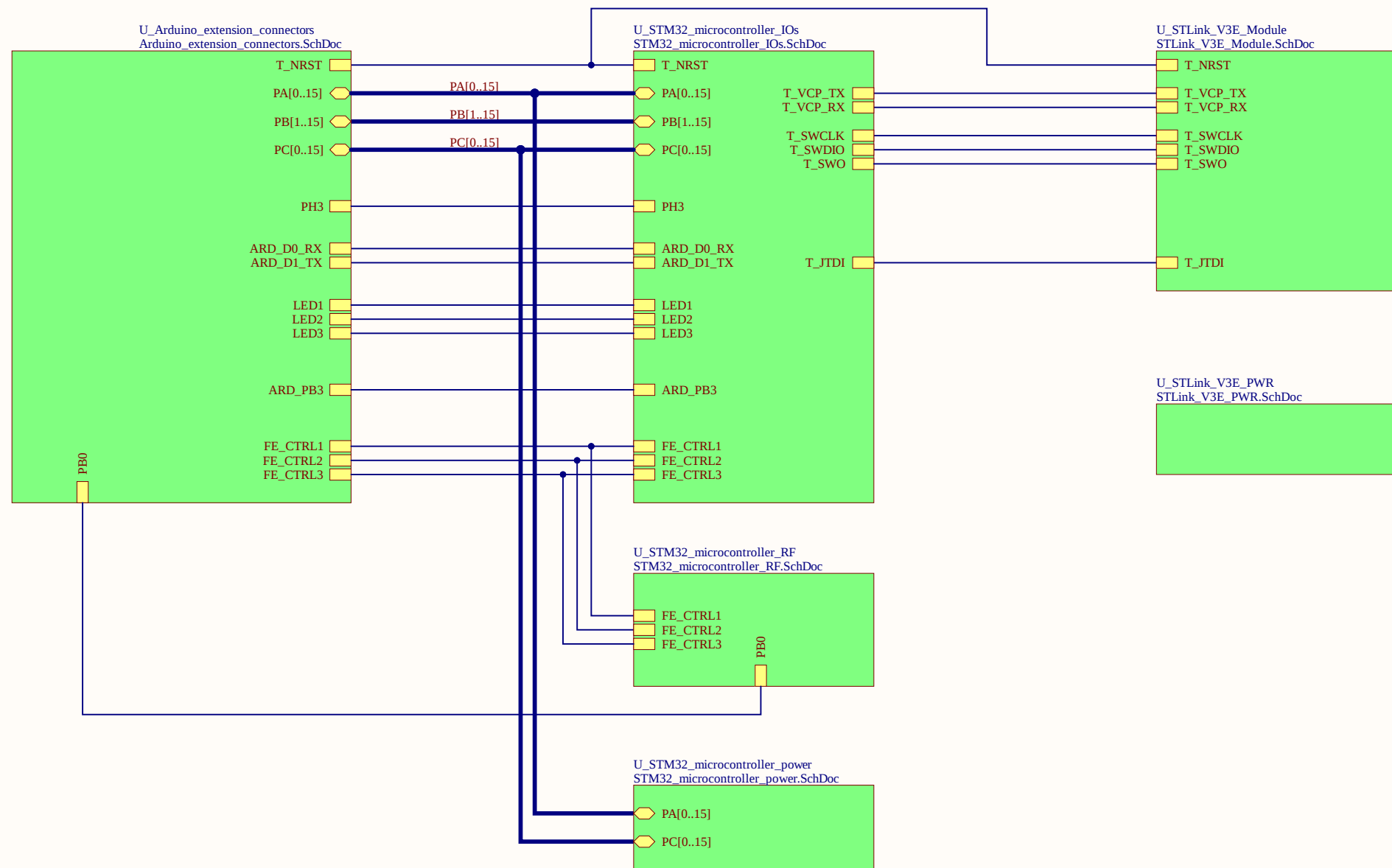
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Title: Project overview		
Project: NUCLEO-WL5JC		
Variant: Low-band		
Revision: D-04	Reference: MB1389	
Size: A4	Date: 2020-July-24	Sheet: 1 of 8





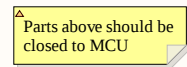
HW100
PCB
MBxxxxx

HW101
BOARD REF
MB1389D-01 sywwxxxxx

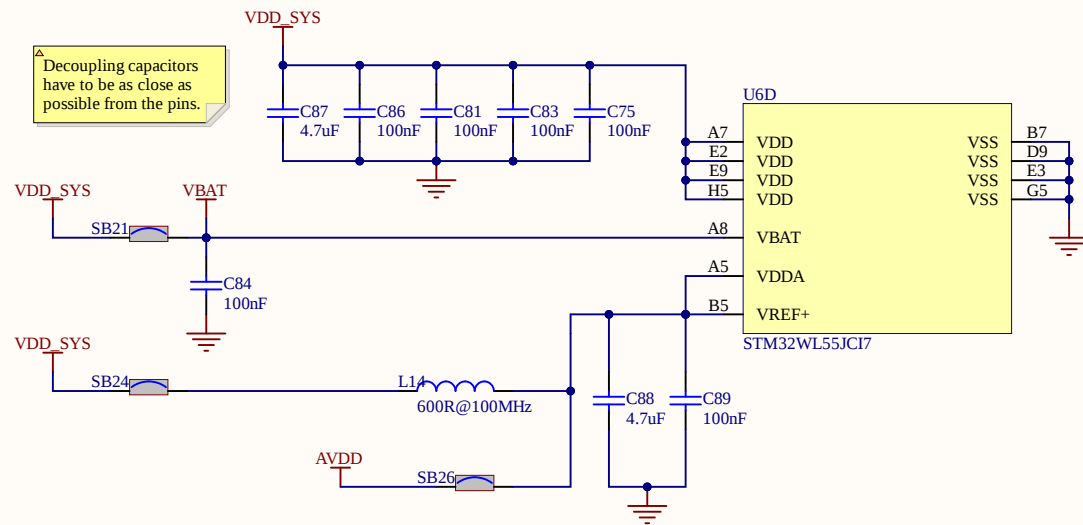
HW102
BOARD CPN
Board CPN

HW108
ES
ES

Title: Top hierarchical view		
Project: NUCLEO-WL5JC		
Variant: Low-band		
Revision: D-04		Reference: MB1389
Size: A4	Date: 2020-July-24	Sheet: 2 of 8

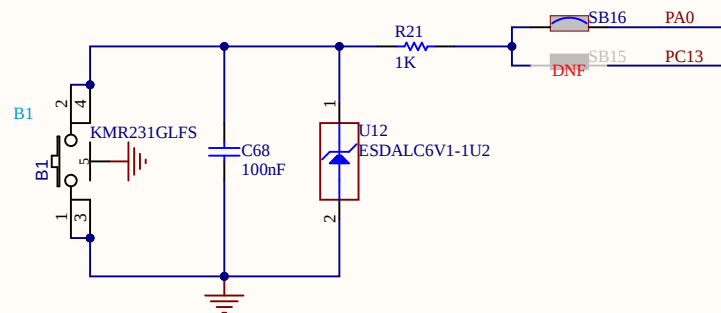


Decoupling capacitors have to be as close as possible from the pins.

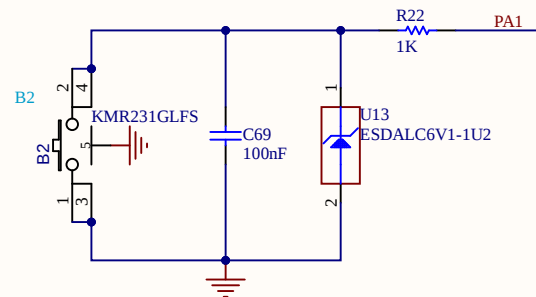


User buttons

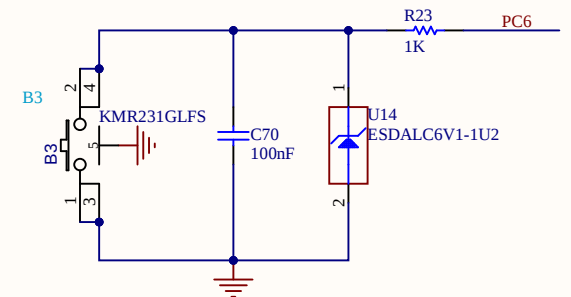
User button 1



User button 2

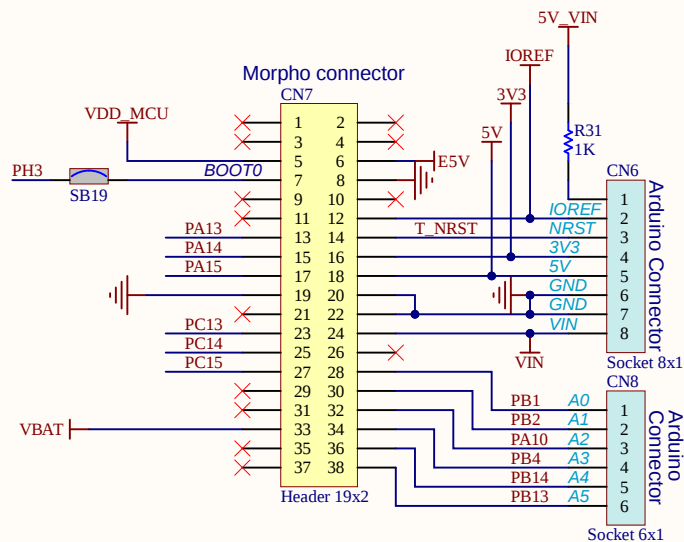
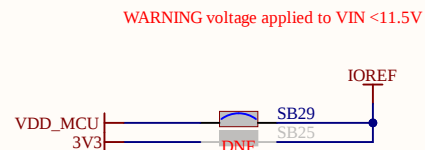
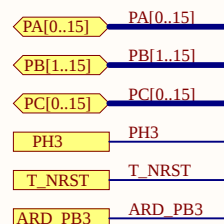


User button 3

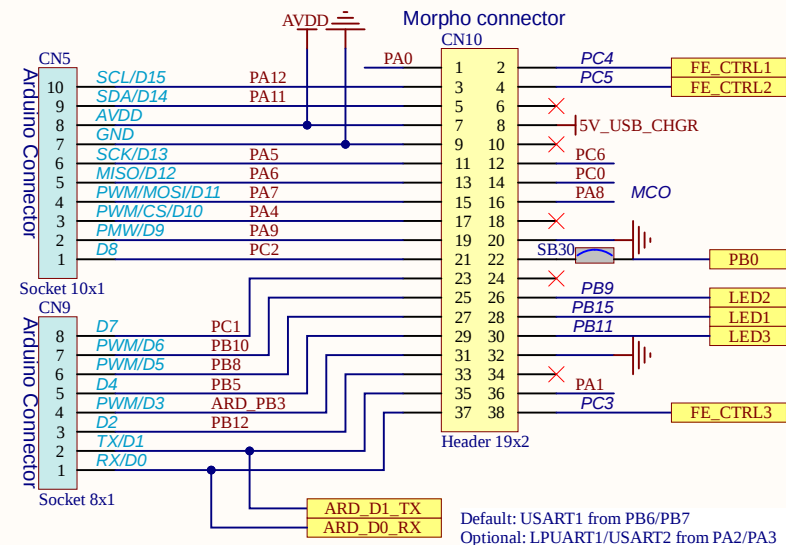


PA[0..15]

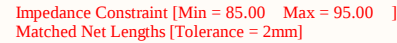
PC[0..15]



MCU



5V_USB_CHGR



Capacitor C90 close to pin 1 of USB STLK connector.

HW11 HW12 HW13 HW14 HW15 HW16



STDC14, Specific constraints for T_SWDIO and T_SWCLK (must have same length and must be Shielded), The routing of the tracks must be done on continuity from ST-LINKV3E --> 47ohms resistors --> Target MCU, to avoid stub noises and for EMC approach (47ohms resistors and ESDALC6V1W5 must be very close to STDC14).

Pin attributions on ESD can be swapped for layout optimisation



3V3_STLK

1 2 3 4

Red

Green

LD_BICOLOR_CMS

COM

R19 330R

R20 330R

STLK_LED

Reserved



