STSPIN family
L620x, L622x and L623x

Brushed DC, stepper and
brushless motor drivers

life.augmented

Family portrait

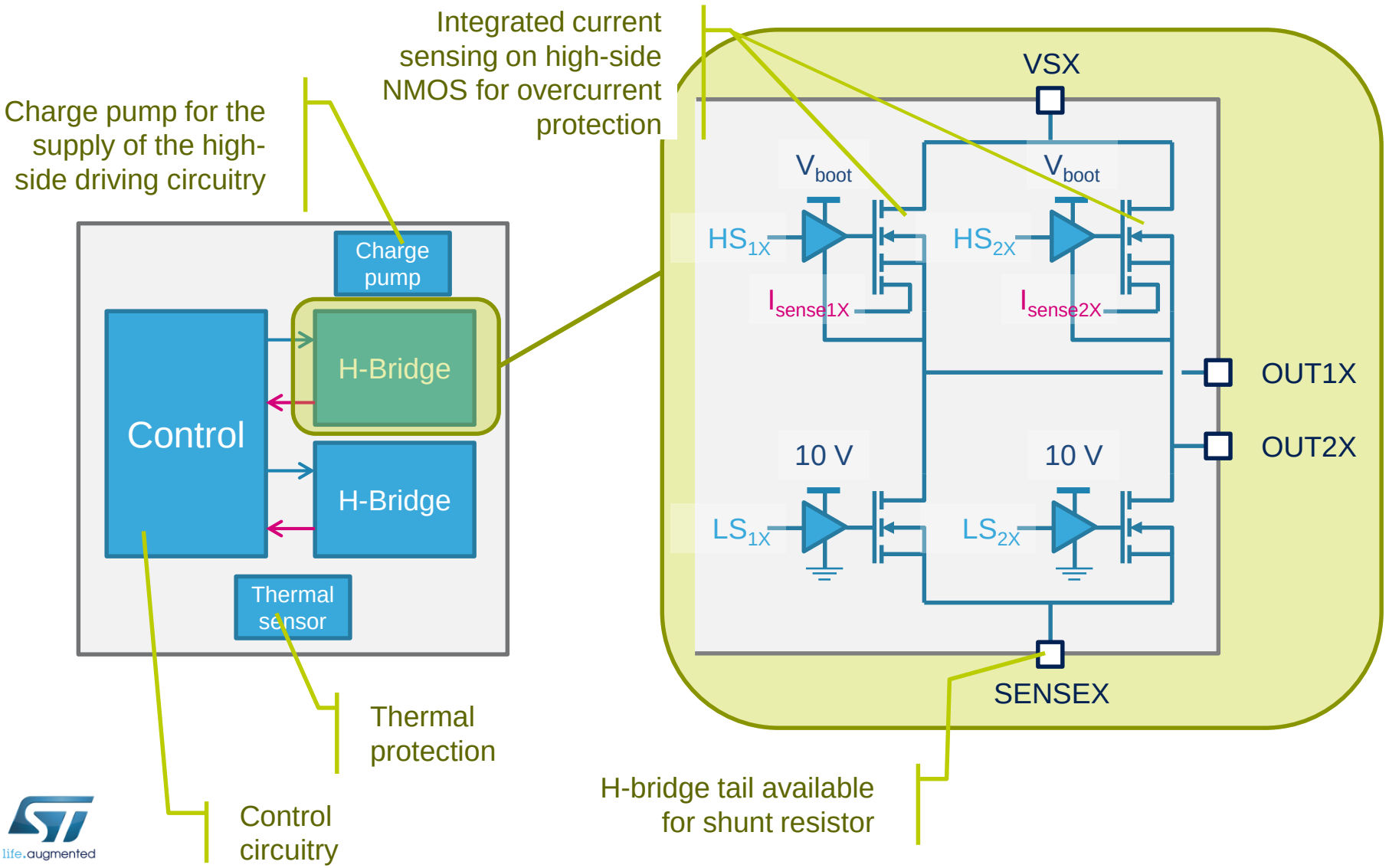
	Dual Brushed DC			Stepper	Brushless	
Part number	L6225 L6205	L6226 L6206	L6227 L6207	L62x8	L6229 L6235	L6230
Power stage	Dual full-bridge			Dual full-bridge	Triple half-bridge	
OCD	✓	✓	✓	✓	✓	✓
Adjustable OCD threshold		✓				
UVLO	✓	✓	✓	✓	✓	✓
Thermal shutdown	✓	✓	✓	✓	✓	✓
PWM current control			✓	✓	✓	

Electrical characteristics

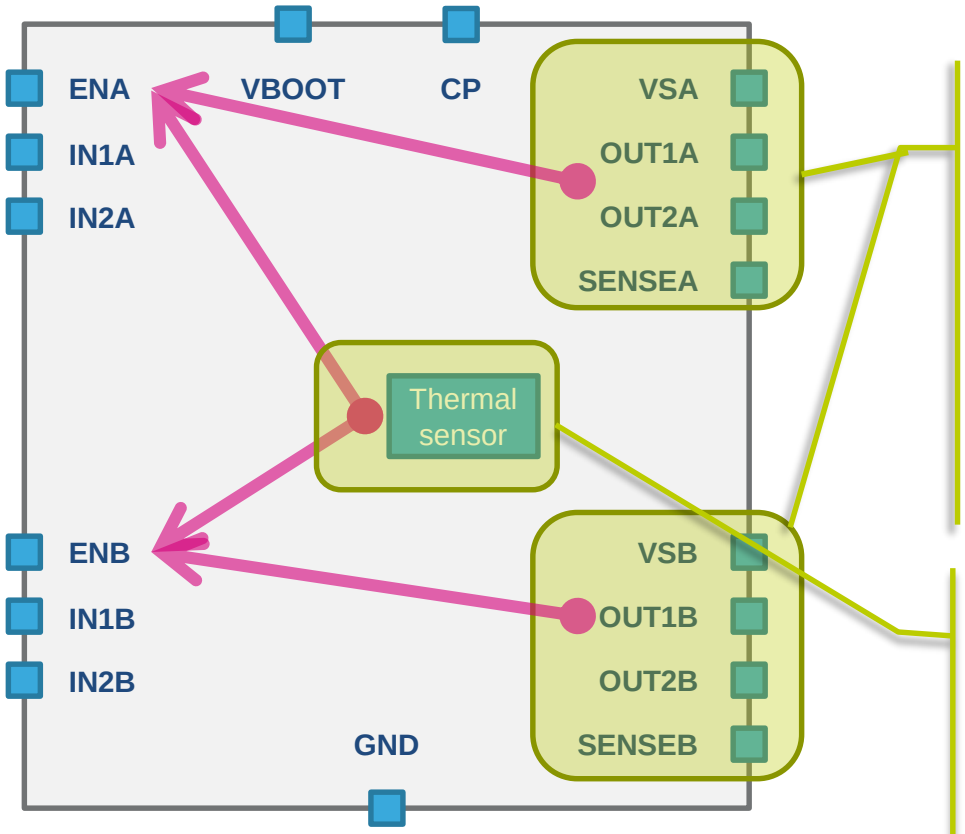
Parameter	L620x, L6235	L622x, L6229, L6230
Operating supply voltage	from 8 to 52 V	
$R_{DS(on)}$	0.3 Ω	0.73 Ω
Max. load current	2.8 Arms	1.4 Arms
Protections	**Non-dissipative overcurrent** Thermal protection Undervoltage-lockout (UVLO)	
Packages	PowerSO, SO, PDIP, **QFN (7 x 7 mm)**	PowerSO, SO, PDIP, **QFN (5 x 5 mm)**

Dual full-bridge power stage

Dual Brushed DC and Stepper drivers



life.augmented



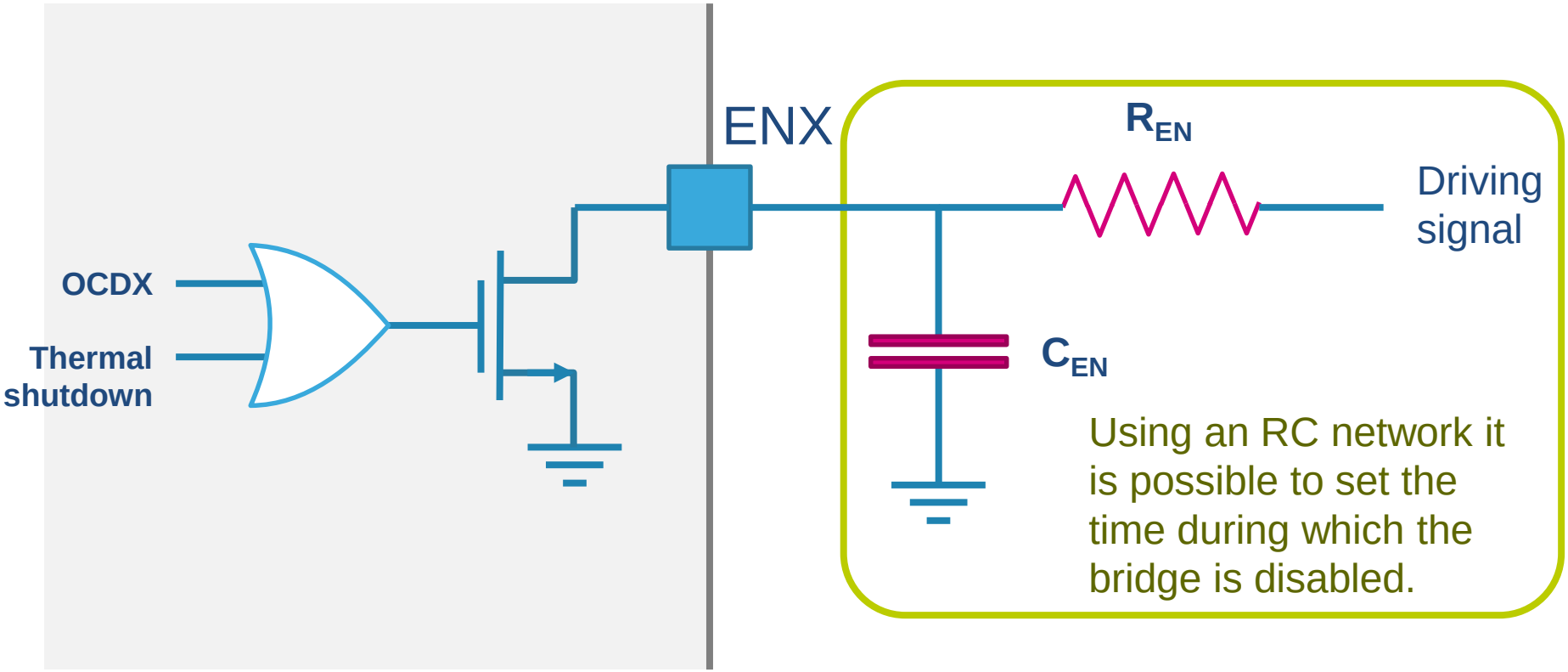
Non dissipative overcurrent protection @ 5.6 A (L6205) or 2.8 A (L6225)

When an overcurrent event occurs on one full-bridge, the respective ENX pin is internally forced low.

Thermal shutdown

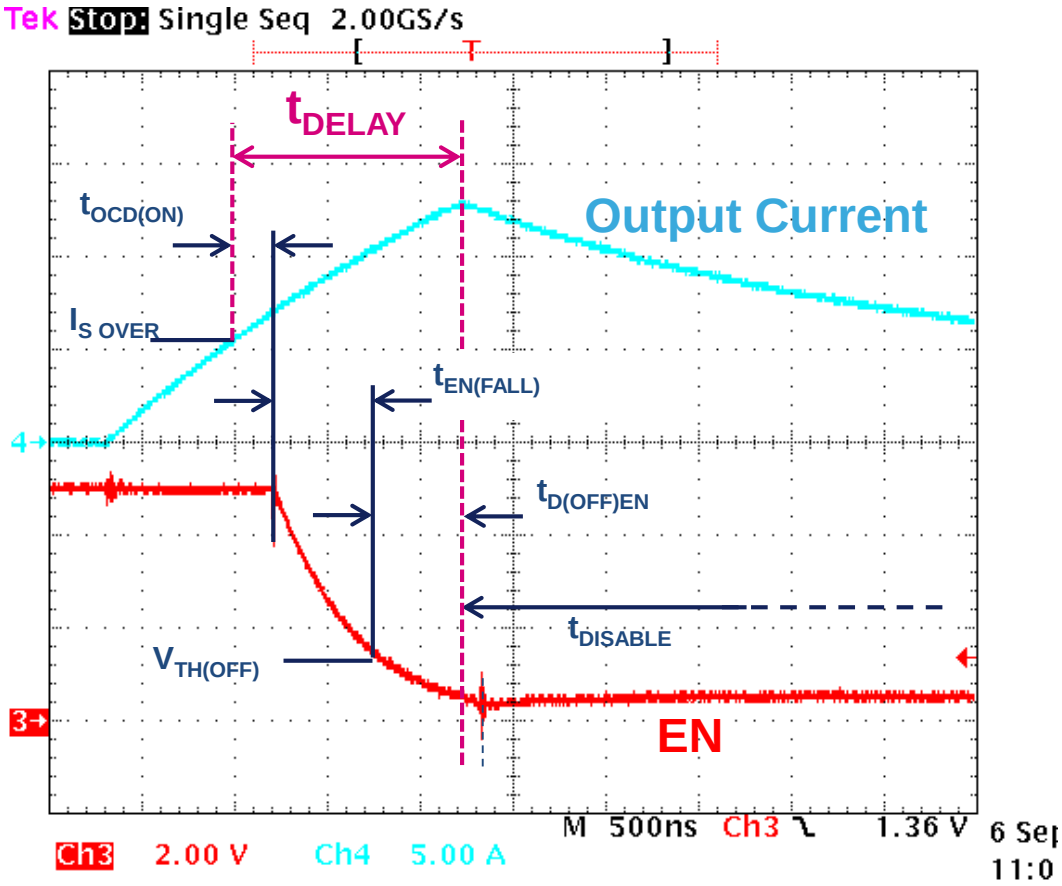
When the device temperature exceeds the shutdown threshold, both ENX pins are internally forced low.

Overcurrent protection



NOTE: OCD stands for overcurrent detection.
In L62x6 ICs, the protection is implemented by shorting the OCDA\B outputs with the respective ENA\B inputs.

Overcurrent protection



The delay between the OC event and the shutdown of the bridge depends on:

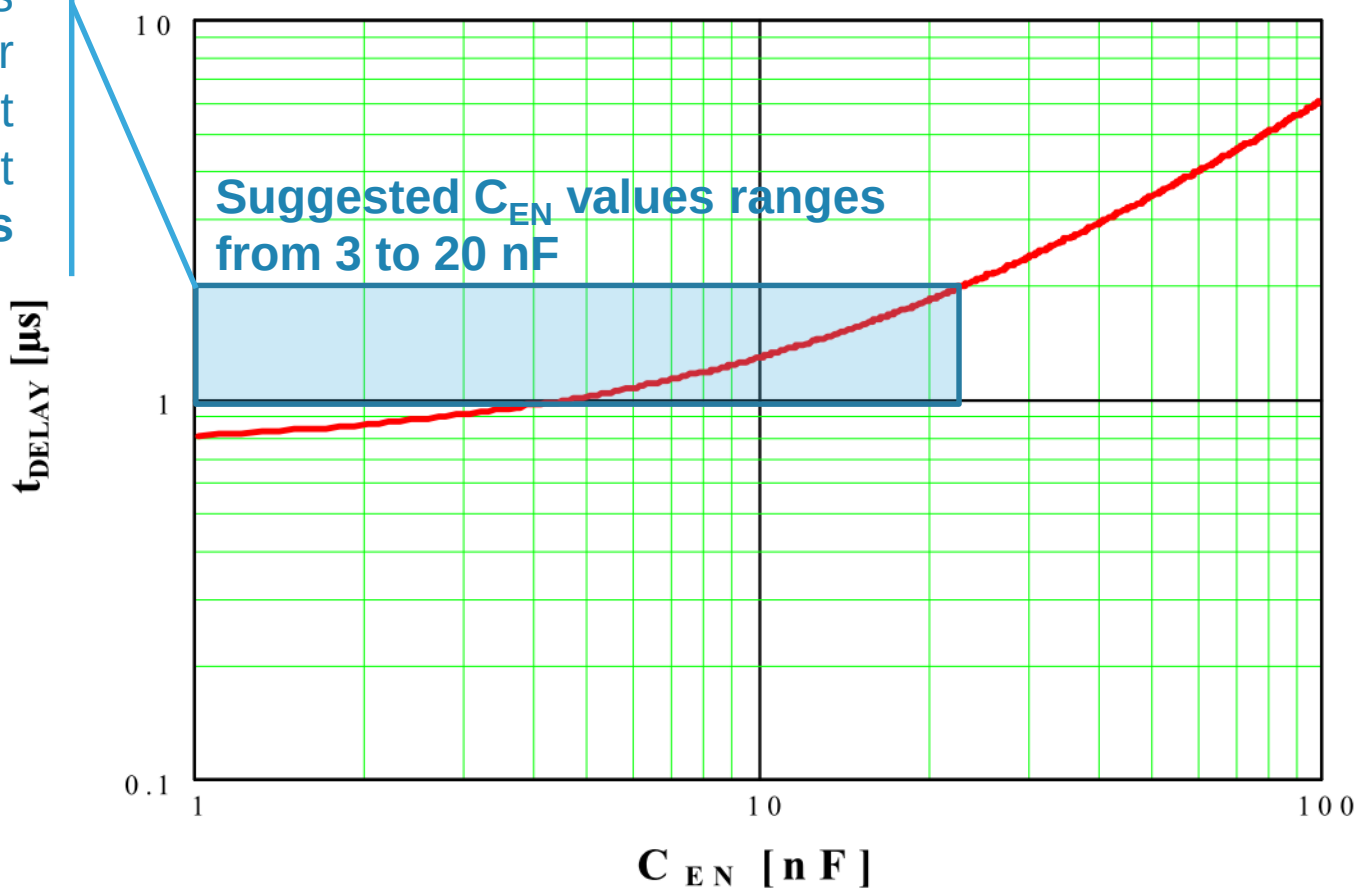
- The delay of the OCD comparator $t_{OCD(ON)}$
- The discharge time of the C_{EN} capacitor $t_{EN(FALL)}$

$$t_{EN(FALL)} = R_{OPDR} \cdot C_{EN} \cdot ln \frac{V_{DD}}{V_{TH(OFF)}}$$

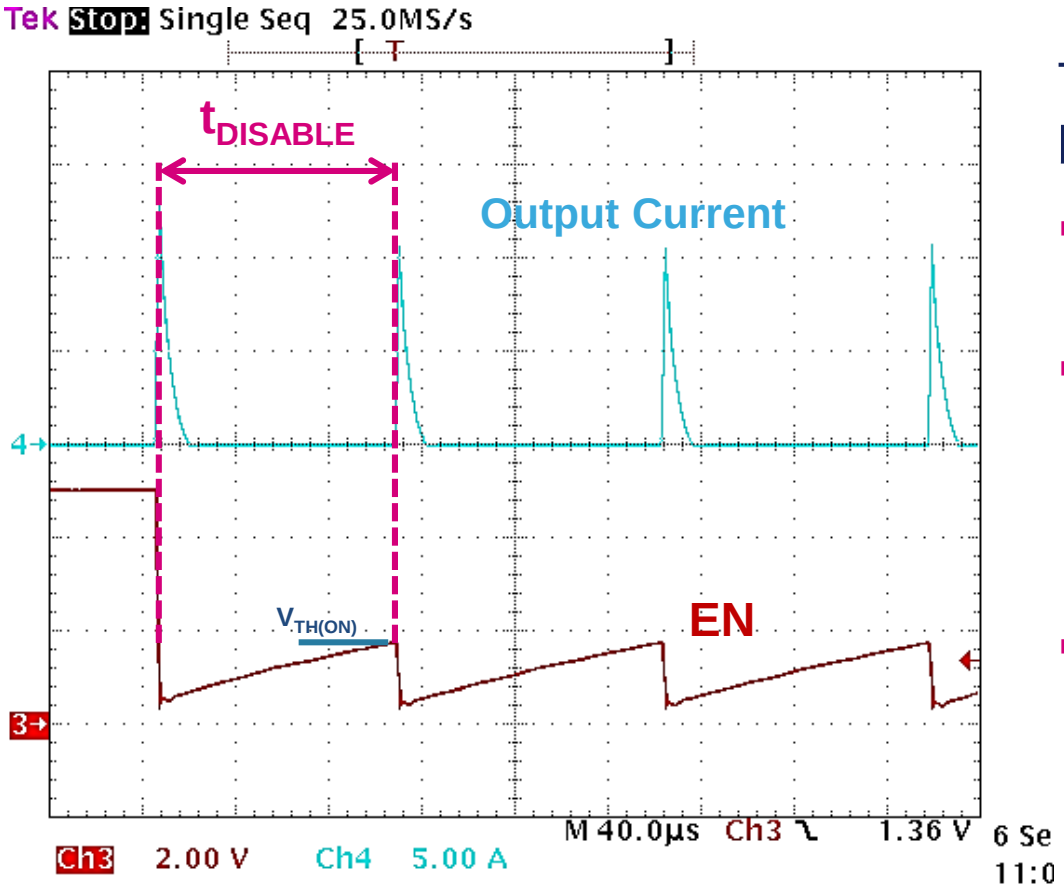
- The delay time of the driving circuitry $t_{D(OFF)EN}$

Overcurrent protection

The value depends on C_{EN} capacitor dimensioning and it must be kept **below 1 or 2 µs**



Overcurrent protection



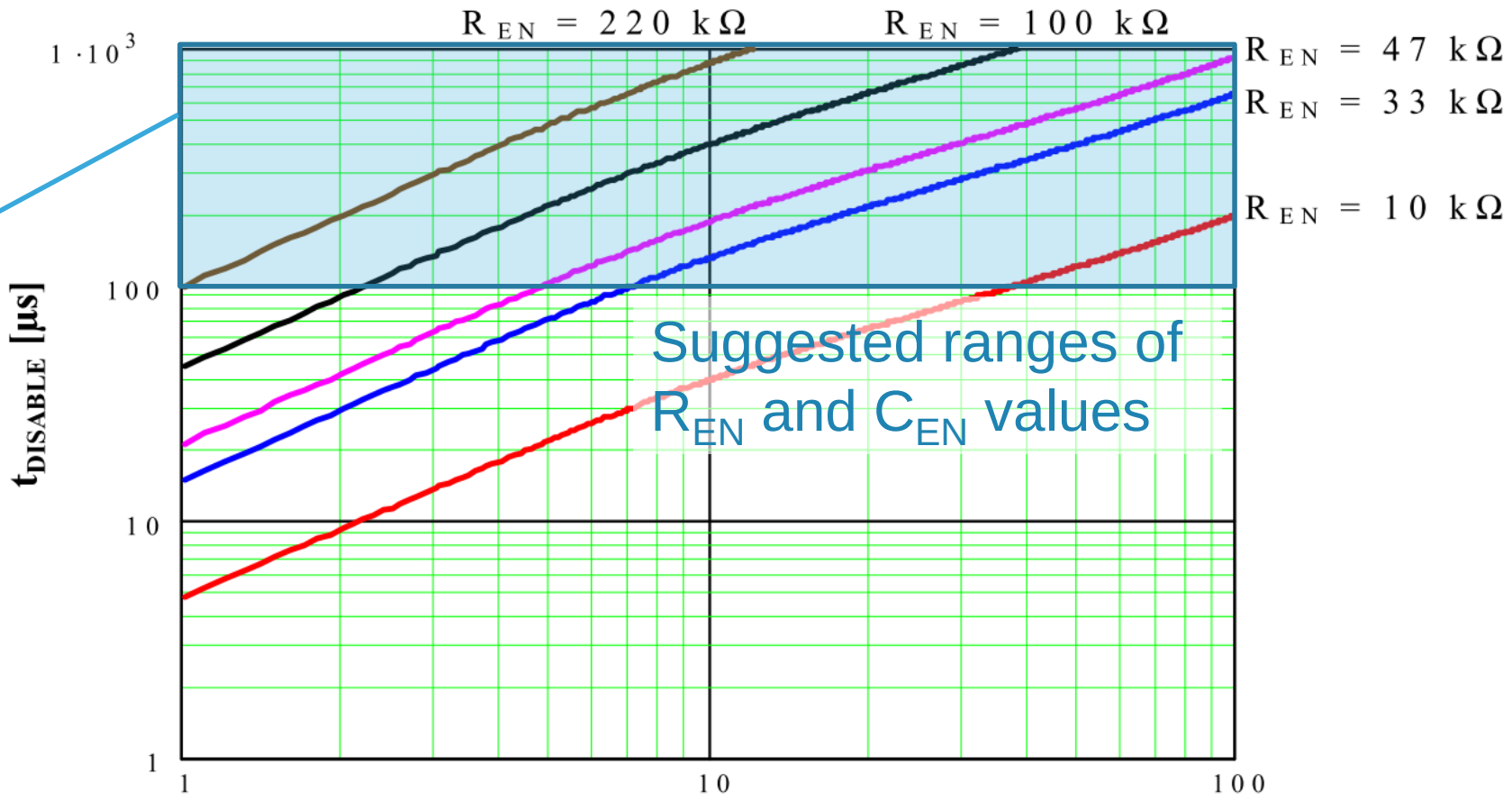
The disable time of the bridge depends on:

- The delay of the OCD comparator $t_{OCD(OFF)}$
- The charge time of the C_{EN} capacitor $t_{EN(RISE)}$

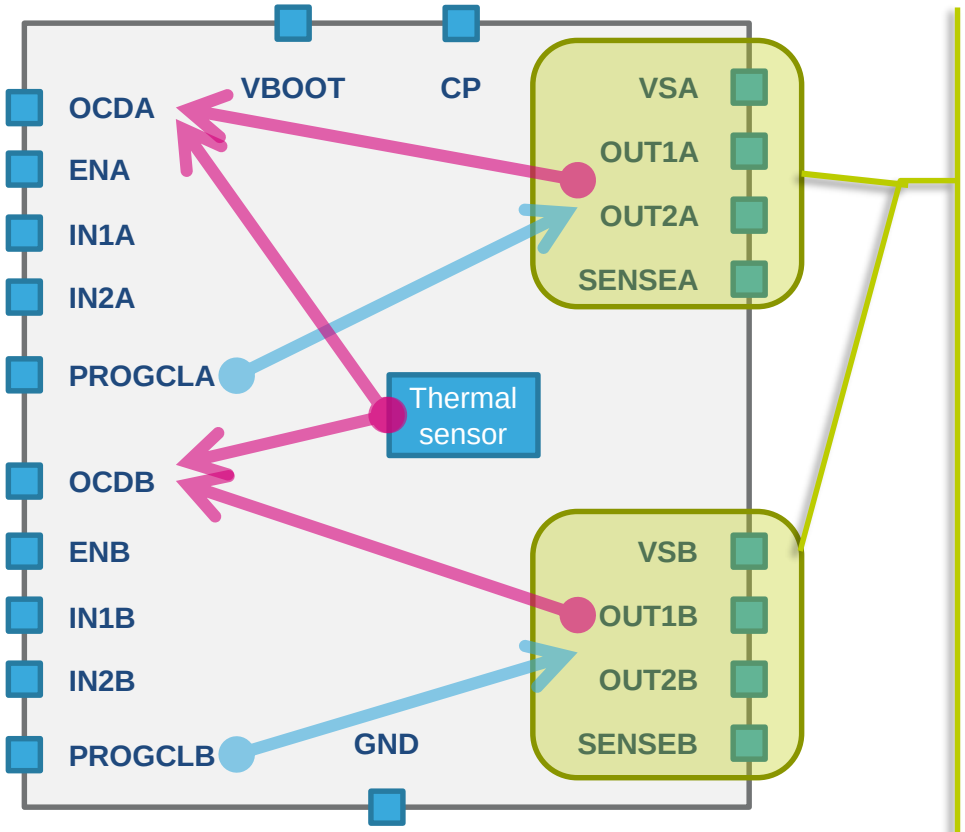
$$t_{EN(RISE)} = R_{EN} \cdot C_{EN} \cdot ln \frac{V_{DD} - V_{TH(OFF)}}{V_{DD} - V_{TH(ON)}}$$

- The delay time of the driving circuitry $t_{D(ON)EN}$

Overcurrent protection



The value depends on REN and CEN dimensioning and it must be long enough to guarantee that **the load current is reduced to zero**.
This way cumulative effects are avoided in case of subsequent overcurrent events.



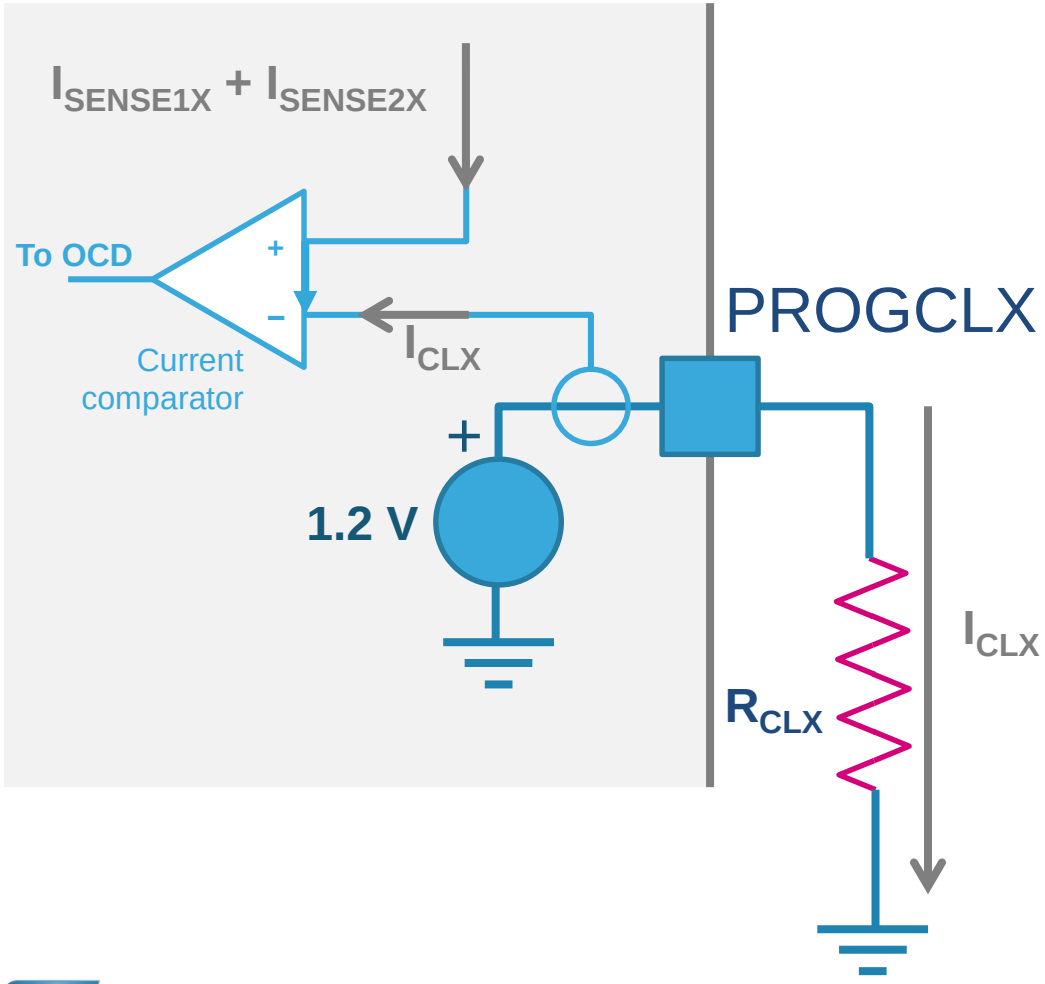
Programmable non-dissipative overcurrent protection up to 5.6 A (L6206) or 2.8 A (L6226)

The overcurrent threshold can be set through a resistor connected to PROGCLX pin.

When an overcurrent event occurs on one full-bridge, the respective OCDX pin is forced low (open drain output).

Thermal shutdown protection forces low both OCDX pins at the same time.

Adjustable overcurrent protection (L62x6)



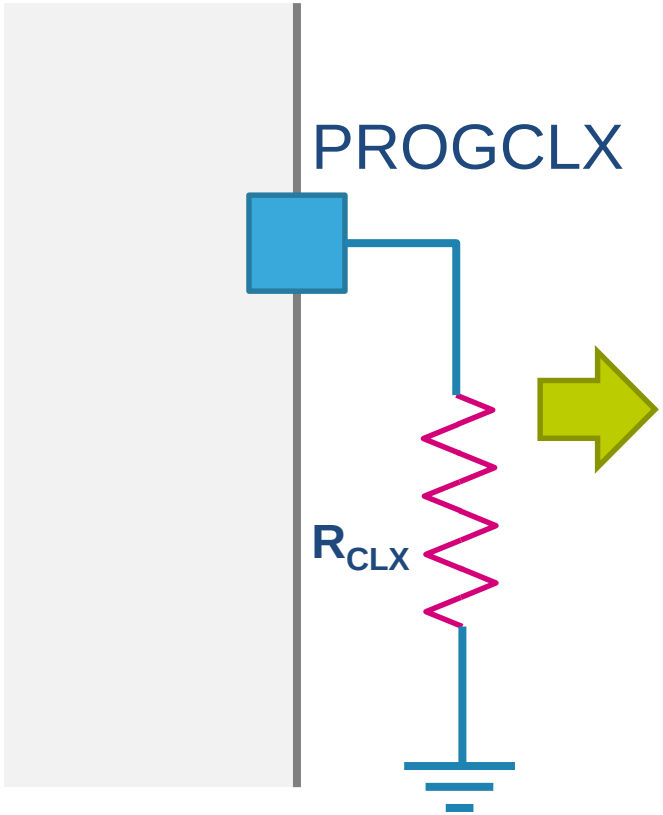
In L62x6 devices, the current flowing into the R_{CLX} resistor is compared to the current from sensing circuitry.
If $I_{SENSE1X} + I_{SENSE2X} > I_{CLX}$ an OCD occurs.

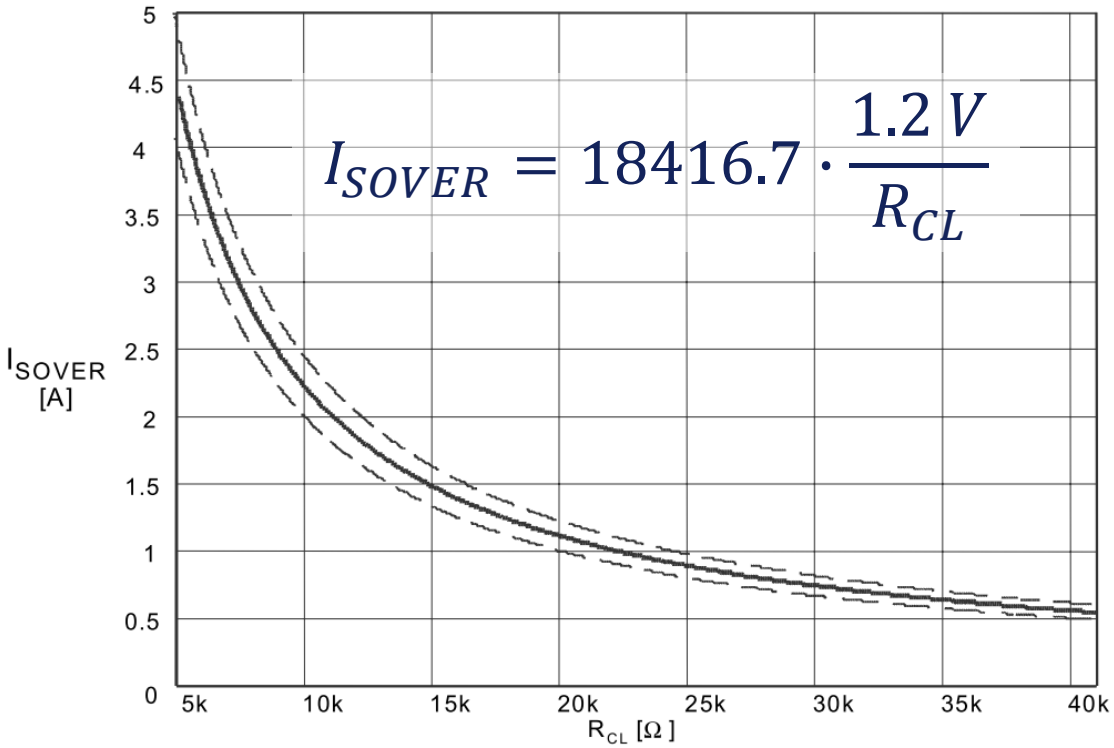
The sense current is a fraction of the actual current flowing into the MOSFET:

$$I_{SENSEYX} = I_{OUTYX}/18416.7$$

NOTE: For L622x devices, the scaling ratio is 9208.3 instead of 18416.7

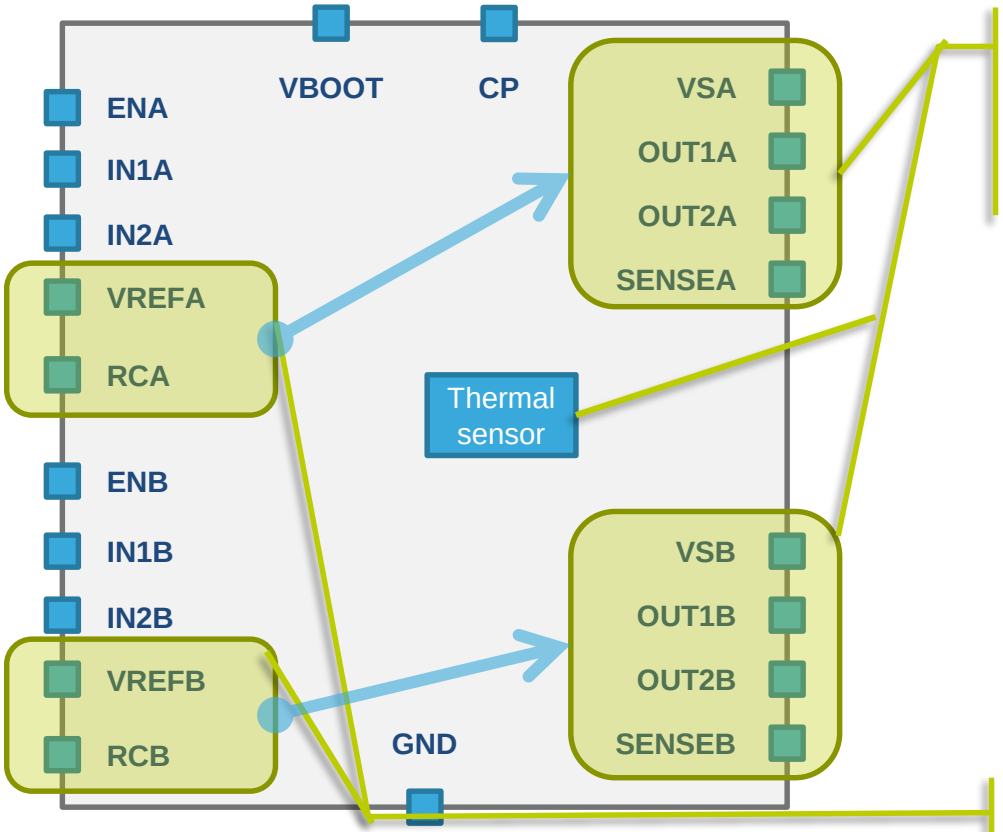
Adjustable overcurrent protection (L62x6)





NOTE: I_{SOVER} refers to the L6206 version. The value is halved in the L6226 case.

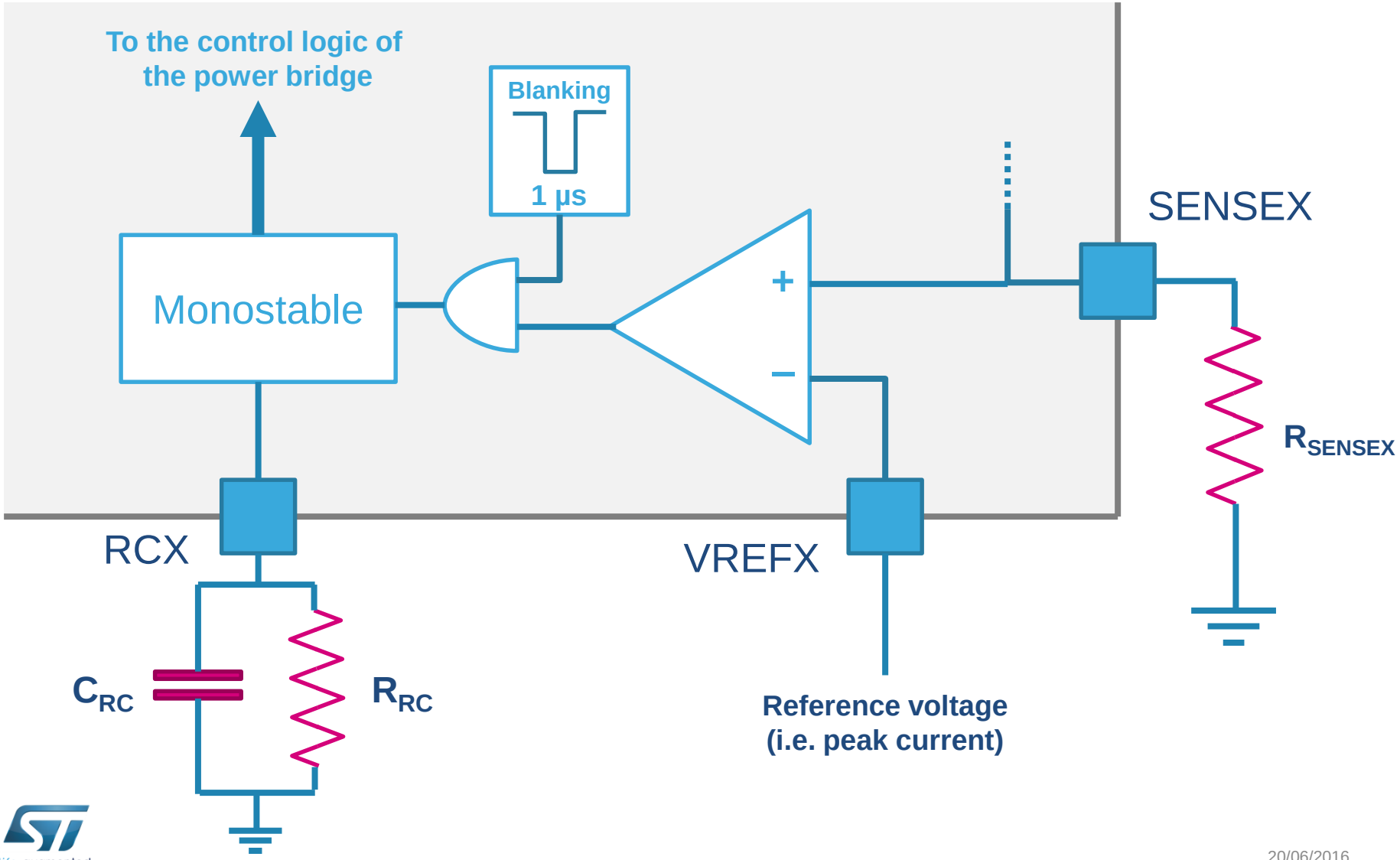
L62x7



Non-dissipative overcurrent protection and overtemperature protection are equal to the L62X5

Independent PWM current control with fixed OFF time for each full-bridge.

PWM current control

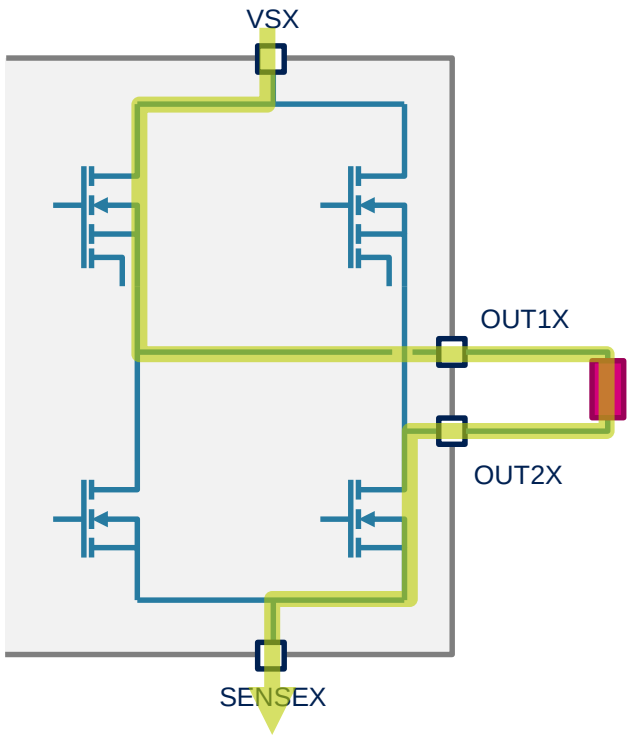


PWM current control

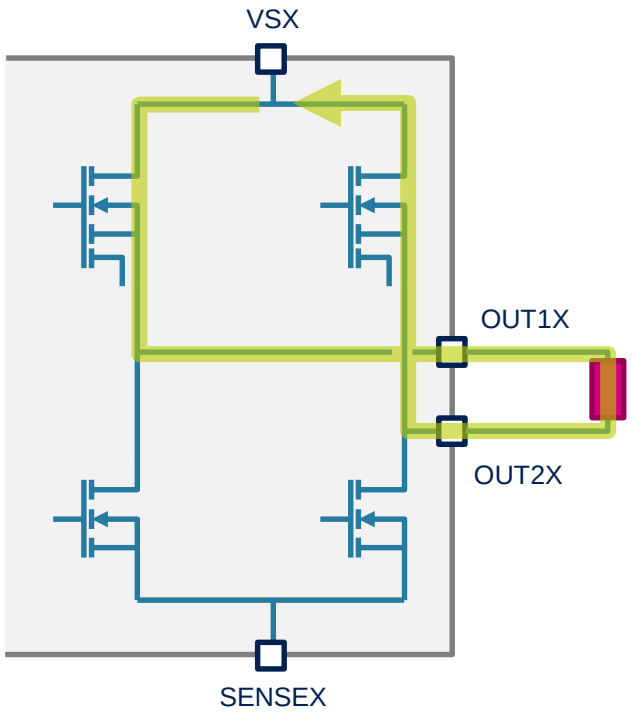
The PWM current controller uses a **slow decay** recirculating the current on the **high-side MOSFETs**.

This way the device is always protected against overcurrent events.

ON time

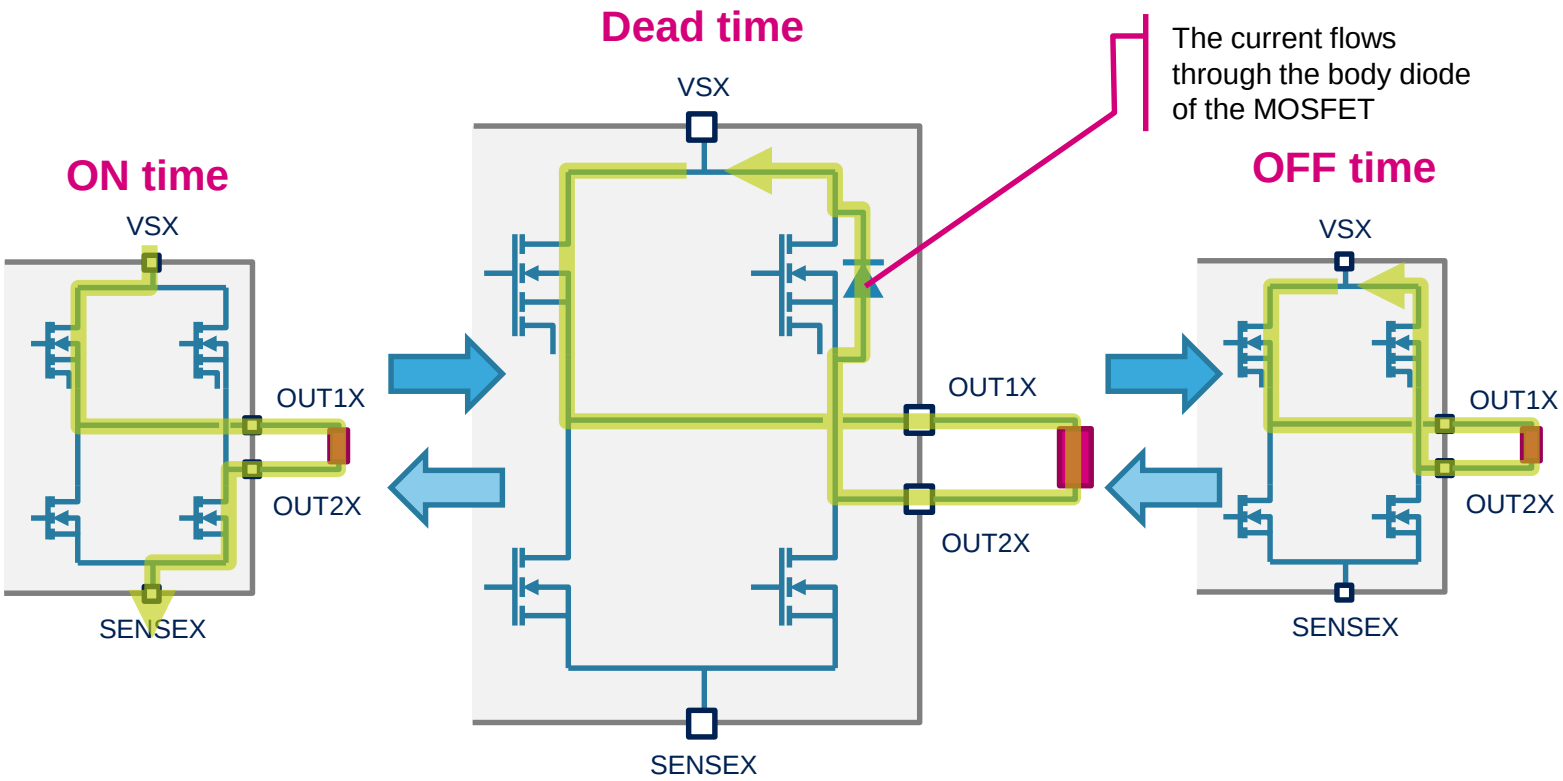


OFF time



PWM current control

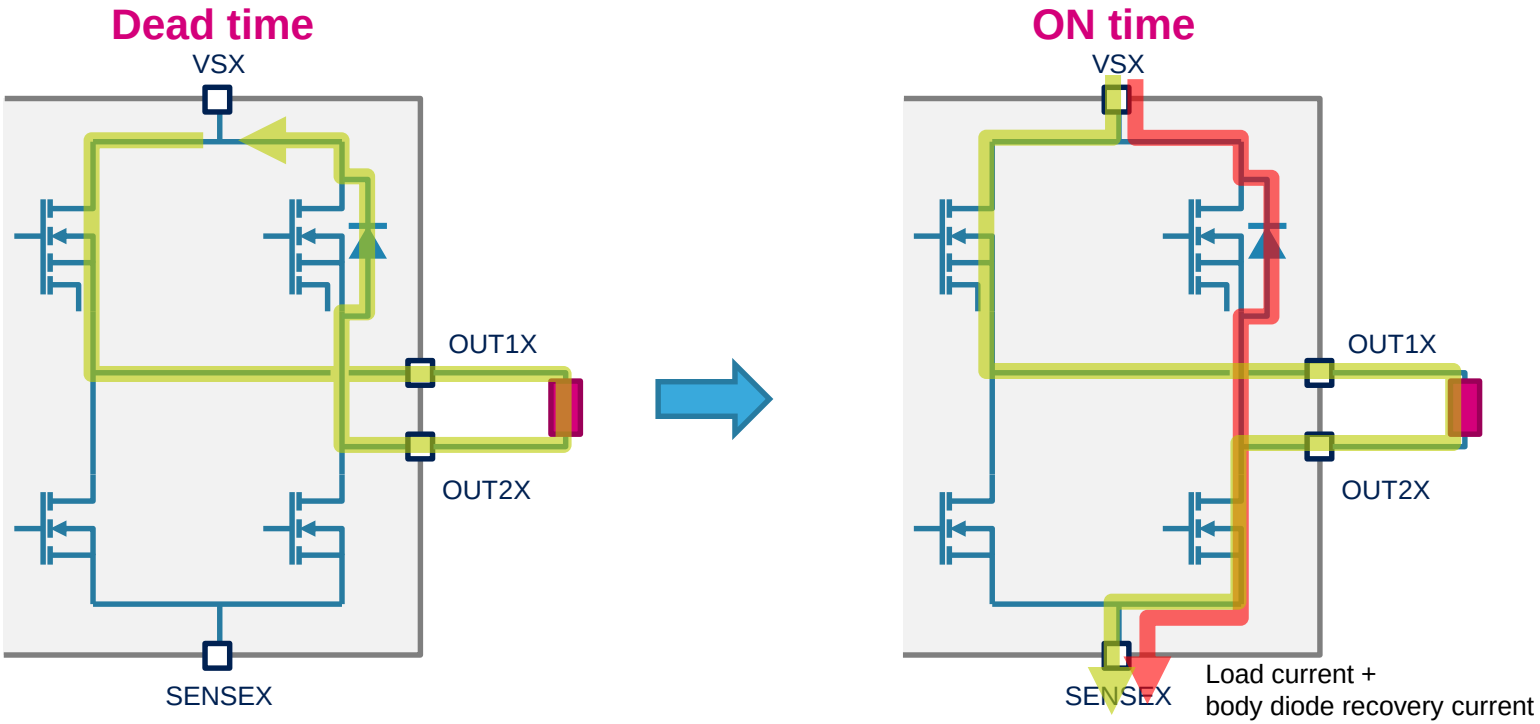
Every time the power bridge switches from the ON time to the OFF time and vice-versa, the switching side is kept for a short time in a high impedance state (both MOSFETs are turned OFF).
This is called **dead time** and is needed to avoid cross-conduction.



PWM current control

When the power bridge switches from dead time to ON time, the turning OFF of the body diode generates a strong current spike which flows into the sense resistor.

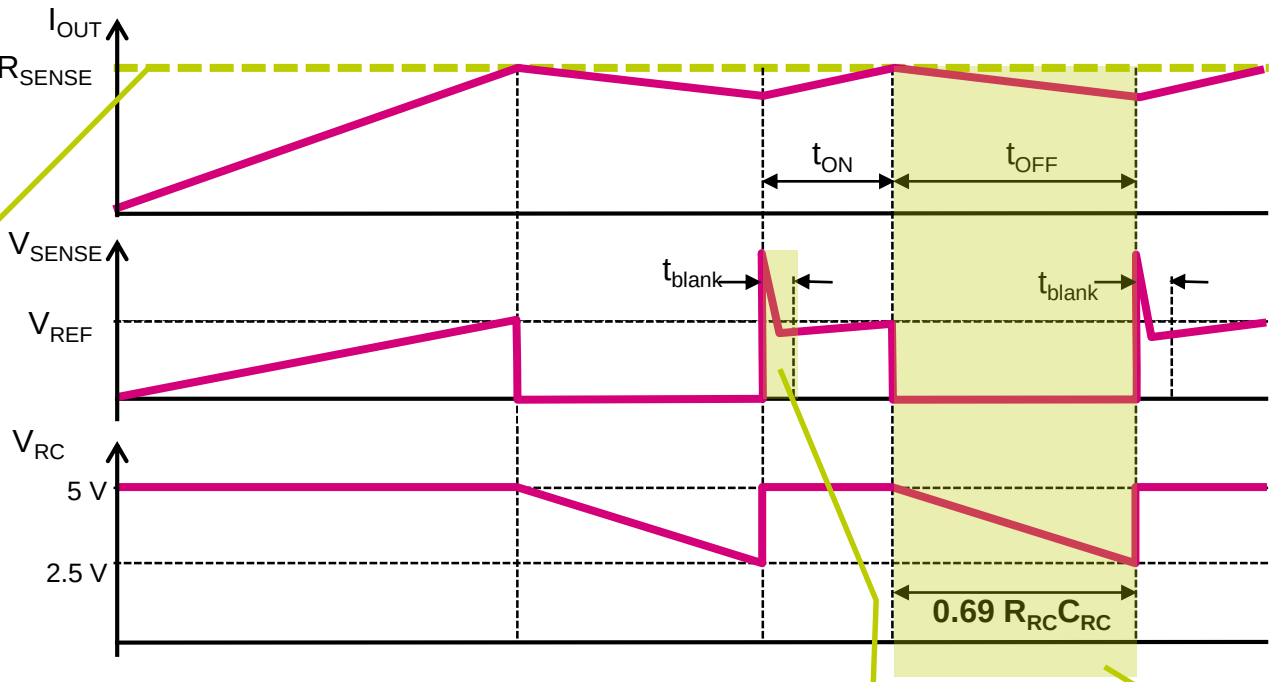
This spike is filtered by the blanking circuit in order to avoid spurious triggering of the PWM current control.



PWM current control

The peak current is set by the VREFX voltage according to the sense resistor:

$$I_{peak} = V_{REF}/R_{SENSE}$$



The 1 µs blanking time masks the current peaks due by the turn-off of the body diode.

The OFF time is defined by the RC network connected to the RCX pin:

$$t_{OFF} \approx 0.69 \cdot R_{RC} \cdot C_{RC}$$

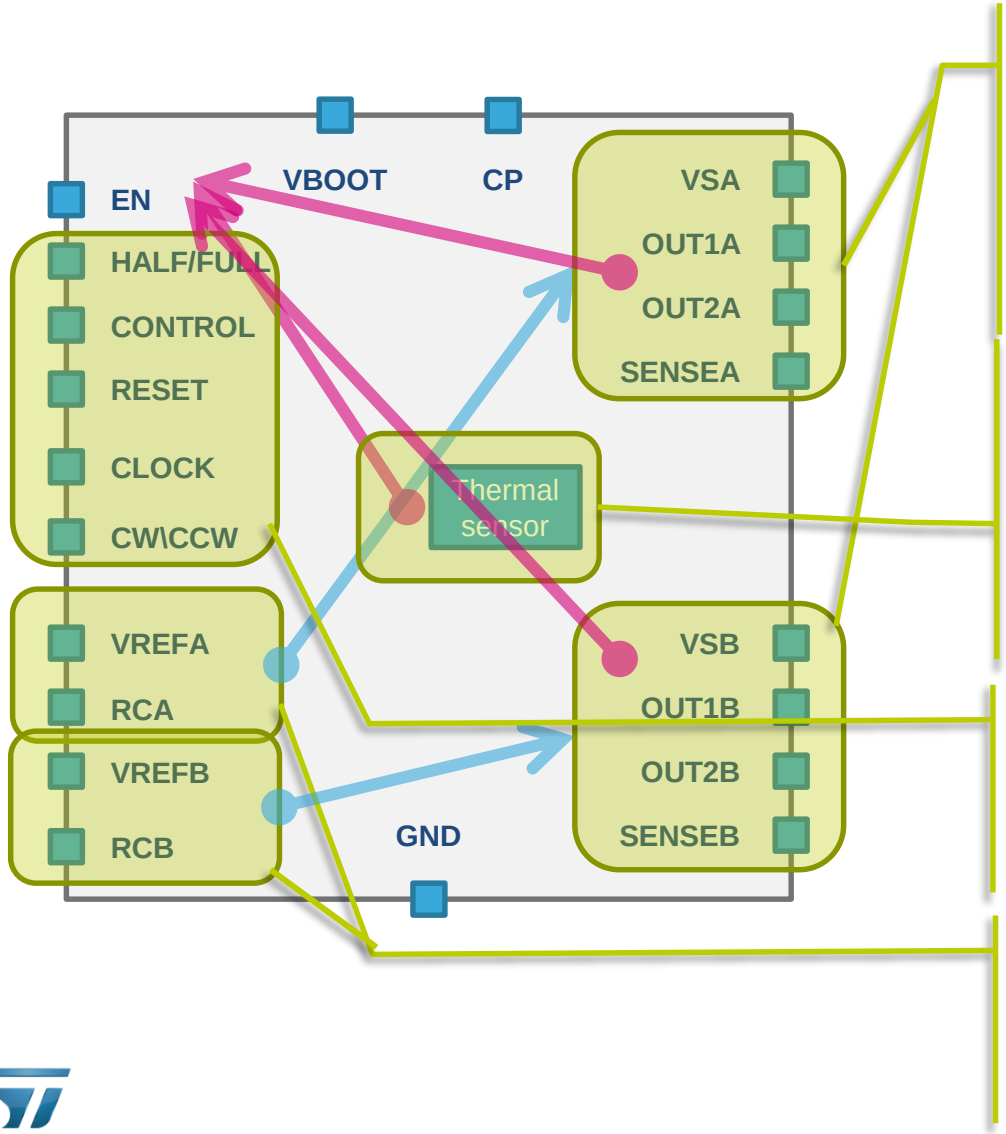
Shunt resistor selection

The sense resistor must be selected according to the **operative range of the SENSE** pin and the **power dissipation limit** of the resistor.

Trade-off for the sizing of the sense resistor

Higher values	Lower values
▪ Higher precision of the control of the peak current (comparator works better at higher voltages)	▪ Lower precision of the control of the peak current (offset of the comparator becomes significant)
▪ Higher power dissipation on the sense resistor	▪ Lower power dissipation on the sense resistor

A good trade-off can be obtained using a VREF voltage between 100 and 200 mV



Non-dissipative overcurrent protection @ 5.6 A (L6208) or 2.8 A (L6228)

When an overcurrent event occurs on one full-bridge, the respective EN pin is internally forced low.

Overtemperature protection

When the device temperature exceeds the shutdown threshold, both EN pins are internally forced low.

Stepper sequencer with clock and direction input and half/full step operation

Independent PWM current control with fixed OFF time for each full-bridge.

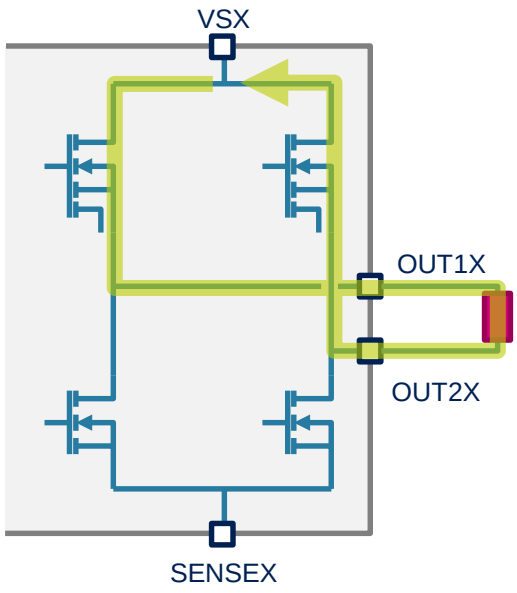
PWM current control in L62x8

The PWM current controller can be configured to use a **slow decay** or a **fast decay** through the CONTROL input.

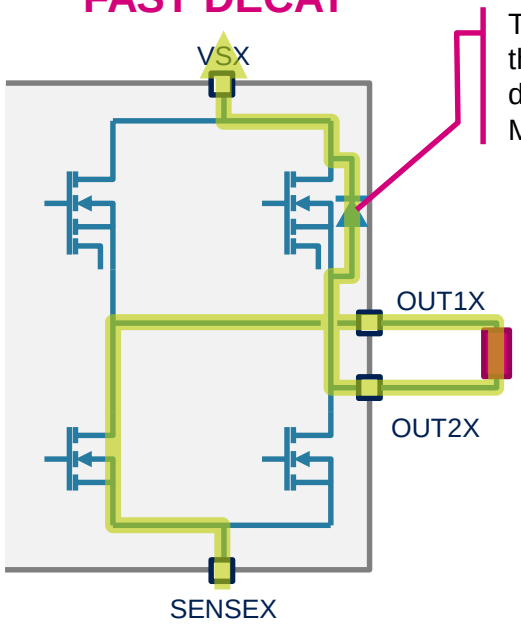
When the **slow decay** is set, the current recirculates on the **high-side MOSFETs**. This way the device is always protected against overcurrent events.

When the **fast decay** is set, the device performs a **quasi-synchronous rectification**. This way the load current cannot be inverted during the fast decay.

SLOW DECAY



FAST DECAY



PWM current control in L62x8

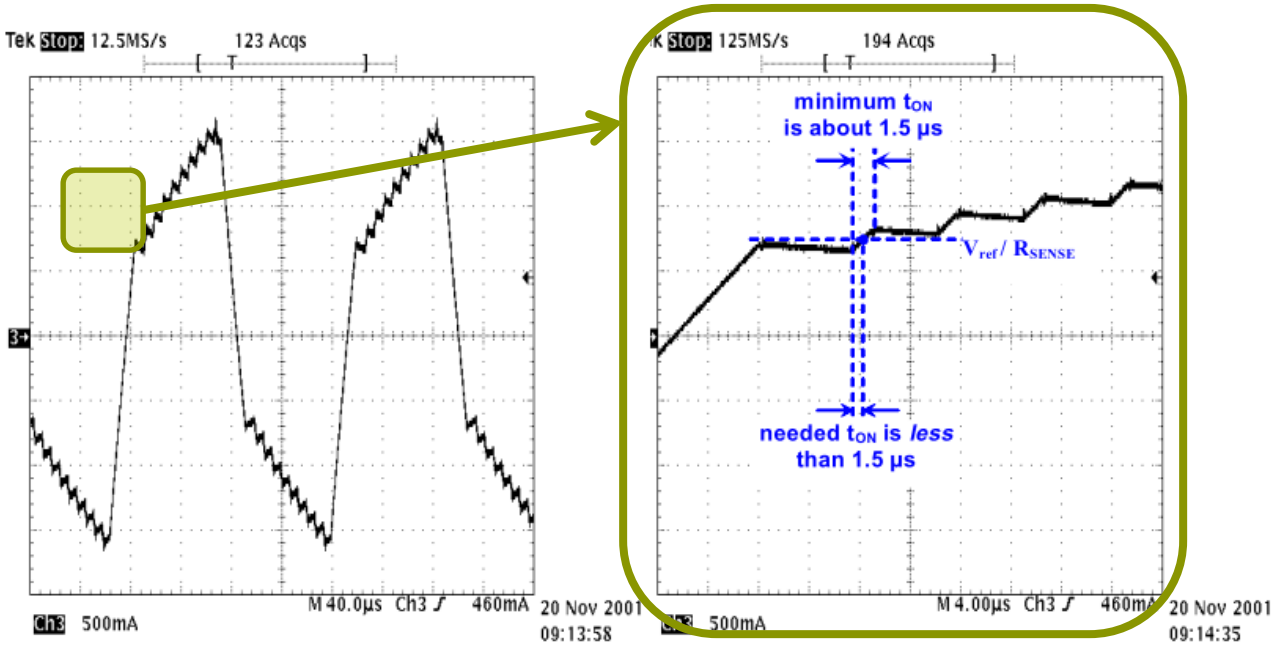
The decay mode should be selected according to the application needs

Slow decay	Fast decay
■ Lower current ripple at the same OFF time	■ Higher current ripple at the same OFF time
■ Lower power dissipation: the current always flows through the MOSFET (low $R_{ds(ON)}$)	■ Higher power dissipation: the current flows through the body diode (high equivalent $R_{ds(ON)}$)
■ Lower switching frequency: a longer OFF time is needed.	■ High switching frequency: a shorter OFF time is needed.
■ The control is less stable because it is more sensitive to the BEMF	■ The control is more stable because it is less sensitive to the BEMF

Minimum ON time

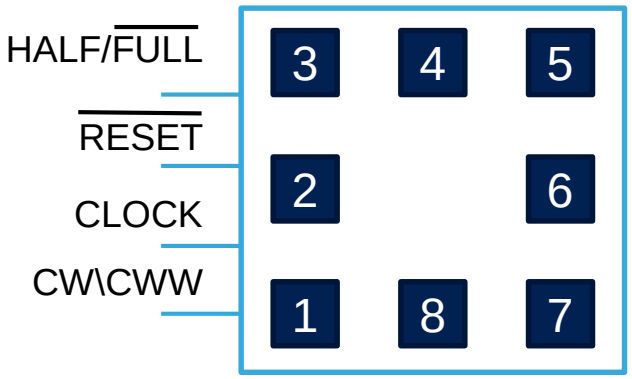
The PWM current control **must** turn on the phases for a **minimum time** in order to check the current value (otherwise current does not flows into the sense resistor).

This limit could cause the system to **lose the control of the current**:



Using the **fast decay** method, in most cases, avoids the occurrence of the minimum ON time issue.

Integrated state machine



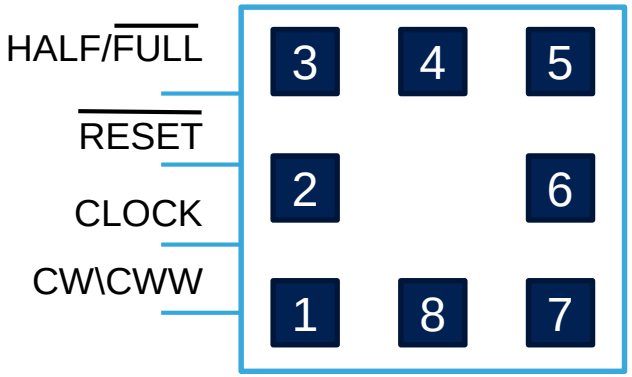
The device integrates a state machine which can perform full-step driving (normal or wave mode) or half-step driving according to the HALF/FULL input value.

Each state of the machine corresponds to a specific pair of phase currents.

1	2	3	4	5	6	7	8
I_{OUTA} = -	I_{OUTA} = 0	I_{OUTA} = +	I_{OUTA} = +	I_{OUTA} = +	I_{OUTA} = 0	I_{OUTA} = -	I_{OUTA} = -
I_{OUTB} = -	I_{OUTB} = -	I_{OUTB} = -	I_{OUTB} = 0	I_{OUTB} = +	I_{OUTB} = +	I_{OUTB} = +	I_{OUTB} = 0

NOTE: The current direction is forced by the state machine, the current level is determined by the respective PWM current control.

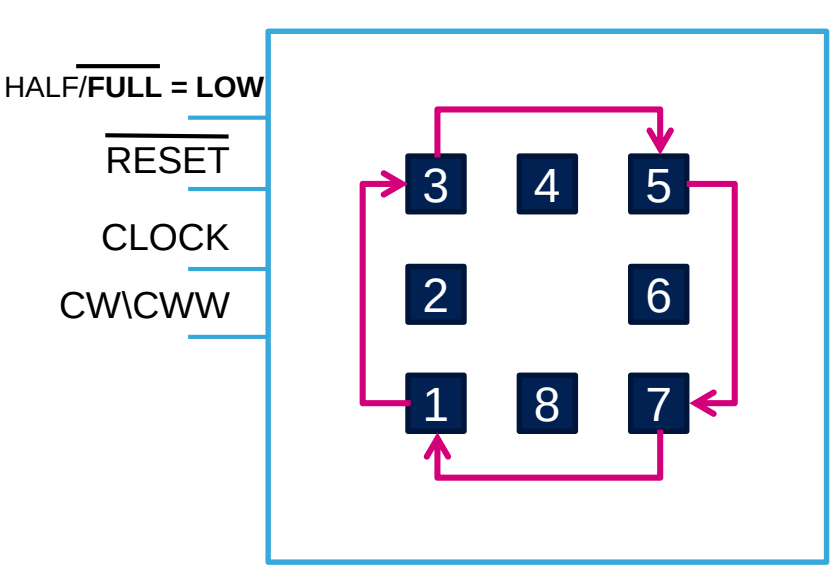
Integrated state machine

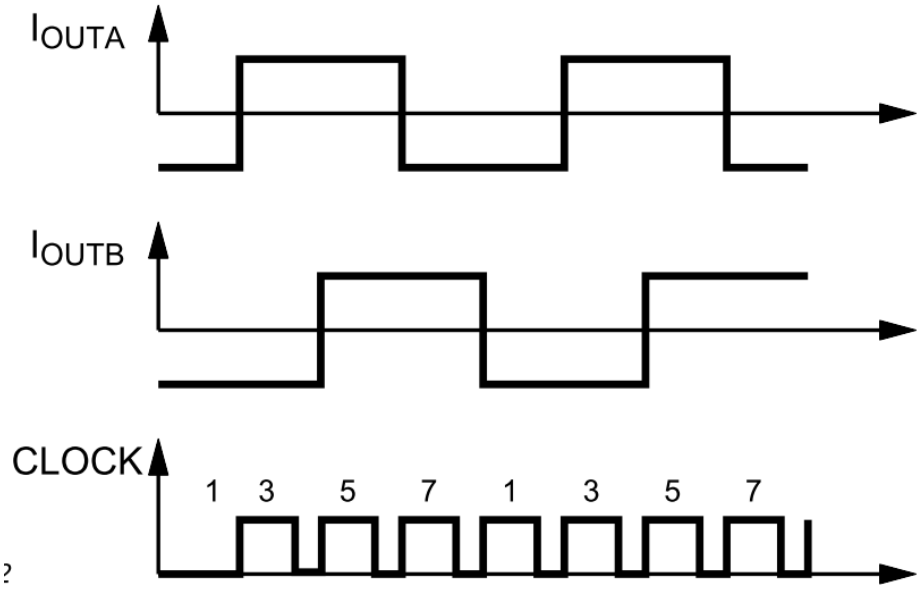


- RESET forces the state machine to the state 1 (active low).
- CLOCK makes the state machine jump to the next state.
- HALF/FULL determines if the next state is one (high) or two steps (low) away from the present one.
- CW\CCW determines the direction of the rotation of the state machine.

Integrated state machine

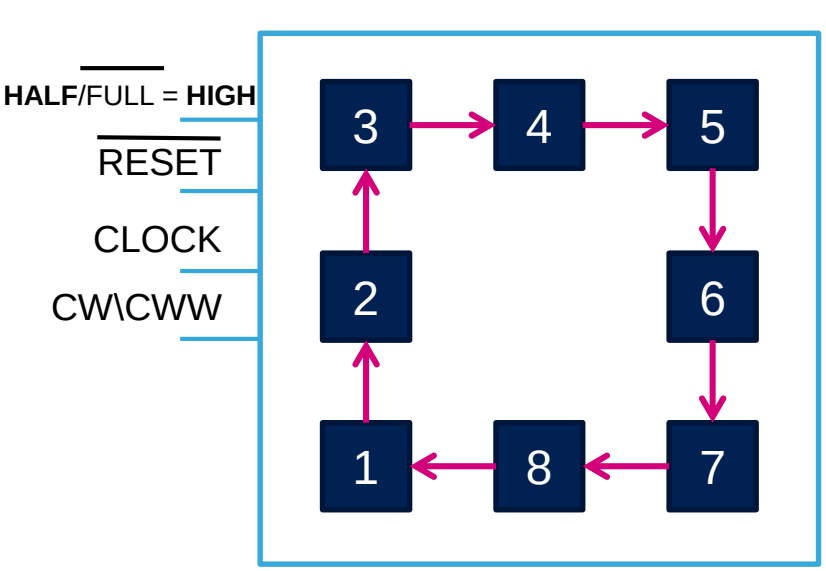
Full-step normal mode (2 phase on)

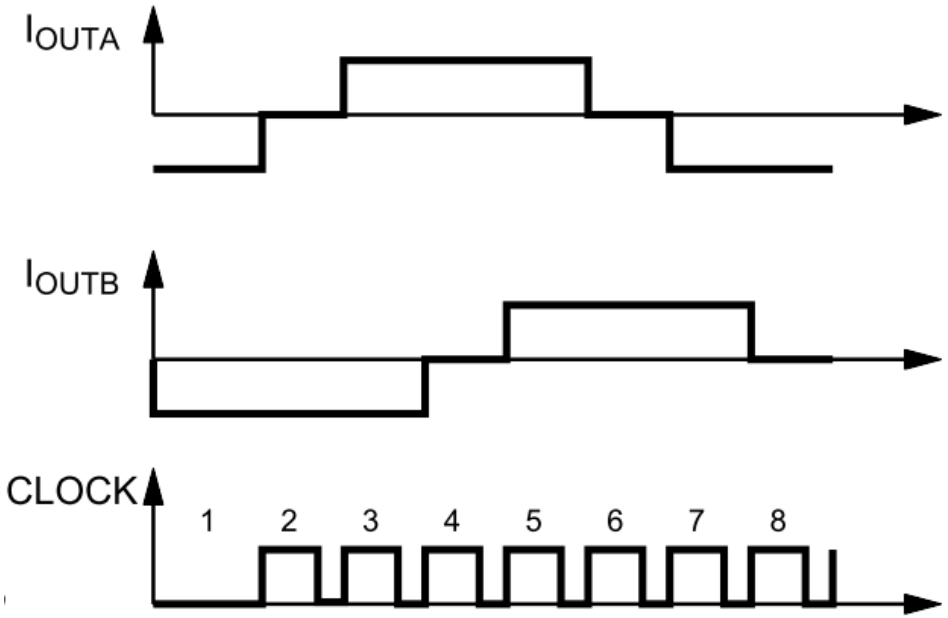




Integrated state machine

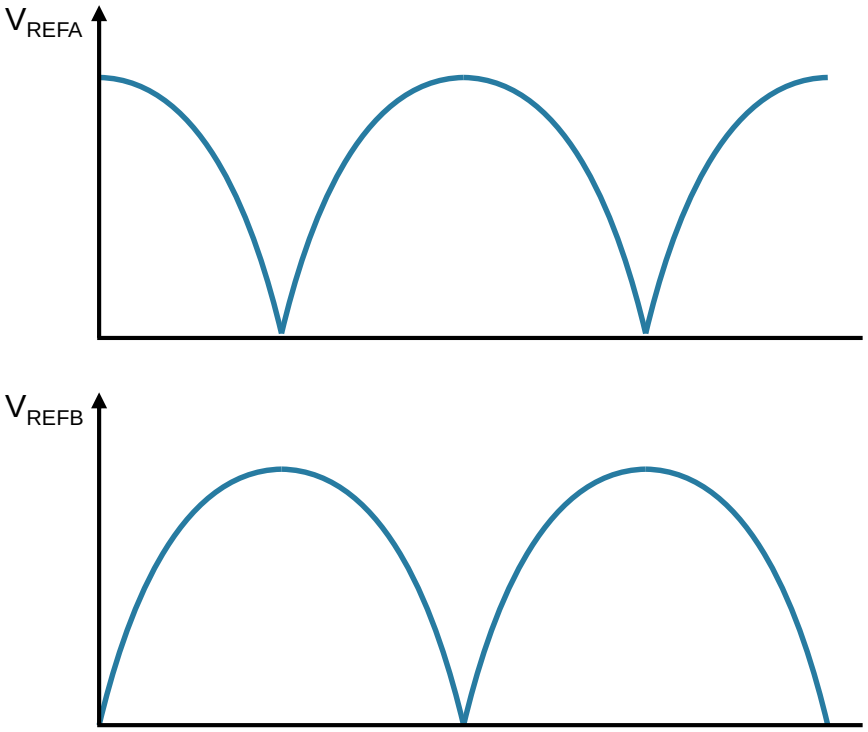
Half-step





Microstepping

The device can be used to perform **microstepping** driving applying a proper reference voltage for the two PWM current controllers.

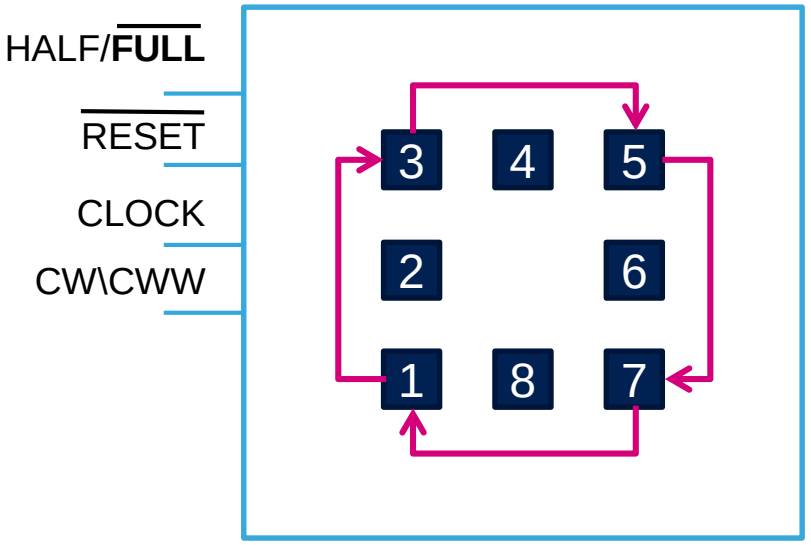


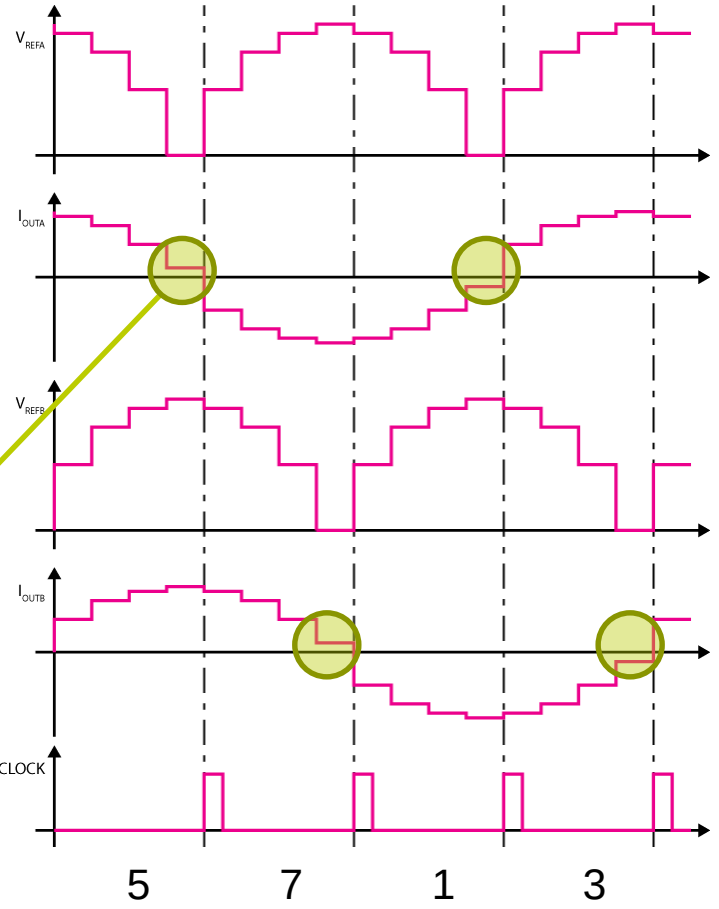
To obtain a sinusoidal phase current, the reference is a rectified sinewave.

A and B references are shifted 90° and must be kept synchronized with the clock and direction inputs.

Microstepping

Using the state machine in full-step configuration, the driving zero crossing of the current could be distorted.

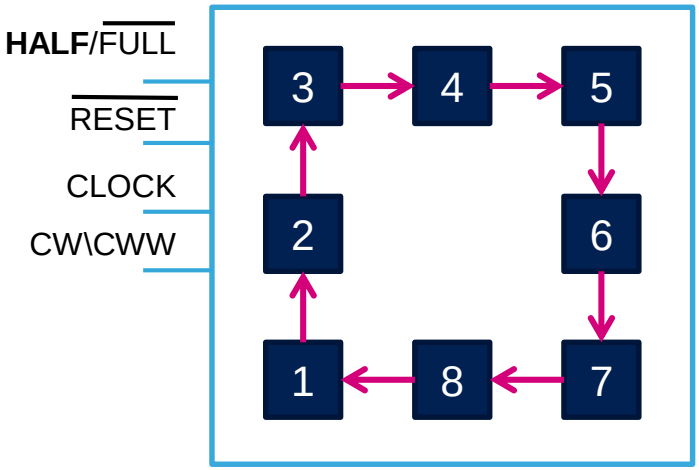


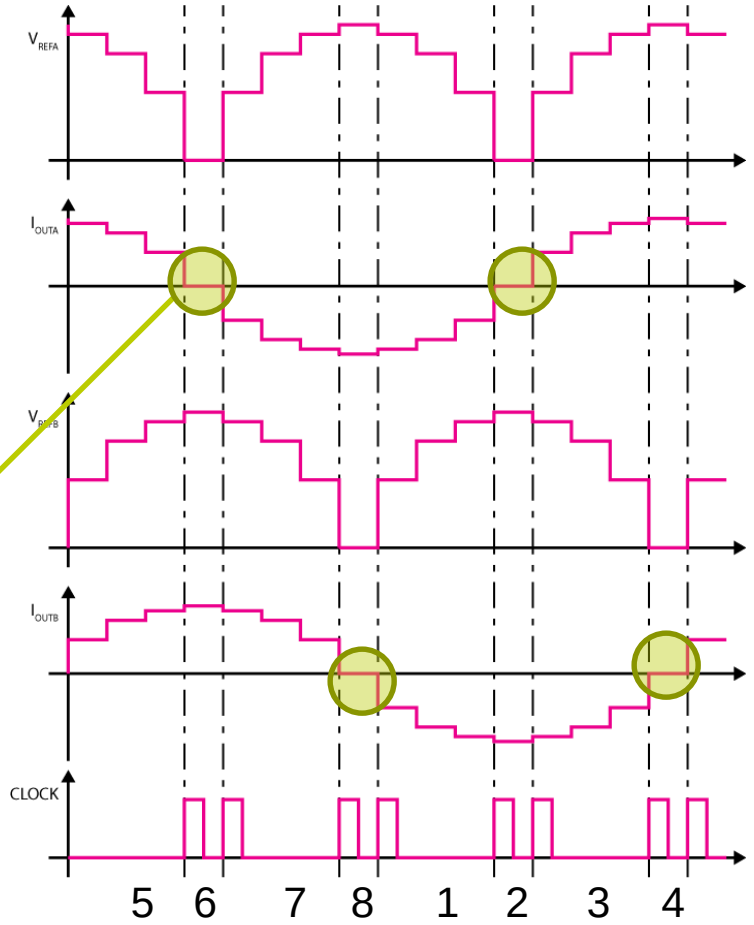


The current cannot be zero even if VREF = 0 due to control circuitry limitations.

Microstepping

Using the state machine in half-step configuration, the zero current is implemented correctly.

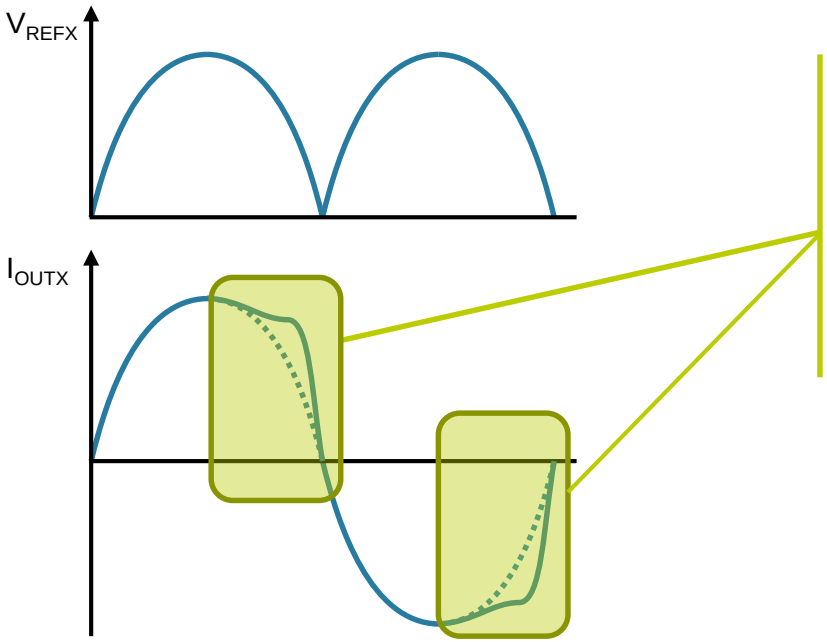




The zero crossing of the sinewave is a part of the control sequence of the half-step driving.

Microstepping

The decay mode heavily affects the performance of microstepping.

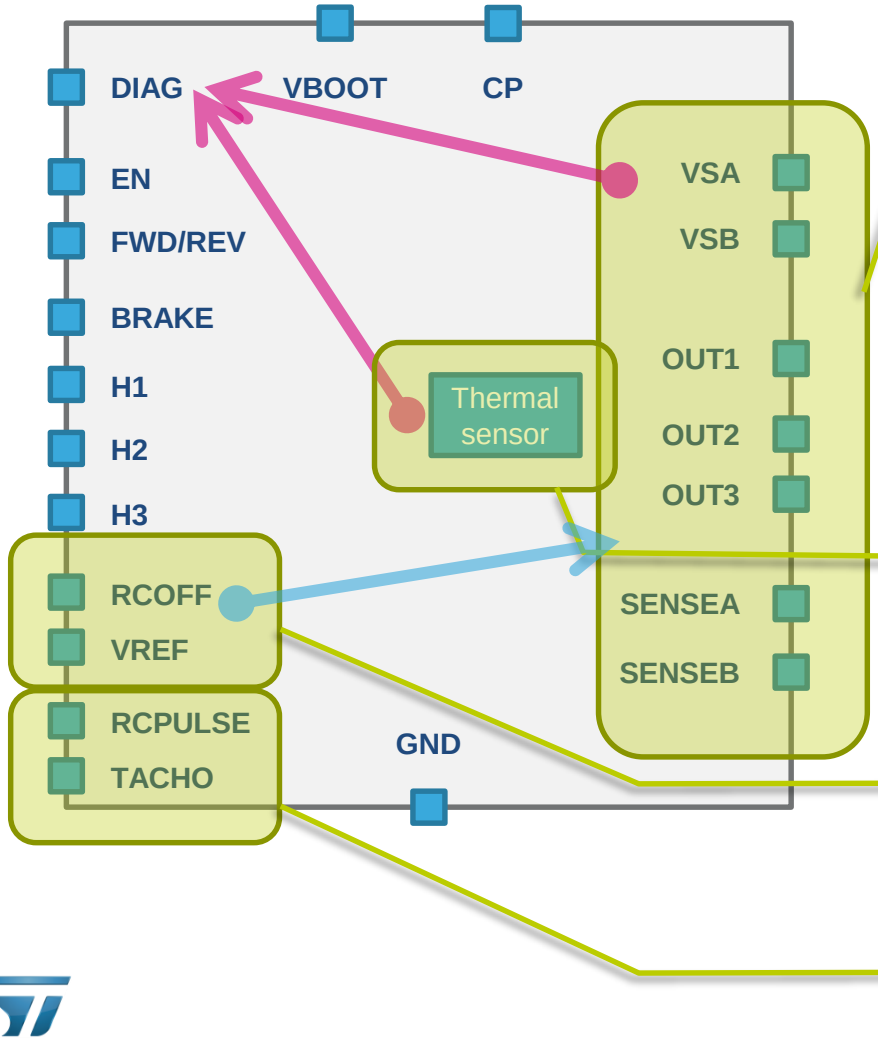


Using the slow decay, the negative slope of the sinewave can be heavily distorted:

the effectiveness of the decay at high speed or low currents is lower and the PWM control is no longer able to follow the requested profile.

The **mandatory** decay mode for microstepping is **fast decay**.

L6235 and L6229



Non-dissipative overcurrent protection @ 5.6 A (L6235) or 2.8 A (L6229)
When an overcurrent event occurs on one half-bridge, the DIAG pin is internally forced low.

Over-temperature protection
When the device temperature exceeds the shutdown threshold, the DIAG pin is internally forced low.

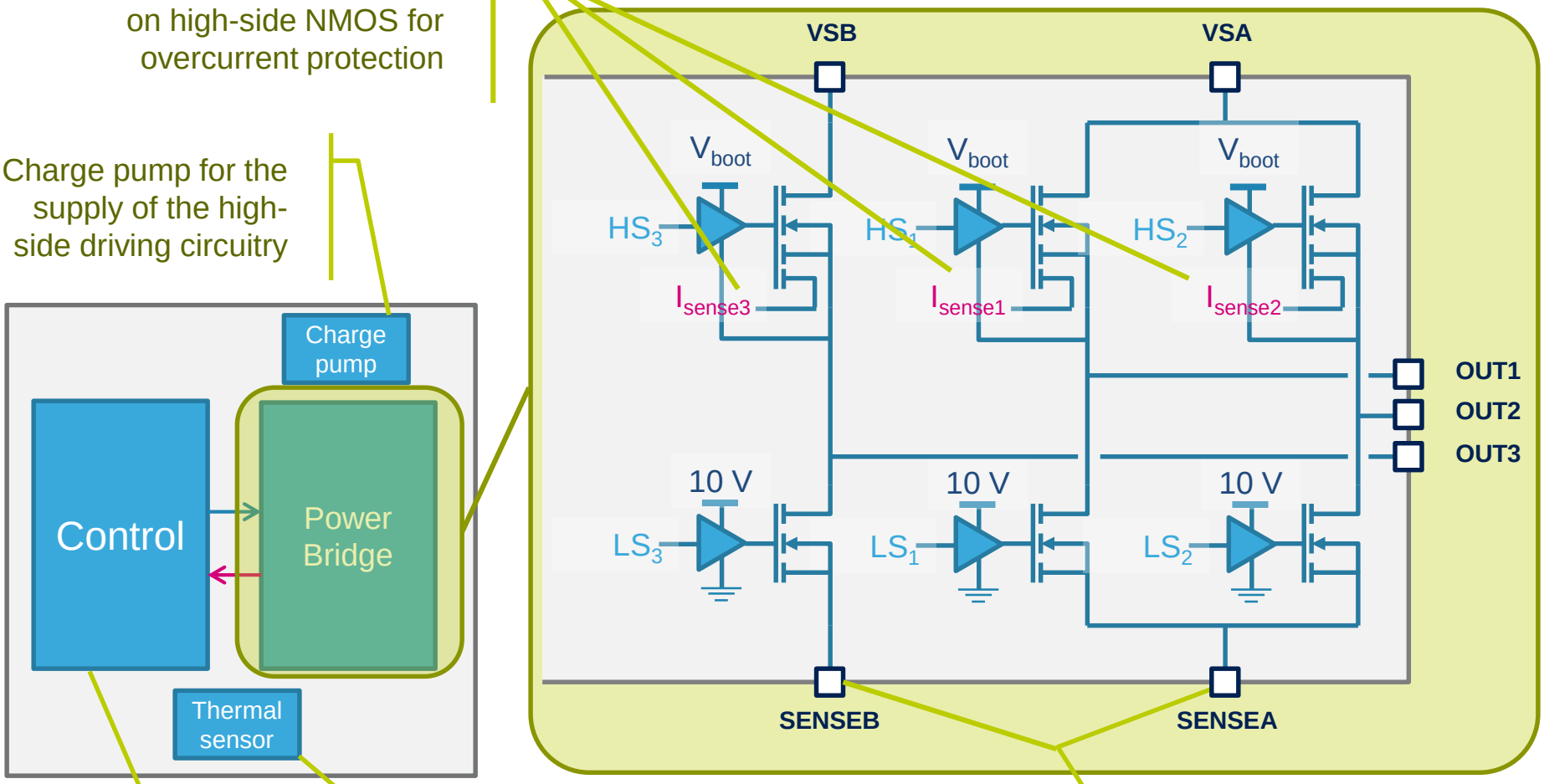
PWM current control with fixed OFF time.

TACHO output for easy implementation of an analog speed loop

Triple half-bridge

Integrated current sensing on high-side NMOS for overcurrent protection

Charge pump for the supply of the high-side driving circuitry



Control circuitry

Thermal protection

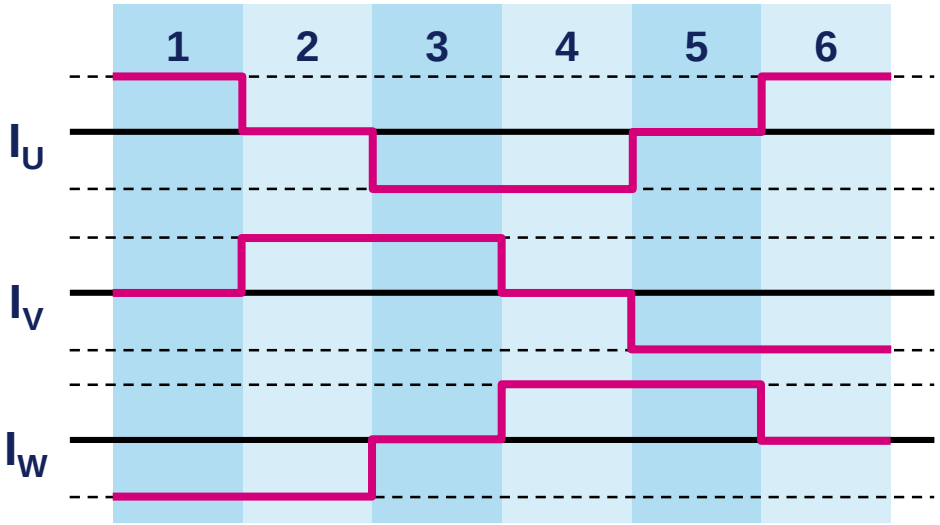
H-bridge tail available for shunt resistor (3 separated SENSE pins in the L6230)

life.augmented

6-step driving and Hall decoding

The device implements a 6-step control based on the Hall effect information.

- Hall effect decoding imposes the phase combination according to the direction selected by FWD/REV pin.
- PWM current control limits the phase current (torque control).



6-step driving and Hall decoding

The device integrates a control logic for the decoding of the Hall sensors

				Forward direction			Backward direction		
#	H1	H2	H3	OUT1	OUT2	OUT3	OUT1	OUT2	OUT3
1	H	L	L	VS	High Z	PWM	PWM	High Z	VS
2	H	H	L	High Z	VS	PWM	High Z	PWM	VS
3(1)	L	H	L	PWM	VS	High Z	VS	PWM	High Z
3b(2)	H	H	H	PWM	VS	High Z	VS	PWM	High Z
4	L	H	H	PWM	High Z	VS	VS	High Z	PWM
5	L	L	H	High Z	PWM	VS	High Z	VS	PWM
6(1)	H	L	H	VS	PWM	High Z	PWM	VS	High Z
6b(2)	L	L	L	VS	PWM	High Z	PWM	VS	High Z

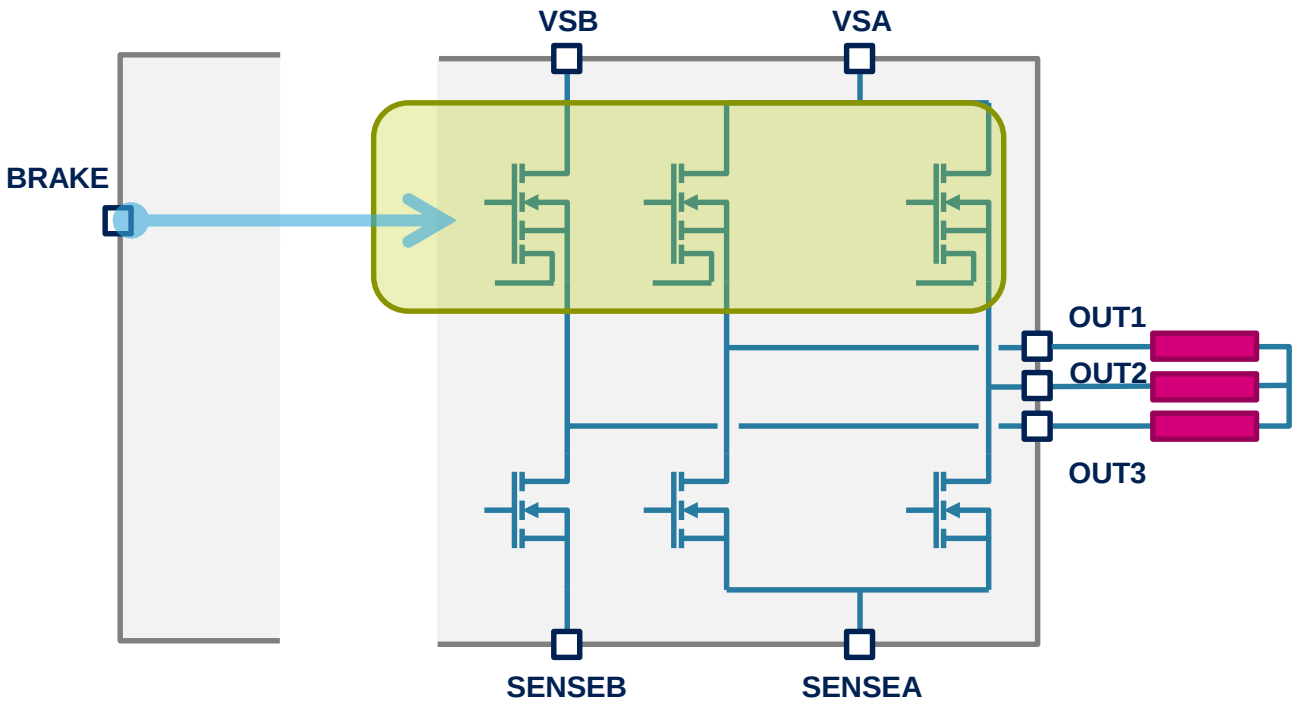
(1) **NOTE:** This combination is used when 120° Hall sensors are mounted

(2) **NOTE:** This combination is used when 60° Hall sensors are mounted

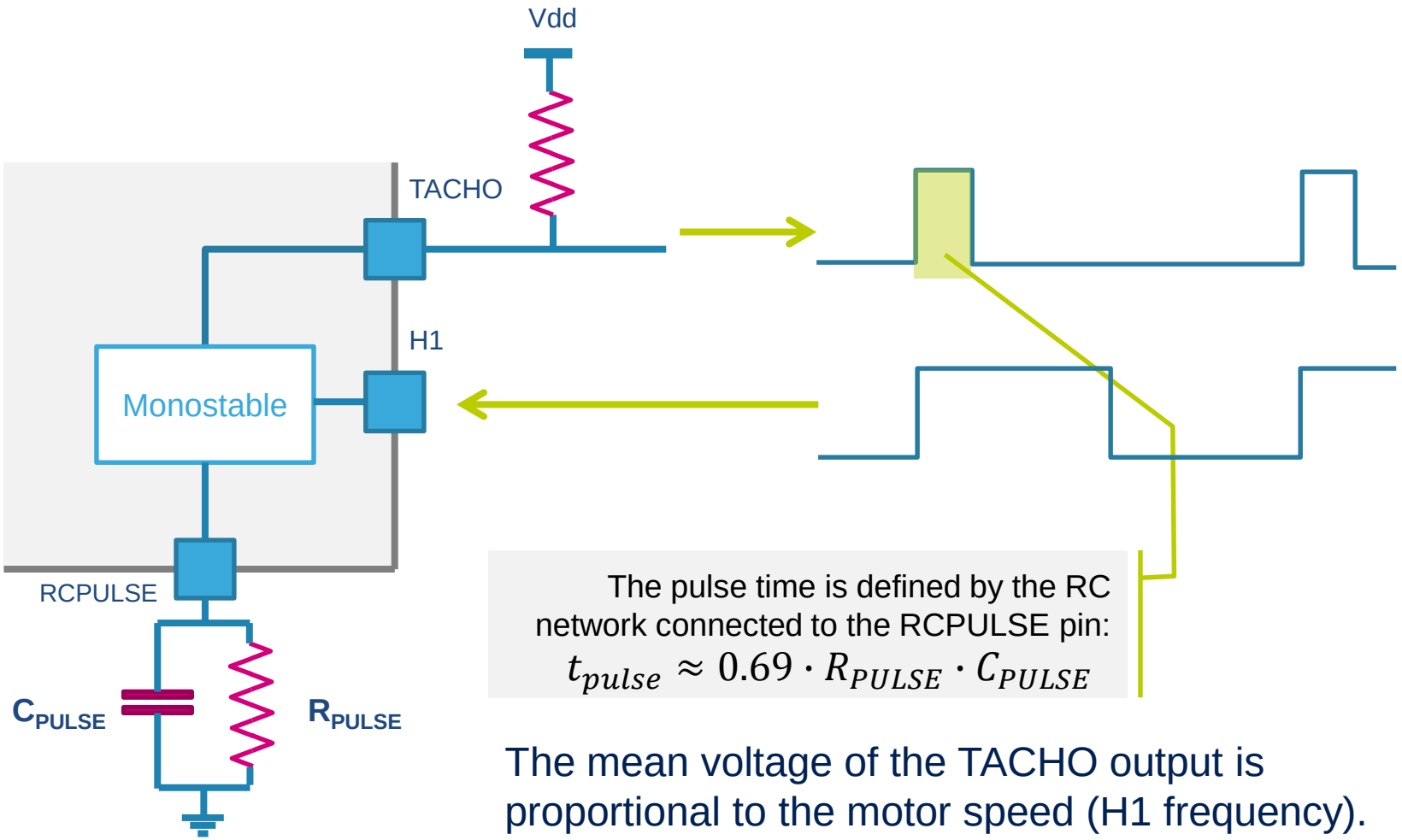
Protected BRAKE function

When the BRAKE input is forced low, all the high-side MOSFETs of the three half-bridges are immediately turned ON stopping the motor.

The overcurrent protection is still active protecting the device.



TACHO



The pulse time is defined by the RC network connected to the RCPULSE pin:

$$t_{pulse} \approx 0.69 \cdot R_{PULSE} \cdot C_{PULSE}$$

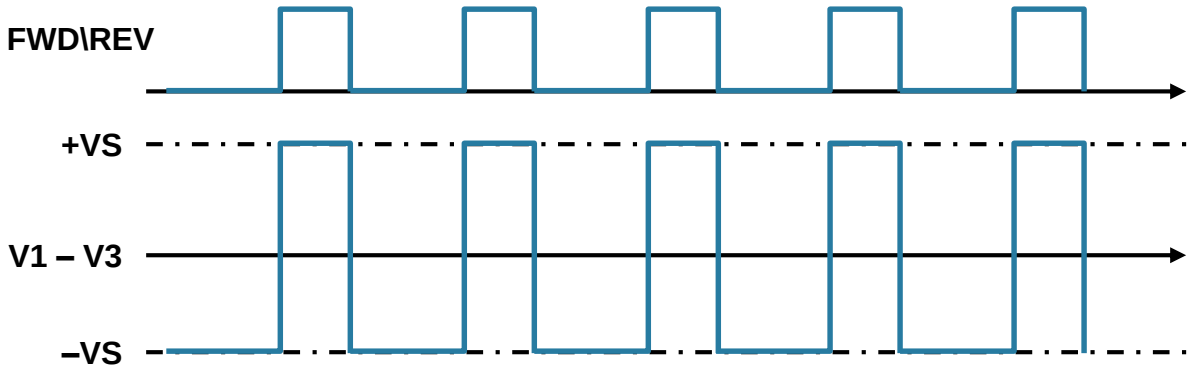
The mean voltage of the TACHO output is proportional to the motor speed (H1 frequency). This can be used as a feedback for an analog speed loop.

6-step voltage mode

It is possible to drive the motor using a voltage mode technique instead the PWM current control.

Applying a PWM on the **FWD\REV** pin it is possible to apply a controlled 6-step voltage on the motor phases:

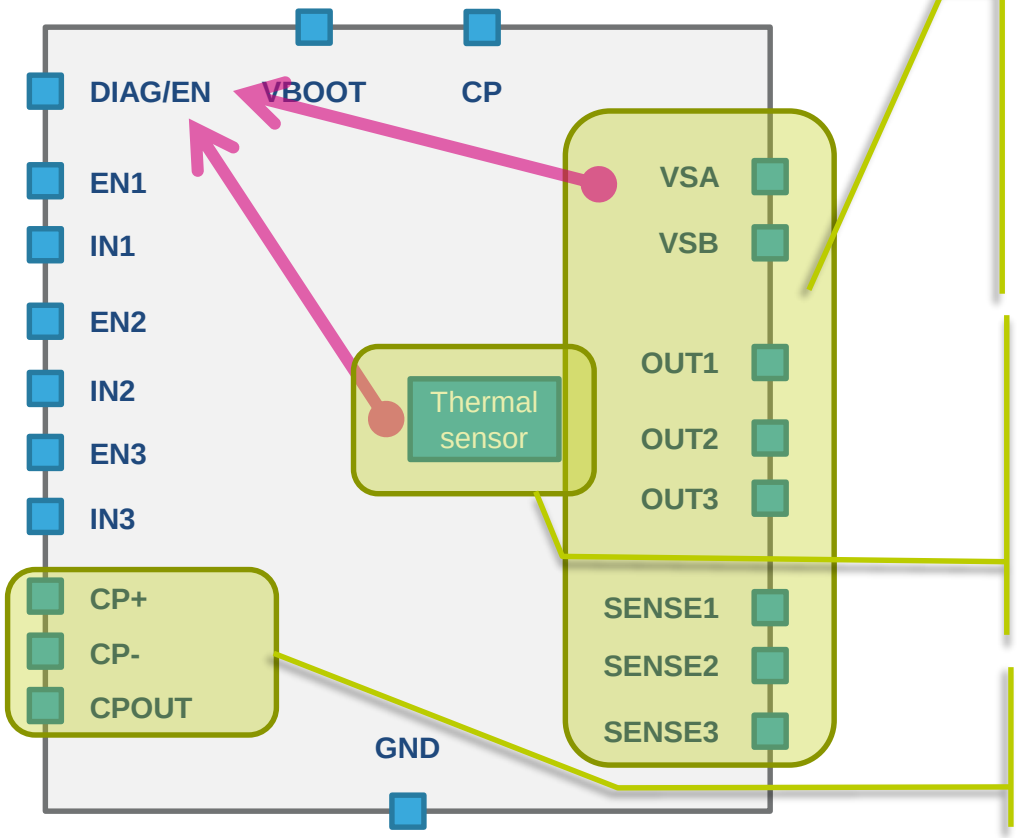
H1	H2	H3
H	L	L



The mean voltage applied between the two motor phases is:

$$V_{13} = V_S \cdot DutyCycle - V_s \cdot (1 - DutyCycle)$$

NOTE: In this case the PWM current control could be used as a current limiter



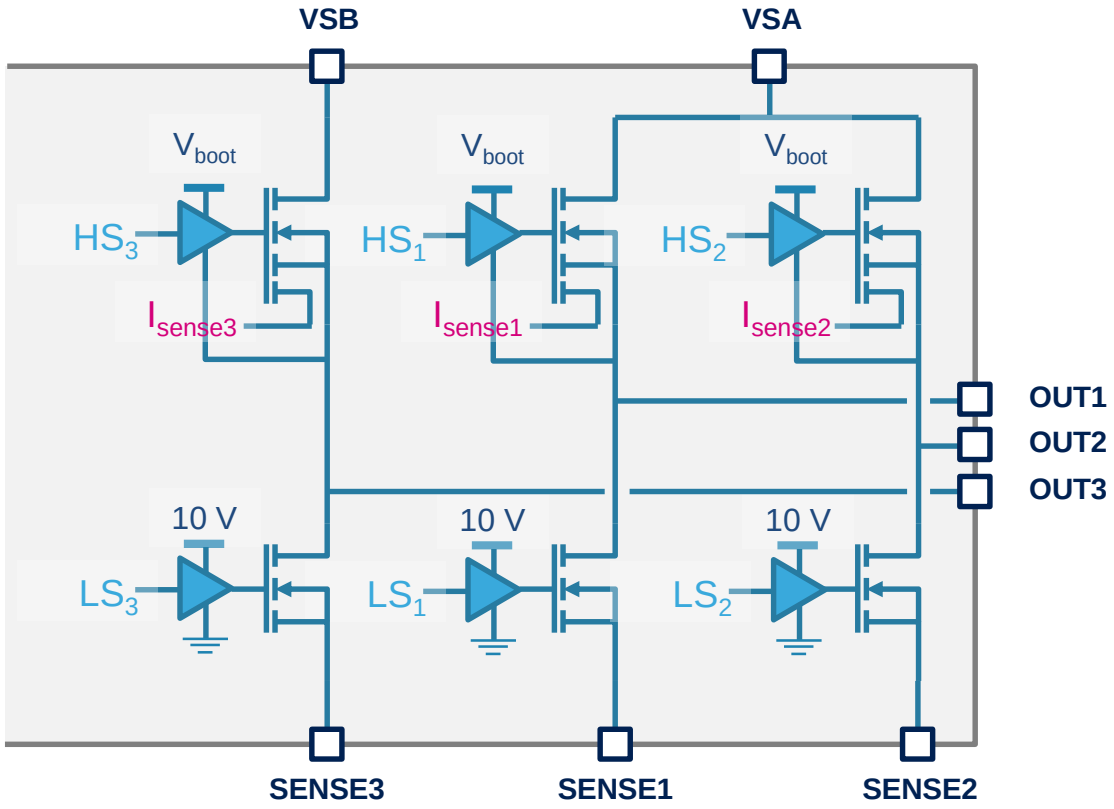
Non dissipative overcurrent protection @ 2.8 A
When an overcurrent event occurs on one half-bridge, the DIAG pin is internally forced low.

Over-temperature protection
When the device temperature exceeds the shutdown threshold the DIAG pin is internally forced low.

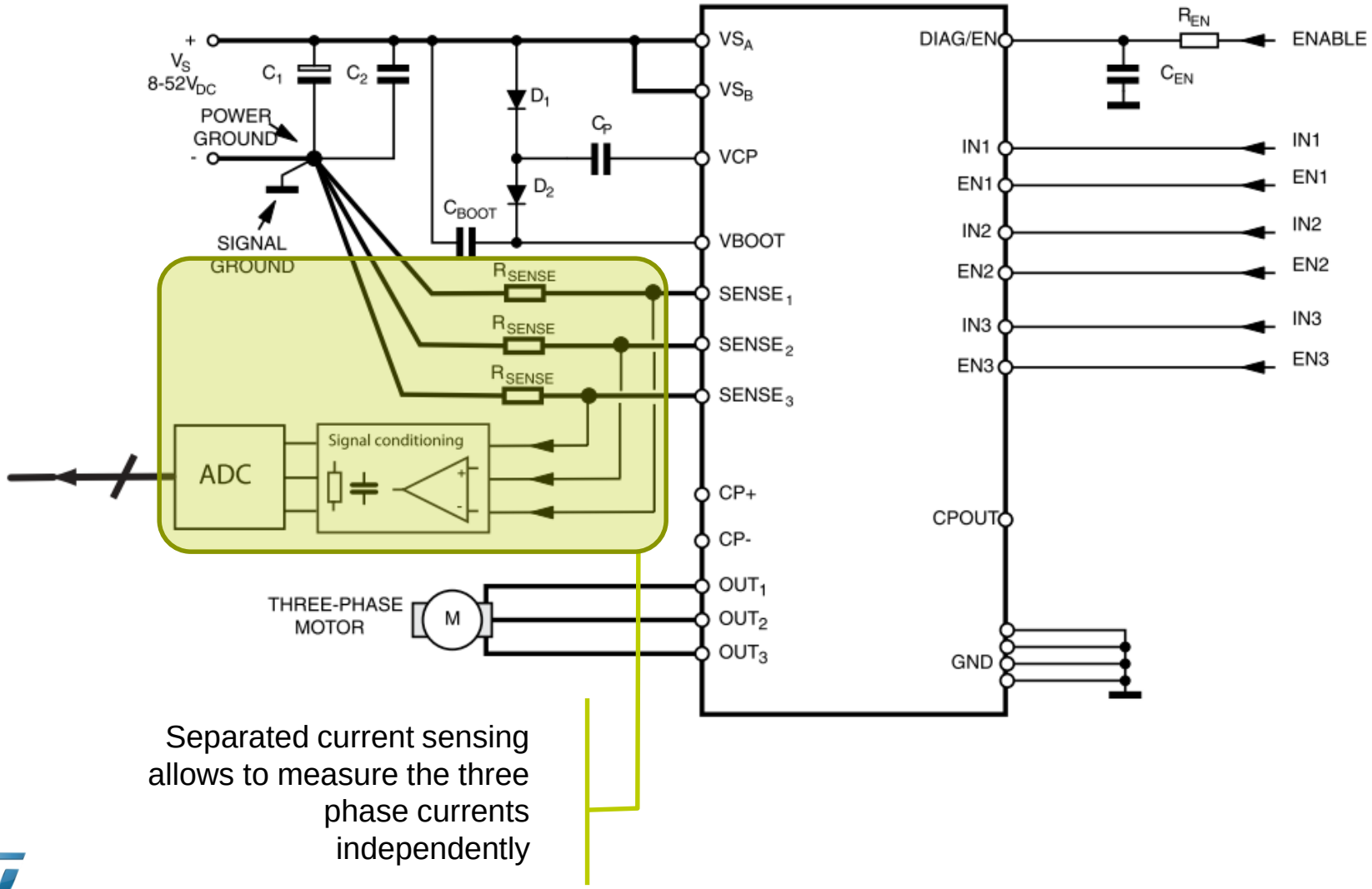
Integrated comparator at user disposal.

Separated sense pins

The three separated sense pins makes the L6230 suitable for the most advanced control methods such as Field Oriented Control.



L6230: Field oriented control example



Separated current sensing allows to measure the three phase currents independently

Current rating vs. power dissipation

The **current rating** of the power stage is determined by the design of the integrated circuitry.

The maximum **power dissipation** is determined by the thermal performance of the application (package, layout, ambient temperature).

The power dissipation limit is usually stricter than the one imposed by the circuitry.

Current rating vs. power dissipation

A practical example:

L6206 in PowerSO package with optimal layout @ ambient temperature of 25 °C

Maximum power dissipation allowed by the thermal design:

$$P_{max} = \frac{T_{j,max} - T_{amb}}{R_{th,ja}} = \frac{150°C - 25°C}{15°C/W} = \mathbf{8.33\ W}$$

Maximum junction temperature

Junction to ambient thermal resistance

Power dissipation due to the maximum allowed current:

$R_{ds(ON)}$ of the high side and low side MOSFETs @ 125 °C

Maximum output current (r.m.s.)

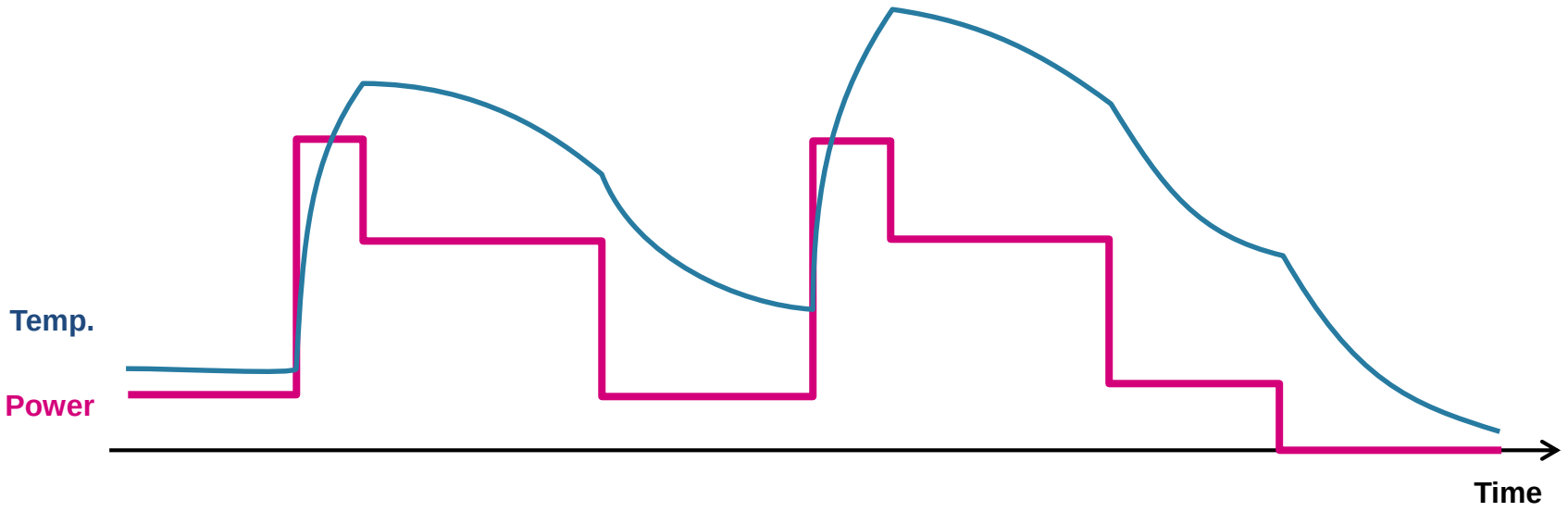
$$P_{diss} = 2 \times \left(R_{ds(ON)HS} + R_{ds(ON)LS}\right) \times I_{max}^2 =$$

$$= 2 \times (0.53\ \Omega + 0.47\ \Omega) \times 2.8^2\ A^2 = \mathbf{15.68\ W}$$

Package selection and thermal design

In order to define the most suitable package for a specific application, the **profile of the operative current** and the **ambient temperature** must be considered.

The profile of the operative current defines the expected power vs. time chart and the respective trend of the junction temperature.



Package selection and thermal design

A practical example:

A constant load current of 1 A @ ambient temperature of 40 °C

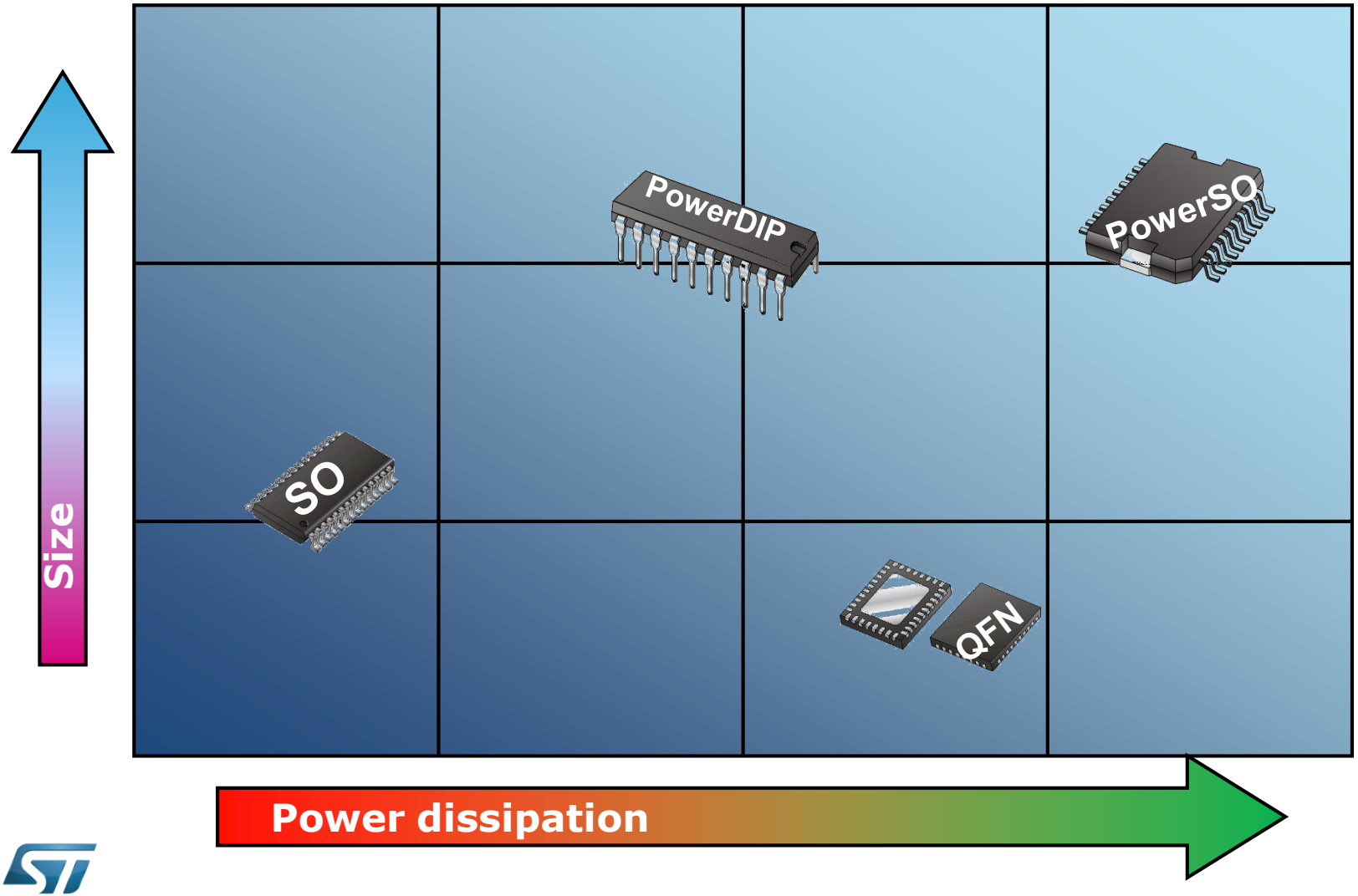
$$P_{diss,0X} = 2 \times \left(R_{ds(ON)HS} + R_{ds(ON)LS}\right) \times {I_{max}}^2 =$$
$$= 2 \times (0.53\ \Omega + 0.47\ \Omega) \times 1^2\ A^2 = \mathbf{2\ W}$$
$$P_{diss,2X} \approx 2 \times P_{diss,0X} = \boldsymbol{4\ W}$$

Expected junction temperature

$$T_j = P_{diss} \times R_{th,ja} + T_{amb}$$

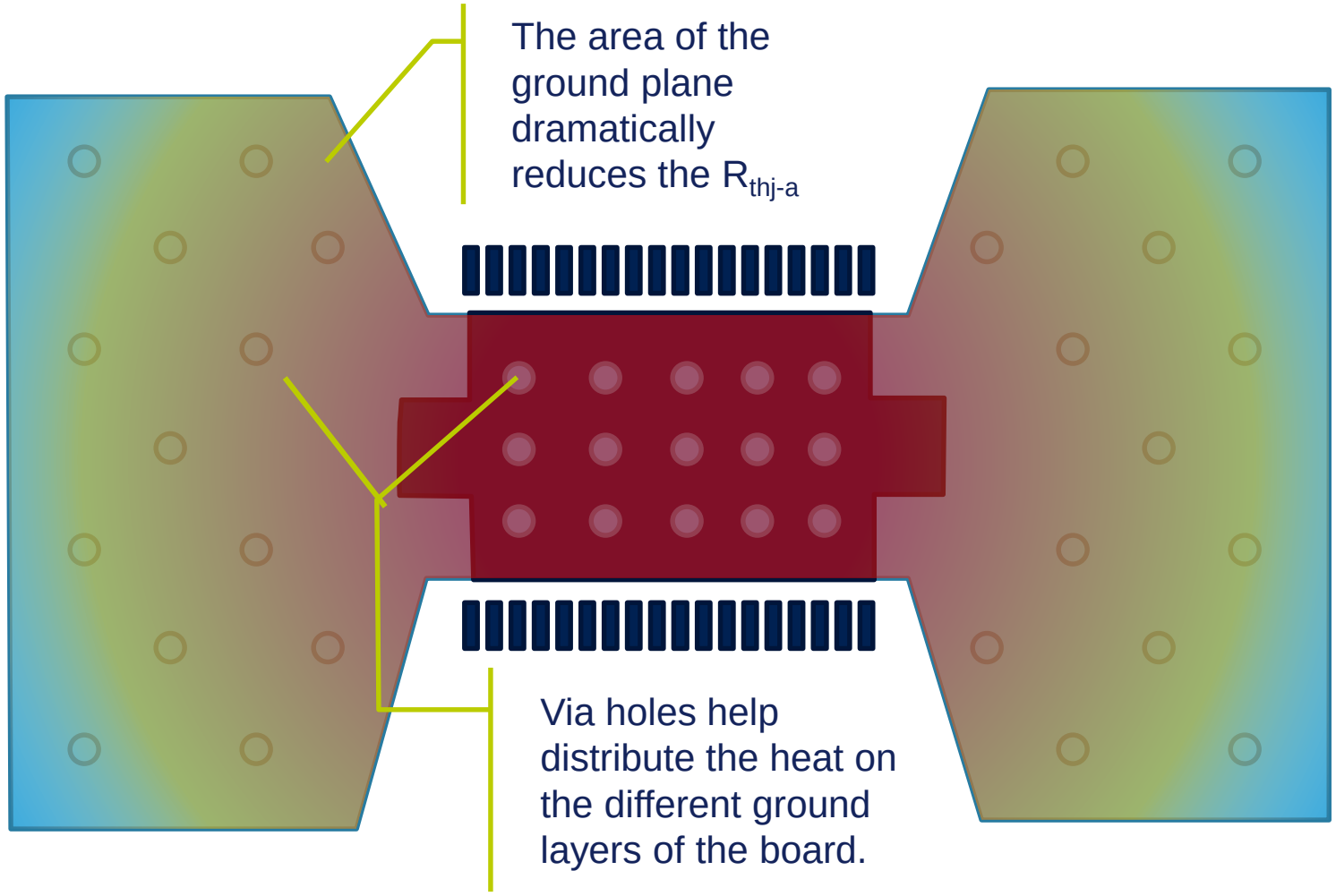
	QFN5x5 R_{thja} = 35 °C/W	QFN7x7 R_{thja} = 23 °C/W	SO R_{thja} = 51 °C/W	PDIP R_{thja} = 33 °C/W	PowerSO R_{thja} = 15 °C/W
L620X		86 °C	142 °C	106 °C	70 °C
L622X	180 °C		244 °C	172 °C	100 °C

Package selection and thermal design



Package selection and thermal design

The board layout is a critical part of the thermal design of the application.

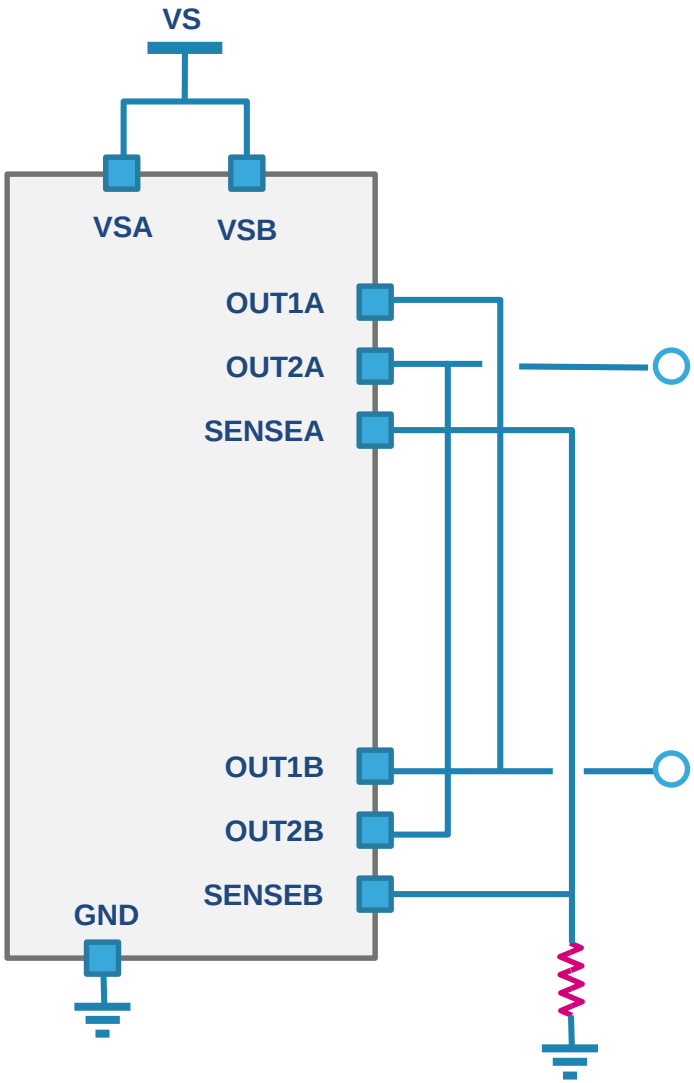


Package selection and thermal design

Layout suggestions:

- If the package has an **exposed pad** (e.g. PowerSO and QFN), it must be **connected to all the ground planes** of the board using **many via holes**.
- The **top and the bottom ground planes** of the board give the higher contribution to the power dissipation. The area of those layers **must be maximized**.
- **Connecting the ground planes** of the board with a diffused **grid of via holes** helps ensure a better distribution of the heat.

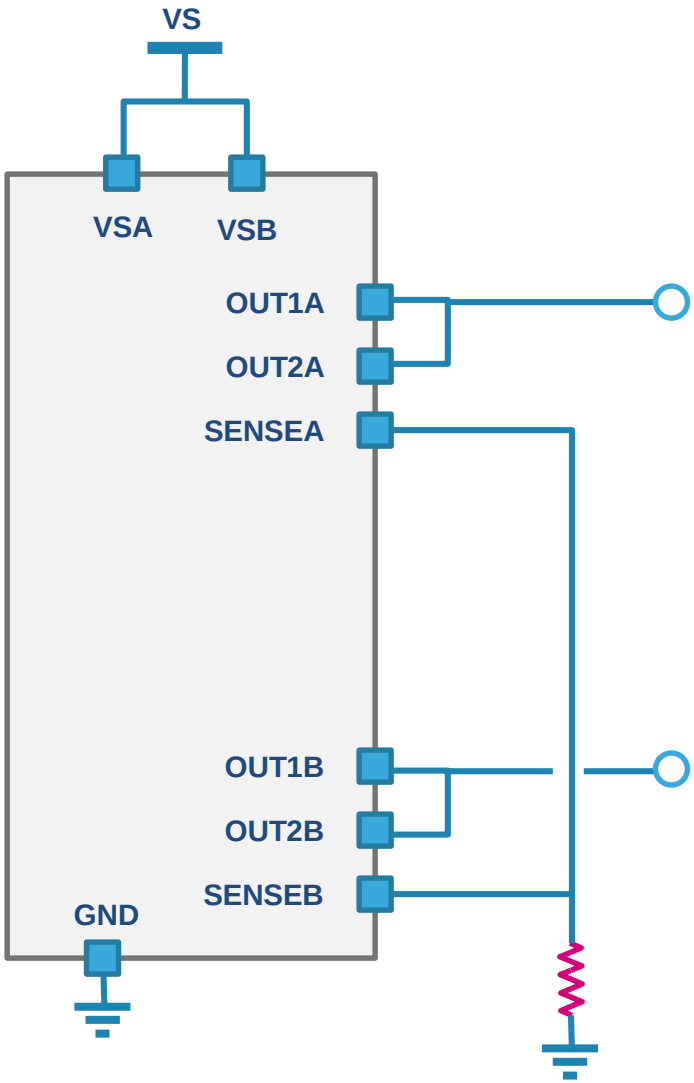
Paralleling



L62x5 and L62x6 only

- Equivalent $R_{DS(ON)}$: **0.15 Ω** Typ. (0.3 Ω for L622x)
- Max. RMS current: **5.6 A** per Eq. Half bridge (2.8 A for L622x) **1 at a time**
- Max. peak current: **11.2 A** per Eq. Half Bridge (5.6 A for L622x) **1 at a time**
- Overcurrent threshold: **11.2 A** per Eq. Half Bridge (5.6 A for L622x) **1 at a time**

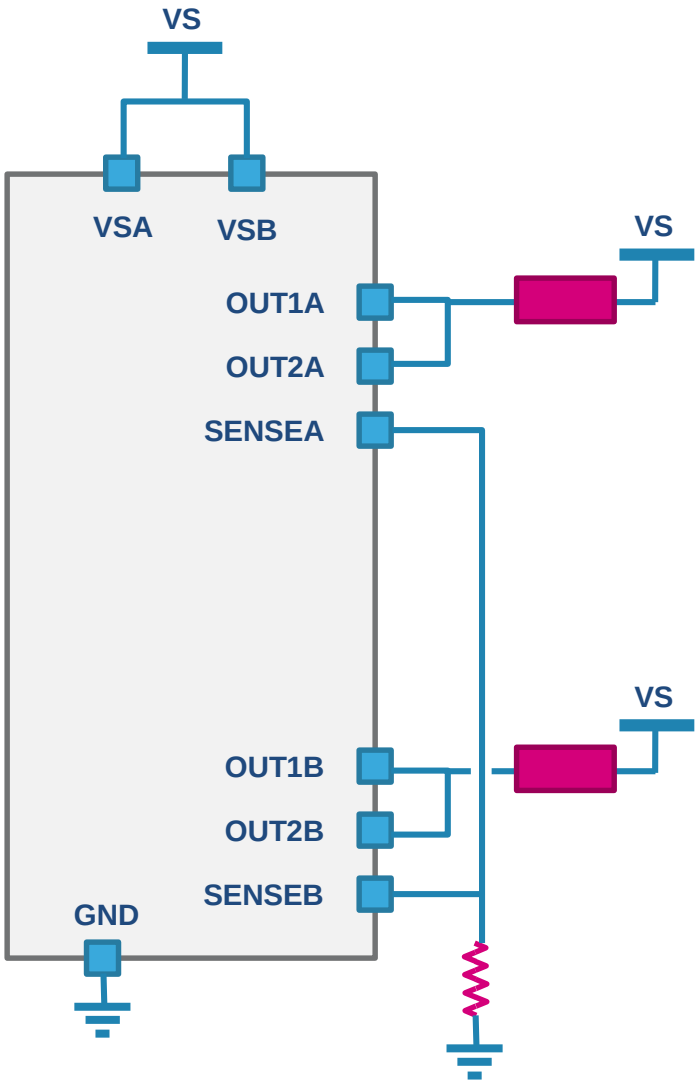
Paralleling



L62x5 and L62x6 only

- Equivalent $R_{DS(ON)}$: **0.15 Ω** Typ. (0.3 Ω for L622x)
- Max. RMS current: 2.8 A per Eq. Half bridge (1.4 A for L622x)
- Max. peak current: 5.6 A per Eq. Half Bridge (2.8 A for L622x)
- Overcurrent threshold: 5.6 A per Eq. Half Bridge (2.8 A for L622x)

Paralleling



This is the only parallel configuration available for the L62x7 devices

- Equivalent $R_{DS(ON)}$: **0.15 Ω** Typ. (0.3 Ω for L6227)
- Max. RMS current: 2.8 A per Eq. Half bridge (1.4 A for L6227)
- Max. peak current: 5.6 A per Eq. Half Bridge (2.8 A for L6227)
- Overcurrent threshold: 5.6 A per Eq. Half Bridge (2.8 A for L6227)

Competitive advantages

- Integrated non-dissipative overcurrent
- Robust
- Scalable architecture
- Different packages

Further information and full design support can be found at www.st.com/stspin