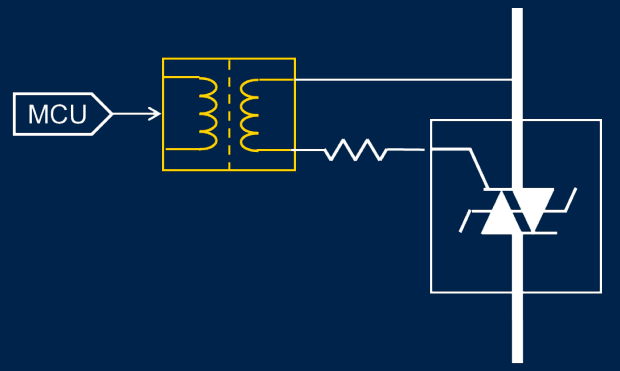


STSID140 miniature isolated driver Optimized for thyristors

Content

1 Current solutions for driving thyristors

2 Isolation technologies used in gate drivers

3 STSID140-12 a novel miniature isolated gate driver for thyristors

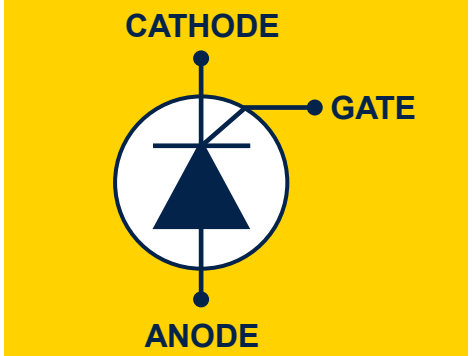
4 Benchmarking STSID140 vs optotriacs and pulse transformer solutions

5 Collaterals

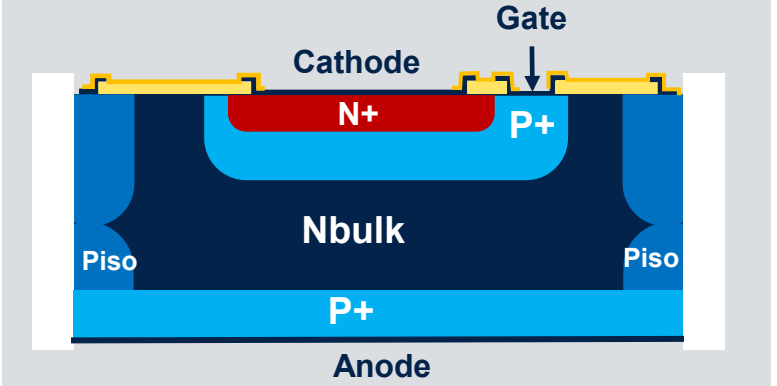
Current solution for driving thyristors

How a thyristor works

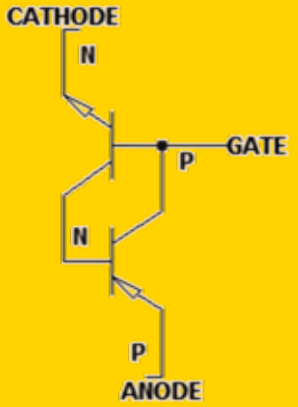
Symbol



Construction



Equivalent schematic



NPN and PNP transistors are connected as a **latching** device.

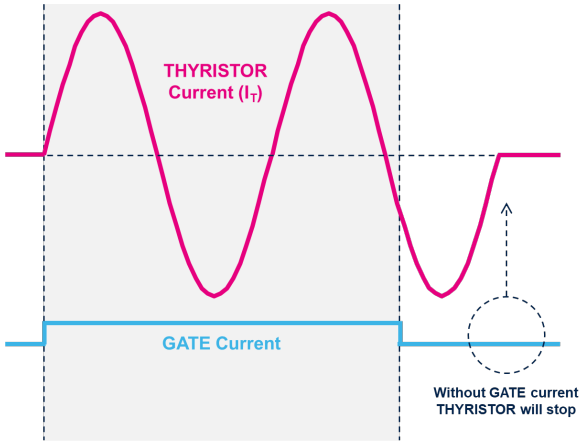
When current is supplied to the gate, NPN current flows from collector to emitter.

This turns on the PNP transistor that continues to supply gate current to the NPN (gate current can be stopped).

When current flowing from anode to cathode stops, the thyristor **turns off** automatically. Another gate pulse is required to re-latch the device.

Specific requirements for thyristor gate drivers

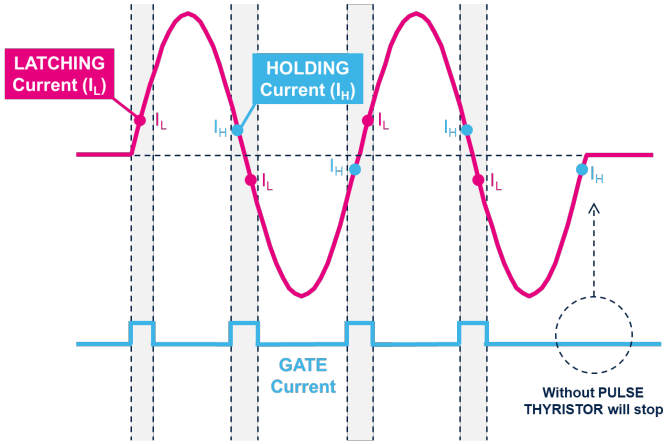
Continuous



MOSFETs are driven by gate **voltage**

Thyristors are driven by gate **current**

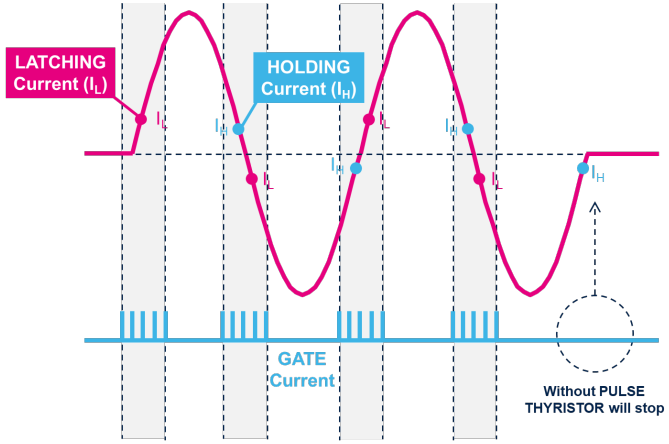
Pulsed



Period = 10 ms (100 Hz)

Width = 1 ms

PWM



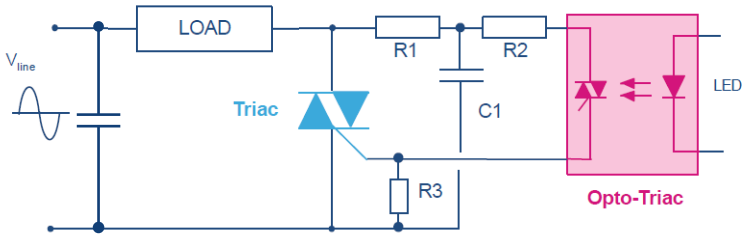
Period = 100 µs (10 kHz)

Duty = 10% (10 µs)

Significant power savings

State-of-the-art thyristor gate circuit

Optotriac

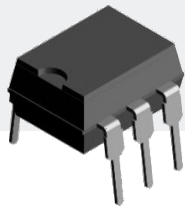


Advantages / benefits

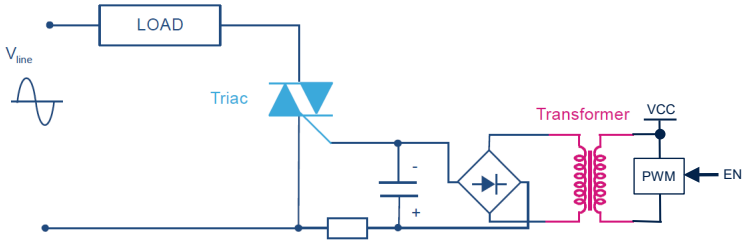
- Compact package saving board space
- Safety insulation > 3 kV available

Drawbacks

- Work only with Q1 & Q3 triac quadrants
- Reliability and aging of opto cells



Pulse transformer



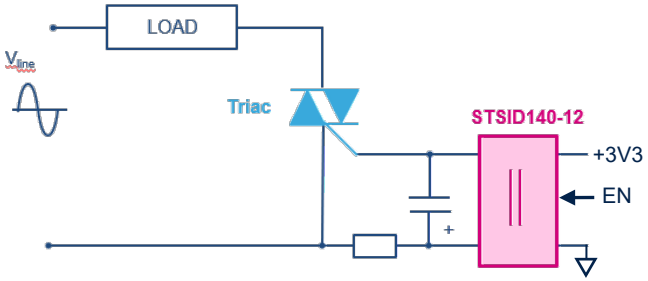
Advantages / benefits

- Robust and reliable – used in automotive
- Energy savings in PWM control
- Safety insulation > 3 kV available

Drawbacks

- High frequency switching
- Large and bulky

STSID140-12



Advantages / benefits

- Reliable magnetic isolation technology
- EMI noise immunity (save x2 HV capa)
- Optimize energy transfer from LV to HV
- Board space saving: DFN package
- Work with all SCR & triacs quadrants

Drawbacks

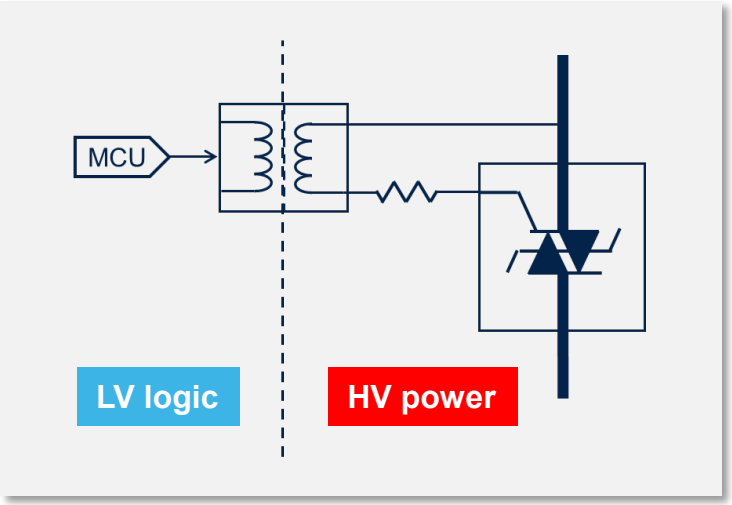
- Fist product in catalog, roadmap coming

Isolation technologies used in gate drivers

Galvanic isolation

Prevents unwanted AC and DC currents from flowing between two parts of a system, enabling safe signal and power transfer

Galvanic isolation between LV logic and HV power

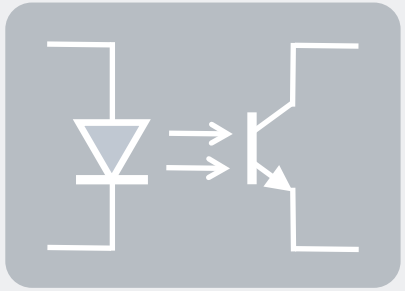


Insulating material and associated dielectric strength

Insulator materials	Dielectric strength
Air	~1 VRMS / µm
Epoxy	~20 VRMS / µm
Silica-filled mold compounds	~100 VRMS / µm
Polyimide	~300 VRMS / µm
SiO_2	~500 VRMS / µm

Galvanic isolation technologies

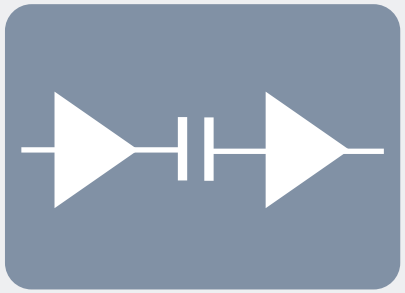
Optical



Air, epoxy, mold compound

- × Requires output supply (except optotriac)
- × Less efficient
- × Lower data rates
- × No long-term lifetime data

Capacitive



SiO2

- × Requires output supply
- ✓ efficient
- ✓ High data rates
- ✓ Lifetime data based on working voltage

Magnetic

Epoxy, polyimide

- ✓ No output supply required
- ✓ More efficient
- ✓ High data rates
- ✓ Lifetime data based on working voltage

Selected for **STSID140**

Surge voltage test

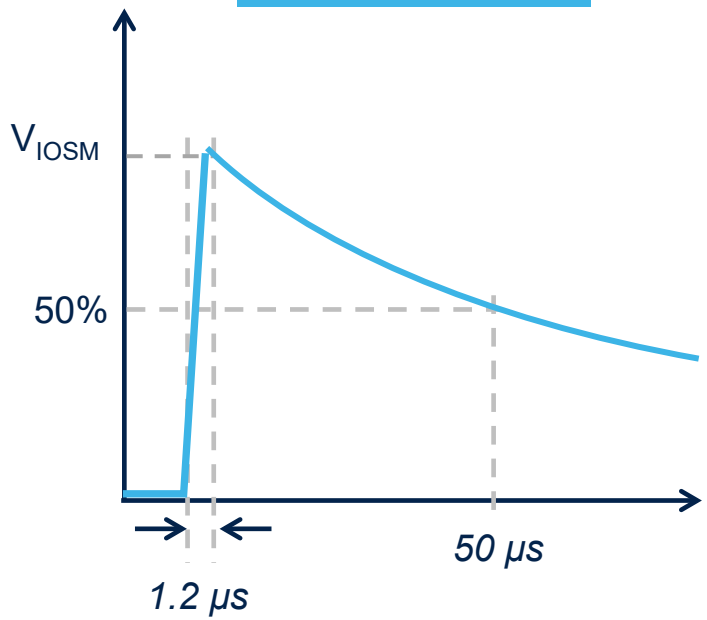
STSID140 is tested against short-duration surges (such as lightning strikes) to verify immunity to very high voltage levels

The impulse test assesses the **whole device** including package creepage. It must be executed in air without arching. Its value is reported as V_{IMP} in the product datasheet.

The surge test assesses the **internal insulation** and should be performed in dielectric oil to avoid arching.
Its value is reported as V_{IOSM} in the product datasheet.

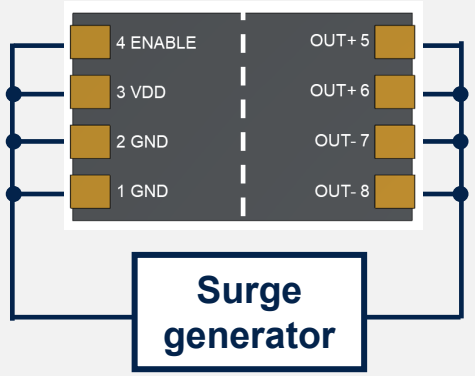
IEC60747-17 mandates
$V_{IOSM} > 1.3 \times V_{IMP}$

IEC 61000-4-5 WAVEFORM



25 positive pulses followed by 25 negative pulses

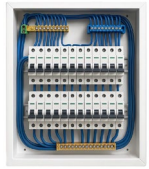
STDIS140



Surge voltage input to output
V_{IOSM} = ± 4000 V peak
V_{IMP} = ± 2500 V peak

Overvoltage categories

The concept of **overvoltage category** is used for equipment energized by the supply mains and is based on the **IEC 60664-1** standard. It classifies the positions of equipment along the supply mains distribution line, assuming installations that are closer to the generation system are exposed to transient overvoltages with higher amplitude.



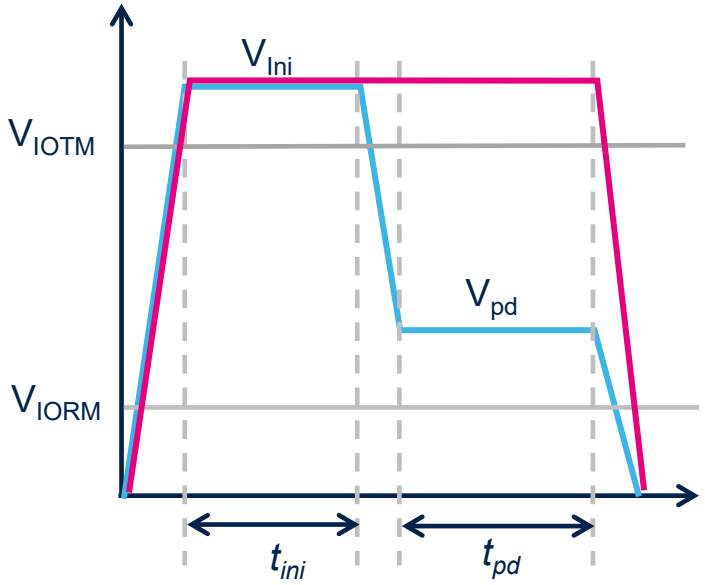
	Overvoltage category	I	II	III	IV
	Where	Equipment for connection to circuit in which measures are taken to limit transient overvoltages	Equipment connected to the fixed installation through plugs	Equipment in fixed installations with permanent connection to distribution panel	The origin of the installation
	Examples	Protected electronics circuits	Appliance, tools	Control panels, sockets	Distribution lines, electricity meters
Expected transient according to VRMS	< 100 VRMS	500 V	800 V	1500 V	**2500 V**
	< 150 VRMS	800 V	1500 V	**2500 V**	4000 V
	< 300 VRMS	1500 V	**2500 V**	4000 V	6000 V
	< 600 VRMS	**2500 V**	4000 V	6000 V	8000 V
	STSID140-12	**Voltage < 600 VRMS**	**Voltage < 300 VRMS**	**Voltage < 150 VRMS**	**Voltage < 100 VRMS**
	compliant	YES	YES	NO	NO

Partial discharge test

STSID140 is subject to a partial discharge test that uses charge distribution to identify potential defect within a dielectric barrier

IEC 60747-17

Method B1 **Method B2**



The Method A and B tests consists of 2 parts

- **Isolation test:** HV test to screen out units with defective isolation barrier
- **Partial discharge test:** Follow the 5pC test standard that is required for all isolation technologies

Method A: Qualification test

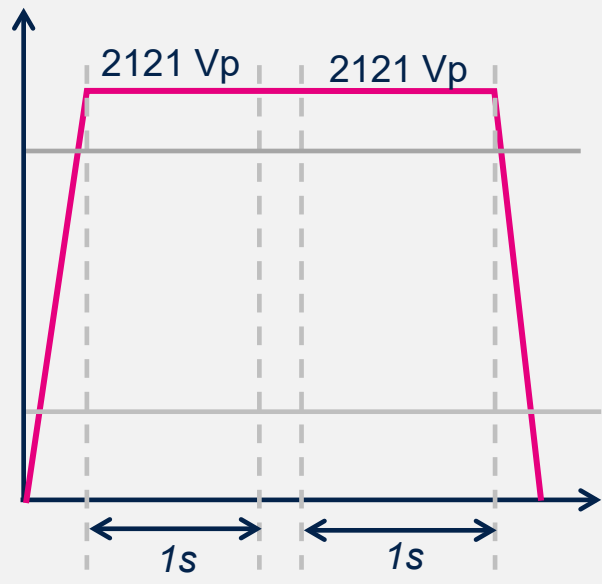
Certification standard required to verify VIOTM by sampling

Method B: Qualification test & Production test

The certification standard requires 100% of the device to be tested in production

Applied voltage	Isolation test	Partial discharge
Method A	**VIOTM, 60s**	**1.3 x VIORM, 10s**
Method B1	1.2 x VIOTM, 1s	1.5 x VIORM, 1s
Method B2	**1.2 x VIOTM, 1s**	**1.2 x VIOTM, 1s**
UL1577	**VISO, 60s**	**1.2 x VISO 1s**

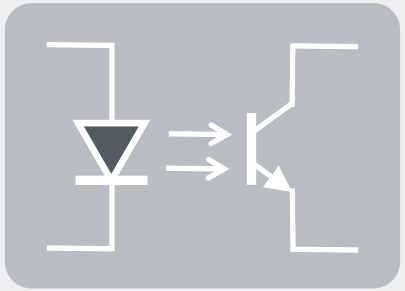
STSID140



Isolation voltage input to output
Repetitive, V_{IORM} = **618 V** peak
Transient, V_{IOTM} = **1767 V** peak
UL1577, V_{ISO} = **1250 V** rms

Overview of galvanic isolation standards and certifications

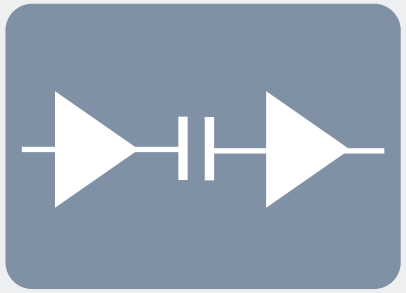
Optical



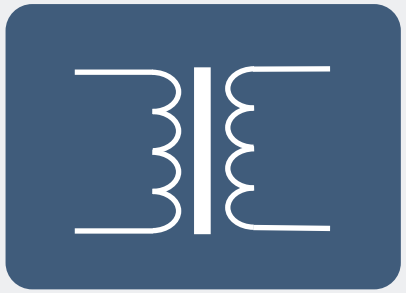
IEC 60747-5-5

UL1577

Capacitive



Magnetic



IEC 60747-17

VDE-0884-17

Functional
Insulation required for operation with no consideration for protection against electrical shock

Basic
Insulation with a single level of electrical protection. If it fails, there is a risk of exposure to electrical shock

Failure <1000 ppm 24 years @ **VIORM**

Reinforced
Insulation with a dual level of electrical protection. If one fails there is no risk of exposure to electrical shock

Failure <1ppm 30 years @ **VIORM**

VIOSM > ±10 kV

STSID140-12 a novel miniature isolated gate driver for thyristors

Understanding datasheet isolation characteristics

STSID140-12 datasheet compliance with IEC 60747-17

Partial discharge measurement test

DC resistance across insulation

Isolation voltage according to UL1577

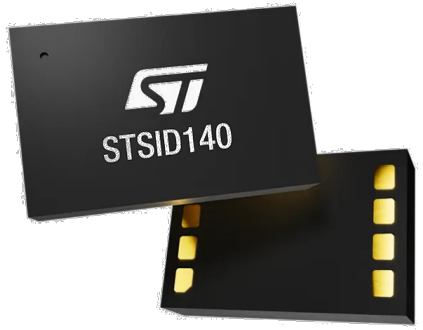
Maximum “Temporary overvoltage”.
Used in different IEC standards
Expressed in peak value

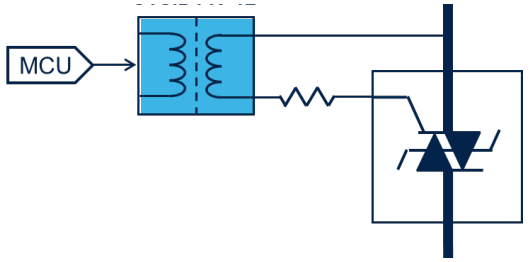
Maximum operating voltage in application (peak, RMS, and DC value)

Maximum isolation ratings for surge and “Short pulses”.
Used in different IEC standards
Expressed in peak value

Symbol	Test conditions		Value	Unit
Q_{PD}	Apparent charge, method b2: 100 % final production test for 1 s, $V_{PD} = V_{INI} = 1.2 \times V_{IOTM} = 2121\ V_{PK}$, $t_{INI} = 1$ s	Max.	5	pC
	Method a: After I/O safety test subgroup 2/3, $V_{INI} = V_{IOTM}$, $t_{INI} = 60$ s, $V_{PD} = 1.2 \times V_{IORM} = 741\ V_{PK}$, $t_m = 10$ s			
	Method a: After environmental tests subgroup 1, $V_{INI} = V_{IOTM}$, $t_{INI} = 60$ s, $V_{PD} = 1.3 \times V_{IORM} = 803\ V_{PK}$, $t_m = 10$ s			
R_{IO}	Minimum input to output isolation (2) resistance, $V_{I/O} = 500$ V	$T_J = 25$ °C	$>10^{12}$	Ω
		$T_J = 125$ °C	$>10^{9}$	Ω
V_{ISO}	Input to output (2), insulation RMS voltage (100 % final production test at 1500 V_{RMS} for 1 s)	60 s	1250	V_{RMS}
V_{IOTM}	Input to output (2), maximum transient isolation AC peak voltage (100 % final production test at 2121 V_{PK} for 1 s)	60 s	1767	V_{PK}
V_{IORM}	Input to output (2), maximum rated repetitive peak isolation voltage	AC	618	V_{PK}
		DC	450	V_{DC}
V_{IOWM}	Input to output (2), maximum RMS working voltage		437	V_{RMS}
V_{IMP}	Impulse voltage, peak value of 1.2/50 µs waveform without flashover, input to output (2), according to *IEC 61000-4-5*		±2.5	kV
V_{IOSM}	Internal isolation barrier breakdown peak voltage, input to output (2), according to *IEC 61000-4-5* conditions, 1.2/50 µs waveform (3)		±4	kV

Part numbering scheme





ST **SID** **1** **40** - **12** **Y**

BRAND
STMicroelectronics

SID
Surface-mount isolated driver

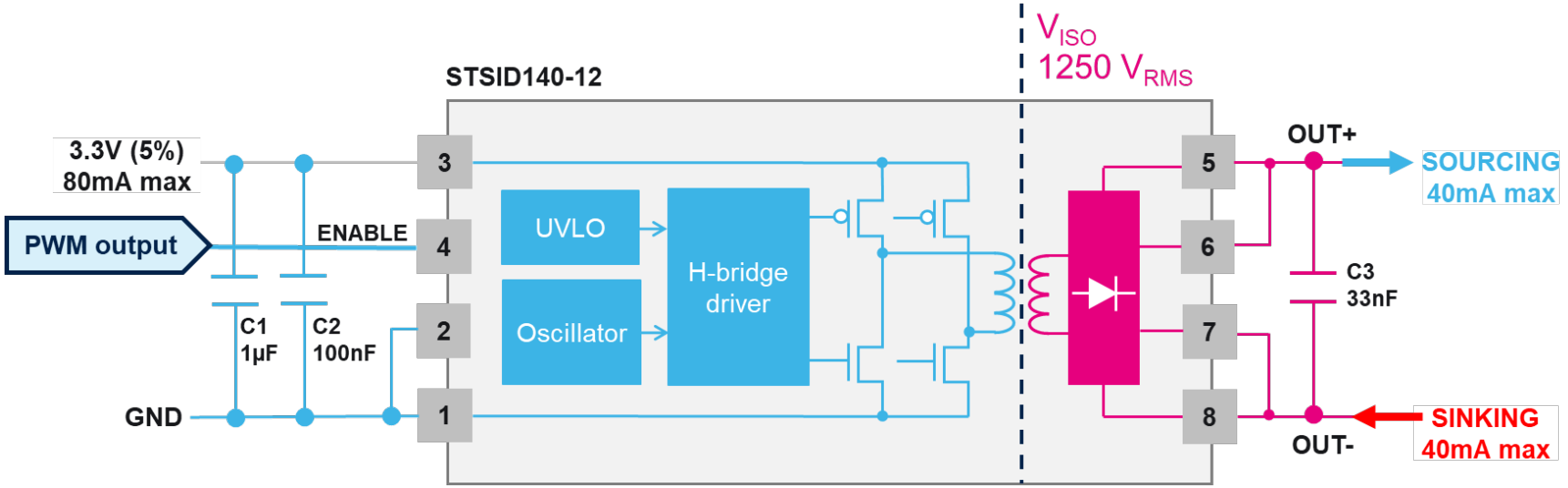
Number of thyristors
1: Single thyristor
2: Dual thyristor

Y = automotive grade

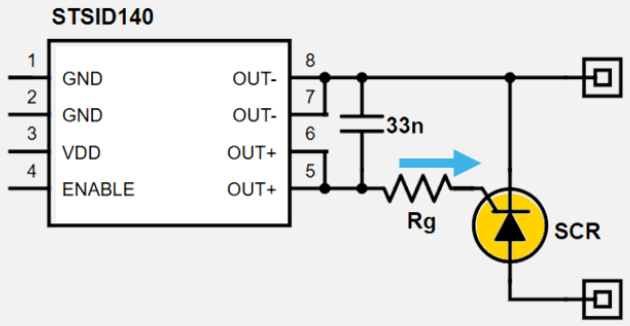
Isolation voltage
12: VISO = 1250 VRMS
25: VISO = 2500 VRMS

Thyristor gate current
40: 40 mA
70: 70 mA

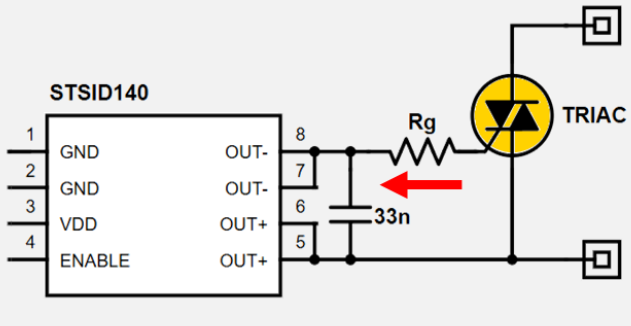
STSID140-12 block diagram



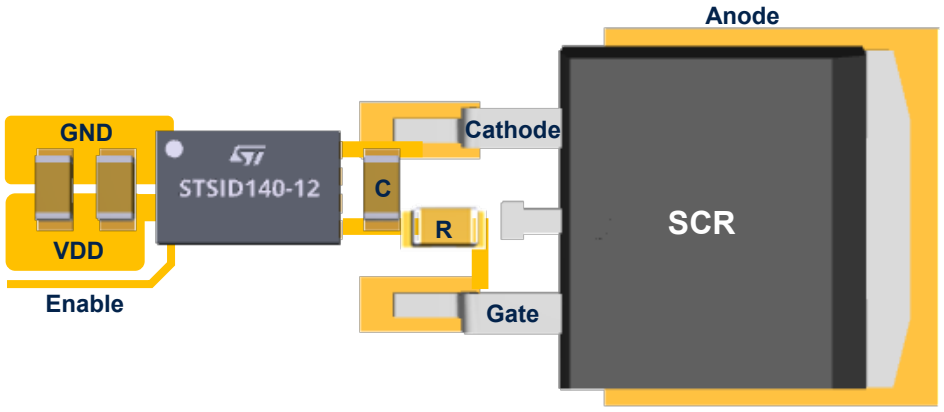
SCR positif gate current (sourcing)
gate connected to **OUT+**

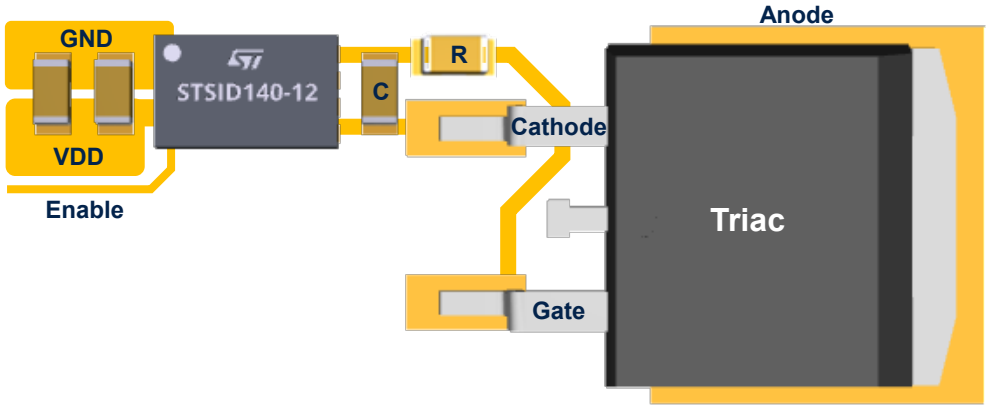


TRIAC negatif gate current (sinking)
gate connected to **OUT-**

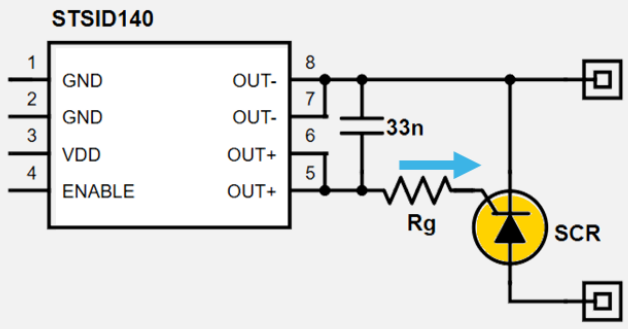


STSID140-12 thyristor connection

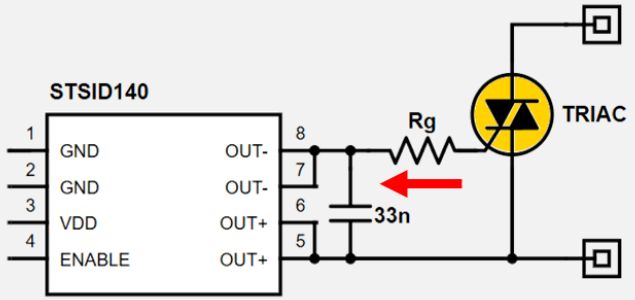




SCR positif gate current (sourcing) gate connected to **OUT+**

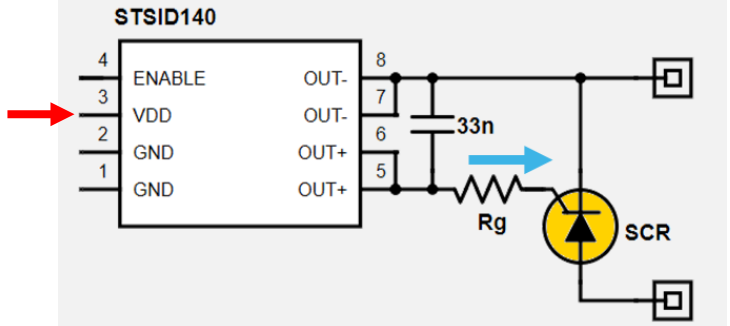


TRIAC negatif gate current (sinking) gate connected to **OUT-**

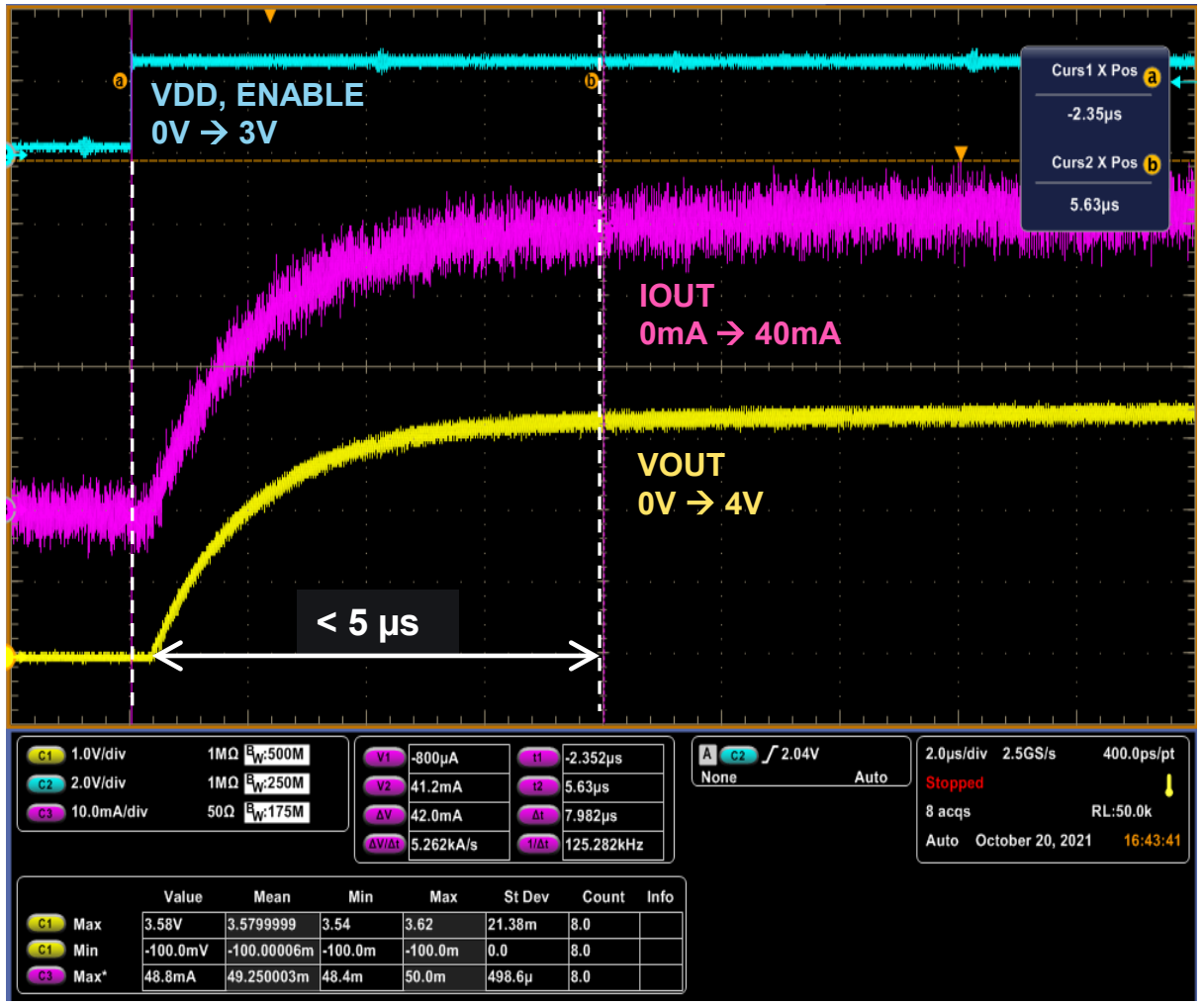


STSID140-12 startup

SCR positif gate current (sourcing)
gate connected to **OUT+**

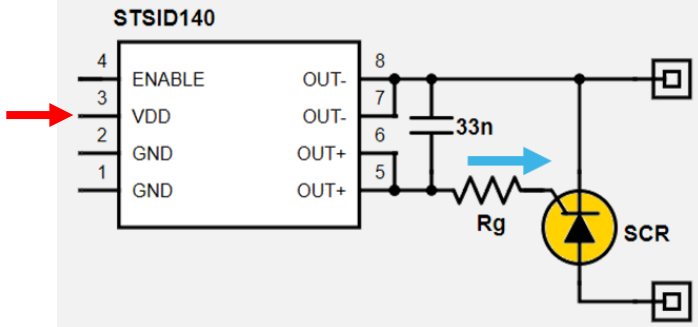


Startup time
< 5 µs



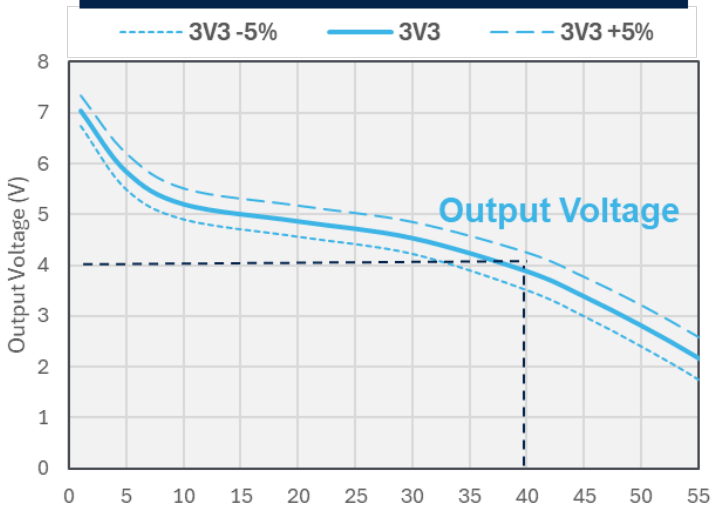
STSID140-12 performance

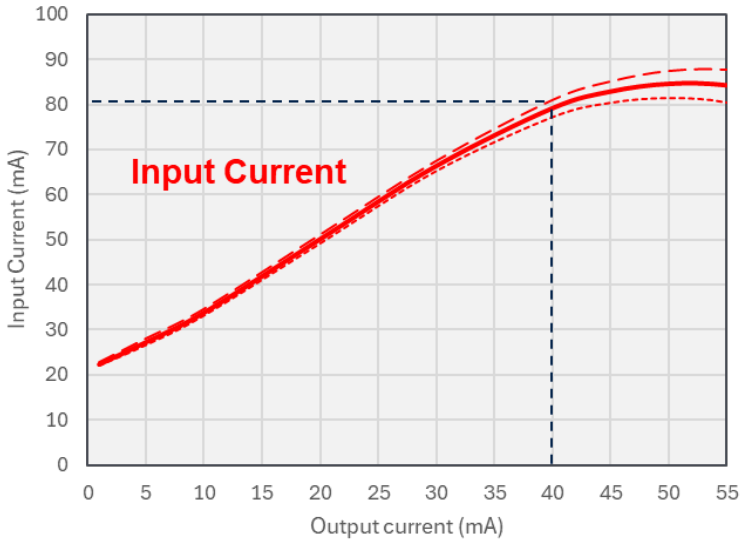
SCR positif gate current (sourcing) gate connected to **OUT+**



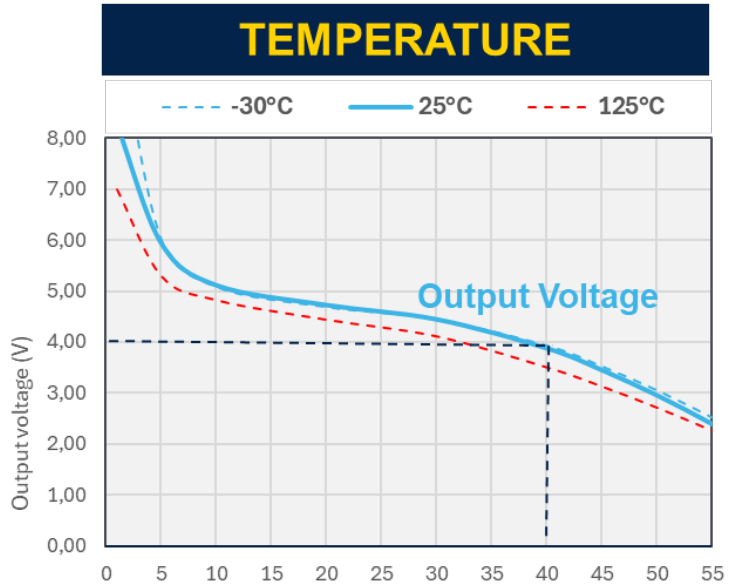
Stable performance over **VDD** and **temperature** range

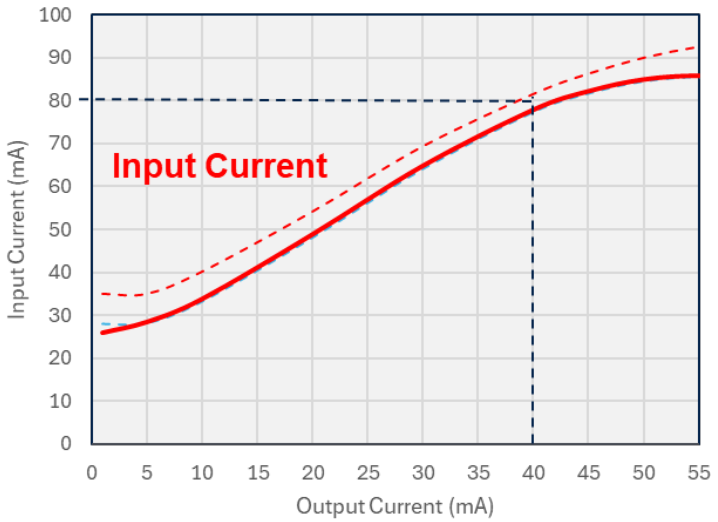
VDD





TEMPERATURE



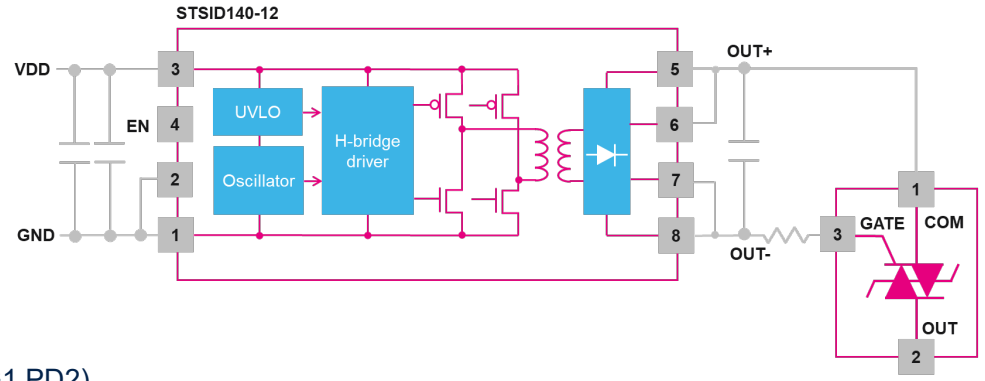


STSID140-12 main features

Smallest isolated driver optimized for thyristor control

Gate driver for thyristor control:

- 40 mA current output
- Direct MCU drive from single 3.3V supply
- Standby current <5 µA
- Maximum junction temperature: 125°C

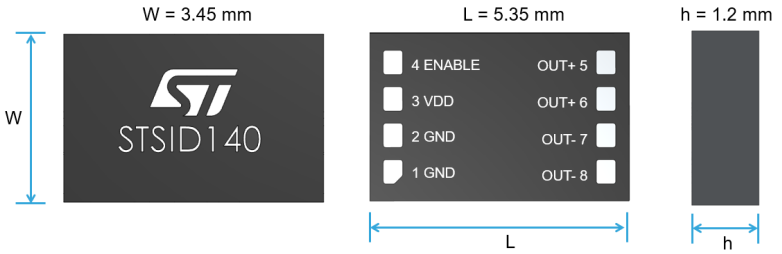


Input-output functional insulation:

- VISO = 1.25 kV RMS / 1.77 kV PEAK
- Creepage distance: 3.92 mm (780 V RMS MG1 PD2)

EMC performances:

- Low EMI conducted & radiated noise emission
- Option for zero cross or random switching
- High static immunity:
  - ± 2 kV contact ESD according to IEC61000-4-2
  - ± 2.5kV lightning according to IEC61000-4-5
  - ± 4 kV EFT burst according to IEC61000-4-4

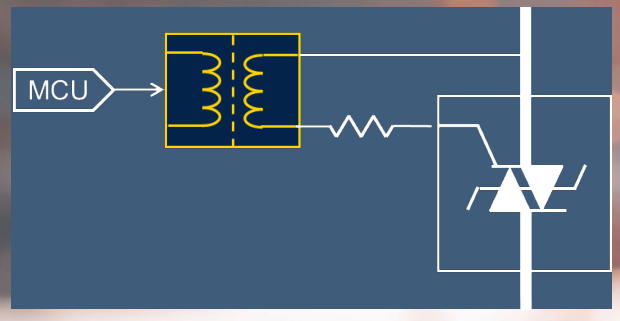


Package:

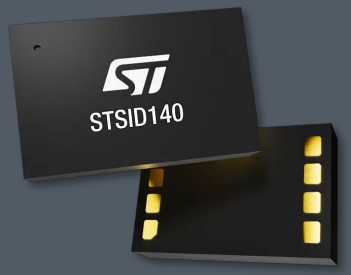
- DFN SMD compact package: 5.35 x 3.45 x 1.2 mm
- Halogen-free molding, lead-free plating, ECOPACK®2 compliant

STSID140-12 benefits

Smallest isolated driver optimized for thyristor control



1. **Best-in-class EMI & EMC**
   Improves noise immunity & reduces input line filtering.
2. **Free extra feature**
   Zero-cross or random switching.
3. **Compact design for SMD automatic assembly**
   5.35 x 3.45 x 1.2 mm.
4. **Energy efficiency**
   Gate control energy transferred from +3.3V.
5. **High reliability**
   TC, H3TRB, and ELFR successfully passed.

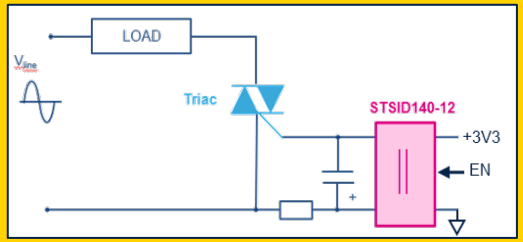


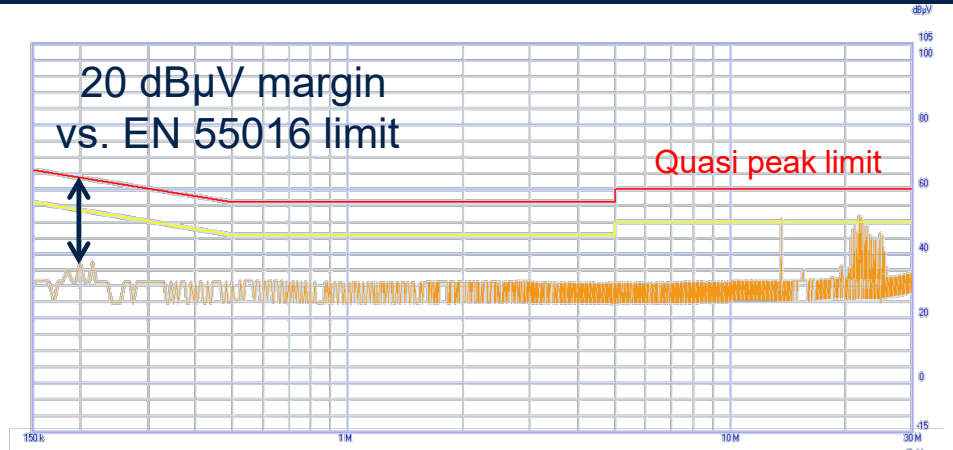
Benchmarking STSID140 vs optotriacs and pulse transformer solutions

Conducted EMI performance 150 kHz – 30 MHz

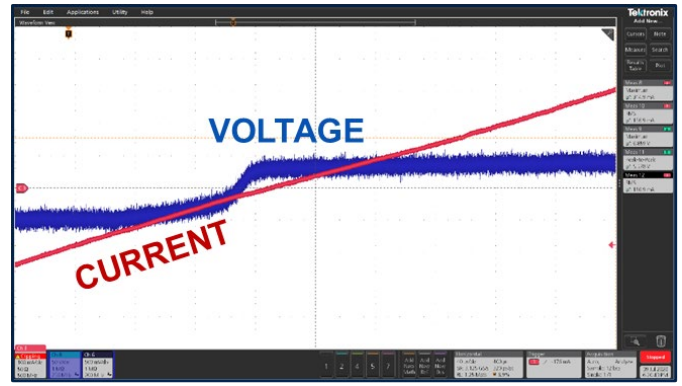
Compliance with EN 55016-2-1 conducted EMI noise limits (quasi-peak)

STSID140-12

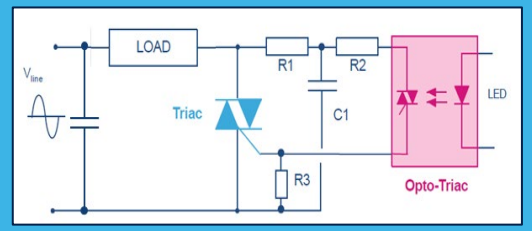


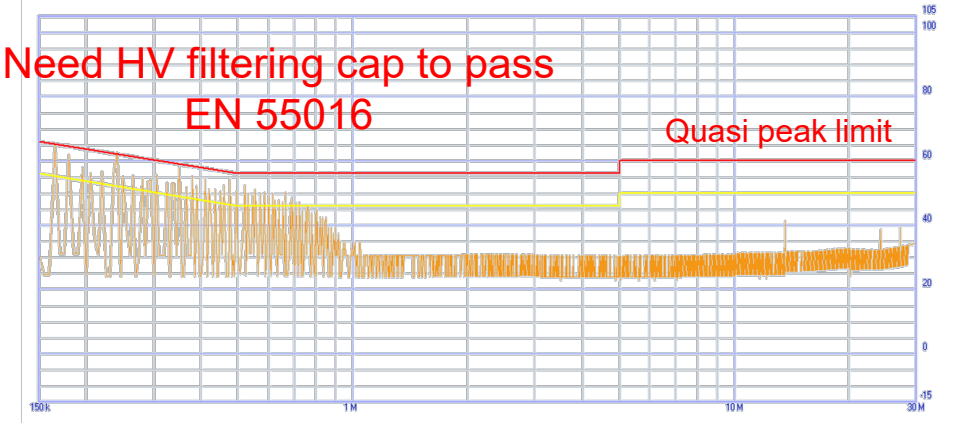


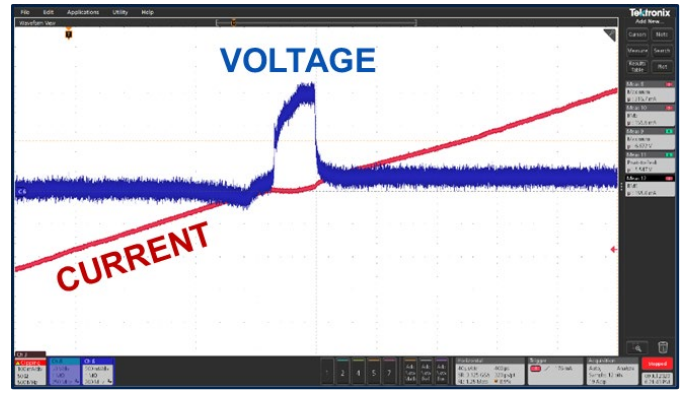
Zero voltage crossing



Optotriac





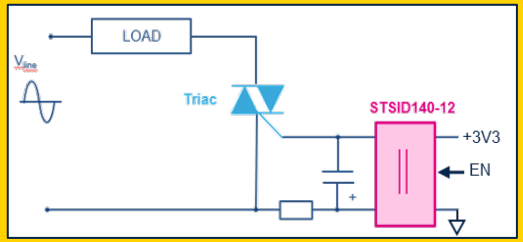


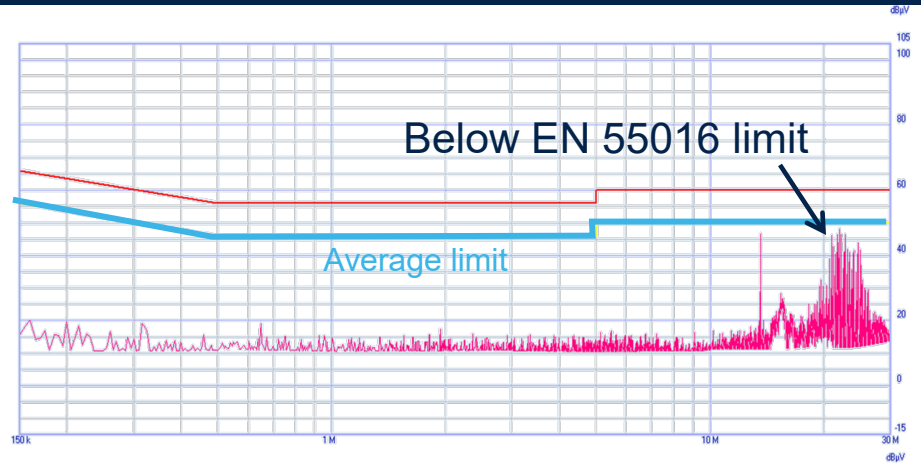
*with optimized circuit of gate resistor and RC snubber versus triac I_{GT}

Conducted EMI performance 150 kHz – 30 MHz

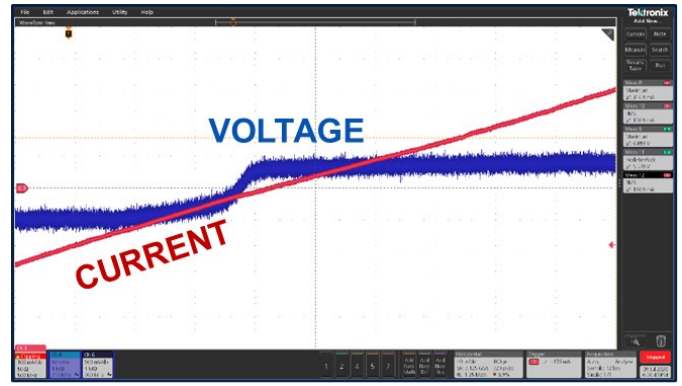
Compliance with EN 55016-2-1 conducted EMI noise limits (average)

STSID140-12

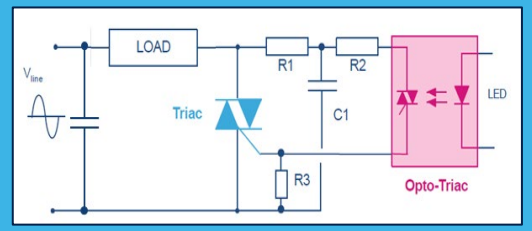


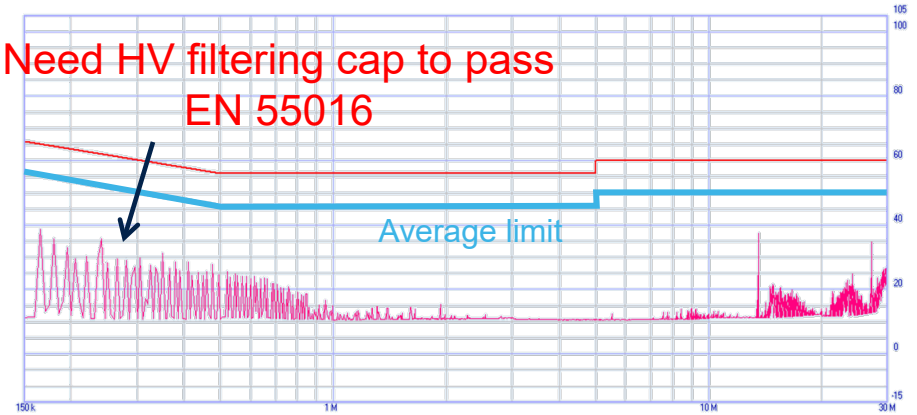


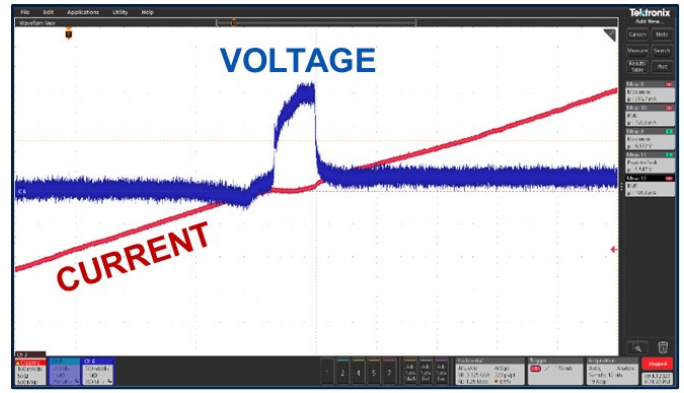
Zero voltage crossing



Optotriac

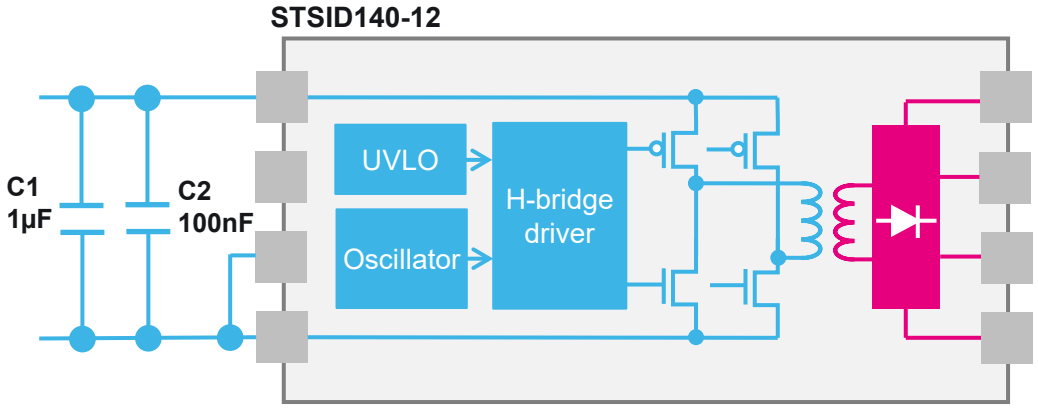


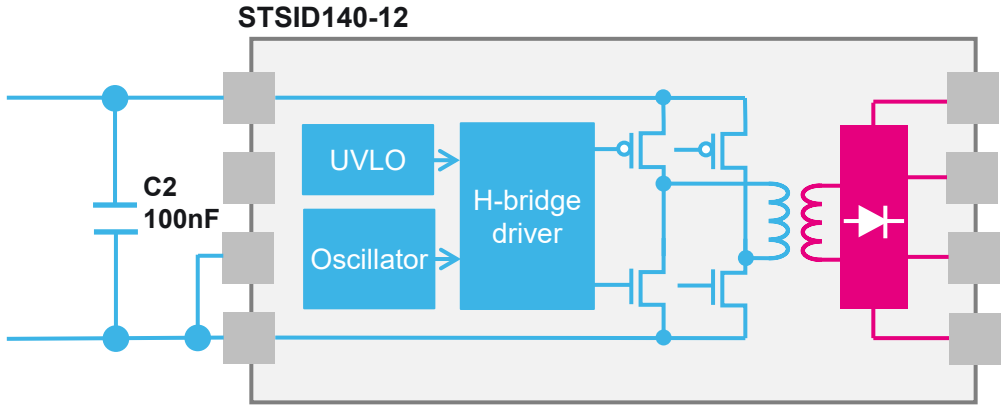


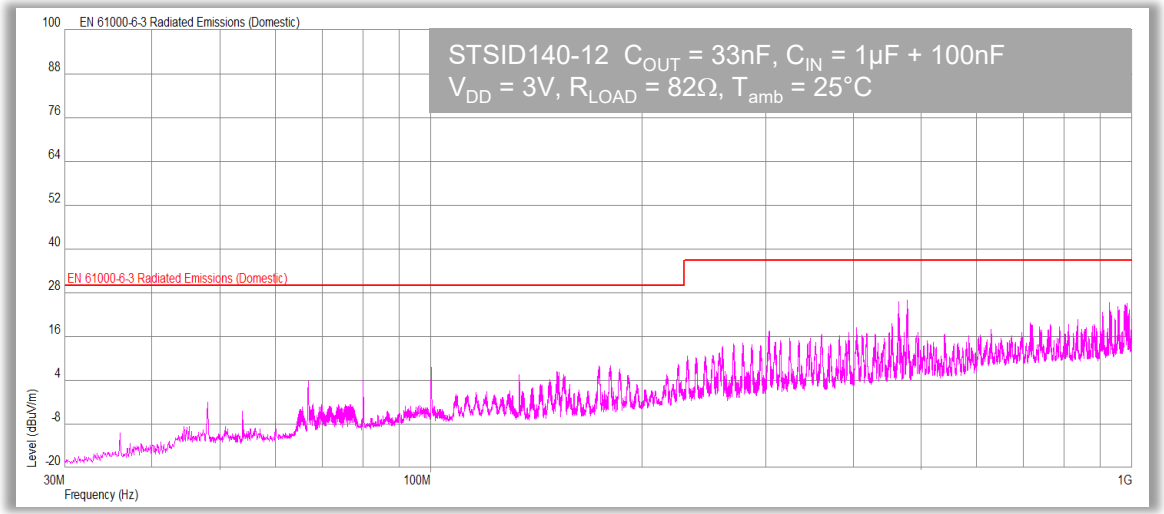


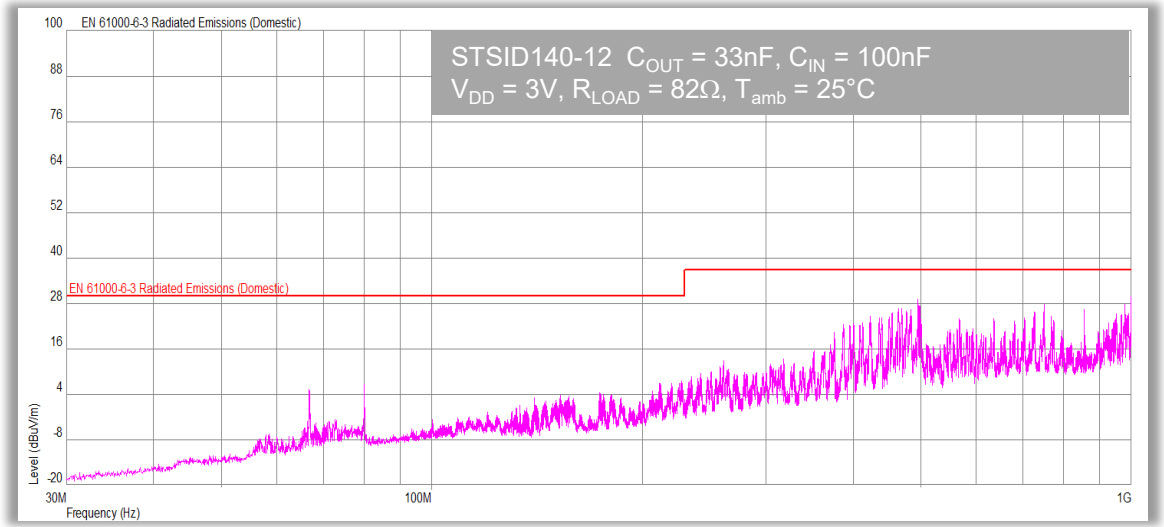
*with optimized circuit of gate resistor and RC snubber versus triac I_{GT}

Radiated EMI performance 30 MHz – 1 GHz





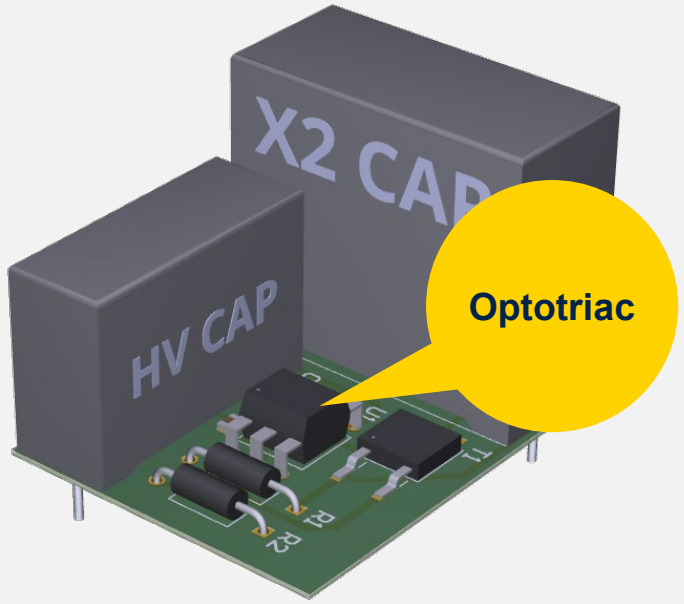




Passing **EN 55016-2-3** test with margin

Driving thyristors in applications where size is critical

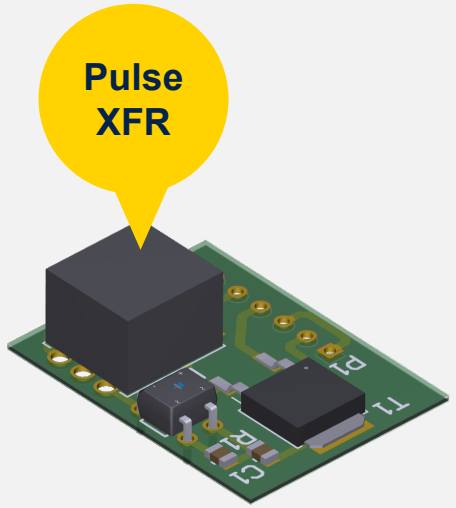
Optotriac



42 cm³

Surface: 15 cm²
Height: 28 mm

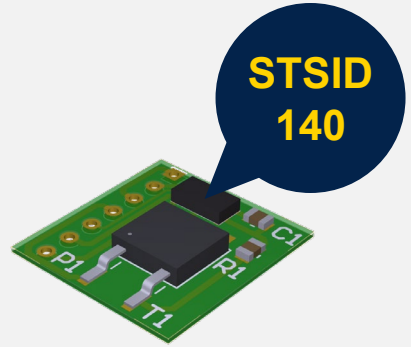
Pulse transformer



7 cm³

Surface: 5 cm²
Height: 14 mm

STSID140-12

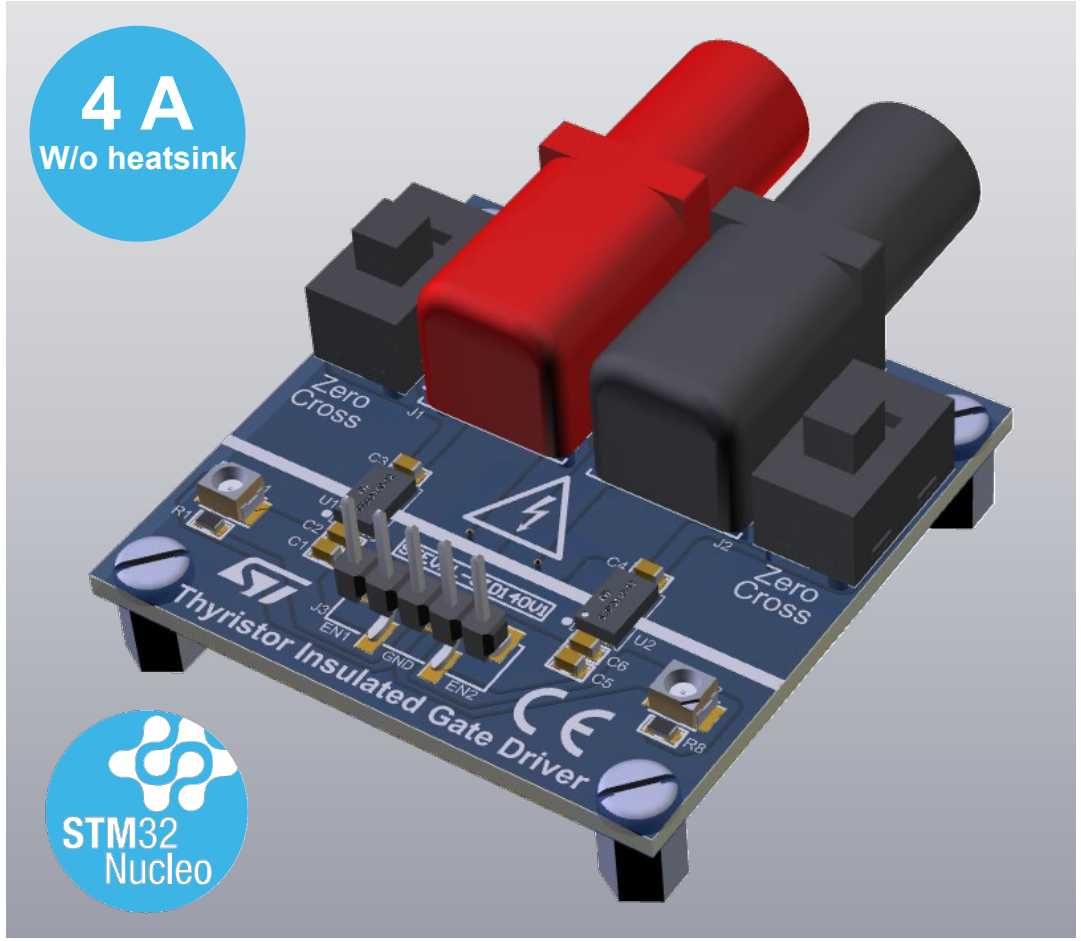


1.3 cm³

Surface: <3 cm²
Height: 4.5 mm

Content

STEVAL-SID140V1 evaluation board

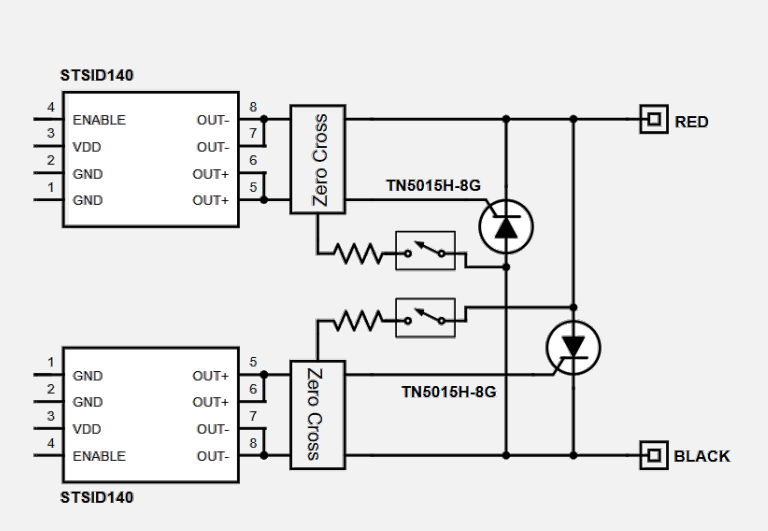


Solid-state relay
Support random & zero cross
With enhanced immunity and lowest EMI

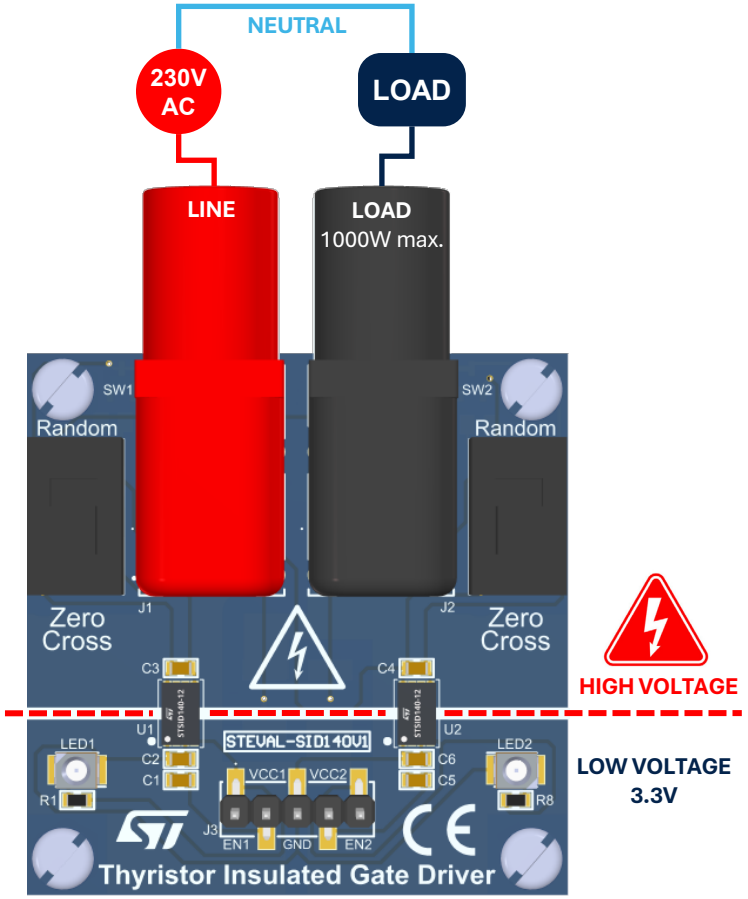
Isolated gate driver evaluation board
Quick & easy evaluation of STSID140
Schematic, Gerber, and documentation online

Mass market STEVAL
Mass market evaluation board (CE marking)
More detail on st.com

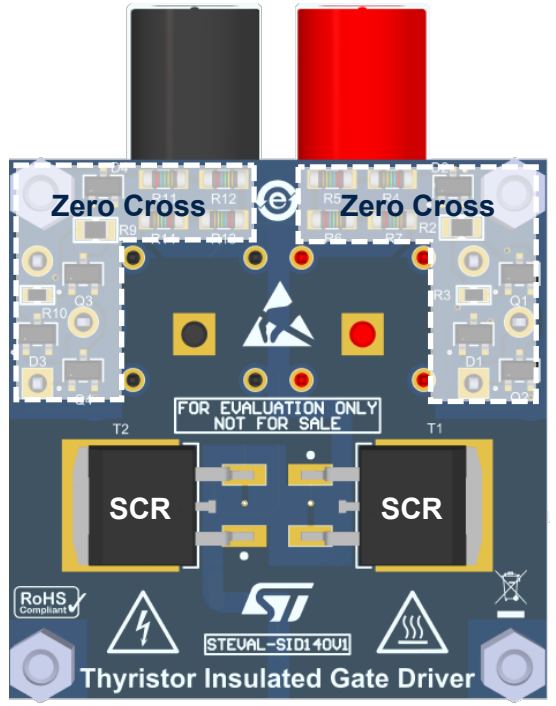
STEVAL-SID140V1 evaluation board



Block diagram

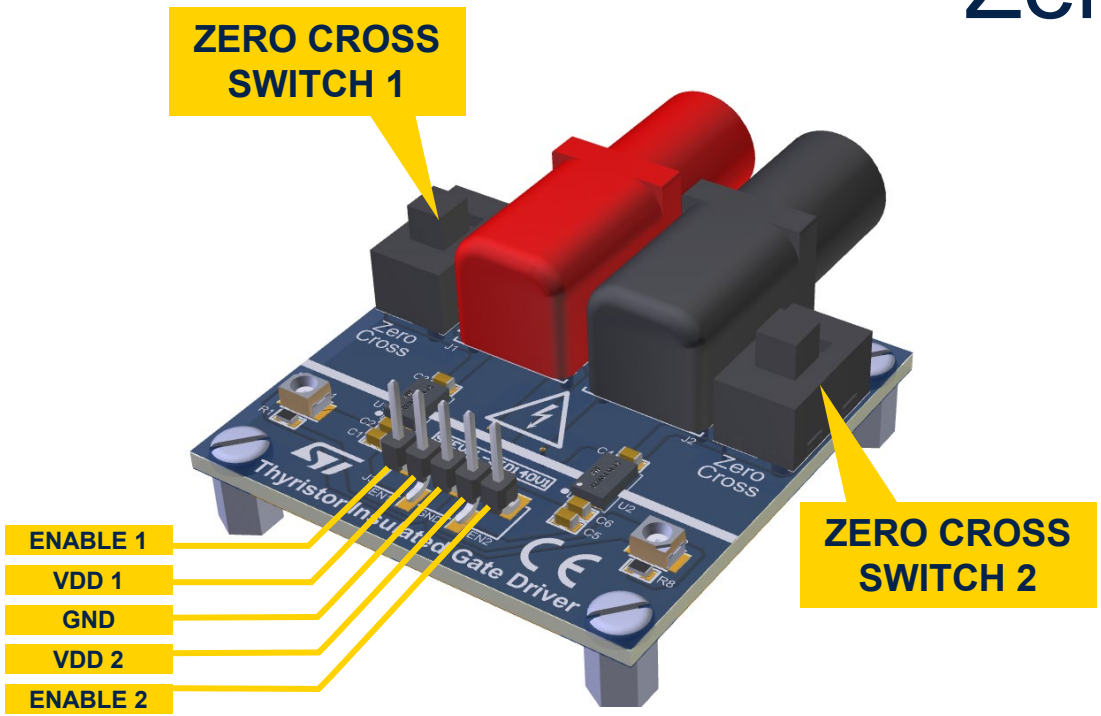


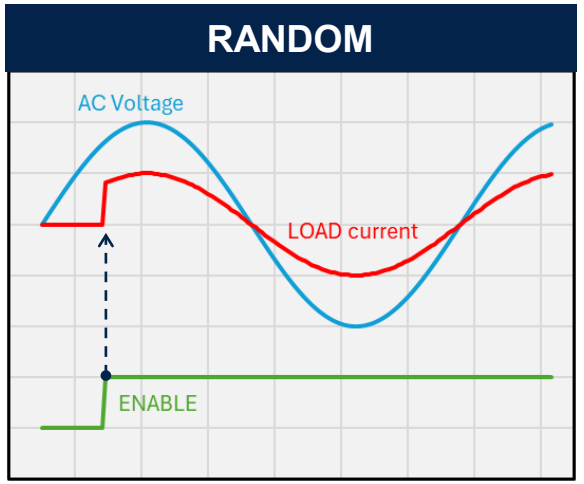
Top

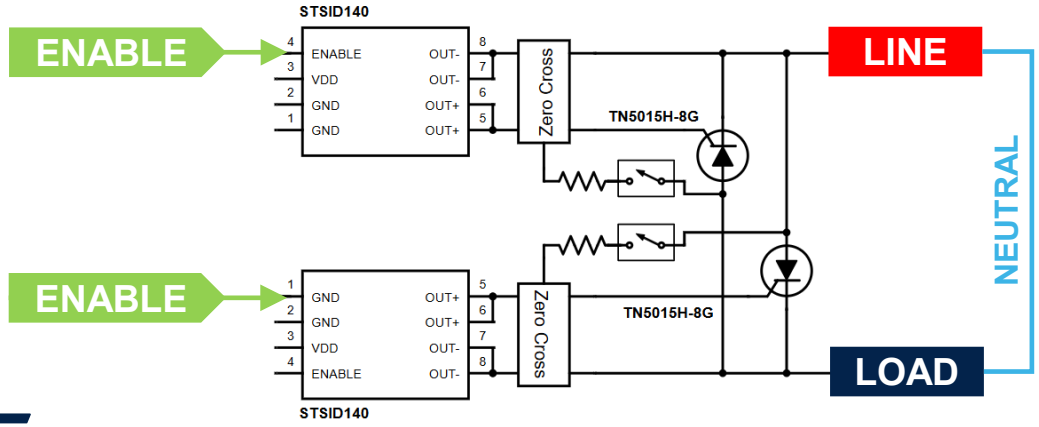


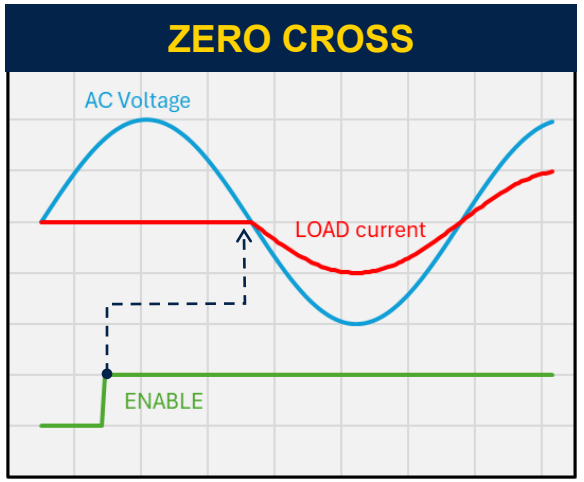
Bottom

Zero-cross & random switching



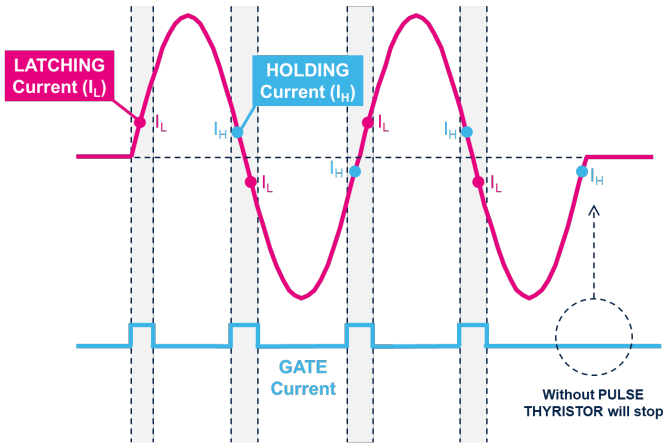






STEVAL-SID140V1 random

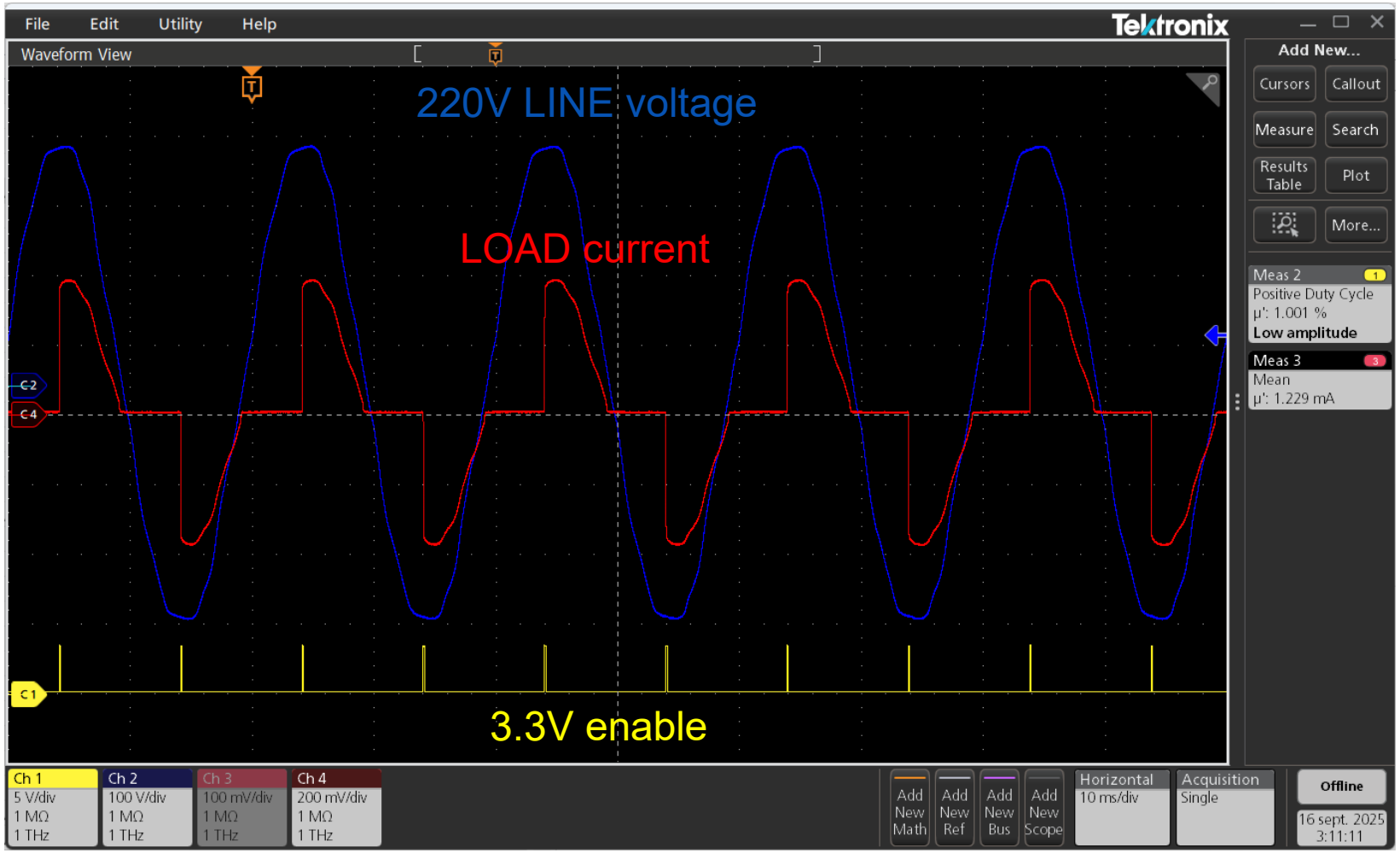
Pulsed



Period = 10 ms (100Hz)

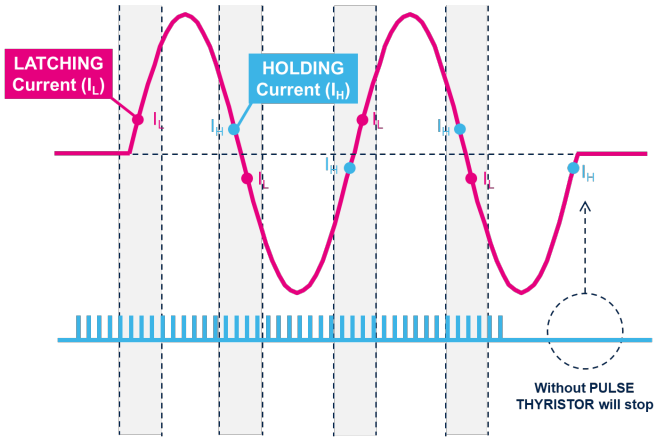
Width = 100 µs

IDD = 2 mA (avg)



STEVAL-SID140V1 zero cross

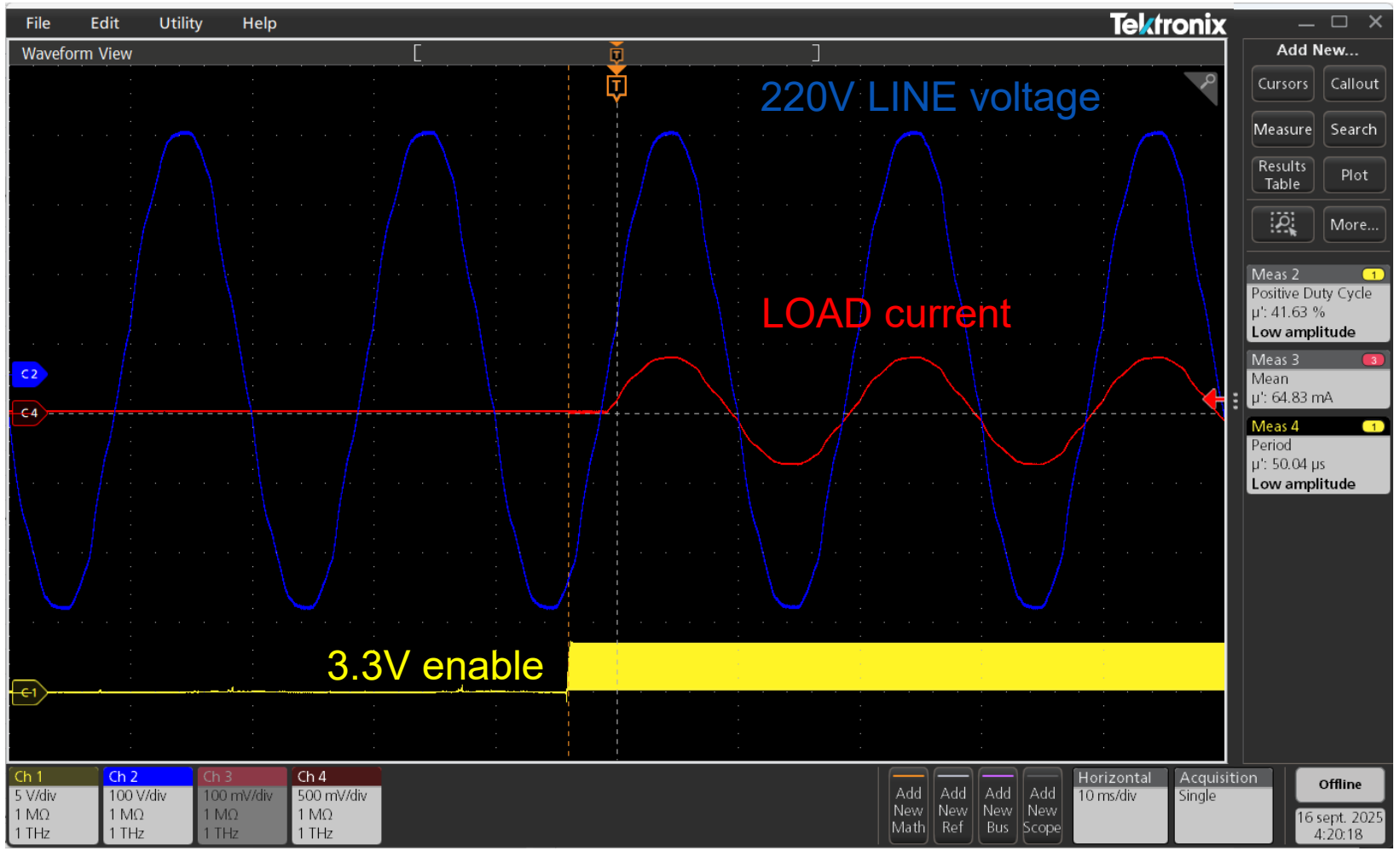
Pulsed



Period = 50 µs (20 kHz)

Width = 20 µs

IDD = 65 mA (avg)



Takeaways

STSID140 miniature isolated driver optimized for thyristors

- Complete product range including SCR, triacs, AC switches and best-in-class isolated drivers
- System solution with evaluation board, reference design, schematic, layout, and firmware
- Innovative product range including advanced packages for higher power density
- Integrated high volume production capability for industrial & automotive grade products

Our technology starts with You

Find out more at www.st.com