High density I²C EEPROM with 110 nm* technology

ST EEPROM

* F9V process

“ If only

My high-density EEPROM had an optimized footprint, competitive pricing, and efficient power consumption

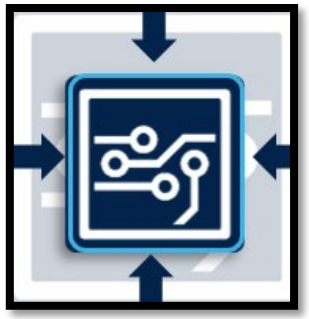
This is where we come in

New 110 nm process
addressing customer needs

ST technology roadmap 110 nm for new design

- Optimized footprint
- Competitive pricing
- Consumption effectiveness
- Wide V_{CC} range
- Plug-in replacement 150 nm

Smaller die



New features

Software Write Protection

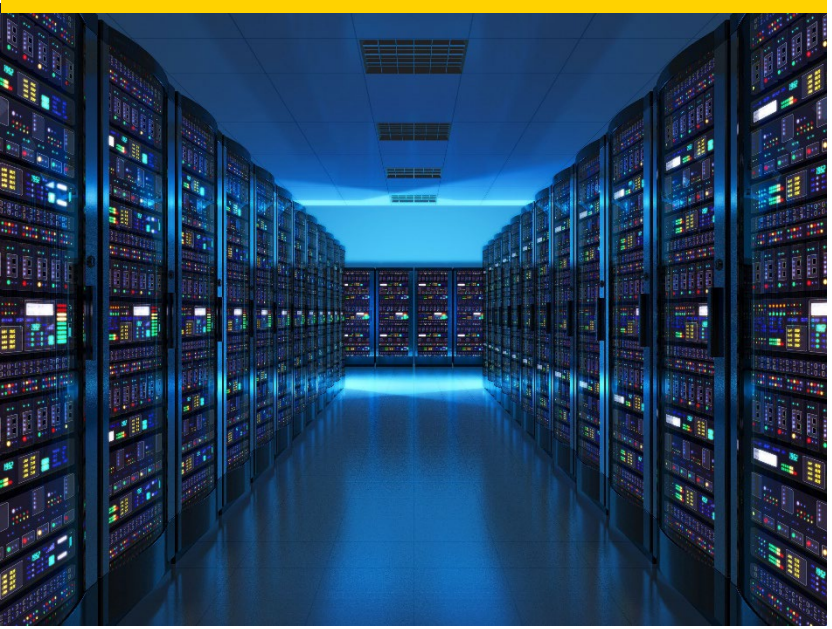
Custom Device Adress

Consumption optimization

Availability

Focus application domains

Industrial

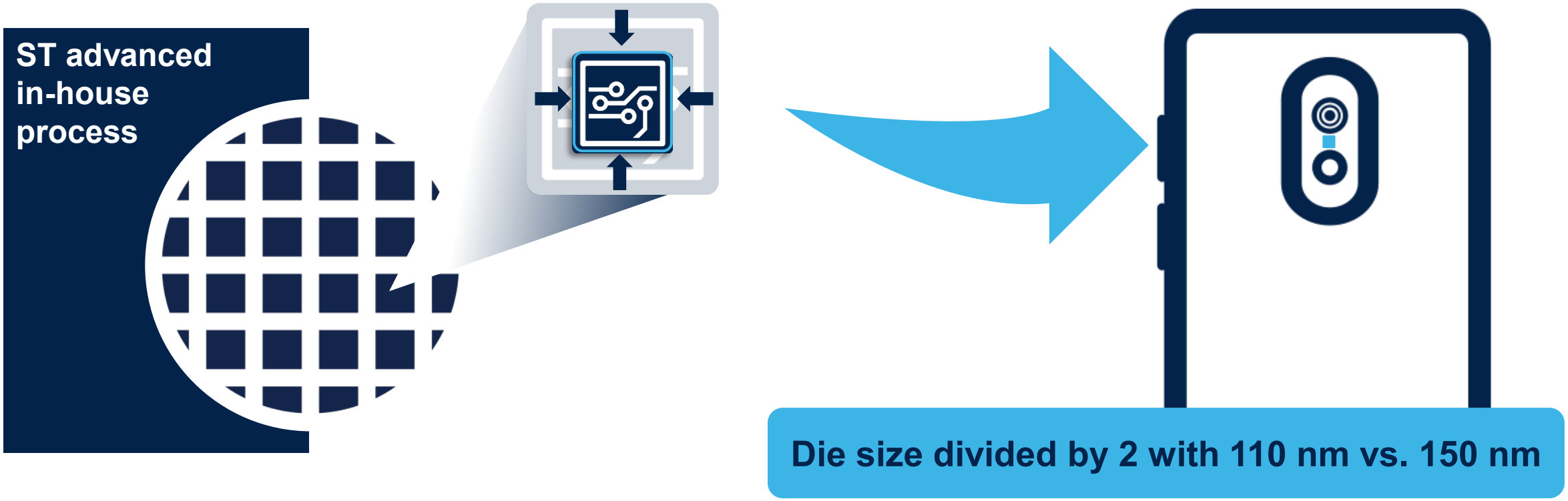


Mobile

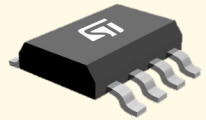
Consumer/Healthcare

WLCSP designed for mobile
Die size reduced

Improved thickness and footprint



110 nm (F9V) process
I²C standard EEPROM portfolio

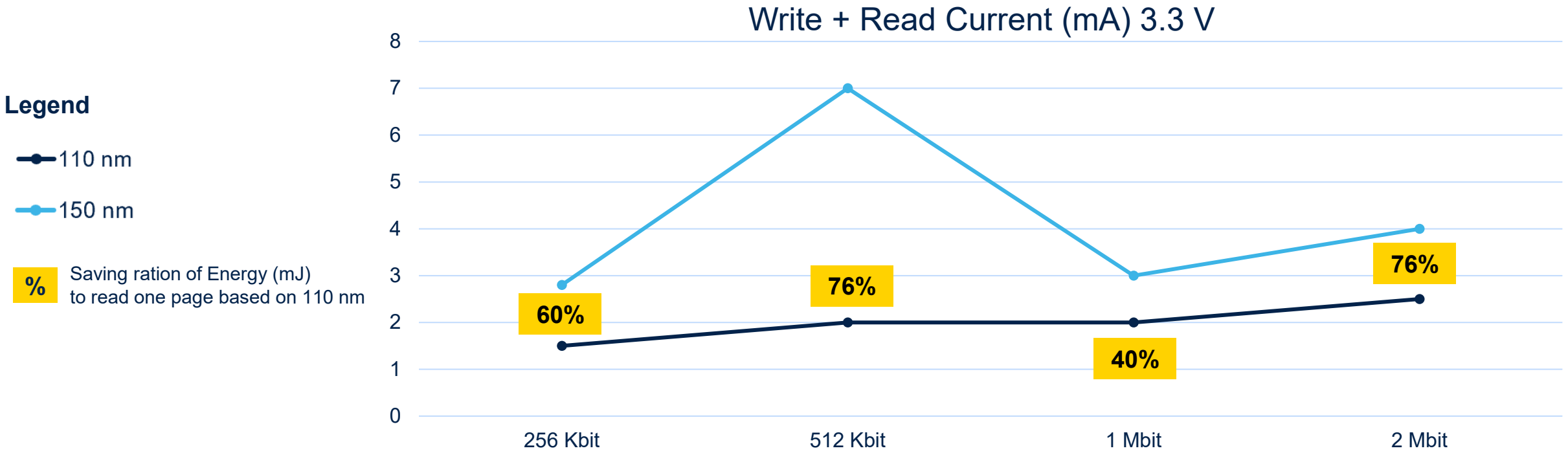
Click on product name to download the Datasheet		PACKAGE					
		WLCSP 4-ball	WLCSP 5-ball	DFN5	DFN8	TSSOP8	SO8N
		 (*)					
MEMORY DENSITY	256 Kbit (**)	M24256X-F			M24256E-F		
	512 Kbit					M24512E-F	
	1 Mbit	M24M01X-F	M24M01E-F			M24M01E-F	
	2 Mbit		M24M02E-F			M24M02E-F	

Mobile	Standard	APPLICATION
M24---X 	M24---E	  

Notes:
(*) - No WC (write control) in WLCSP 4-ball package
(**) - No SWP (software write protection) in DFN5, DFN8, TSSOP8, and SO8N packages for 256 Kbit memory density

Consumption 150 nm vs.110 nm

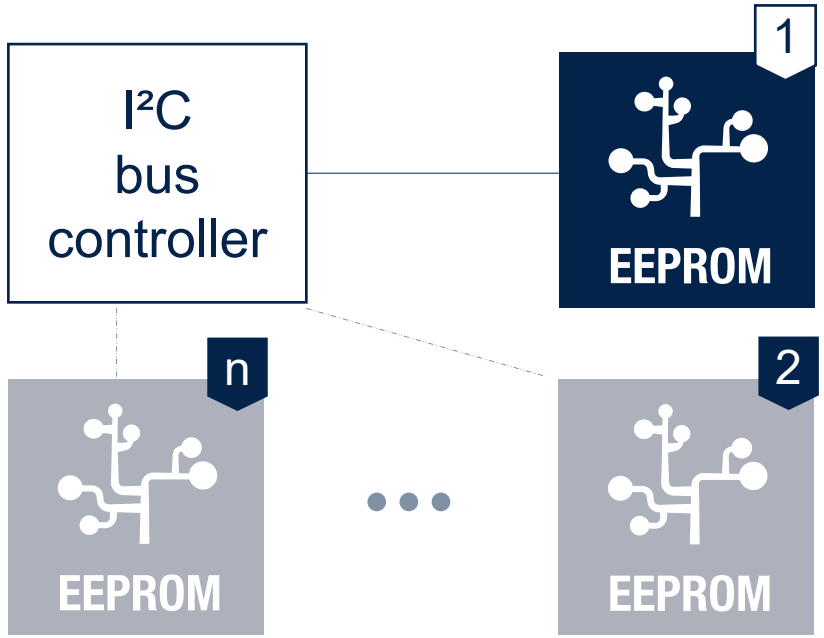
From 40 % up to 76% energy saving vs. 150 nm



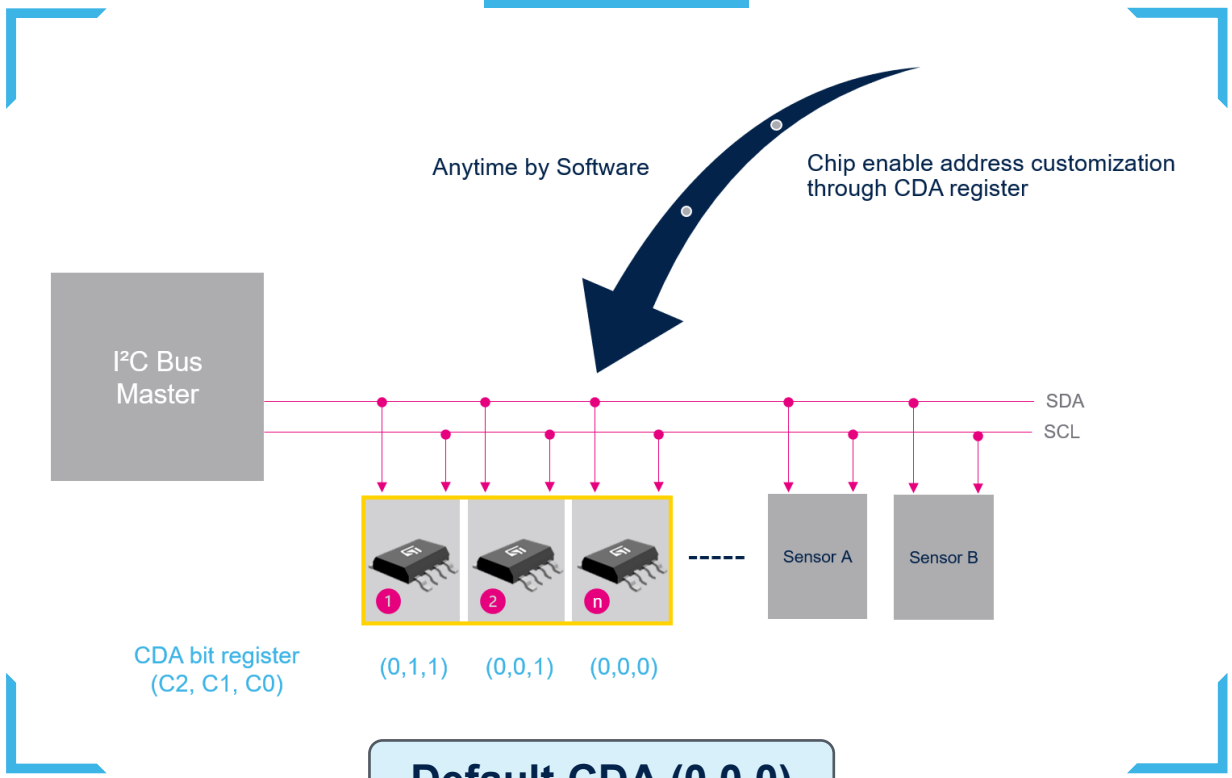
Note: In this schematic, we are showcasing results at 3.3 V. However, our EEPROM portfolio is also available in 1.8 V and 5.5 V versions.

CDA register
for multiple EEPROMs on same bus

Customer request



ST feature

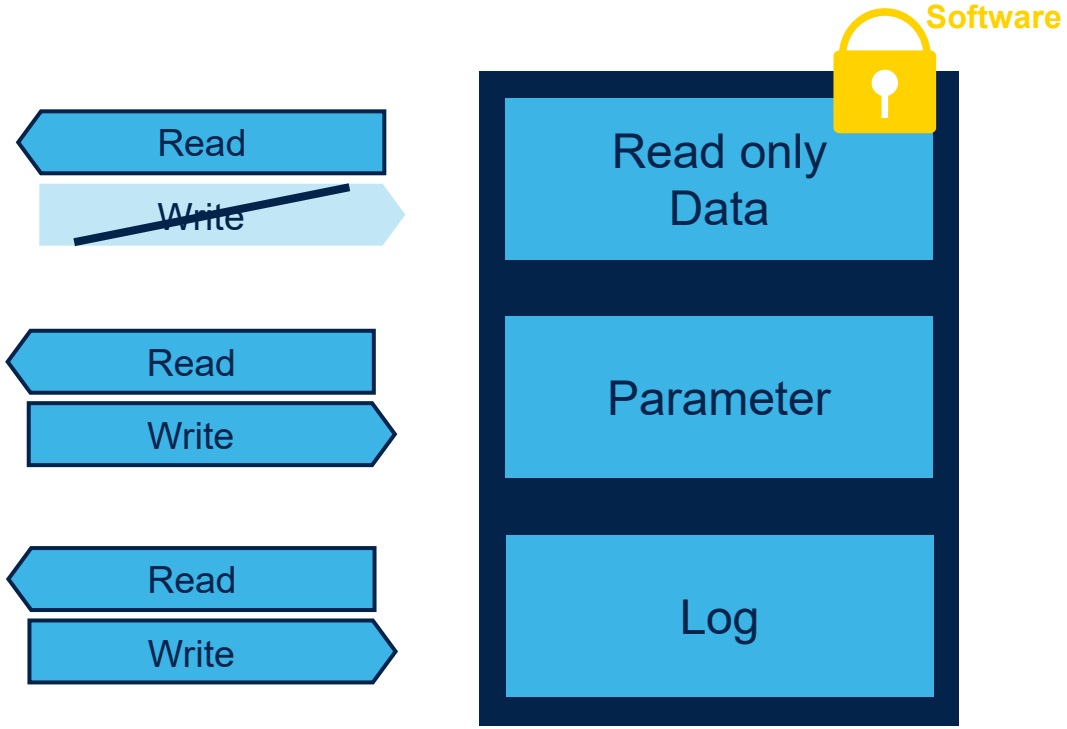


Default CDA (0,0,0)

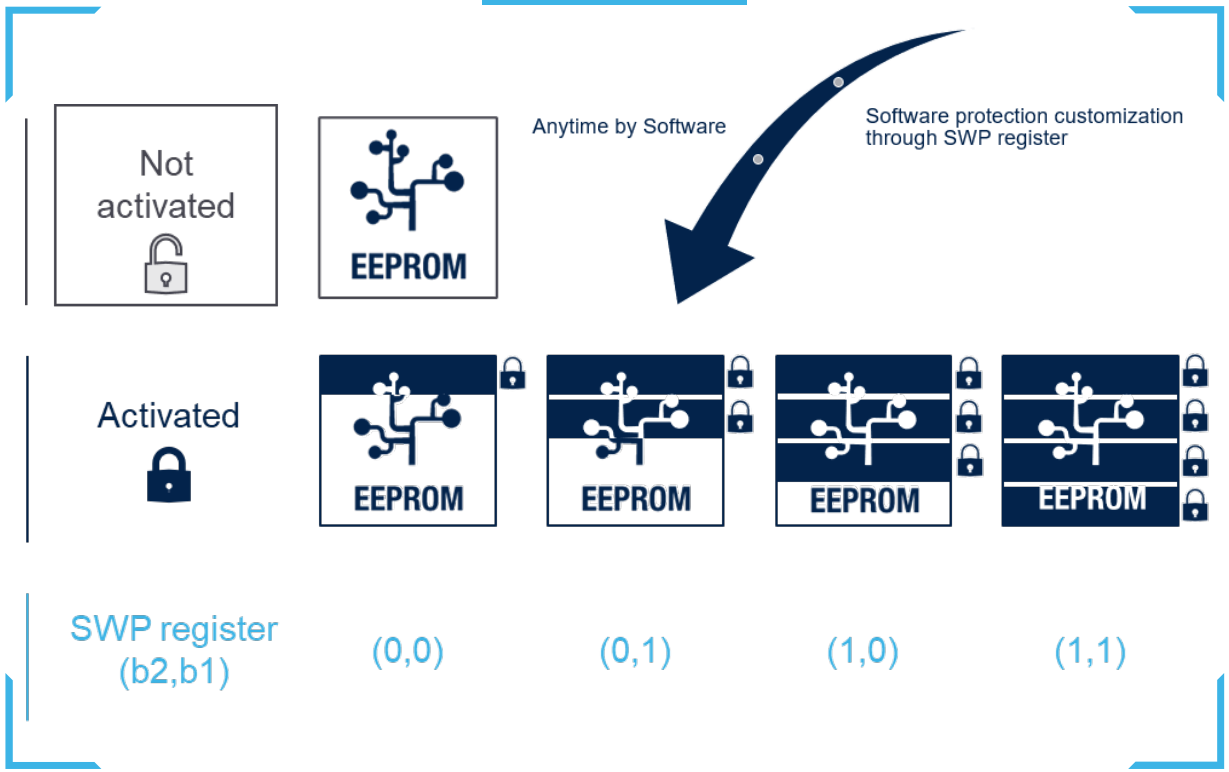
+ existing customized CDA (0,0,1)

Write Protect Software
for data protection

Customer request

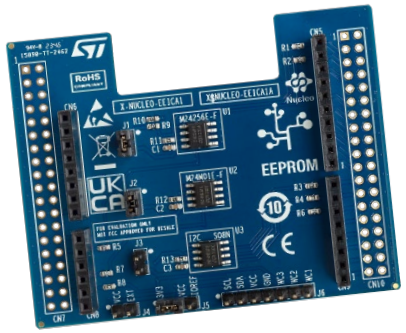


ST feature



Development tools for 110 nm EEPROM technology

STM32 Nucleo expansion board



Discover the
X-NUCLEO-EEICA1
18.23$

STM32Cube expansion package

STM32 CubeExpansion

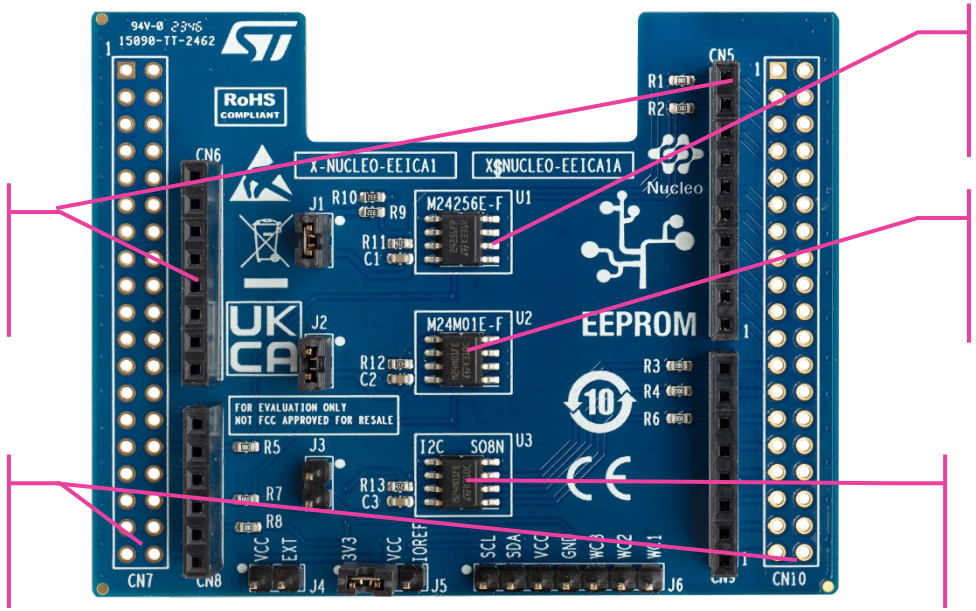
Get start prototyping with
X-CUBE-EEPRMA1
FREE

Try the new generation of EEPROM for your next design

Standard I²C EEPROM memory expansion board

Arduino Uno & ST Zio connectors:
Easy access to add-ons

ST morpho extension pins:
Direct access to all MCU I/Os



M24256E-F
Standard I²C EEPROM

M24M01E-F
Standard I²C EEPROM

External I²C EEPROM

Can be plugged on top of an STM32 NUCLEO-F401RE, NUCLEO-L053R8, NUCLEOG474RE, or NUCLEO-H743ZI development board

New high density I²C EEPROM 85°C – 110 nm

From 256-Kbit to 2-Mbit

M24256E-F, M24512E-F, M24M01E-F, M24M02E-F

High endurance (4 million write cycles), low supply (1.6 V)

- **Footprint compliant with legacy EEPROM**
- **Long-term price competitiveness**

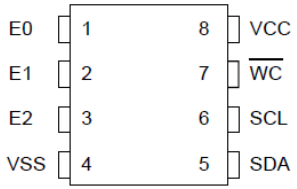
Densities	NRND Legacy RPNs	New RPNs	Packages	New CPNs
256 Kbits	M24256-BF M24256-BR M24256-BW M24256-DF M24256-DR	M24256E-F M24256X-F	**SO8N** **TSSOP** **DFN8** **DFN5** **WLCSP4**	M24256E-FMN6TP M24256E-FDW6TP M24256E-FMC6TG M24256E-FMH6TG M24256X-FCU6T/VF
512 Kbits	M24512-DF M24512-R M24512-W	M24512E-F M24512X-F*	**SO8N** **TSSOP** **DFN8** **WLCSP4***	M24512E-FMN6TP M24512E-FDW6TP M24512E-FMC6TG M24512X-FCP6T/VF (*availability Q2-2025)
1 Mbit	M24M01-DF M24M01-R	M24M01E-F M24M01X-F	**SO8N** **TSSOP** **DFN8** **WLCSP5** **WLCSP4**	M24M01E-FMN6TP M24M01E-FDW6TP M24M01E-FMC6TG M24M01E-FCS6T/VF M24M01X-FCU6T/VF
2 Mbits	M24M02-DR	M24M02E-F	**SO8N** **TSSOP** **DFN8** **WLCSP5**	M24M02E-FMN6TP M24M02E-FDW6TP M24M02E-FMC6TG M24M02E-FCS6T/VF

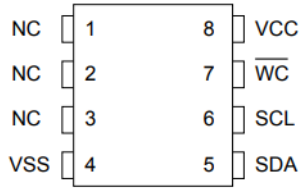
Footprint compliant ⇒ existing PCB can be reused

Dedicated **CP** on-demand **with pre-programmed default device address ⇒ no software change**

Design changes
M24256-*yzz* vs. M24256E-F

Item	150 nm technology	110 nm technology	Why choose the 110 nm technology?
Pin package	• 8 pins: SCL/SCDA/Vcc/Vss/Ei/WC • Ei pins for hardware chip enable address setting	• M24xxxE-F: 8-pin package • SCL/SCDA/Vcc/Vss & (WC). • And 3 “Not Connected” pins (Ei pins)	• 8-pin package (footprint) fully compliant • Ei pins: the Chip Enable Address is managed by software thru CDA*
***Configurable device address register (CDA)**	The Chip Enable Address is managed by hardware through Ei pins.	The Chip Enable Address is managed by software through the CDA register.	For 110 nm products, the Chip Enable Addressing is managed by software. M24526E-FMN6TP is delivered with Chip Enable Address 0, address which can be modified later. M24256E-FMN6T4 have pre-programmed and locked Chip Enable Address “100”
****Device Type Identifier**	The device ‘understands’: • 1010 for addressing the memory array • 1011 for addressing the identification page	• 1010 for addressing the memory array • 1011 for addressing the Identification page, ID Page lock status register and CDA register.	100 nm products offer same DTI**: • 1010 for memory array and 1011 for Identification page (F8H) • 1011 for registers. • The registers selection depends on MSB address values





**configurable device address register*

Our technology starts with You

Find out more at st.com/eeprom

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