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Digital Controller Eases Design Of Interleaved PFC For Multi-kilowatt Converters

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In power supply applications requiring higher power up to and beyond a kilowatt, the design of power factor correction (PFC) boost converters using interleaved stages rather than a single stage becomes advantageous. That's because the combination of multiple interleaved stages allows for use of smaller, lower-profile components including smaller filter components. However, the controller IC options that have been available to date have required specialized design and programming skills in order to implement PFC at the kilowatt level, while also imposing performance restrictions due to bandwidth limitations associated with digital control of the compensation loop.

To overcome these difficulties, a new digital controller has been developed that is suitable for multi-channel interleaved PFC topologies operating in continuous conduction mode (CCM). The operation and application of this IC, the STNRGPF01, are presented in this article.

The main characteristics and specifications of the controller are provided in the first section. The control structure is then discussed: this is based on a semi-digital control scheme where the time critical functions such as fast overcurrent protection and input current control are performed using analog parts to attain precise, cycle-by-cycle regulation.

All the non-time-critical functions, such as multiplier, feed-forward compensation, voltage protections and voltage control loop are implemented digitally. The experimental results for a 3-kW three-channel interleaved PFC prototype, provided in the last section of the article, show the suitability of the proposed approach and the benefits of combining digital and analog control techniques.

Benefits And Challenges Of Interleaved PFC

In applications where the required power is greater than 1 kW and where the form factor is a design constraint, interleaved converters are often used. Interleaving of PFCs consists of using two or more active single-switch stages (Fig. 1), each rated for a lower power, instead of a single stage rated for the full power and more challenging to design.

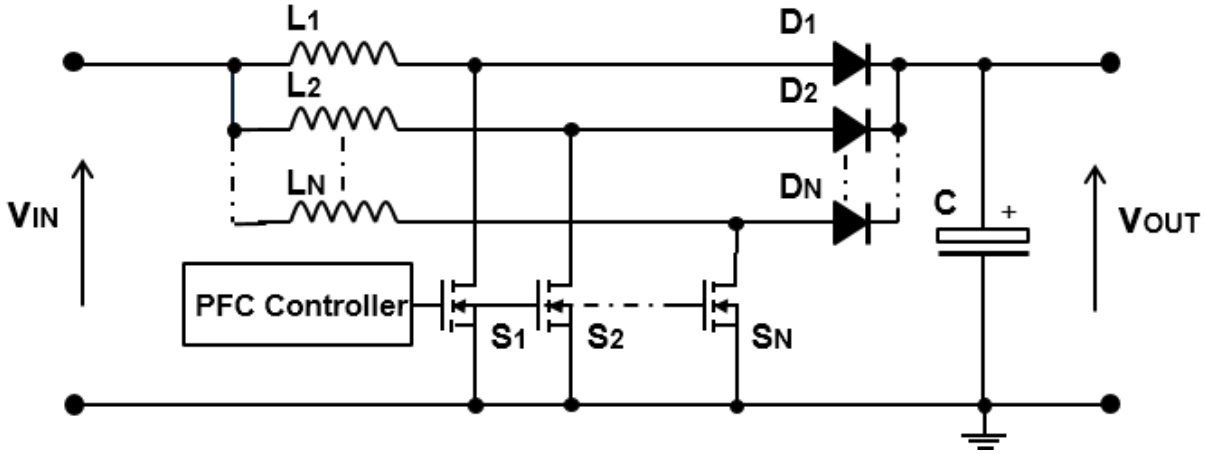

Fig. 1. Interleaved boost PFC with N active channels.

The main advantages of an interleaved converter are ripple cancellation, reduction of magnetic component size and volume, lower EMI and better thermal management. By interleaving, the equivalent inductor current ripple

is reduced and it is completely cancelled for some precise values of duty cycle (i.e. D = 0.5 for two-channel boost; D = 0.33 and D = 0.66 for three-channels PFCs).

The ripple-cancellation effect, which is a consequence of operating the paralleled stages with a phase shift equal to 360 degrees divided by the number of stages, is also very important not only for EMI and power density but also for efficiency.

Few analog ICs are available for the implementation of interleaved topologies. Most of them limit the designer to the use of two interleaved PFC stages operated in critical conduction mode (CrCM) with constant on time (COT) control. This allows the use of these controllers in applications rated up to about 800 W. Only very few ICs are suitable for continuous conduction mode (CCM) control.

That's significant because CCM is very important and almost mandatory as the power requirement of the application increases. In any case, some of the functions required for compliance with new regulatory standards (i.e. ENERGY STAR) such as phase shedding, needed to ensure low standby power and flat efficiency curves, are difficult to manage and implement in analog controllers, especially as the number of active phases increases.

On the other hand digital controllers are available. They are more flexible compared to analog ICs and also more expensive. Powerful MCUs and DSPs allow the implementation of advanced functions, the use of more sophisticated topologies and provide interface and communication peripherals. But they require a lot of engineering resources, skills and time to be programmed. In addition, full digital control has bandwidth limitations compared to an analog implementation.

This article presents the STNRGPF01, a three-channel interleaved CCM PFC digital controller, and discusses the associated control and configuration strategy to provide the flexibility of digital control and the fast dynamics of analog controllers. Ease of use and fast development time are other advantages highlighted throughout the article.

The STNRGPF01 Controller

The STNRGPF01 is a digital configurable ASIC developed by STMicroelectronics. It is able to drive up to three channels in CCM interleaved PFC boost topologies to meet the IEC 61000-3-2 standard for electrical equipment.

The architecture is shown in the block diagram of Fig. 2. The controller is built around an 8-bit CPU with a 16-MHz clock and it can be configured using a dedicated software tool.

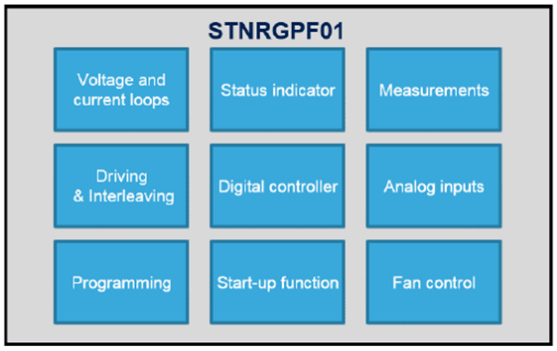

Fig.2. The STNRGPF01 PFC controller architecture.

The measurement block uses 10-bit analog-to-digital converters (ADCs) with up to eight configurable channels. This block is used for the acquisition of the feedback signals necessary for the implementation of the control scheme shown in Fig. 3.

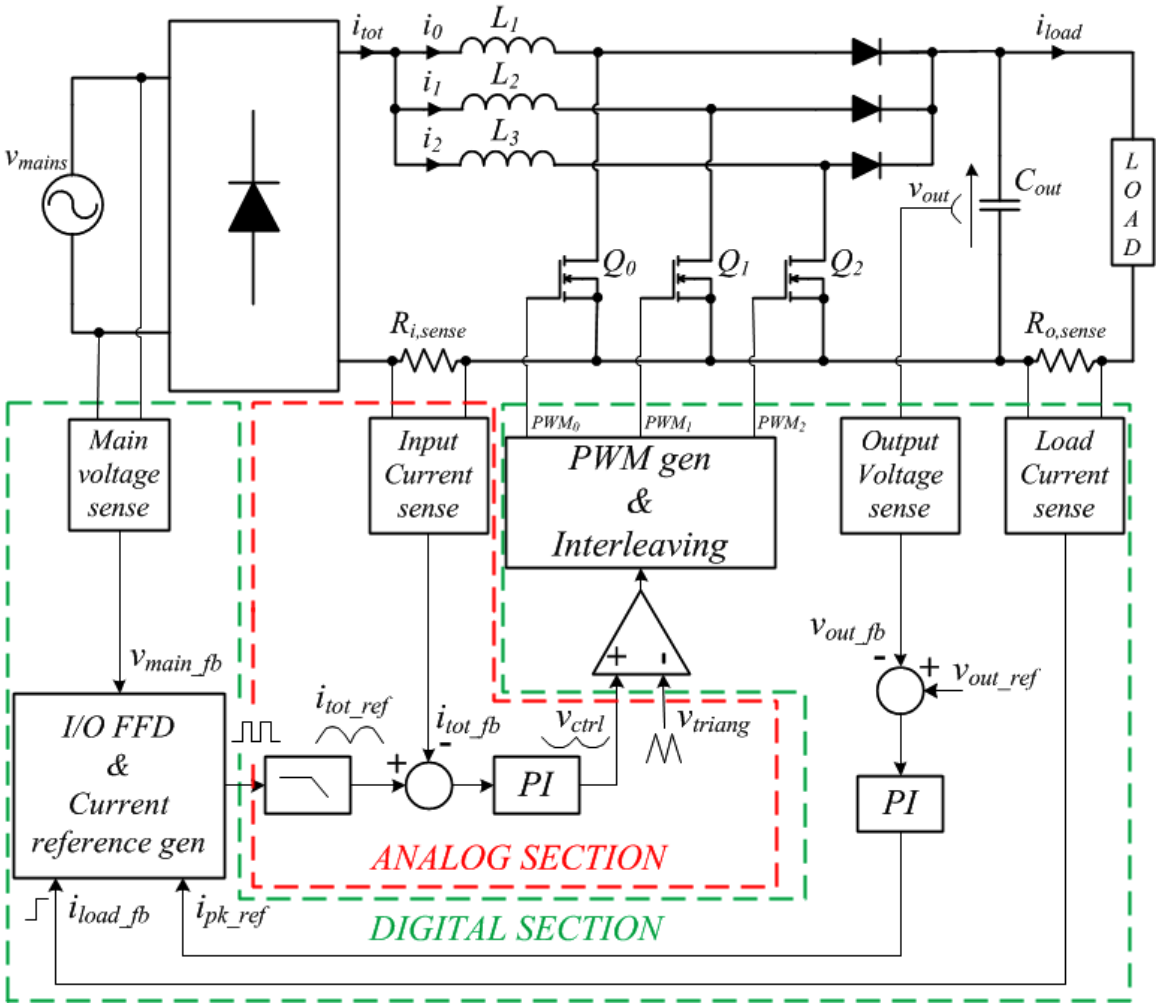

Fig. 3. Control scheme implemented with the STNRGPF01.

An outer voltage control loop is used to regulate the PFC bus voltage to a preselected value while an inner current loop regulates the total average inductor current. This is sensed by means of a resistor R_{i_sense} placed on the ground return path of the PFC current. The difference between the output voltage feedback V_{out_fb} and reference V_{out_ref} is sent to a digital PI controller, which calculates the peak of total input average current i_{pk_ref}. The PFC current reference is internally generated and is available on the output of an I/O Feed Forward (I/O FFD) block as a PWM waveform.

The PWM is then filtered and used as the total average sinusoidal input current reference i_{tot_ref} for the inner current loop. This is implemented using standard analog techniques as highlighted by the red dashed line of Fig. 3. The difference between the current reference i_{tot_ref} and the input current feedback i_{tot_fb} is sent to an analog PI controller whose output v_{ctrl} is used to generate the master PWM_0 signal by comparison with a triangular wave V_{triang} at the switching frequency. This is detailed in Fig. 4 which shows, the digital voltage control loop and the use of two fast comparators, internal to the controller, for the generation of the master PWM signal.

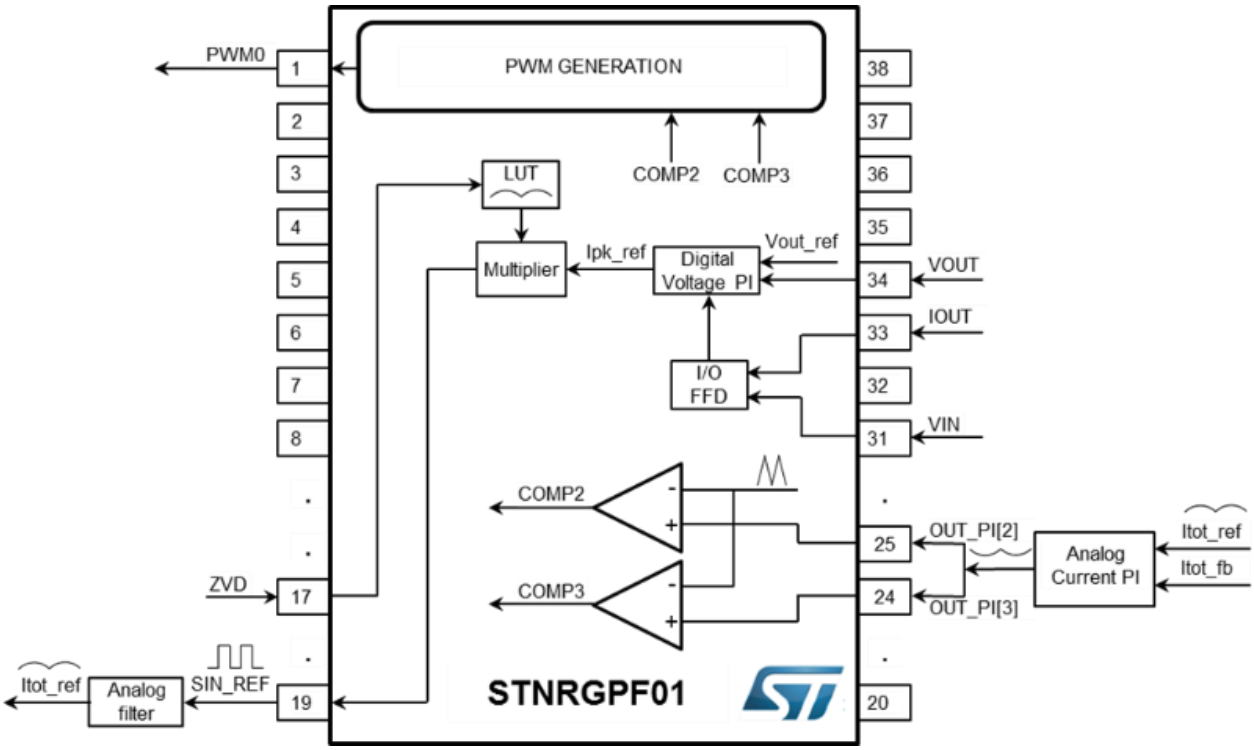

Fig. 4. Detail of the generation of the PWM_0 master signal for interleaved PFC control.

The outputs of the two comparators, COMP2 and COMP3, are sent to the driving and interleaving block where the three PWM signals used to control the three power switches are generated.

The interleaving operation is highlighted in Fig. 5. The master signal (PWM0) rising and falling edges are used to determine the phase shift and the duty cycle of each of the two slave signals by means of two event-driven state machines embedded in the STNRGPF01 (SMED1 and SMED2 for PWM1 and SMED4 and SMED5 for PWM2).

The output of the SMEDs are SET & RESET signals processed by two flip-flops in order to generate the PWMs signals for the two slave channels. The phase delay of the slave signals is determined by synchronizing the SMEDs with a timer counter managed by the CPU and triggered by PWM0.

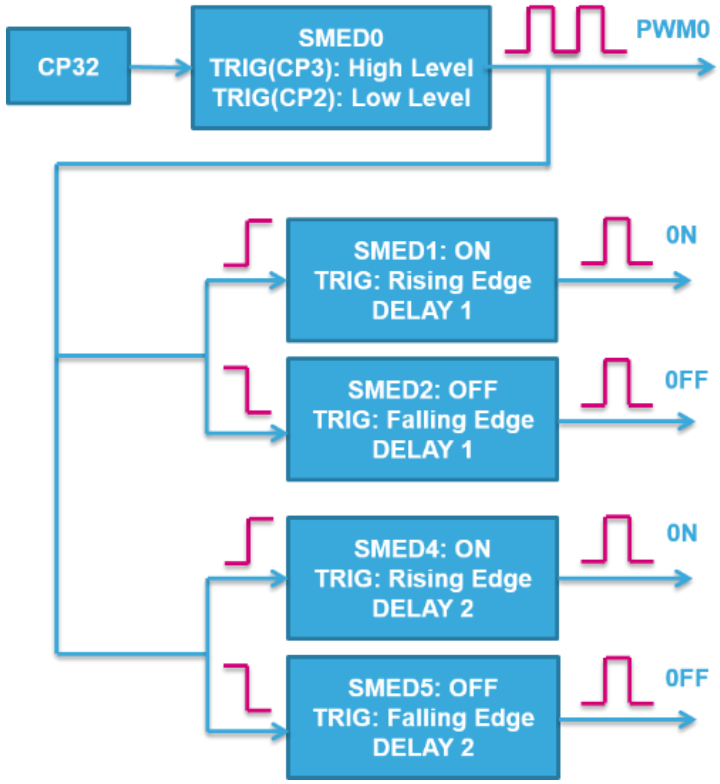

Fig. 5. Interleaving operation of the STNRGPF01.

The digital section, highlighted in Fig. 3 by the green dashed line, is also used for input voltage and load feed-forward functions. When the mains voltage changes suddenly or a load current step occurs a fast transient response is present. Finally, the programming block has I^2C and UART interface, which can also be used for monitoring and communication functions.

Designing The Current-Control Loop

The interleaved boost converter small-signal transfer functions are obtained using the state-space averaging (SSA) method and a linearization operation (Taylor's series around an operating point). It is useful in order to calculate the PI regulators' parameters and satisfy bandwidth and phase margin stability requirements. For the sake of simplicity it was assumed that:

1) The converter works in CCM mode only.

2) Active and passive components are ideal.

3) The parallel boost inductors are identical and the total power is shared symmetrically in the three channels.

4) The perturbations on the mains voltage are neglected and this is assumed to be constant during several switching cycles.

In the following equations the notation "~" indicates small-signal variables while the uppercase letters refer to steady-state operating point variables. The control-to-input current transfer function is shown in equation 1.

$$G_i(s) = \frac{\tilde{\imath}_{tot}}{\tilde{\delta}} = \frac{C_{OUT}V_{OUT}^3 s + P_{OUT}(1+\frac{1}{\eta})V_{OUT}}{C_{OUT}L_{PFC}V_{OUT}^2 s^2 + L_{PFC}P_{OUT}s + N_{ch}V_{IN}^2} \quad (1)$$

From this it is clear that the control-to-input current transfer function depends on the number of channels and input voltage value for a fixed output power and regulated output voltage value. In the high-frequency region the following approximation can be used to simplify equation 1.

$$G_i(s) = \frac{\tilde{\imath}_{tot}}{\tilde{\delta}} \simeq \frac{V_{OUT}}{sL_{PFC}} \quad (2)$$

Figs. 6 and 7 show the Bode diagrams of the control-to-input current transfer function for different values of the input voltage and number N_{ch} of active channels respectively.

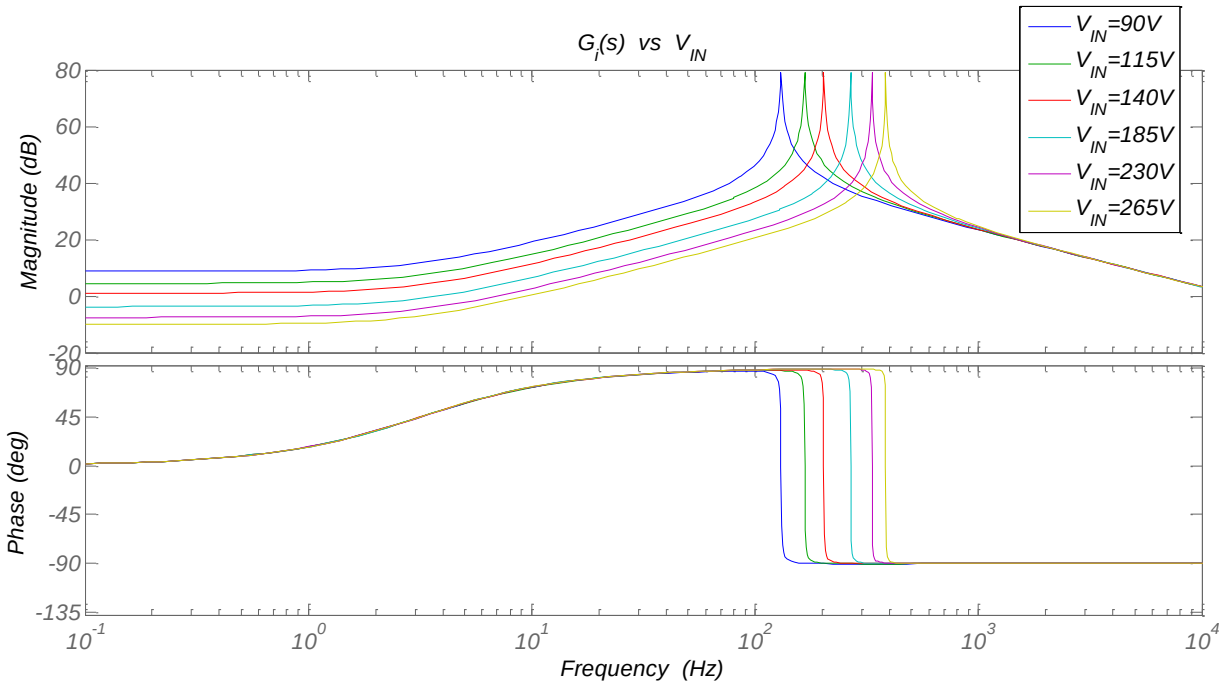

Fig. 6. Bode diagram of control-to-input current transfer function for different values of input voltage.

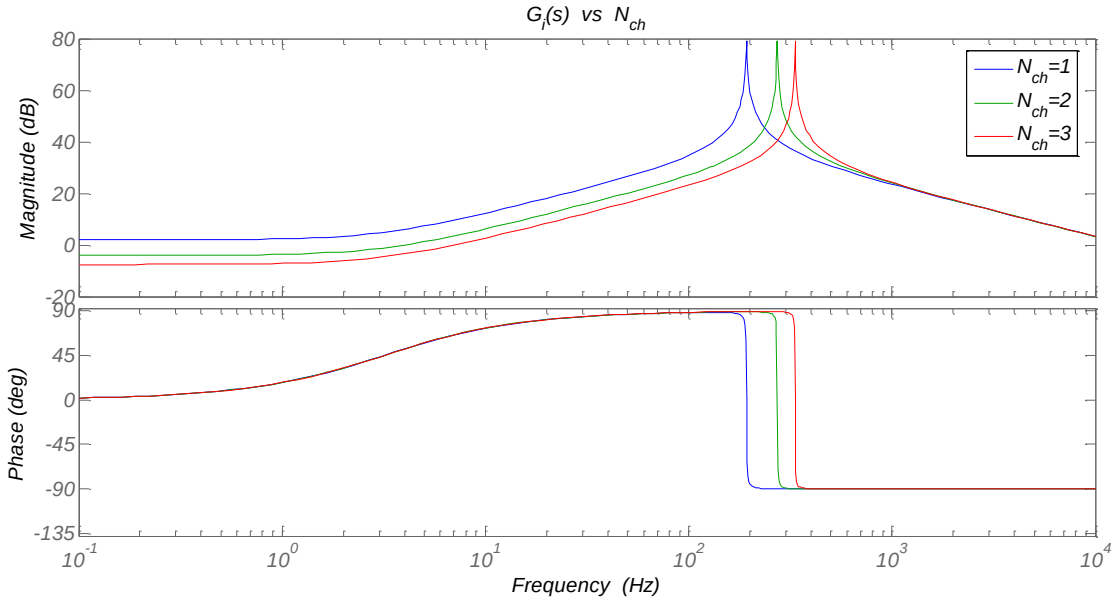

Fig. 7. Bode diagram of control-to-input current transfer function for different Nch values with 230-Vac input.

The current control loop block diagram is shown in Fig. 8. In this diagram, V_{pk_triang} is the peak-to-peak voltage of the triangular carrier and K_{PI_out} is a scaling factor used to match the PI regulator maximum output voltage and the triangular carrier peak voltage.

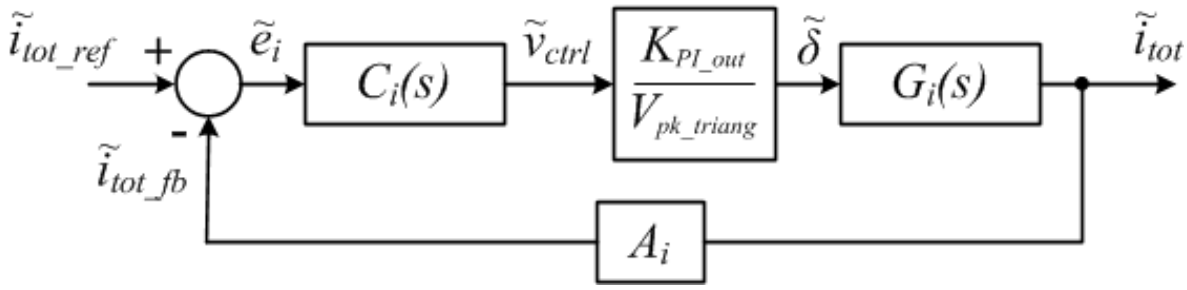

Fig. 8. Block diagram of PFC current control loop.

A_i is the input current sensing gain and $C_i(s)$ is the compensator transfer function. The open-loop compensated transfer function is then given by:

$$T_i(s) = C_i(s)L_i(s) \tag{3}$$

where

$$L_i(s) = \frac{K_{PI\_out}}{V_{pk\_triang}} A_i G_i(s) \tag{4}$$

As mentioned in the previous section the current controller is implemented with standard analog techniques and a type-2 compensation amplifier was chosen for this design (Fig. 9).

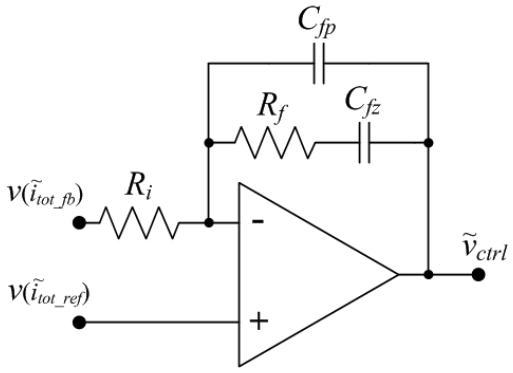

Fig. 9. Type-2 compensation amplifier.

The transfer function of this compensator is given by equation 5.

$$C_i(s) = \frac{1}{(C_{fz} + C_{fp})R_i} \frac{C_{fz}R_f s + 1}{s(\frac{C_{fz}C_{fp}R_f}{(C_{fz} + C_{fp})} s + 1)} \tag{5}$$

The locations of poles and zero are:

$$f_{pi0} = 0$$

$$f_{pi1} = \frac{(C_{fz} + C_{fp})}{2\pi C_{fz}C_{fp}R_f} \approx \frac{1}{2\pi C_{fp}R_f}$$

$$f_{zi1} = \frac{1}{2\pi C_{fz}R_f} \tag{6}$$

where the first pole is placed at the origin to form an integrator. The second pole f_{pi1} can be simplified as in equation 7 if $C_{fp} << C_{fz}$:

$$f_{pi1} = \frac{(C_{fz} + C_{fp})}{2\pi C_{fz}C_{fp}R_f} \approx \frac{1}{2\pi C_{fp}R_f} \tag{7}$$

This pole is usually placed at one half of switching frequency in order to attenuate switching noise without interfering with current loop regulation.

The zero f_{zi1} of the compensator is selected such that it provides sufficient phase margin at the chosen crossover frequency. Typically these parameters are selected according to Eq. 8 where f_{sw} is the switching frequency, f_{Tides} is the desired crossover frequency and PM_{ides} is the desired phase margin. The table summarizes the design parameters used for the implementation of a 3-kW three-channel interleaved PFC converter.

$$\begin{aligned} f_{Ti_{des}} &< \frac{1}{10} f_{sw} \\ PM_{i_{des}} &= 45 - 60\,^{\circ} \\ f_{zi1} &= f_{Ti1}/2 \end{aligned} \tag{8}$$

Table. Main parameters used to design a 3-kW interleaved PFC.

Parameter	Description	Value
P_{OUT}	Output power	3 kW
N_{ch}	Number of channels	3
V_{IN}	RMS nominal input voltage	230 V
V_{OUT}	RMS nominal output voltage	400 V
f	Line frequency	50 Hz
η	Estimated efficiency	98 %
L_{PFC}	single channel boost inductor	120 µH
C_{OUT}	Output capacitor	4x470 µF
V_{pk_triang}	Peak-to-peak voltage of triang. wave	2 V
K_{PI_out}	PI out scale factor	0.5909
A_i	Input current sensing gain	0.0927
A_v	Output voltage sensing gain	1.9128
A_{MUL}	Digital multiplier gain	3.3086
A_{SMED}	Digital to analog gain	0.00068
f_{sw}	Switching frequency	111 kHz
f_{Ti_des}	Current loop crossover frequency	7.5 kHz
f_{Tv_des}	Voltage loop crossover frequency	10 Hz

PM_{i_des}	Current loop phase margin	60°
PM_{v_des}	Voltage loop phase margin	60°
f_{PI_ctrl}	Voltage loop control frequency	1 kHz

Based on these parameters and the previous guidelines for the placement of the poles and zero, the type-2 compensator amplifier parameters can be calculated as follows.

Starting from the selection of R_i, a 5.6-kΩ resistor is used. The value of R_f is then calculated so that the error amplifier brings the control-to-input current transfer function to 0 dB at the desired closed-loop crossover frequency. Looking at the Bode plot in Fig. 7 the required gain of the error amplifier is given by:

$$A_{Ci(s)} = 10^{6.6/20} = 2.1 \tag{9}$$

Hence the value of R_f is calculated as

$$R_f = R_i / A_{Ci(s)} = 2.6\text{k}\,\Omega$$

A 2.4-kΩ resistor can be used.

The high-frequency pole capacitor is calculated from equation 10.

$$C_{fp} = \frac{1}{\pi f_{sw} R_f} = \frac{1}{\pi \cdot 111 \cdot 10^3 \cdot 2400} = 1.1\ nF \tag{10}$$

and a 1-nF capacitor is selected for the implementation.

Lastly, using equations 6 and 8 the value the value of C_{fz} can be calculated as:

$$C_{fz} = \frac{1}{2\pi \frac{f_{Ti}}{2} R_f} = \frac{1}{\pi \cdot 7500 \cdot 2400} = 17.6\ nF$$

A 15-nF capacitor is then used.

The Bode plot of the current compensator amplifier is shown in Fig. 10 while the plot of the current open loop transfer function $T_i(s)$ is shown in Fig. 11.

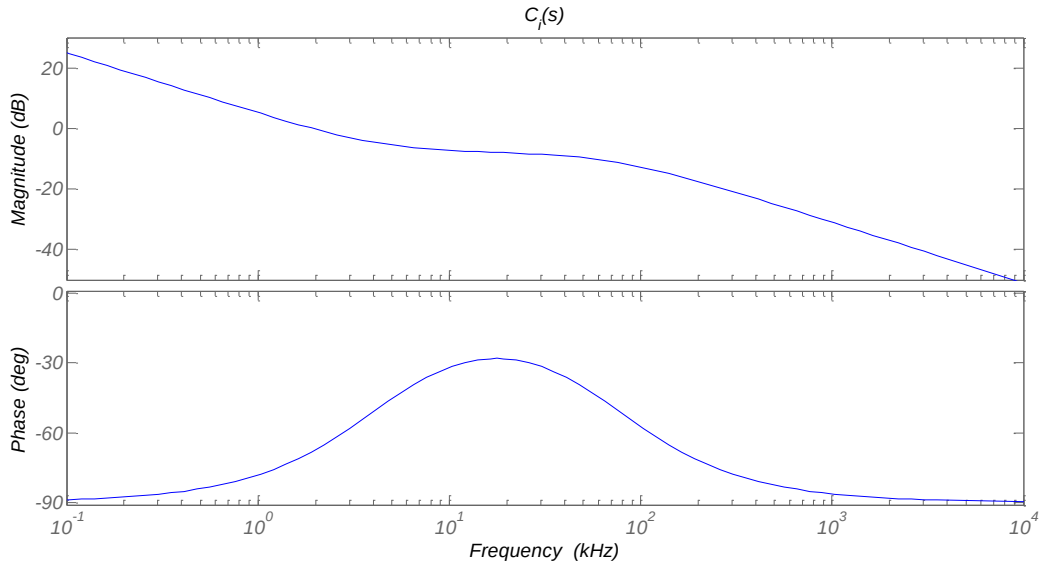

Fig. 10. Bode diagram of current compensator $C_i(s)$.

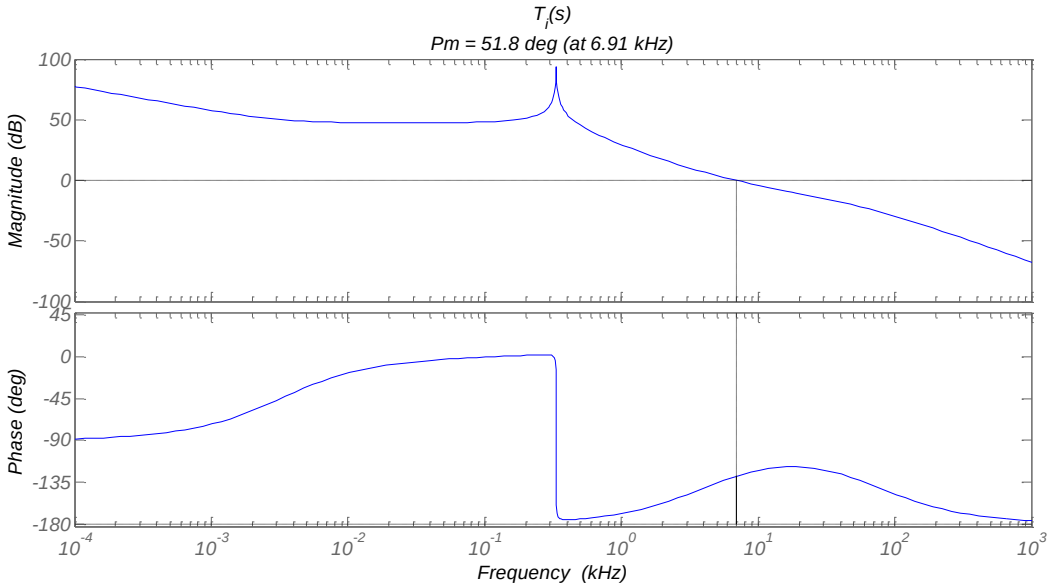

Fig. 11. Bode diagram of compensated current open-loop transfer function, $T_i(s)$.

The method performed above with the suggested pole/zero placement achieves a phase margin of 51.8° and a crossover frequency of 6.91 kHz, very close to the desired one.

Voltage Loop Design

Using similar considerations to the ones shown in the previous section, the control-to-output voltage transfer function is given in equation 11.

$$H_v(s) = \frac{\tilde{v}_{out}}{\tilde{\delta}} = \frac{2\left(N_{ch}V_{IN} - \frac{P_{OUT}}{\eta V_{IN}} L_{PFC} s\right) V_{OUT}^2}{C_{OUT} L_{PFC} V_{OUT}^2 s^2 + L_{PFC} P_{OUT} s + N_{ch} V_{IN}^2} \quad (11)$$

and the input current-to-output voltage transfer function is given in equation 12.

$$G_v(s) = \frac{\tilde{v}_{out}}{\tilde{\imath}_{tot}} = \frac{\tilde{v}_{out}}{\tilde{\delta}} \frac{\tilde{\delta}}{\tilde{\imath}_{tot}} = \frac{2\left(N_{ch}V_{IN} - \frac{P_{OUT}}{\eta V_{IN}} L_{PFC} s\right) V_{OUT}^2}{C_{OUT} V_{OUT}^3 s + P_{OUT}(1 + \frac{1}{\eta}) V_{OUT}} \quad (12)$$

Since voltage loop crossover frequency is generally selected in the range of 5 to 15 Hz, the right half plane zero (higher frequency) can be neglected. The complete cascaded control block diagram is shown in Fig. 12.

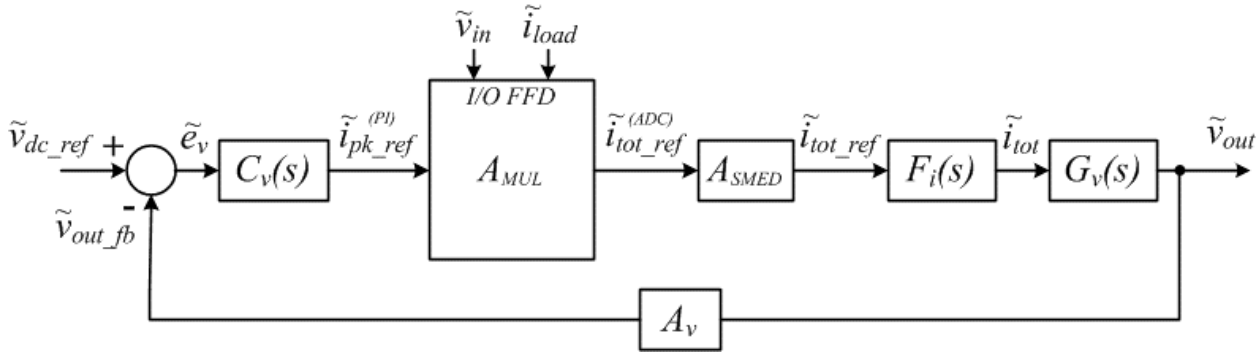

Fig. 12. Block diagram of complete control loop.

In this diagram:

$\tilde{v}_{out}$ = small-signal output voltage

$\tilde{v}_{out\_fb}$= small-signal output voltage sense

$\tilde{v}_{dc\_ref}$= small-signal output voltage reference

$\tilde{v}_{in}$= small-signal input voltage sense

$\tilde{\imath}_{load}$= small-signal load current sense

$\tilde{e}_v$ = small-signal voltage error

$\tilde{\imath}_{pk\_ref}^{(PI)}$= small-signal PI peak current reference

$\tilde{\imath}_{tot\_ref}^{(ADC)}$= small-signal digital sinusoidal current reference

$F_i(s)$= input current closed-loop transfer function

$C_v(s)$ = output voltage compensator transfer function

A_{MUL}= digital multiplier gain for digital current reference generation

A_{SMED}= digital to analog gain for analog current reference generation

A_v= output voltage sensing gain

The I/O FFD block will be analyzed in detail in the next section. For now, it can be simply considered as a constant gain block A_{MUL}. The output voltage loop regulation is done with a digital PI controller:

$$C_v(s) = \frac{K_{P\_Vdc}s + K_{I\_Vdc}}{s} \tag{13}$$

The PI parameters are calculated to achieve the following design targets:

$$\begin{aligned} f_{Ti\_des} &= 5 - 15\ Hz \\ PM_{i\_des} &= 45 - 60\ ^\circ \end{aligned} \tag{14}$$

Considering the open-loop compensated transfer function shown in equation 15:

$$T_v(s) = C_v(s)L_v(s) \tag{15}$$

where

$$L_v(s) = A_{MUL}A_{SMED}F_iG_v(s)A_v \tag{16}$$

and that a stable system is obtained if the following two conditions are verified:

$$\begin{cases} \left|T_v\left(j\omega_{Tv\_des}\right)\right| = 1 \\ \angle T_v\left(j\omega_{Tv\_des}\right) = -180^\circ + PM_{v\_des} \end{cases} \tag{17}$$

The compensator parameters can be obtained by solving the following system:

$$\begin{cases} K_{I\_Vdc} = \dfrac{\omega_{Tv\_des}}{\left|L_i\left(j\omega_{Tv\_des}\right)\right|\sqrt{1+\tan^2\left(PM_{v\_des} - 90^\circ - \angle L_v\left(j\omega_{Tv\_des}\right)\right)}} \\ K_{P\_Vdc} = \dfrac{K_{I\_Vdc}\tan\left(PM_{v\_des} - 90^\circ - \angle L_v\left(j\omega_{Tv\_des}\right)\right)}{\omega_{Tv\_des}} \end{cases} \tag{18}$$

which is solved by

$$\begin{cases} K_{I\_Vdc} = 35.7965 \\ K_{P\_Vdc} = 0.5181 \end{cases}$$

Finally, Figs. 13 and 14 show the Bode diagrams of the voltage-loop compensator and the compensated open-loop transfer function.

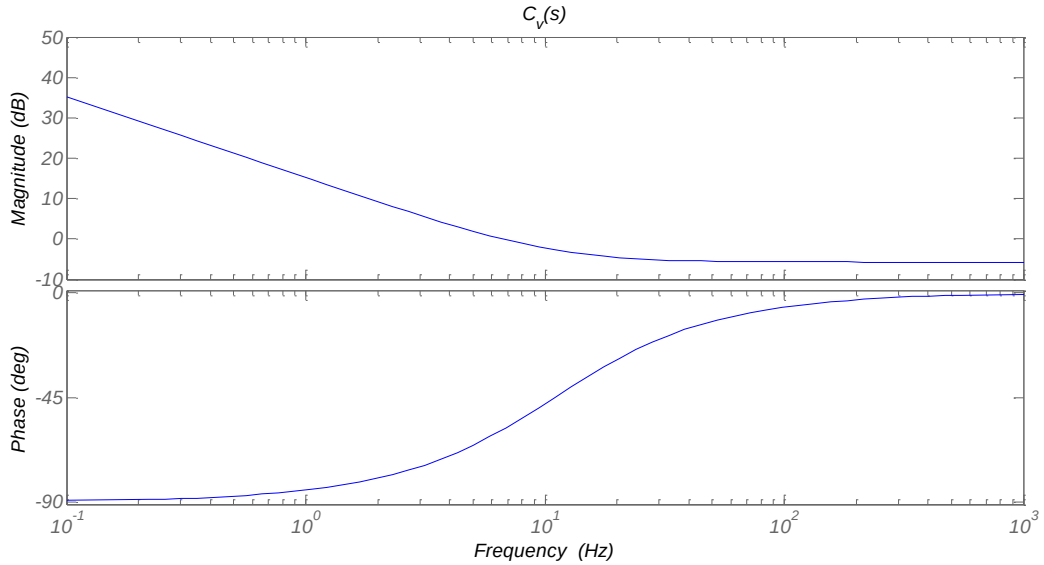

Fig. 13. Bode diagram of voltage compensator $C_v(s)$.

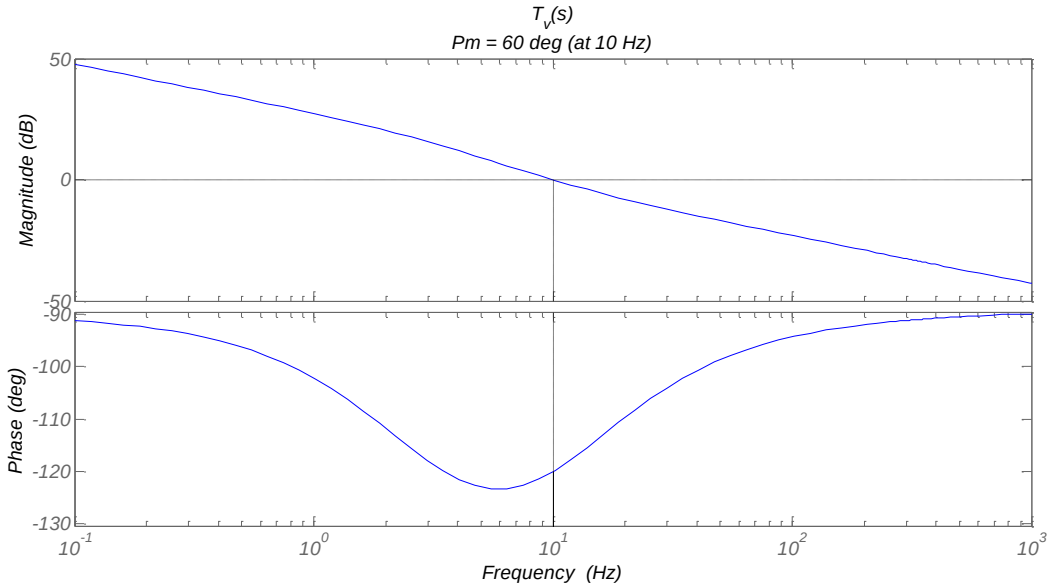

Fig. 14. Bode diagram of voltage open-loop transfer function $T_v(s)$.

With the calculated parameters a phase margin of 60° at the crossover frequency of 10 Hz is obtained. Note that the integral gain K_{IVdc} cannot be directly used by the firmware routine. In fact, it has to be divided by the execution frequency of the digital PI, which is one of the parameters listed in the table.

$$K_{I_{Vdc}}{}^{*} = \frac{K_{I_{Vdc}}}{f_{PI_{ctrl}}} = \frac{35.79}{1000} = 0.03579 \tag{19}$$

I/O Feed-Forwards And Current-Reference Generation

The low bandwidth of the voltage loop may cause regulation problems when the mains voltage or load current changes suddenly. So, the purpose of the I/O FFD block (Fig. 15) is to solve these problems by reducing the system transient response time.

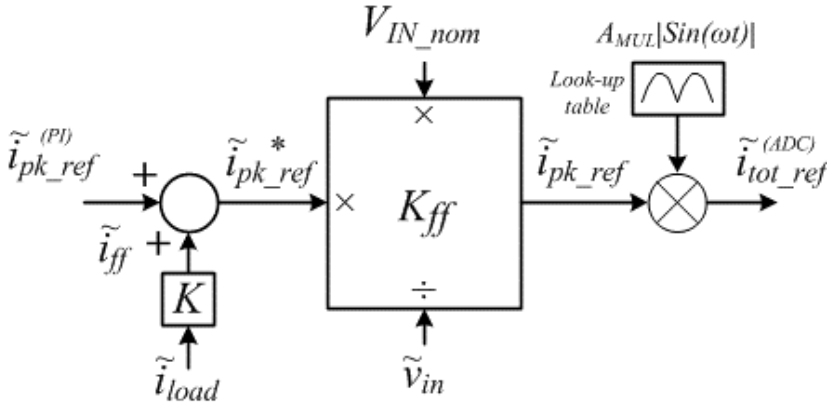

Fig. 15. I/O FFD block.

This is done by summing a portion of load current $\tilde{i}_{ff}$ to the output of the voltage PI regulator. This term provides an immediate contribution to quickly change the peak current reference $\tilde{i}^{*}_{pk\_ref}$ when a load step occurs, as detailed in equation 20.

$$\tilde{i}^{*}_{pk\_ref} = \tilde{i}^{(PI)}_{pk\_ref} + \tilde{i}_{ff} \tag{20}$$

Then $\tilde{i}^{*}_{pk\_ref}$ is multiplied for a coefficient K_{ff} which takes into account input voltage fluctuations with respect to the nominal voltage. The input voltage feed-forward equation is:

$$\tilde{i}_{pk\_ref} = \frac{\tilde{i}^{*}_{pk\_ref}}{\frac{\tilde{v}_{in}}{V_{IN\_nom}}} = \tilde{i}^{*}_{pk\_ref} K_{ff} \tag{21}$$

From equation 21 it is clear that an increase in the RMS input voltage causes a decrease of $\tilde{i}_{pk\_ref}$ and vice versa. A pseudo-sinusoidal shaped current reference is obtained by multiplying $\tilde{i}_{pk\_ref}$ and the output of a look-up table:

$$\tilde{i}^{(ADC)}_{tot\_ref} = \tilde{i}_{pk\_ref} A_{MUL} |\sin(\omega t)| \tag{22}$$

where the A-D converter gain is taken into account as

$$\tilde{i}_{tot\_ref}^{(ANALOG)} = \tilde{i}_{tot\_ref}^{(ADC)} A_{SMED} \tag{23}$$

This current reference is available as a PWM signal on pin 19 of the device so it has to be filtered by a proper analog circuit in order to be used as the reference of the current control loop.

Experimental Results

The described control concept was used to implement a 3-kW three-channel interleaved boost converter. The following specifications were used for this prototype:

- Input voltage range, V_{IN} = 90 to 265 Vac
- Line frequency range, f = 47 to 63 Hz
- Output power, P_{OUT} = 3 kW (1.5 kW at 115 V)
- Output voltage, V_{OUT} = 400 V
- Switching Frequency, f_{sw} = 111 kHz
- Cycle-by-cycle regulation
- Input voltage and load feed-forwards
- Phase shedding function
- Number of interleaved channels, Nch = 3.

A picture of the 3-kW three-channel interleaved PFC is shown in Fig. 16. The implementation achieves a power density of 52 W/in^3 thanks to a compact layout and the small size of the magnetic components, which are a consequence of the interleaving effect and switching frequency selection.

Fig. 16. Implementation of a 3-kW three-channel interleaved PFC.

The STNRGPF01 controller is placed on the vertically mounted PCB. The connector on the upper left hand side of this board is used to program the controller. The programming and customization of the controller functions can be done by using a dedicate software tool called E-design suite.[5]

The design parameters reported above can be used as inputs to the software together with other specific parameters (mainly the ones reported in the table above) such as current and voltage control-loop bandwidth. In this way a complete design is automatically generated including a schematic and bill of materials. The design of both the analog and digital controllers discussed in the previous sections of this article are provided as well.

Most importantly, a binary code customized for the application input parameters is generated. This binary code can be downloaded into the STNRGPF01 through the programming port. By doing so, there is no need to write and debug complex code and the development time is dramatically reduced.

The main waveforms of the converter operating at full load in steady-state conditions when supplied from a 115-Vac source are shown in Fig. 17.

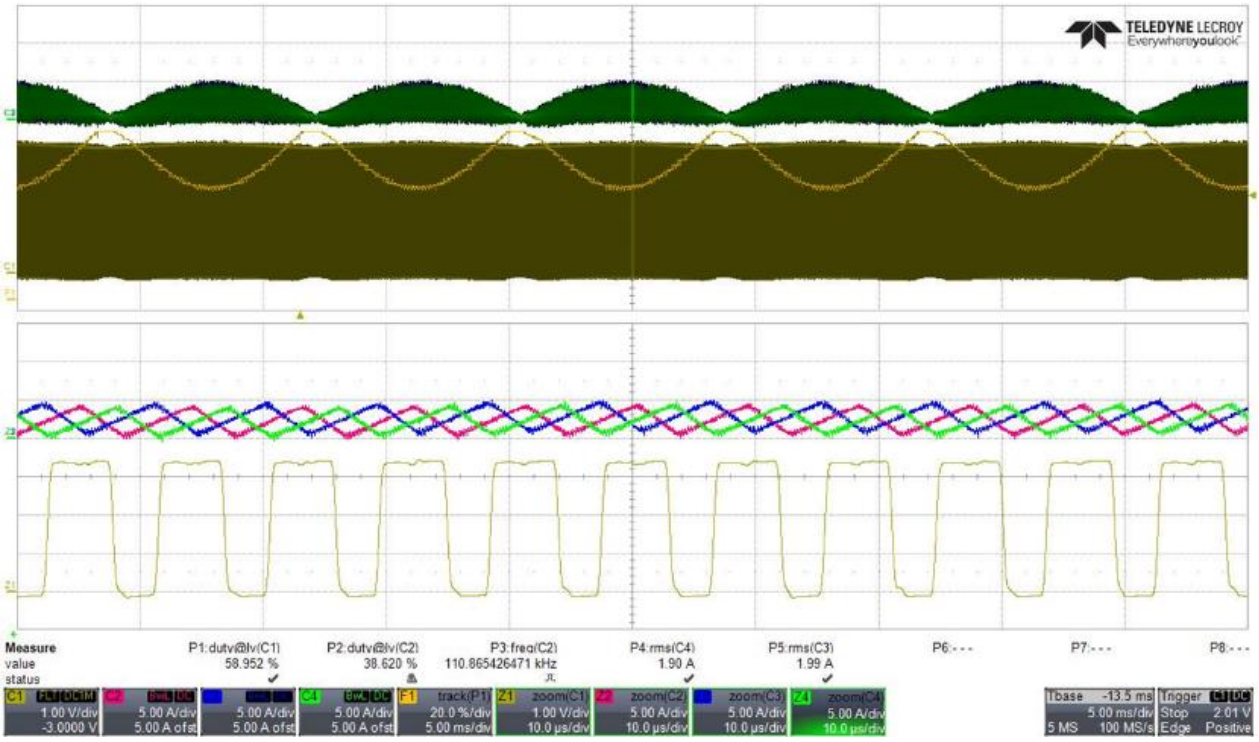

Fig. 17. Main converter waveforms in steady state.

The interleaving effect on the currents is clear. The PFC operates in CCM condition having 120° of phase shift between the phases. The master PWM signal is shown by the yellow trace and has a duty cycle of about 60%.

The dynamic response of the converter can be appreciated in Fig. 18. The PFC is initially unloaded with the dc bus voltage regulated at 430 Vdc with burst-mode control. As soon as a 2-kW load is applied, the output voltage is quickly regulated at the reference value corresponding to 400 V. The initial undershoot is effectively reduced by the load feed forward action triggered by the load step.

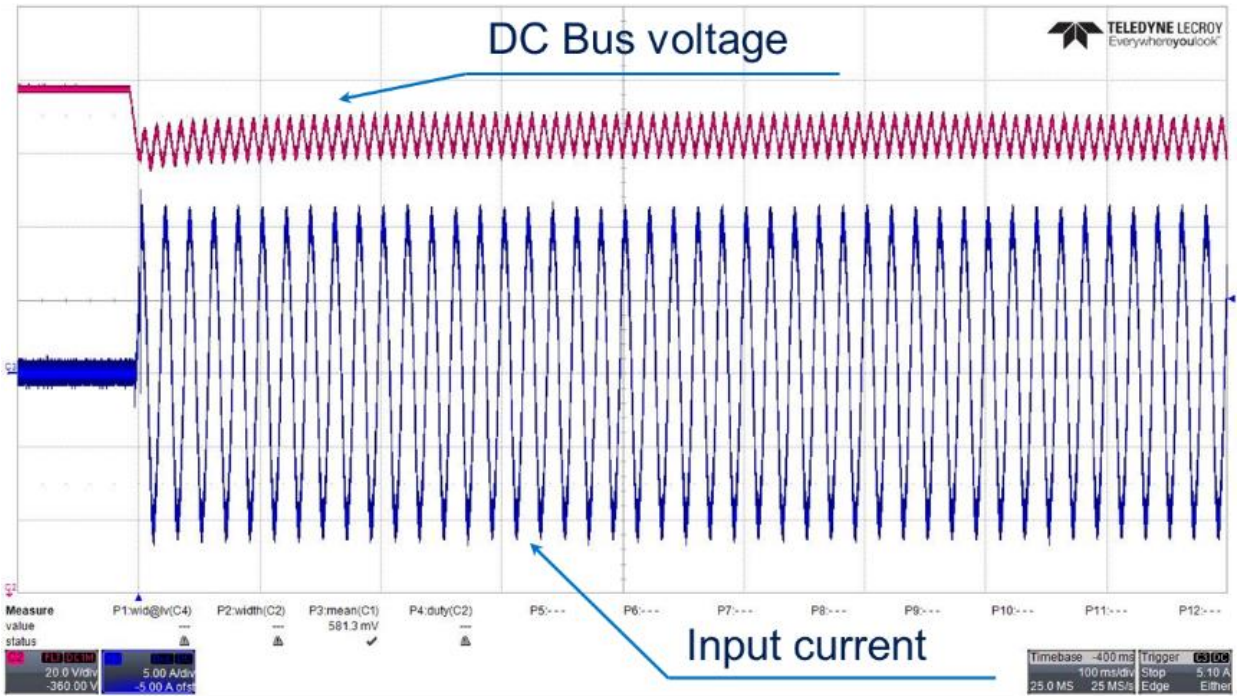

Fig. 18. Load transient, from no load to 2 kW.

The PFC interrupts the burst mode to meet the load requirement and when the load is disconnected it returns to burst mode as it is possible to notice in Fig. 19. This details a transition from no load to 2 kW and back to no-load operation.

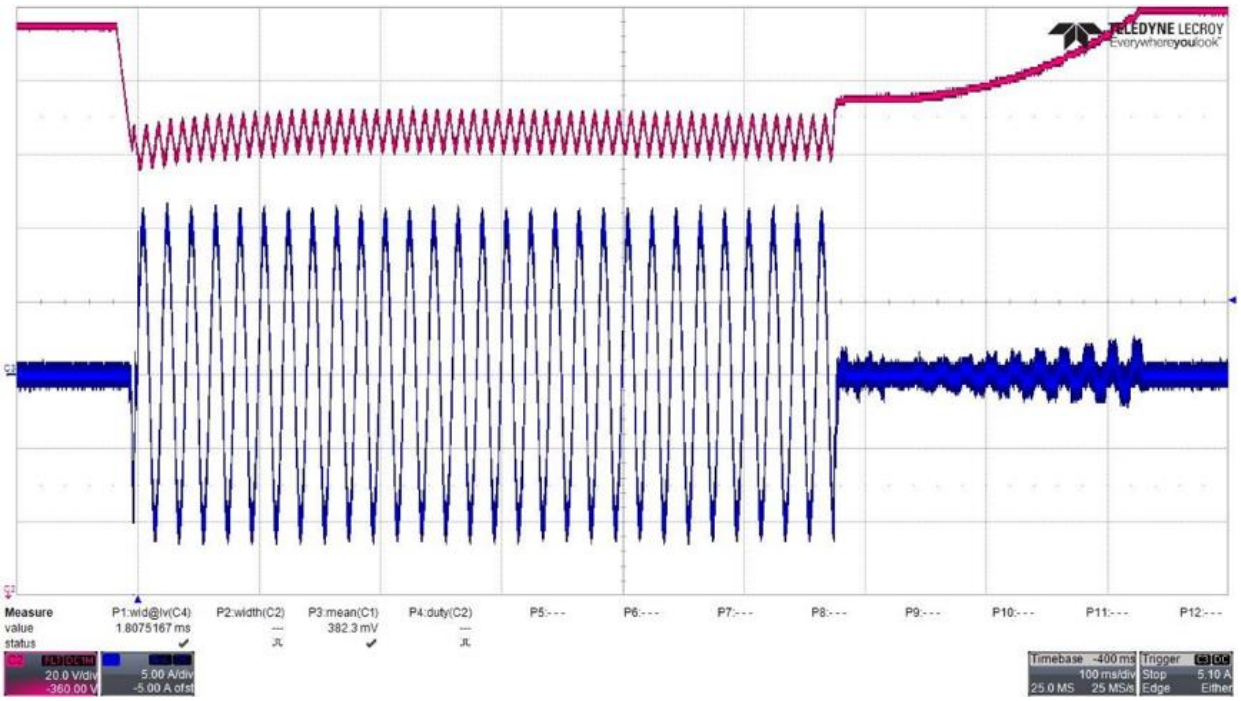

Fig. 19. Load transient, from no load to 2 kW to no load.

Fig. 20 shows a similar transient response when the 2-kW load is suddenly applied while the converter is not operating in burst mode as a 400-W load is already supplied. A 10% to 100% (and 100% to 10%) load transition is highlighted in Fig. 21. The PFC is supplied directly from the ac grid at 230 Vac. The dynamic response is fast and the dc bus voltage is tightly regulated at the reference value.

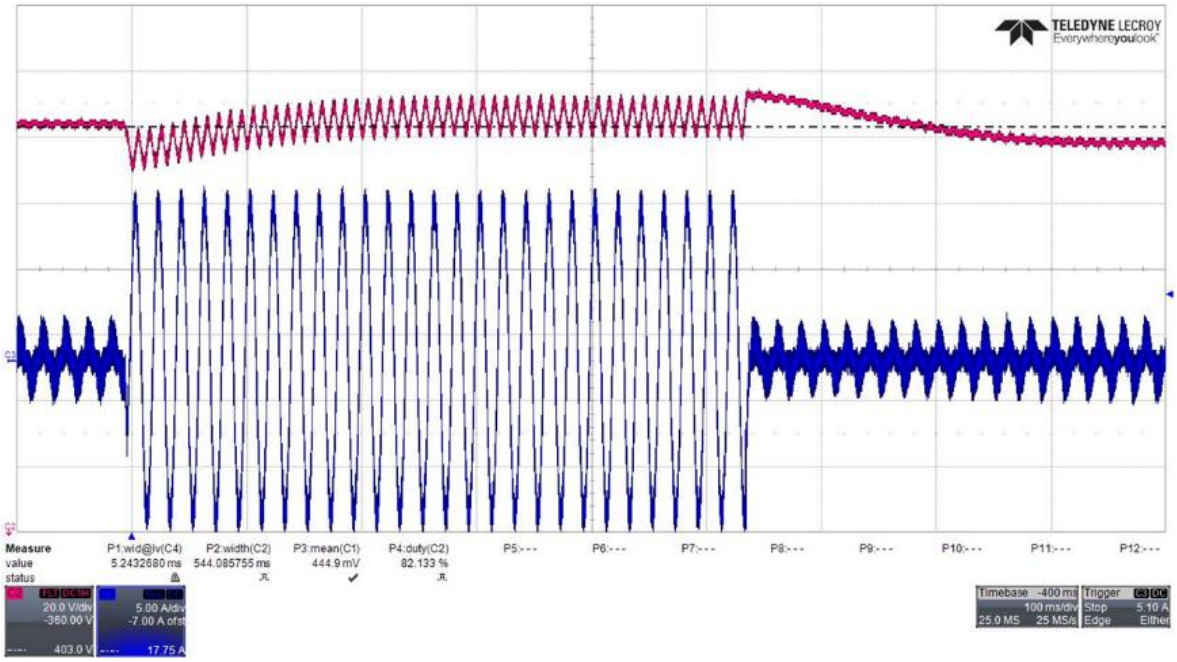

Fig. 20. Transient response, from 0.4 kW to 2 kW to 0.4 kW.

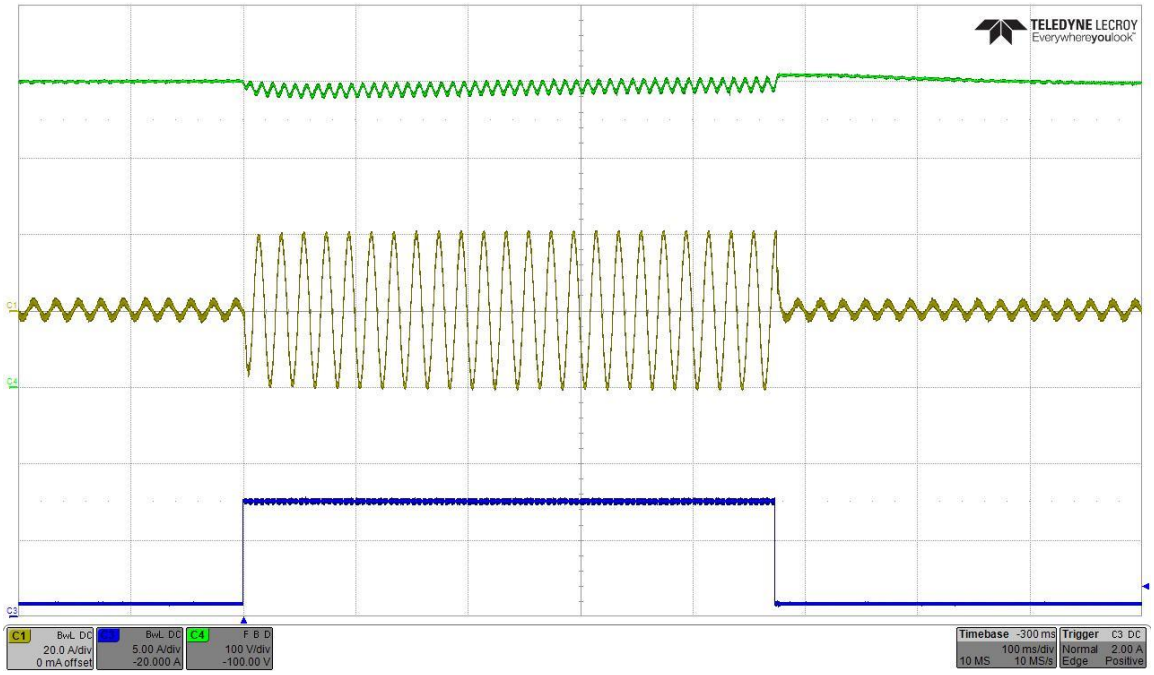

Fig. 21. A 10% to 100% load transition with 230-Vac input; load current (blue), input current (yellow) and bus voltage (green) are shown.

The line voltage and current measurements are shown in the next two figures for the case where input is 115 Vac and a 1.5-kW load is applied (Fig. 22) and where input is 230 Vac and the nominal rated power is drawn (Fig. 23). An almost unity power factor is achieved in both cases. The current is almost perfectly in phase with the line voltage and has a very low harmonic distortion both at low input voltage and high input voltage.

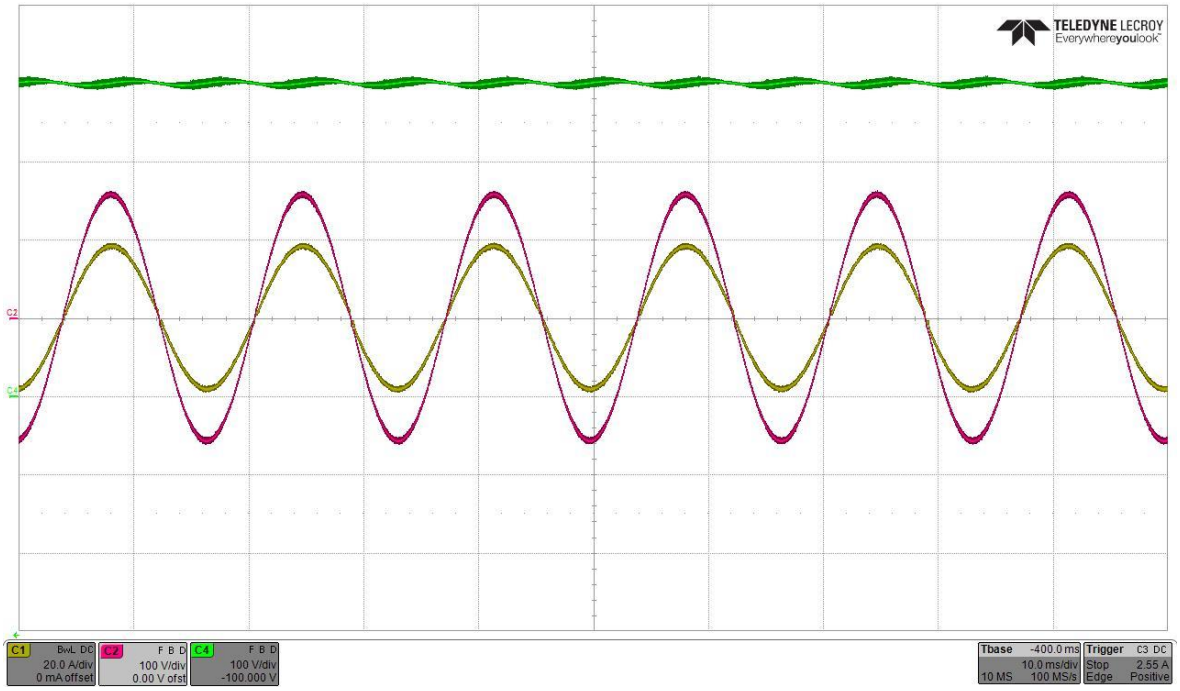

Fig. 22. PFC input voltage and current at 1.5 kW with 115-Vac input.

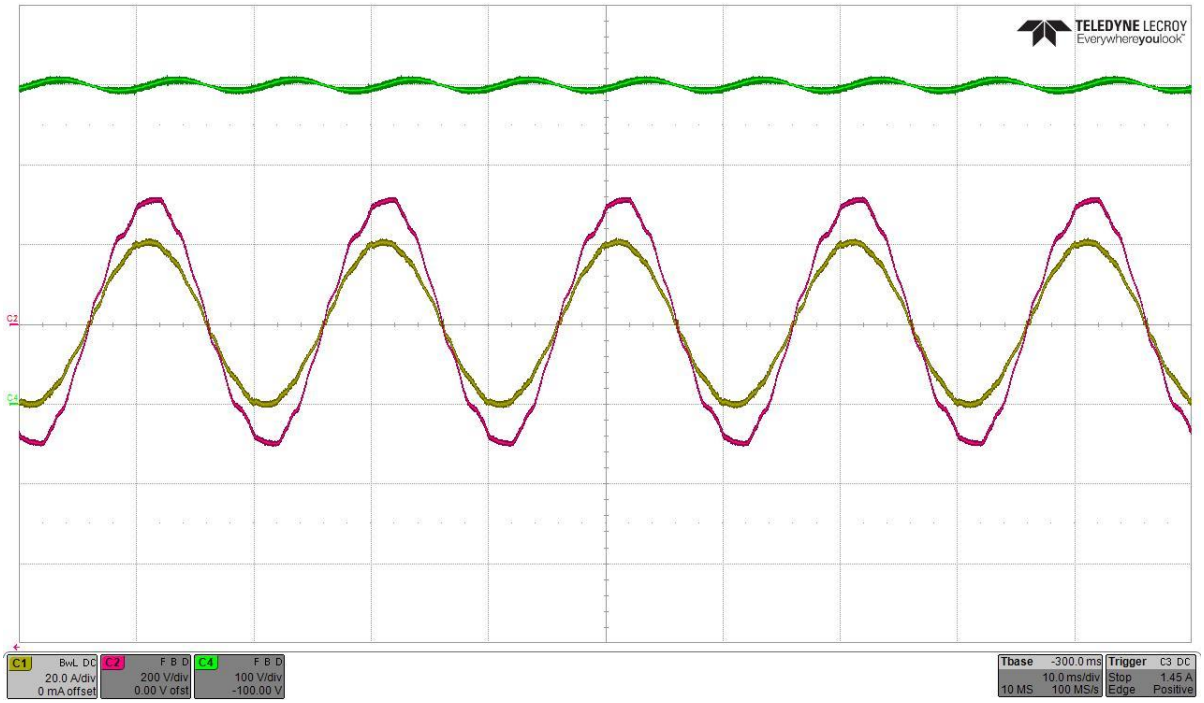

Fig. 23. PFC input voltage and current at 3 kW with 230-Vac input.

Note that in Fig. 23 the input ac voltage includes some harmonic distortions. Even so, given the fast dynamic response of the proposed control scheme, the line current follows the reference current without distortion and delay. In both of the cases illustrated in Figs. 22 and 23 the zero crossing distortion is minimal.

Fig. 24 shows that the current THD is well below 10% both at 115 Vac and 230 Vac even if the load is as low as 20% of the nominal value. At full power the THD is below 3% if the PFC is supplied at 115 Vac and it is equal to 3% at 230 Vac and full power. The power factor is shown in Fig. 25 as a function of the output load, with values higher than 0.99 at low power.

The measured efficiency is shown in Fig. 26. The phase shedding control strategy results in a flat efficiency curve, ideal to meet the most stringent requirement of new standards and regulations.

The precise Voltech PM6000 digital power meter was used to measure the PF and THD of the line current as well as the efficiency of the PFC. The maximum power that the converter can manage is de-rated at 115 Vac input for thermal reasons.

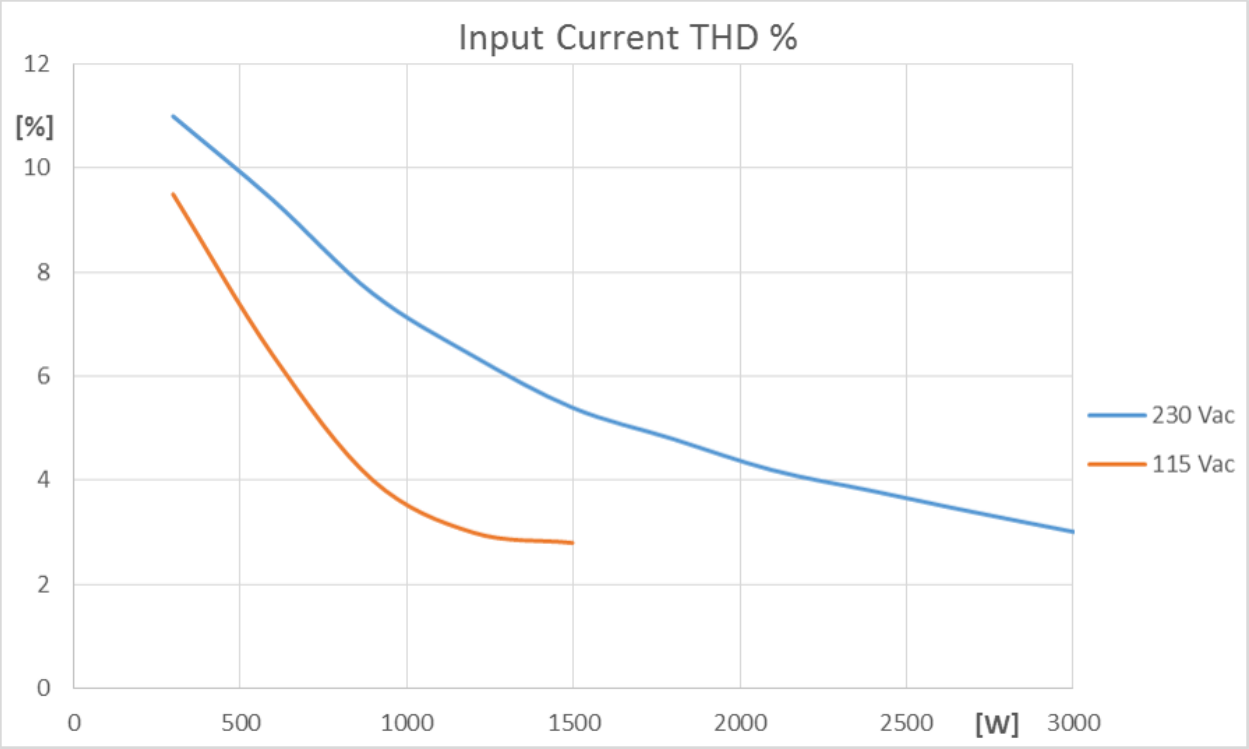

Fig. 24. Current THD% at 115 Vac (blue) and 230 Vac (purple).

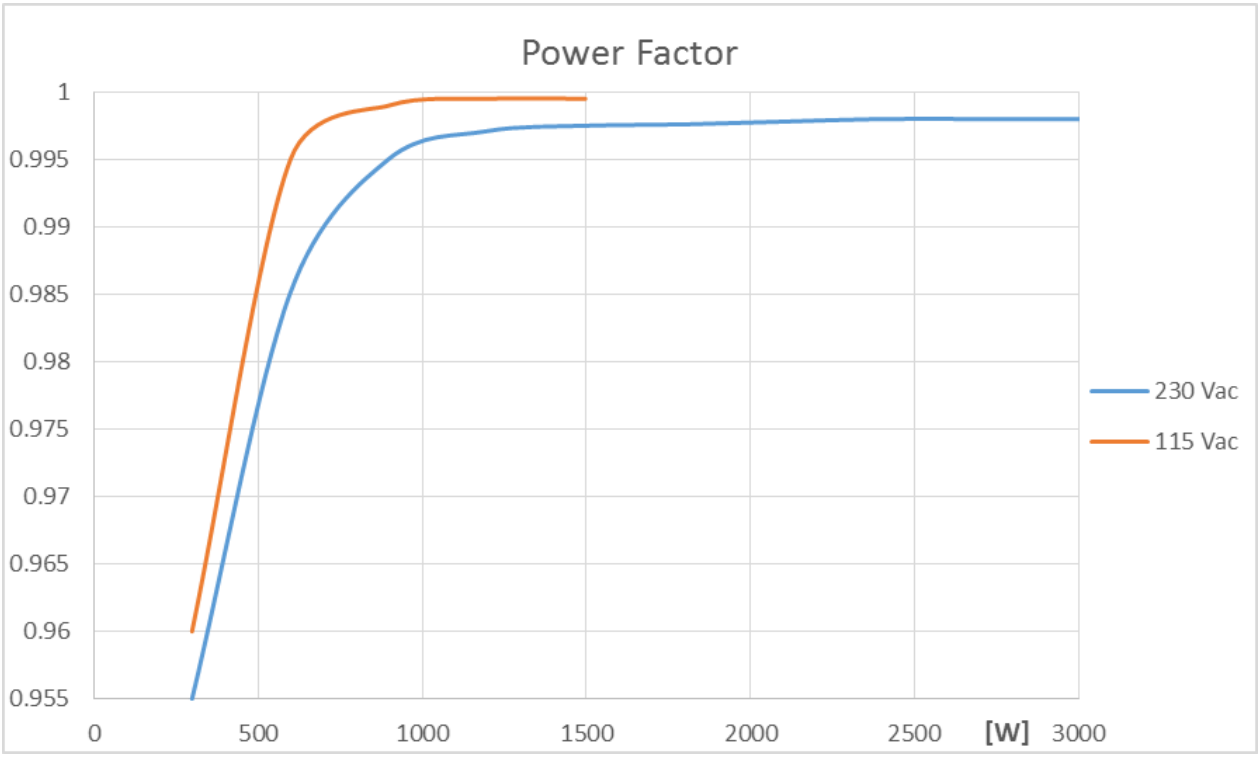

Fig. 25. Power factor vs. output PFC power (W) at 115 Vac (blue) and 230 Vac (purple).

Fig. 26. Efficiency of the 3-kW PFC.

Conclusion

A new device called the STNRGPF01, which is suitable for CCM interleaved boost PFC converters, was presented in this article. This device implements a semi-digital control scheme to combine the advantages of analog cycle-by-cycle regulation with the flexibility of a digital system.

In explaining this control scheme, the design of both the analog and the digital sections, which control the input current and output voltage regulation, respectively, were discussed and a step-by-step procedure was provided that the power supply designer can use to determine the main parameters necessary for the implementation of these control functions. This procedure is also used in a configuration software called E-design and intended to help the designer in achieving quick prototyping and configuration of the chip.

An evaluation board was realized in order to test the STNRGPF01 and verify the achievable performance of a 3-kW three-channel interleaved PFC. The test results show very good performance in terms of efficiency, PF and current THD. The measured efficiency at 230 Vac was about 99% (from 40% to full load). The achieved current THD was 3% (lower than 3% at low line, 1.5 kW) and the PF was higher than 0.99 for an output power higher than 20% of nominal.

References

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For further reading on power factor correction in power supply applications, see the How2Power Design Guide, select the Advanced Search option and select "Power Factor Correction" in the Popular Topics category.