

 <div data-bbox="491 98 539 264"> I Q R </div>	IBIS QUALITY REPORT	date	1 (9)
		16-Feb-24	

IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	vni2140j_ibis.ibs
IBIS Version:	4.0

	IBIS QUALITY REPORT	date	2 (9)
		16-Feb-24	

Contents

1. MODELING..... 3

1.1 Component description..... 3

1.2 Modeling conditions 3

1.3 Circuit for data extraction 5

2. IBISCHK6 CHECK 5

2.1 Result Check by IBISCHK6 6

3. FUNCTIONAL CHECK..... 6

3.1 Functional verification..... 7

4. EXTRA INFORMATION 9

	IBIS QUALITY REPORT	date	3 (9)
		16-Feb-24	

1. MODELING

IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

1.1 Component description

Component name	Technology	Component description
VNI2140J	VIPower	The VNI1240J device is a dual high-side smart power solid state relay

1.2 Modelling conditions

Simulator used	AMS 2012.1_1 (Mentor Graphics)
----------------	--------------------------------

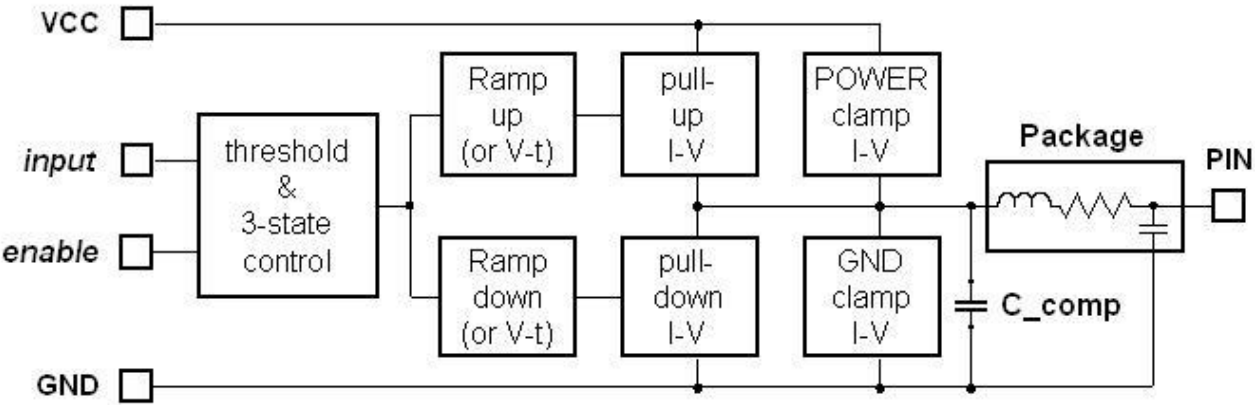


Figure 1: IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	85
Voltage Supply [Volt]	3.3	3.0	3.6
Process setting	nom	weak	strong

	IBIS QUALITY REPORT	date	4 (9)
		16-Feb-24	

Model names (of Component)	Model Type	C_comp (typ, min, max)
mod_input	Input	8.056pF (typ), 7.690pF(min) , 8.820pF(max)
mod_diag	Open-Drain	8.056pF (typ), 7.690pF(min) , 8.820pF(max)
mod_output	Open-Source	125.5pF (typ), 123.6pF(min), 128.4pF(max)

Model names (of Component)	Threshold and Vmeas	Timing parameters (if used)
mod_input	Vil=0.800V , Vih=2.200V	
mod_output	Vmeas=12.00V	Cref=50.0pF Rref=100

Package	Description
PowerSSO-12	12 pins Power package

	IBIS QUALITY REPORT	date	5 (9)
		16-Feb-24	

1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modelling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.

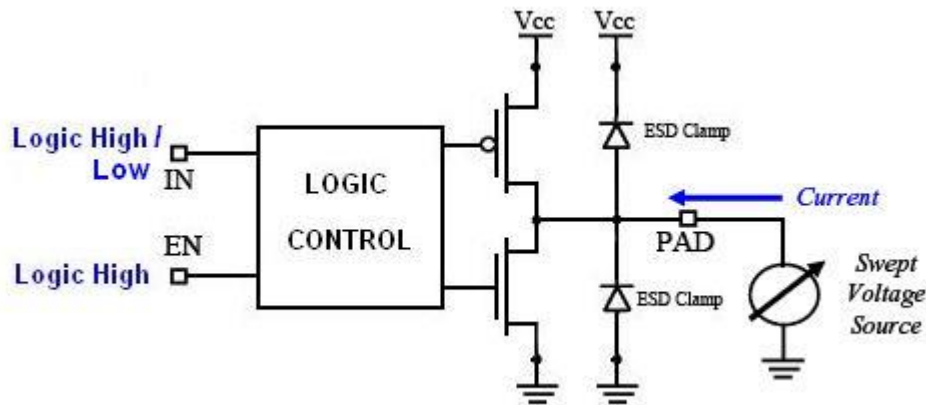


Figure 2: Simulation Setup to extract **I/V** data from I/O model type

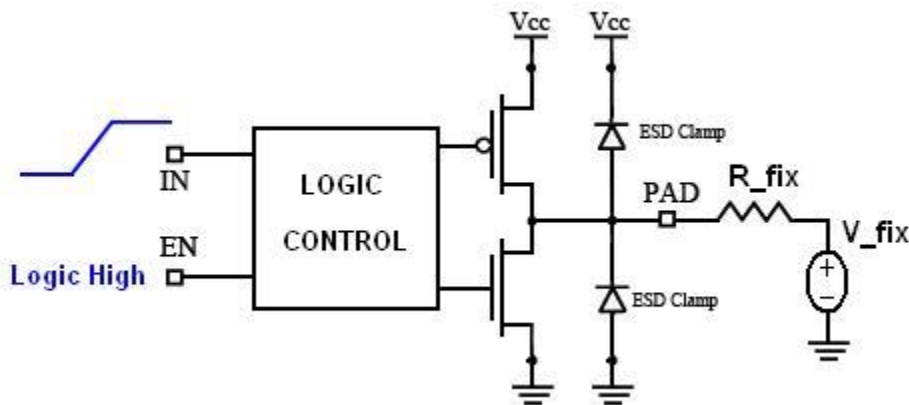


Figure 3: Simulation Setup to extract **V/T** data from I/O model type (see also Table 1)

V/T data condition extractions	Load conditions
Rising waveform	R_fix=50 Ohm, V_fix= 0 V
Rising waveform	R_fix=10KOhm, V_fix= 24.0 V
Falling waveform	R_fix=10KOhm, V_fix= 24.0 V
Falling waveform	R_fix=50 Ohm, V_fix= 0 V

Table 1: V/T curve extraction load conditions

2. IBISCHK6 CHECK

The created IBIS model must be checked using IBISCHK6 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

	IBIS QUALITY REPORT	date	6 (9)
		16-Feb-24	

2.1 Result Check by IBISCHK6

IBISCHK6 V6.0.1

Checking vni1240j_ibis.ibs for IBIS 4.2 Compatibility...

NOTE (line 212) - Pulldown Minimum data is non-monotonic

NOTE (line 217) - Pulldown Typical data is non-monotonic

NOTE (line 221) - Pulldown Maximum data is non-monotonic

NOTE - Combined Pulldown for Model: mod_diag Typical data is non-monotonic based on piece-wise linear interpolation

NOTE - Combined Pulldown for Model: mod_diag Minimum data is non-monotonic based on piece-wise linear interpolation

NOTE - Combined Pulldown for Model: mod_diag Maximum data is non-monotonic based on piece-wise linear interpolation

Errors : 0

File Passed

Adding comments about the Warning or Note:

The output check contains some Notes about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.

3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions (Figure 4), must match. These output comparisons are presented in TYP, MIN and MAX condition. This section cannot be defined for Input and Terminator model type, because they are input-only model types.

	IBIS QUALITY REPORT	date	7 (9)
		16-Feb-24	

How well results are matched?	Put "X" into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshoot and/or Undershoot regions.	
Curves match well.	X

3.1 Functional verification

Circuit used for output comparison results is illustrated in figure 4.

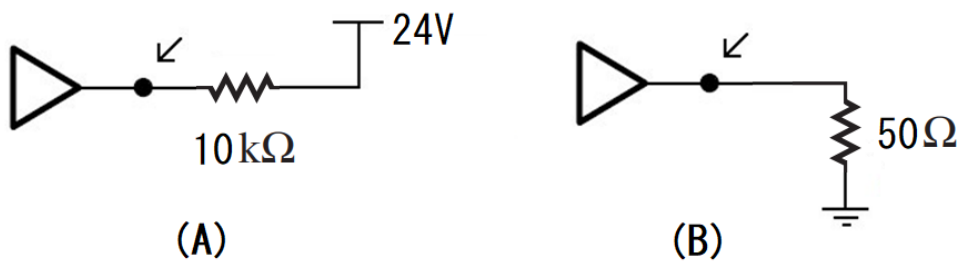


Figure 4: Circuits used for functional check: mod_diag (A), mod_output (B)

	IBIS QUALITY REPORT	date	8 (9)
		16-Feb-24	

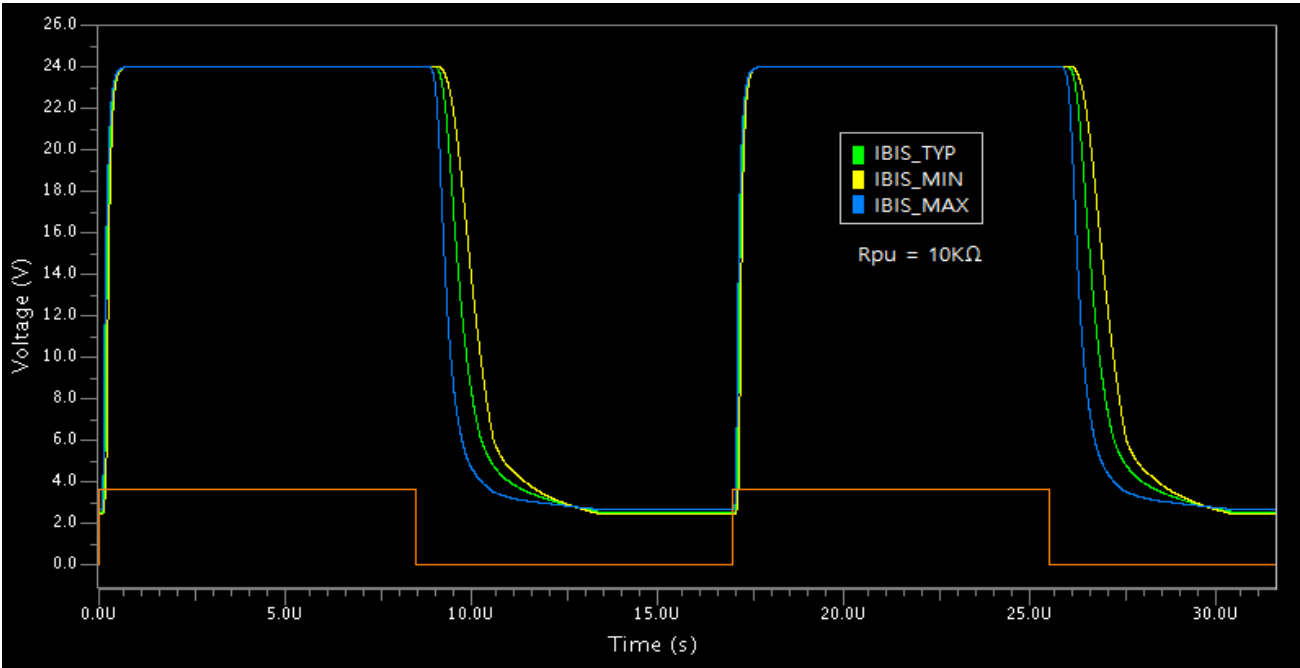


Figure 5: IBIS simulation results of "mod_diag" Model

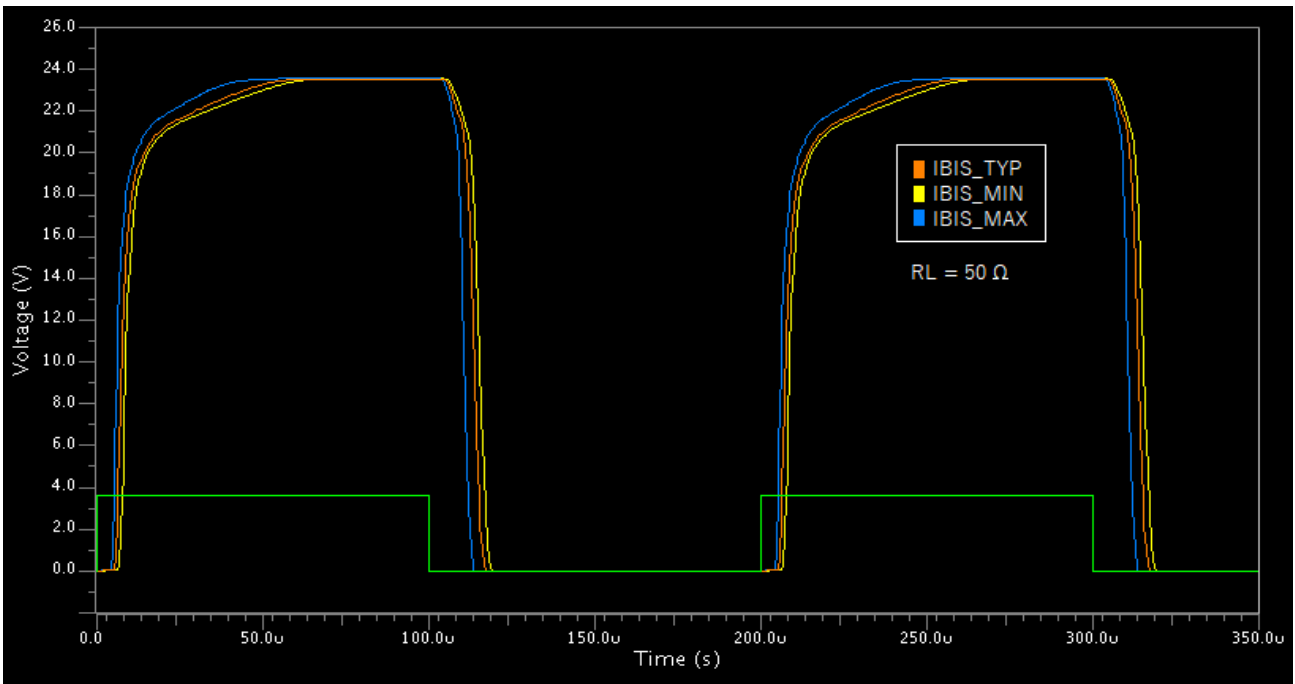


Figure 6: IBIS simulation results of "mod_output" Model

Output Comparisons:

Adding comments about the comparison:

	IBIS QUALITY REPORT	date	9 (9)
		16-Feb-24	

4. EXTRA INFORMATION

This section can contain other extra information, to explain some other features of peculiar IBIS model.

Other specifications	description