

 <div data-bbox="488 98 536 264"> I Q R </div>	IBIS QUALITY REPORT	date	1 (8)
		13-Mar-25	

IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	m95m01_a125_3v3_tssop08.ibs
IBIS Version:	4.0



	IBIS QUALITY REPORT	date	2 (8)
		13-Mar-25	

Contents

1. MODELING..... 3

1.1 Component description..... 3

1.2 Modeling conditions 3

1.3 Circuit for data extraction 5

2. IBISCHK6 CHECK 6

2.1 Result Check by IBISCHK6 6

3. FUNCTIONAL CHECK..... 7

3.1 Functional verification..... 7

4. EXTRA INFORMATION 8

	IBIS QUALITY REPORT	date	3 (8)
		13-Mar-25	

1. MODELING

IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

1.1 Component description

Component name	Technology	Component description
M95M01-A125	CMOS	The M95M01A125 is a 1-Mbit serial SPI bus EEPROM memory with high-speed clock. This IBIS model is in TSSOP8 package.

1.2 Modeling conditions

Simulator used	AMS 2015.4 (Mentor Graphics)
----------------	------------------------------

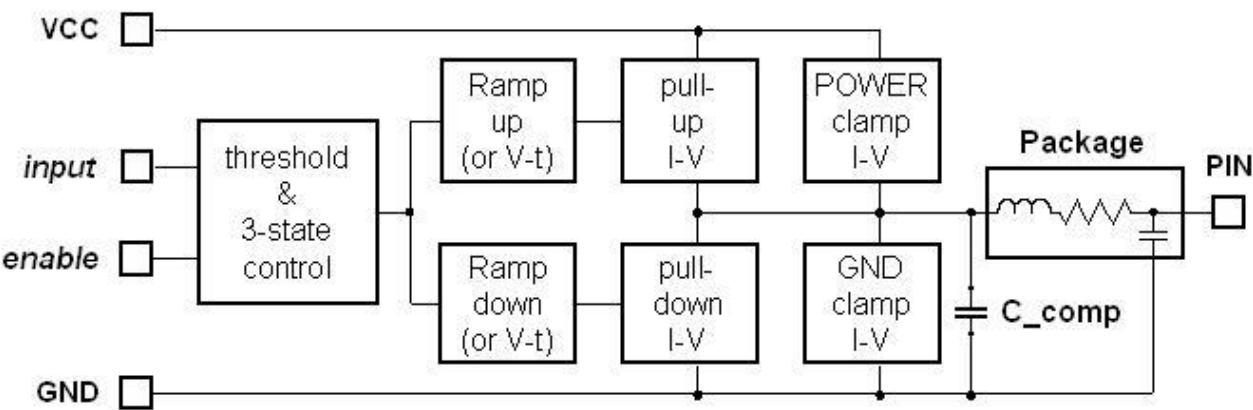


Figure 1: IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	125
Voltage Supply [Volt]	3.3	3.0	3.6
Process setting	nom	weak	strong

	IBIS QUALITY REPORT	date	4 (8)
		13-Mar-25	

Model names (of Component)	Model Type	C_comp (typ, min, max)
mod_s	Input	3.207pF (typ), 2.940pF(min) , 3.586pF(max)
mod_q	I/O	3.856pF (typ), 3.517pF (min) , 4.038pF(max)
mod_w	Input	3.207pF (typ), 2.940pF(min) , 3.586pF(max)
mod_c	Input	3.207pF (typ), 2.940pF(min) , 3.586pF(max)
mod_h	Input	3.207pF (typ), 2.940pF(min) , 3.586pF(max)

Model names (of Component)	Threshold and Vmeas	Timing parameters (if used)
mod_s/w/h	Vil=0.990V , Vih=2.310V	
mod_q	Vmeas=1.650V	Cref=30pF

Package	Description
TSSOP8	8 pin thin shrink small outline

	IBIS QUALITY REPORT	date	5 (8)
		13-Mar-25	

1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.

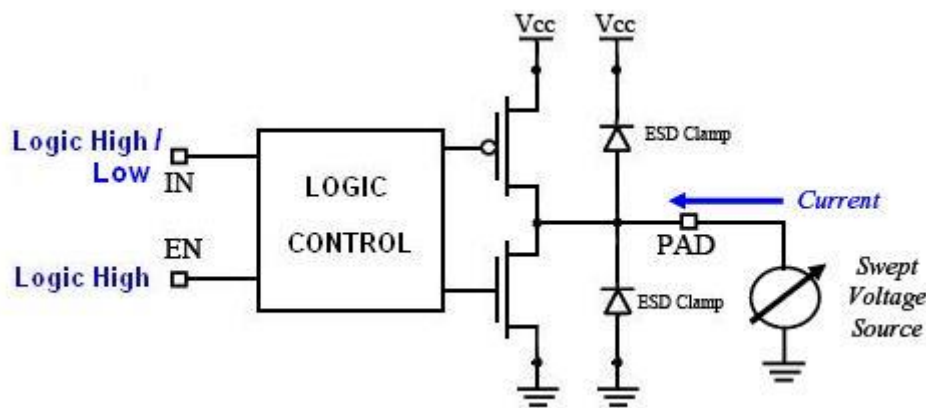


Figure 2: Simulation Setup to extract **I/V** data from I/O model type

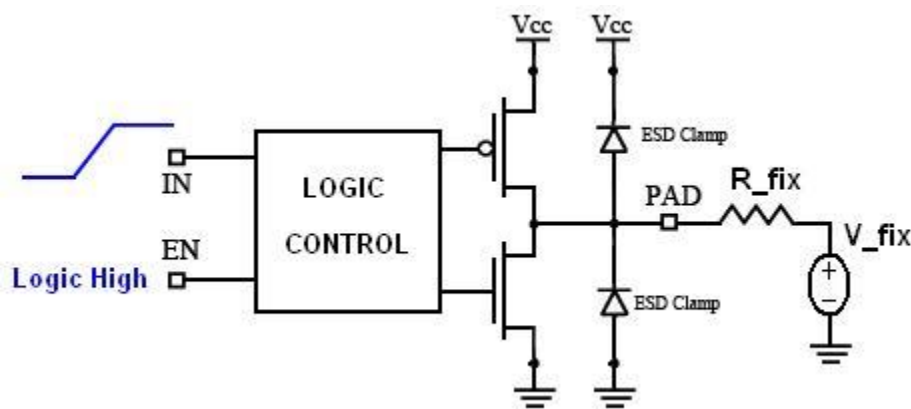


Figure 3: Simulation Setup to extract **V/T** data from I/O model type
(see also Table 1)

V/T data condition extractions	Load conditions
Rising waveform	R_fix=50 Ohm, V_fix= 0 V
Rising waveform	R_fix=50 Ohm, V_fix= 3.3 V
Falling waveform	R_fix=50 Ohm, V_fix= 3.3 V
Falling waveform	R_fix=50 Ohm, V_fix= 0 V

Table 1: V/T curve extraction load conditions

	IBIS QUALITY REPORT	date	6 (8)
		13-Mar-25	

2. IBISCHK6 CHECK

The created IBIS model must be checked using IBISCHK6 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

2.1 Result Check by IBISCHK6

IBISCHK6 V6.0.1

Checking m95m01e-a125_3v3_tssop08.ibs for IBIS 4.2 Compatibility...

NOTE (line 477) - Pulldown Maximum data is non-monotonic

NOTE (line 479) - Pulldown Typical data is non-monotonic

NOTE (line 479) - Pulldown Minimum data is non-monotonic

Errors : 0

File Passed

Adding comments about the Warning or Note:
The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.

	IBIS QUALITY REPORT	date	7 (8)
		13-Mar-25	

3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions (Figure 4), must match. These output comparisons are presented in TYP, MIN and MAX condition. This section cannot be defined for Input and Terminator model type, because they are input-only model types.

How well results are matched?	Put “X” into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshoot and/or Undershoot regions.	
Curves match well.	X

3.1 Functional verification

Circuit used for output comparison results is illustrated in figure 4.

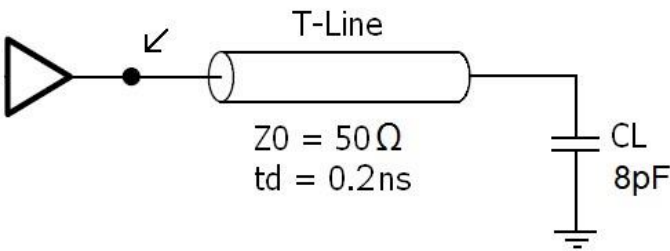


Figure 4: Circuit used for functional check

	IBIS QUALITY REPORT	date	8 (8)
		13-Mar-25	

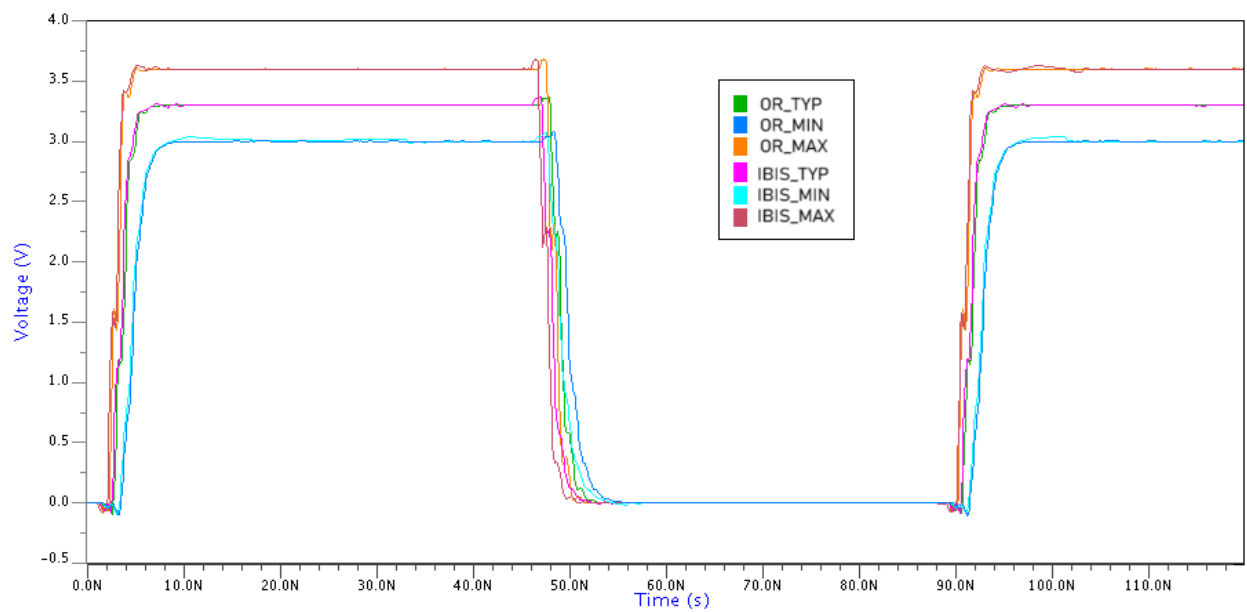


Figure 5: IBIS vs Eldo comparison results of “mod_q” Model

Output Comparisons:

Adding comments about the comparison:

4. EXTRA INFORMATION

This section can contain other extra information, to explain some other features of peculiar IBIS model

Other specifications	description