

STM32MP15XXAB_1DDR3Lx16

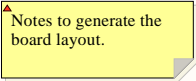
Schematics not complete, only for layout example

Table of contents

- Sheet 1: Project (this page)
- Sheet 2: Top
- Sheet 3: STM32 MPU I/Os
- Sheet 4: Power MPU
- Sheet 5: Power PMIC
- Sheet 6: eMMC
- Sheet 7: 1DDR3L_16bits

Legend

- General comment such as function title, configuration, ...
- Text to be added to silkscreen.
- Warning text.



Open Platform License Agreement

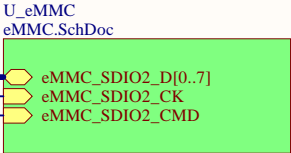
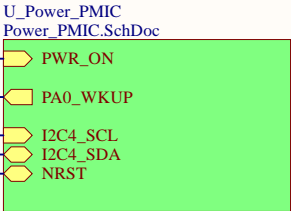
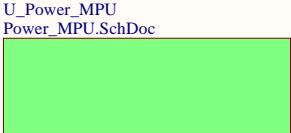
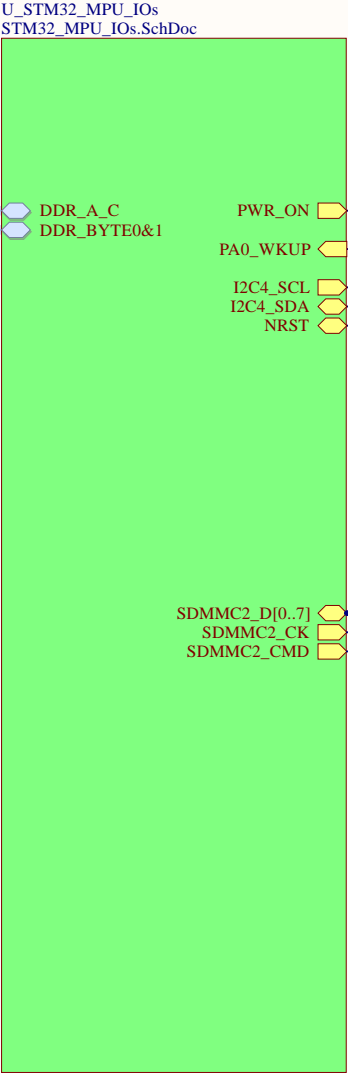
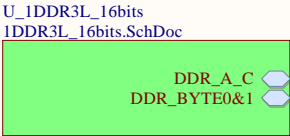
The Open Platform License Agreement (“Agreement”) is a binding legal contract between you (“You”) and STMicroelectronics International N.V. (“ST”), a company incorporated under the laws of the Netherlands acting for the purpose of this Agreement through its Swiss branch 39, Chemin du Champ des Filles, 1228 Plan-les-Ouates, Geneva, Switzerland.

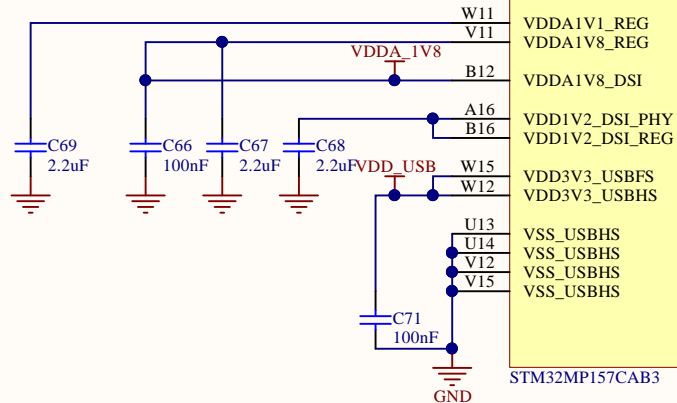
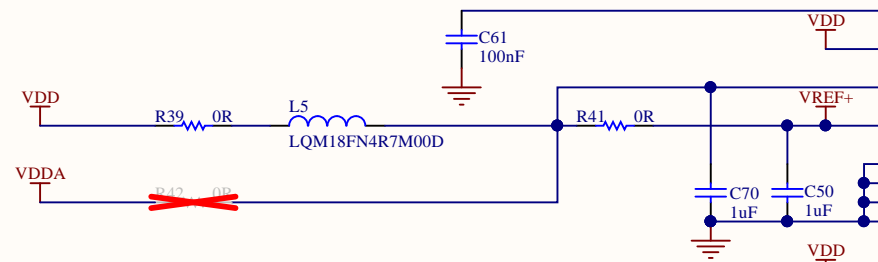
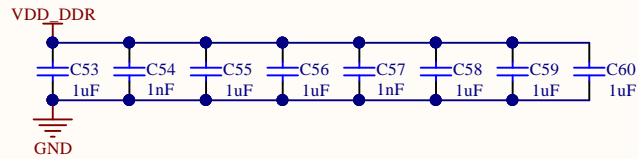
By using the enclosed reference designs, schematics, PC board layouts, and documentation, in hardcopy or CAD tool file format (collectively, the “Reference Material”), You are agreeing to be bound by the terms and conditions of this Agreement. Do not use the Reference Material until You have read and agreed to this Agreement terms and conditions. The use of the Reference Material automatically implies the acceptance of the Agreement terms and conditions.

The complete Open Platform License Agreement can be found on www.st.com/opla.

U_STM32MP15XXAB_1DDR3Lx16-Top
STM32MP15XXAB_1DDR3Lx16-Top.SchDoc







VDD_CORE	UID		
E7	VDDCORE	VSS	A1
E9	VDDCORE	VSS	A19
E11	VDDCORE	VSS	B2
E13	VDDCORE	VSS	B6
F4	VDDCORE	VSS	C3
F6	VDDCORE	VSS	C17
F8	VDDCORE	VSS	D1
F10	VDDCORE	VSS	D4
F12	VDDCORE	VSS	D5
G5	VDDCORE	VSS	D8
G7	VDDCORE	VSS	E2
G9	VDDCORE	VSS	E4
G11	VDDCORE	VSS	E5
H4	VDDCORE	VSS	E6
H6	VDDCORE	VSS	E8
H8	VDDCORE	VSS	E10
H10	VDDCORE	VSS	E12
H12	VDDCORE	VSS	E14
J7	VDDCORE	VSS	E16
J9	VDDCORE	VSS	F5
J11	VDDCORE	VSS	F7
J13	VDDCORE	VSS	F9
K8	VDDCORE	VSS	F11
K10	VDDCORE	VSS	F15
K12	VDDCORE		
L9	VDDCORE	VSS	G2
L11	VDDCORE	VSS	G4
L13	VDDCORE	VSS	G6
M10	VDDCORE	VSS	G8
M12	VDDCORE	VSS	G10
N11	VDDCORE	VSS	G12
N13	VDDCORE	VSS	G14
P12	VDDCORE	VSS	H5
R13	VDDCORE	VSS	H7
	VDD	VSS	H9
K6	VDD	VSS	H11
L5	VDD	VSS	H13
L7	VDD	VSS	H15
M6	VDD		
M8	VDD	VSS	J3
N5	VDD	VSS	J6
N7	VDD	VSS	J8
N9	VDD	VSS	J10
P6	VDD	VSS	J12
P8	VDD	VSS	J14
P10	VDD	VSS	K2
R9	VDD	VSS	K5
R11	VDD	VSS	K7
	VDD	VSS	K9
E15	VDDQ_DDR	VSS	K11
F14	VDDQ_DDR	VSS	K13
G15	VDDQ_DDR	VSS	K15
H14	VDDQ_DDR		
J15	VDDQ_DDR	VSS	L6
K14	VDDQ_DDR	VSS	L8
L15	VDDQ_DDR	VSS	L10
M14	VDDQ_DDR	VSS	L12
N15	VDDQ_DDR	VSS	L14
P14	VDDQ_DDR	VSS	M5
R15	VDDQ_DDR	VSS	M7
	VDDQ_DDR	VSS	M9
H3	VBAT	VSS	M11
R7	VDD	VSS	M13
	VDD	VSS	M15
M4	VDDA	VSS	N6
N3	VREF+	VSS	N8
		VSS	N10
		VSS	N12
M3	VREF-	VSS	N14
N4	VSSA	VSS	P7
P5	VSSA	VSS	P9
R5	VSSA	VSS	P11
	VSSA	VSS	P13
		VSS	P15
L3	VDD_ANA		
J5	VDD_PLL	VSS	R2
G13	VDD_PLL2	VSS	R6
		VSS	R8
A12	VDD_DSI	VSS	R10
		VSS	R12
W11	VDDA1V1_REG	VSS	R14
V11	VDDA1V8_REG	VSS	R16
		VSS	T4
B12	VDDA1V8_DSI	VSS	U3
		VSS	U6
A16	VDD1V2_DSI_PHY	VSS	U8
B16	VDD1V2_DSI_REG	VSS	U17
		VSS	W1
W15	VDD3V3_USBF5	VSS	W19
W12	VDD3V3_USBH5		
		VSS_ANA	L4
U13	VSS_USBH5	VSS_DSI	C12
U14	VSS_USBH5	VSS_DSI	C13
V12	VSS_USBH5	VSS_DSI	C14
V15	VSS_USBH5	VSS_DSI	C15
		VSS_DSI	C16
		VSS_DSI	J4
		VSS_PLL	F13
		VSS_PLL2	

