ST60A3H1

Errata sheet

ST60A3H1 device errata

Applicability

This document applies to the ST60A3H1 device.

It gives a summary and a description of the device errata, with respect to the device datasheet.

Deviation of the real device behavior from the intended device behavior is considered to be a device limitation.

1 Summary of device errata

Table 1 gives a reference to the ST60A3H1 device limitations and their status:

- A = workaround available
- N = no workaround available
- P = partial workaround available

The applicability of a workaround may depend on specific conditions of the target application. The adoption of a workaround may cause restrictions to target application. Workaround for a limitation is deemed partial if it only reduces the rate of occurrence and/or consequences of the limitation, or if it is fully effective for only a subset of instances on the device or in only a subset of operating modes, of the feature concerned.

Table 1. Summary of device limitations

Feature	Section	Description	Status
eUSB2 tunneling	2.1.1	State L1 not supported in HS mode	A
	2.1.2	Maximum delay reduced to revert from L2 suspend	N
	2.1.3	Old legacy hub 1.1 not supported	N
	2.1.4	Minimum inter-packet delay increased in HS	N
	2.1.5	Desynchronization during a bus reset	N
	2.1.6	Truncated first SYNC bit may cause some USB2 devices to malfunction	A
USB2 compliance tests	2.2.1	Truncated first SYNC bit of a repeated HS packet	N
	2.2.2	EOP length failing	N
	2.2.3	Added crossings on the eye diagram	N
	2.2.4	Shortened L2 suspend time	N
UART tunneling	2.3.1	Full-duplex UART tunneling data rate limitation in LP mode	P
GPIO tunneling	2.4.1	GPIO polarity not reported immediately after entering single direction GPIO tunneling	A
	2.4.2	GPIO polarity not reported immediately after entering bidirectional GPIO tunneling	A
I^2C tunneling	2.5.1	Timing constraints with propagation delay	N
	2.5.2	Lack of debounce filtering	P

2 Description of device errata

The following sections describe the errata of the applicable device and provide workarounds if available. They are grouped by device feature.

2.1 eUSB2 tunneling

2.1.1 State L1 not supported in HS mode

Description

Link power management state L1 is not supported by the ST60A3H1 device for configurations 4_LH and 4_RH when in HS mode.

Workaround

L1 feature must be disabled in the Host.

2.1.2 Maximum delay reduced to revert from L2 suspend

Description

With a USB2 HS device, a maximum delay of two low-speed bit time (1333 ns) is allowed by the USB v2.0 standard to revert from L2 suspend to HS. The ST60A3H1 only allows 970 ns to the USB device from the end of resume to the restoring of HS termination, so if it occurs later, a new enumeration can happen instead of a proper exit from L2 suspend.

Workaround

None.

2.1.3 Old legacy hub 1.1 not supported

Description

Old legacy hub 1.1 (FS hub) are not supported, hub 1.2 and further are supported. More precisely, the ST60A3H1 does not support being connected to a hub 1.1 that drives an LS USB device. Indeed, this FS communication contains LS packets after an FS preamble that is not decoded by the ST60A3H1. See section *Low-speed transactions* in the USB v2.0 standard.

Workaround

None.

2.1.4 Minimum inter-packet delay increased in HS

Description

The USB v2.0 standard defines the minimum inter-packet delay in HS to 8 bits. This is the delay that a USB2 device takes before starting to respond to a previous USB2 Host controller request. Due to the RF transfer, the minimum inter-packet delay is increased to 27 up to 43 bits depending on ST60A3H1 internal settings

Workaround

None.

2.1.5 Desynchronization during a bus reset

Description

In hybrid repeater configurations with eHCI Host controller, the two ST60A3H1 devices can be desynchronized during a bus reset (resulting in lost SOF or data packets). This is a small limitation since the system decided to generate a bus reset anyway.

Workaround

None.

2.1.6 Truncated first SYNC bit may cause some USB2 devices to malfunction

Description

Unlike the USB2 standard, the eUSB2 protocol introduces the possibility to have a truncated first SYNC bit with a duration smaller than 1 complete bit. Current eUSB2 / USB2 repeaters do not filter out these truncated first SYNC bits and propagate them to the USB2 device. Some HS USB2 devices may not function when connected to an eUSB2 / USB2 repeater because of this partial first SYNC bit. This behavior is unrelated to the ST60A3H1.

Workaround

In such cases, it is possible to solve the issue by inserting a USB2 hub between the repeater and the device.

2.2 USB2 compliance tests

USB2 compliance tests are described in the eUSB2 v1.1 specification. They can be executed by using either the XHSETT or HSETT software tool depending on the Host controller (xHCI/eHCI).

The following tests are known to deviate from USB2 compliance, but should not cause significant interoperability issues. However, a USB2 system that includes the ST60A3H1 must address these limitations if a USB2 certification is required.

2.2.1 Truncated first SYNC bit of a repeated HS packet

Description

The first SYNC bit of a repeated HS packet may be truncated. However, this does not have any impact on functionality since the receiver always sees more than 12 full-UI SYNC bits. Characterization has revealed that depending on the first SYNC bit polarity, the ST60A3H1 pair may remove either 6 or 7 SYNC bits that is acceptable for a eUSB2 hybrid repeater as defined in the *Appendix B* of the eUSB2 v1.1 specification.

Workaround

None.

2.2.2 EOP length failing

Description

- The compliance tools for most oscilloscopes expect a bit aligned EOP length whereas, for the ST60A3H1 devices + USB repeaters chain, this length cannot be guaranteed to be an exact multiple of a bit duration. However, the EOP length is always less than the specified dribble limit.
- Another EOP length failing is that the compliance software assumes that the test point is at the Host/Device connector, whereas we check the compliance of Host/ST60A3H1 devices + USB repeaters/Device chain.
- As an eUSB2 hybrid repeater is allowed to add EOP dribble up to 8 random (SE0 or K or J) bit durations when repeating packets (as indicated in *Appendix B* of the eUSB2 v1.1 specification), this USB2 compliance test failure is expected and acceptable.

Workaround

None.

2.2.3 Added crossings on the eye diagram

Description

Since there are truncated SYNC bits and non-bit aligned EOP dribble, the eye can reveal some crossings for the test packet. However, it is verified that these crossings are always at the start and end of the packet. They are therefore considered as having no functional impact.

Workaround

None.

2.2.4 Shortened L2 suspend time

Description

In eUSB2 dual repeater configuration 4_LH or 4_RH, there is a need to waiver the L2 suspend time (EL_38) from the specified range (3.0 ms to 3.125 ms). The measured duration is ~2.7 ms, but this does not have any functional impact as tested in interoperability tests with multiple Host/Devices.

Workaround

None.

2.3 UART tunneling

2.3.1 Full-duplex UART tunneling data rate limitation in LP mode

Description

Data rate is limited to 2.4 Mbit/s in LP mode and 115200 bit/s in ULP mode. For LP mode, the bandwidth is limited to 2.4 Mbit/s, that is, without considering the rare effect of collisions with the ST60A3H1 link-integrity checker.

Workaround

Implement in the application a transmission data error detection. If this is not achievable, then the data rate must be reduced to 1.6 Mbit/s.

2.4 GPIO tunneling

2.4.1 GPIO polarity not reported immediately after entering single direction GPIO tunneling

Description

With single direction GPIO tunneling configuration, the GPIO[0] and GPIO[1] polarity of the source ST60A3H1 may not be reported on the sink ST60A3H1 GPIOs immediately after entering tunneling. This happens if one source ST60A3H1 GPIO is at 1.

Workaround

To ensure proper initialization, the application at the source ST60A3H1 side can operate a double transition 1→0 and 0→1 on the GPIO at each entry into this tunneling configuration. This ensures that the polarities on the sink ST60A3H1 GPIO are aligned at 1.

2.4.2 GPIO polarity not reported immediately after entering bidirectional GPIO tunneling

Description

With bidirectional GPIO tunneling configuration, the GPIO[0] polarity of the source ST60A3H1 may not be reported on the sink ST60A3H1 GPIO[1] immediately after entering tunneling. Similarly, the GPIO[0] polarity of the sink ST60A3H1 may not be reported on the source ST60A3H1 GPIO[1]. This happens if the source or sink ST60A3H1 GPIO[0] is at 0.

Workaround

To ensure proper initialization, the application at the source and/or sink ST60A3H1 side can operate a double transition 0→1 and 1→0 on GPIO[0] at each entry into this tunneling configuration. This ensures that the polarities on the sink and/or source ST60A3H1 GPIO[1] are aligned at 0.

2.5 I²C tunneling

2.5.1 Timing constraints with propagation delay

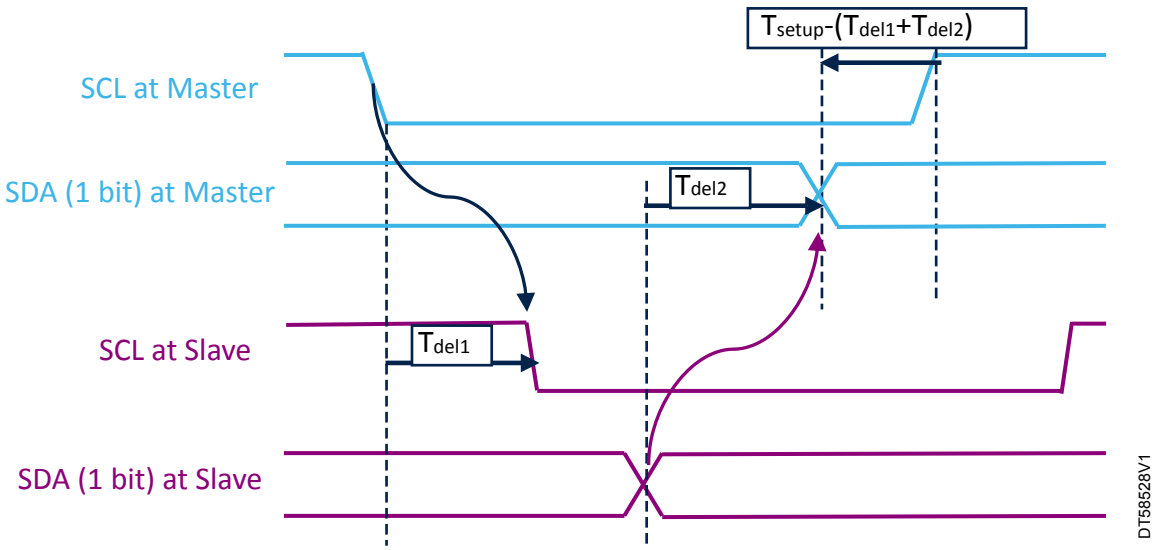
Description

A connected pair of ST60A3H1 devices inserts a propagation delay to the tunneled information. This delay has several contributors:

- Delay inserted at the interfaces, in particular on rising edges due to the weak slope in open drain (this contributor factor depends on the actual pull-up resistor value and capacitive load of the line).
- Duration of the RF encoding/decoding and the transmission of the waveform over the RF channel.
- Processing delays in digital and analog circuitry.

The effect of this delay is particularly visible on the data setup time during a read operation (see Figure 1).

Figure 1. I²C tunneling – read roundtrip



The contributions of T_{del1} and T_{del2} add up to the data setup time $t_{SU;DAT}$. The tunneling delay and roundtrip effect tighten several timing parameters of the I²C protocol. An I²C master/slave pair connected through an ST60A3H1 pair must ensure more stringent timing parameters than those required by the I²C protocol so that the entire chain remains compliant with the protocol for the selected speed rate.

Timing parameters for I²C over the ST60A3H1 are defined in Table 2. I²C tunneling timing specification, in which I/O performance and slopes refer to the ST60A3H1 outputs characteristics.

Timings are at the output of a pair of ST60A3H1 devices making the assumption that the master (or slave) is at the exact limit of I²C timing specification with the bus loaded as per specification.

A postfix "_slave" in parameters name indicates the timing for a transfer (data for a read or acknowledge) from slave to master. Others are related to the direction master to slave.

Table 2. I²C tunneling timing specification

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
T_{of}	Output fall time from VIHmin to VILmax (load conditions 4 kΩ 90 pF)	4	106.5	4	106.5	4	81.5	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	-	-	-	No filtering	-	No filtering	ns
$t_{HD;STA}$	Hold time (repeated) START condition	3.675	-	0.275	-	-0.065	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.30	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock	3.44	-	0.31	-	0.07	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	3.44	-	0.31	-	0.07	-	µs
$t_{HD;DAT}$	Data hold time	0	4.06	0	1.24	0	-	µs
$t_{HD;DAT\_slave}$	Data hold time	0	4.15	0	1.33	0	-	µs
$t_{SU;DAT}$	Data setup time	230	-	80	-	30	-	ns
$t_{SU;DAT\_slave}$	Data setup time	-450	-	-330	-	-300	-	ns
t_r	Rise time of both SDA and SCL signals (load conditions 4 kΩ 90 pF for Standard mode, 2.2 kΩ 90 pF for Fast mode, and 1 kΩ 90 pF for Fast mode+)	350	1000	170	300	72	120	ns
t_f	Fall time of both SDA and SCL signals (load conditions 4 kΩ 90 pF for Standard mode, 2.2 kΩ 90 pF for Fast mode, and 1 kΩ 90 pF for Fast mode+)	4	106.5	4	106.5	4	81.5	ns
$t_{SU;STO}$	Setup time for STOP condition	3.98	-	0.58	-	0.24	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.14	-	1.01	-	0.31	-	µs
$t_{VD;DAT\_slave}$	Data valid time	-	4.19	-	1.37	-	0.84	µs
$t_{VD;ACK\_slave}$	Data valid acknowledge time	-	4.19	-	1.37	-	0.84	µs

Timing requirements defined in this table are stronger than those from the I²C specification. This is to ensure that, despite the latency introduced by the pair of ST60A3H1 devices, the timing constraints are respected end-to-end. They represent:

- For master to slave direction, the timing that the master must comply with, so that at the slave level the timing is seen complying with the I²C specification.
- For slave to master direction, the timing that the slave must comply with, so that at the master level the timing is seen complying with the I²C specification.

Workaround

None.

2.5.2 Lack of debounce filtering

Description

The I^2C specification makes it mandatory for a receiver in fast mode or fast mode plus to be capable of suppressing noise spikes of less than 50 ns on the SDA and SCL inputs, but the ST60A3H1 GPIOs do not feature any such filtering capability.

Workaround

The application must therefore ensure that no glitches lead to erroneous sampling, in particular on the SCL line.

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
10-Mar-2025	1	Initial release.

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