ST25R3916B ST25R3917B ST25R3919B ST25R3920B

Errata sheet

ST25R3916B, ST25R3917B, ST25R3919B, and ST25R3920B device limitations

Silicon identification

This errata sheet applies to the ST25R3916B, ST25R3917B, ST25R3919B, and ST25R3920B products.

Identification by SPI or I²C

The part can be identified by reading the product revision code in the IC identity register at address 3Fh.

The limitations described in this document apply to product revision 4.0, which corresponds to an IC identity register readout of 30h.

1 Summary of silicon limitations

The following table gives a quick reference to all documented limitations.

Legend of Table 1:

- A = limitation present, workaround available
- N = limitation present, no workaround available
- P = limitation present, partial workaround available
- '-' limitation absent or fixed

Table 1. Summary of silicon limitations

Function	Silicon limitations	Workaround			
		ST25R3916B	ST25R3917B	ST25R3919B	ST25R3920B
Section 1.1: Interrupt and associated reporting limitations	Section 1.1.1: Serial peripheral interface (SPI)	A	A	A	A

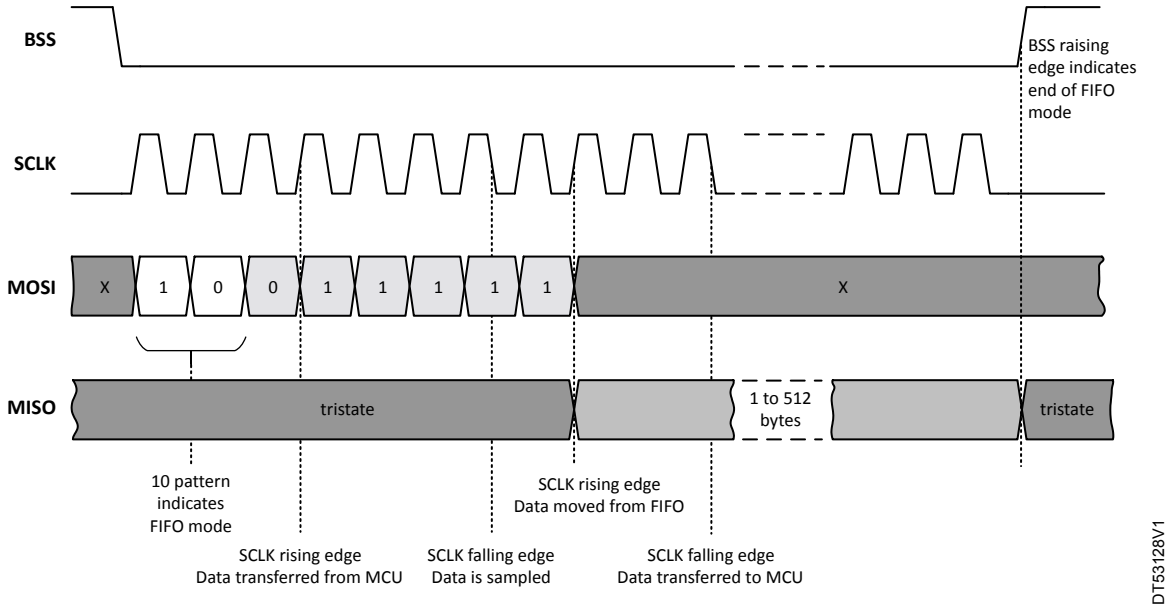
1.1 Interrupt and associated reporting limitations

1.1.1 Serial peripheral interface (SPI)

Description

During the read operation of the interrupt status register, under specific bit patterns of the MOSI line identified as X in Figure 1, the interrupt flags might not be valid, and the interrupt line stays high.

Figure 1. SPI communication: FIFO reading



Workaround

The MOSI line must be driven low after the interrupt status register address bits, as shown in Figure 2 and Figure 3, for reading single and multiple bytes.

Figure 2. SPI communication: reading a single byte

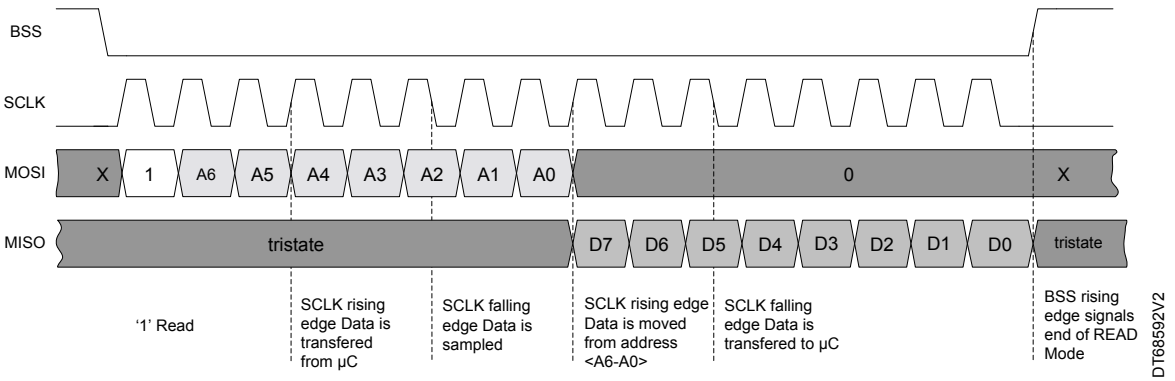
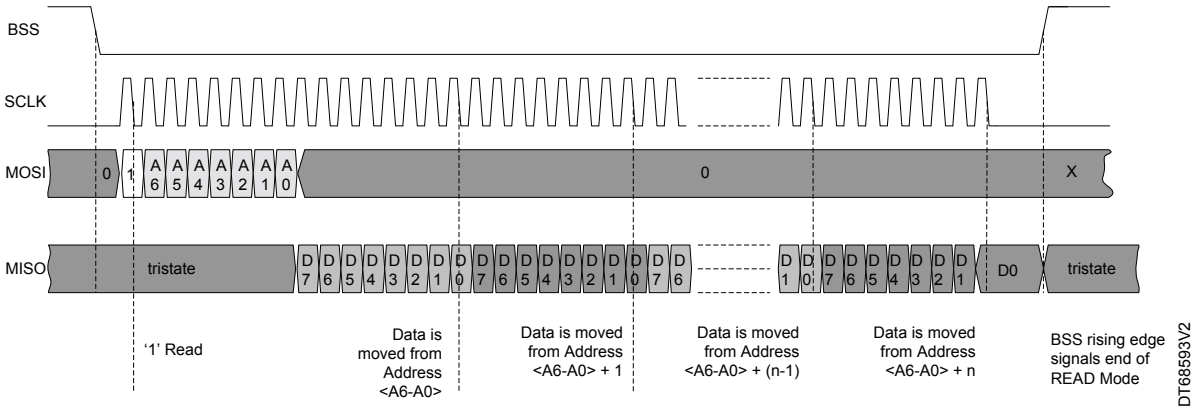


Figure 3. SPI communication: reading multiple bytes



Revision history

Table 2. **Document revision history**

Date	Revision	Changes
28-Jan-2025	1	Initial release.

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