BlueNRG-1

Errata sheet

The BlueNRG-1 device limitations

Silicon identification

This errata sheet applies to the following STMicroelectronics BlueNRG-1 devices:

Order code	Package	Identification information of the device(1)	Device cut
BlueNRG-132	VFQFPN32	0x00000111	1.1
BlueNRG-132	VFQFPN32	0x00000113	1.3
BlueNRG-132S	VFQFPN32	0x00000113	1.3
BlueNRG-134	WLCSP34	0x00000111	1.1
BlueNRG-134	WLCSP34	0x00000113	1.3

1. *Value as read from register CKGEN_SOC - DIE_ID register (0x4090001C)*

Note: For each device limitation the following information is provided:

- *Part number affected: which device and cut is affected by the limitation (the devices and cuts not reported are not affected by it)*
- *Description: limitation description*
- *Impact: limitation impact*
- *Workaround: possible workaround if any*

1 Limitations

1.1 Reduced operating voltage range when brown-out reset (BOR) is enabled

Part number affected: the BlueNRG-132 cut 1.1 and the BlueNRG-134 cut 1.1.

Description: when brown-out reset (BOR) is enabled the operating voltage of the device is reduced to 2.1-3.6 V.

Impact: brown-out reset (BOR) threshold prevents the device from being safely used below 2.1 V.

Workaround: the application using brown-out reset (BOR) must restrict operating range to 2.1 V.

1.2 Brown-out reset (BOR) is not enabled by default

Part numbers affected: the BlueNRG-132 cut 1.1 and the BlueNRG-134 cut 1.1.

Description: the device brown-out reset (BOR) is not enabled by default.

Impact: brown-out reset (BOR) activation requires a software action.

Workaround: brown-out reset (BOR) can be enabled by the software by setting the BOR_CONFIG=BOR_ON preprocessor option in STSW-BLUENRG1-DK (BlueNRG-1, BlueNRG-2 DK SW package).

Note: It is recommended to use SDK 3.0.0 (June 2018) or above for proper operations; the STSW-BLUENRG1-DK compatibility matrix is present in the latest SDK release notes.

1.3 Bit pattern could cause SWD interface not to work

Part numbers affected: the BlueNRG-132 cut 1.1 and the BlueNRG-134 cut 1.1.

Description: During debug connection via serial wire debugger (SWD) port, if a specific bit pattern is sent/ received to/from the SWDIO pin, the chip could not answer anymore subsequent SWD requests, thus breaking the connection. The bit pattern represented as 32 bit word is 0x39E6xxxx.

Impact: using serial wire debugger (SWD) during development and/or production to program the Flash memory can cause some issues if the Flash memory image contains a particular pattern.

Workaround: none.

1.4 Aux ADC end of calibration interrupt flag cannot be cleared

Part numbers affected: the BlueNRG-132 cut 1.1 and the BlueNRG-134 cut 1.1.

Description: the ADC end of calibration interrupt flag cannot be cleared, so it cannot be used. STATUS register includes end of calibration information in bit 2.

Impact: no specific issue, since the interrupt of end of calibration does not have a practical use in the real application scenario.

Workaround: since the end of calibration bit cannot be used, keep the interrupt mask bit associated disabled. There is no interest in such bit.

1.5 ADC WDOG status flag / interrupt cannot be cleared

Part numbers affected: the BlueNRG-132 cut 1.1 and the BlueNRG-134 cut 1.1.

Description: Aux ADC WDOG status flag / interrupt cannot be cleared.

Impact: Aux ADC WDOG IRQ is not usable.

Workaround: none.

1.6 ADC does not work properly when a 32 MHz system clock is being used

Part numbers affected: the BlueNRG-132 cut 1.1, cut 1.3, the BlueNRG-132S cut 1.3, and the BlueNRG-134 cut 1.1, 1.3.

Description: ADC IP does not work properly with a system clock at 32 MHz.

Impact: ADC cannot be used with a system clock at 32 MHz.

Workaround: the application, using a 32 MHz quartz and accessing ADC, should configure system clock to 16 MHz.

1.7 ADC SNR degradation

Part numbers affected: the BlueNRG-132 cut 1.1, and the BlueNRG-134 cut 1.1.

Description: ADC SNR may be randomly degraded depending on ADC clock generator start-up.

Impact: SNR degradation is in the range of 6 dB, therefore the effective number of bit of the ADC is reduced by 1 bit.

Workaround: in case of static signal, multiple acquisitions and averaging allow ADC accuracy to be recovered.

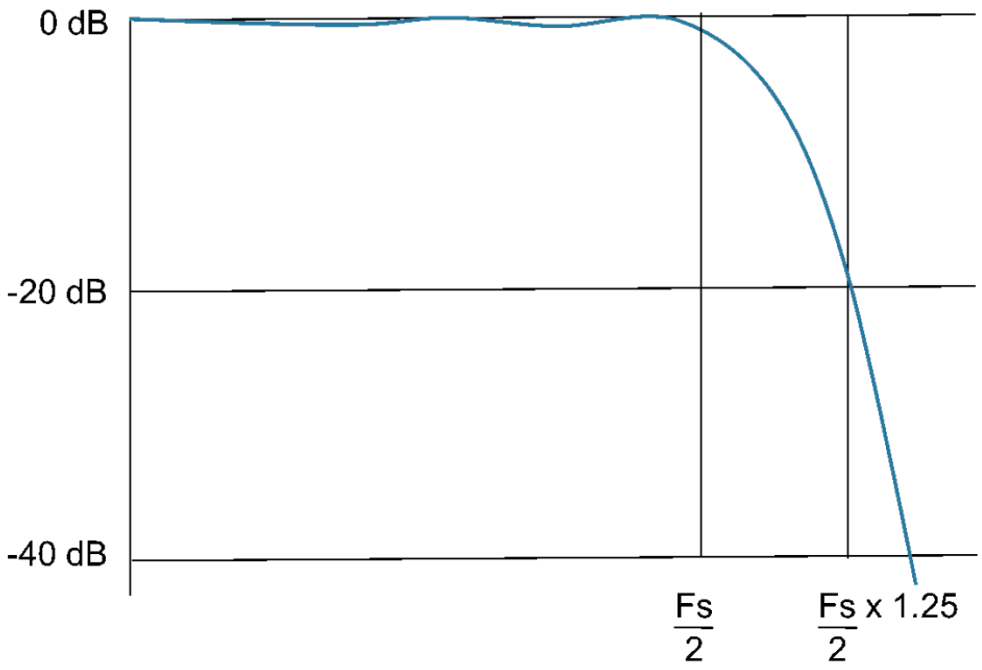
1.8 ADC unwanted aliased signal after the decimation filter

Part numbers affected: the BlueNRG-132 cut 1.1, cut 1.3, the BlueNRG-132S cut 1.3, and the BlueNRG-134 cut 1.1, 1.3.

Description: the bandwidth of the anti-aliasing filter is slightly broader with respect to the signal bandwidth, potentially thus generating unwanted aliased signal after the decimation filter.

Impact: When a pure sine wave, generated in the [Fs/2; 1.25*Fs/2] range, is being sampled, user can notice an attenuated aliased sine wave in the [0.75*Fs/2; Fs/2] range.

Figure 1. Interpolation filter frequency response



In case of waveform acquisition, especially when audio speech and music is caught, no further degradation has been identified.

F_S is the sampling frequency on the output of the downsampling filter, described as ADC data rate in the datasheet.

Workaround: by choosing an appropriate oversampling factor (OSR), so that maximum frequency of the sampled signal is lower than Fs/2, aliasing may be avoided.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
29-Jan-2019	1	Initial release.
27-Jan-2025	2	Updated Section 1.2: Brown-out reset (BOR) is not enabled by default. Added references to new BlueNRG-132S.

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