SPC564A70B4, SPC564A70L7
Errata sheet

SPC564A70x device errata JTAG_ID = 0x0AE03041

Introduction

This errata sheet describes all the functional and electrical problems known in the revision 1.0 of the SPC564A70x device identified with the JTAG_ID = 0x0AE03041.

All the topics covered in this document refer to *RM0068 rev 2* and *SPC564A70B4, SPC564A70L7 datasheet rev 1* (see *Section Appendix A: Further information*).

Device identification:

- Package device marking mask identifier : AAG
- JTAG_ID = 0x0AE03041
- MIDR register:
  - MAJOR_MASK : 0
  - MINOR_MASK : 0

This errata sheet applies to SPC564A70x device in accordance with *Table 1*.

Table 1. Device summary

Part number	Package
SPC564A70B4	PBGA324
SPC564A70L7	LQFP176

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1 Functional problems

1.1 ERR003221:PMC: SRAM standby power low voltage detect circuit is not accurate

Description:

The power management controller (PMC) SRAM standby voltage low power detect circuit cannot reliably detect the brown-out condition if the standby supply is below 1.0 volts. The Status Register Brown Out Flag (PMC.SR[LVFSTBY]) bit may not be set during a brownout condition of the SRAM standby voltage or may be set even though no data has been lost.

Workaround:

The application software should not rely on the PMC.SR[LVFSTBY] bit to detect corrupted SRAM values.

1.2 ERR003377:Pad Ring:Nexus pins may drive an unknown value immediately after power up but before the 1st clock edge

Description:

The Nexus Output pins (Message Data outputs 0:15 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance driver (when used as a general purpose input [GPI] in the application).

Workaround:

1. Do not tie the Nexus output pins directly to ground or a power supply.
2. If these pins are used as GPI, limit the current to the ability of the regulator supply to guarantee correct start up of the power supply. Each pin may draw upwards of 150mA.

If not used, the pins may be left unconnected.

1.3 ERR003378: EQADC: Pull devices on differential pins may be enabled for a short period of time during and just after POR

Description:

The programmable pull devices (up and down) on the analog differential inputs of the eQADC may randomly be enabled during the internal Power On Reset (POR) and until the 1st clock edge propagates through the device. After the first clock edge, the pull resistors will be disabled until software enables them.

Workaround:

Protect any external devices connected to the differential analog inputs. The worst case condition is with a 1.4K ohm resistor to VDDA (5K pull-up enabled) or VSSA (5K pull-down enabled). This may also cause temporary additional current requirements on the VDDA

supply of each eQADC module, up to 15 mA on each eQADC if both the pull up and pull down resistors are enabled simultaneously on all of the differential analog pins.

1.4 ERR003407:FlexCAN: CAN Transmitter Stall in case of no Remote Frame in response to Tx packet with RTR=1

Description:

FlexCAN does not transmit an expected message when the same node detects an incoming Remote Request message asking for any remote answer.

The issue happens when two specific conditions occur:

1. The Message Buffer (MB) configured for remote answer (with code "a") is the last MB. The last MB is specified by Maximum MB field in the Module Configuration Register (MCR[MAXMB]).
2. The incoming Remote Request message does not match its ID against the last MB ID.

While an incoming Remote Request message is being received, the FlexCAN also scans the transmit (Tx) MBs to select the one with the higher priority for the next bus arbitration. It is expected that by the Intermission field it ends up with a selected candidate (winner). The coincidence of conditions (1) and (2) above creates an internal corner case that cancels the Tx winner and therefore no message will be selected for transmission in the next frame. This gives the appearance that the FlexCAN transmitter is stalled or "stops transmitting".

The problem can be detectable only if the message traffic ceases and the CAN bus enters into Idle state after the described sequence of events.

There is NO ISSUE if any of the conditions below holds:

a) The incoming message matches the remote answer MB with code "a".

b) The MB configured as remote answer with code "a" is not the last one.

c) Any MB (despite of being Tx or Rx) is reconfigured (by writing its CS field) just after the Intermission field.

d) A new incoming message sent by any external node starts just after the Intermission field.

Workaround:

Do not configure the last MB as a Remote Answer (with code "a").

1.5 ERR003659:FLASH: Resuming after a suspend during an Erase may prevent the erase from completing.

Description:

If an erase suspend (including the flash put into sleep or disabled mode) is done on any block in the low Address Space (LAS) or the Mid-Address Space (MAS) except the 16KB blocks, or if a suspend is done with multiple non-adjacent blocks (including the High Address Space [HAS]), the flash state machine may not set the FLASH_MCR[DONE] bit in the flash Module Control Register. This condition only occurs if the suspend occurs during certain internal flash erase operations. The likelihood of an issue occurring is reduced by limiting the frequency of suspending the erase operation.

Workaround:

If the suspend feature (including disable and sleep modes) of the flash is used, then software should ensure that if the maximum time allowed for an erase operation occurs without a valid completion flag from the flash (FLASH_MCR[DONE] = 1), the software should abort the erase operation (by first clearing the Enable High Voltage (FLASH_MCR[EHV]) bit, then clearing the Erase read/Write bit (FLASH_MCR[ERS] bit) and the erase operation should be restarted.

Note: The cycle count of the sector is increased by this abort and restart operation.

1.6 ERR003908: Flash: May fail to exit Power On Reset (POR) properly

Description:

There is a low probability (approximately once per 200,000 POR events) that the Flash may fail to respond. This may cause the device to hang in the reset state or to enter an infinite reset loop where it repeatedly attempts to boot from the serial interface, fails, and is reset by the internal watchdog timer. However, the watchdog resets will not recover the flash from the failure state. In devices with two flash arrays where the primary array is functional but the secondary array fails, it is possible that user code in the primary array will be executed. Such code will eventually encounter a machine-check exception when it attempts to access the secondary array.

Workaround:

Internal resets are not effective to recover from this condition. An external hardware RESET or a power down/up cycle is required.

1.7 ERR004480 eQADC: Differential conversions with 4x gain may halt command processing

Description: If the four times amplifier is enabled for a differential analog-to-digital conversion in the Enhanced Queued Analog to Digital Converter (eQADC) and the ADC clock prescaler is set to divide by 12 or greater, then the ADC will stop processing commands if a conversion command is executed immediately after a differential, gain 4x conversion.

Workaround:

1. Do not use a prescaler divide factor greater than or equal to 12 (11 can be used on devices that support odd prescalers).
2. Insert a dummy write command to any internal ADC register after every 4x conversion command.

Note: If the command FIFO preemption feature is used and it is possible to preempt a FIFO which contains the 4x conversion + dummy write workaround, then the preempting command FIFO must be loaded FIRST with a dummy write command and then the desired preempting

conversion command in order to avoid the possibility of following a 4x conversion command with another conversion command in the same ADC.

The level sensitive triggers (when in Low/High Level Gated External Trigger, Single/Continuous Scan modes) can interrupt the command sequence at any point in time, potentially breaking the safe sequence 4x conversion command -> dummy write command.

When using an odd prescaler (ADCx_CLK_ODD = 1), the duty cycle setting (ADCxCLK_DTY) must be kept at the default setting of 0.

Appendix A Further information

A.1 Reference document

1. *SPC564A70B4, SPC564A70L7 32-bit MCU family built on the embedded Power Architecture®* (RM0068, Doc ID 18132)
2. *32-bit, 2 MB Flash, 128 KB SRAM MCU family built on the embedded Power Architecture®* (SPC564A70B4, SPC564A70L7 datasheet, Doc ID 18078)

A.2 Acronyms

Table 2. Acronyms

Acronym	Name
ADC	Analog-to-digital converter
APC	Analog pad control
BAM	Boot assist module
CMU	Clock monitor unit
CPU	Control processing unit
CHIERFR	Controller host interface error flag register
CTU	Cross trigger unit
DMA	Direct memory access
DPM	Decoupled parallel mode
ECSM	Error correction status module
FCCU	Fault collection and control unit
FIFO	First in first out
ILSA_EF	Illegal system bus address error flag
LSM	Lock step mode
MB	Message buffer
MCU	Microcontroller unit
PCR	Pad configuration register
POC	Protocol operation control
RCCU	Redundancy control checker unit
RWE	Read-while-write event error
RWW	Read while write
RXGMASK	RX global mask
RXIMR	RX individual mask register
SBC	Single bit correction-status
SLL	Secondary low/mid address space block lock register

Table 2. Acronyms (continued)

Acronym	Name
SWG	Sine-wave generator
XOSC	External oscilator

Revision history

Table 3. Document revision history

Date	Revision	Changes
15-Feb-2012	1	Initial release.
15-Mar-2012	2	Added following functional problem: – ERR004480
17-Sep-2013	3	Updated disclaimer.

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