



Improve STPM3x power on startup under harsh conditions

A design tip is a description of an application oriented, technical implementation that leads to a specific benefit. For more information or support, visit www.st.com

Main components	
	ASSP for metering applications with up to four independent 24-bit 2 nd order sigma-delta ADCs, 4 MHz OSF and 2 embedded PGLNA

Purpose and benefits

The purpose of this document is to explain how to improve the power-on phase of the STPM32, STPM33 and STPM34 devices when conditions like high temperatures and slow noisy power supply ramp-up are applied.

Description

Under certain conditions like high ambient temperatures ($>70\text{ }^{\circ}\text{C}$), other self-heating conditions like the current dissipated by current shunt sensors (further increasing the temperature around the device, especially in small closed containers), and slow ramp-up phase of the 3.3V power supply together with some ripple, it may be necessary to ensure additional stability to ensure the correctness of the device operation.

For this reason, when necessary, the following design tips are recommended:

1. Keep the Enable (EN) pin low until the 3.3V supply on VCC pin exceeds the 2.5 V Power-on-Reset (POR) voltage level, then drive it high.
2. Add an additional R-C filter (6.8 k Ω with 150 μF) before the anti-burst filter connected to the EN pin.
3. Replace the 100 nF capacitors connected to VREF₁ and VREF₂ with 2.2 μF ones.

Tip #1. Driving EN pin low during the power-up

A dedicated GPIO of the microcontroller can be connected to the EN pin, so that the MCU can keep that pin low during the initial power-up phase. It is also possible that the EN pin is driven low before the power-on-reset threshold (2.5V) and pulled-up after this threshold is exceeded. In Figure 1 below, the EN pin (blue trace) is kept low before VCC (yellow trace) rises and then switched high at VCC = 2.56V. The magenta and the green traces are VDDA (analog voltage) and VREF (reference voltage) respectively.



Figure 1. EN driven separately during VCC power-up (oscilloscope plot)

Tip #2. Adding an additional R-C filter to the EN pin

The Figure 2 below shows the typical application schematics from the STPM3x datasheet (reference: Figure 11, page 14). It corresponds as well to the schematics of the ST evaluation boards EVALSTPM33 and EVALSTPM34.

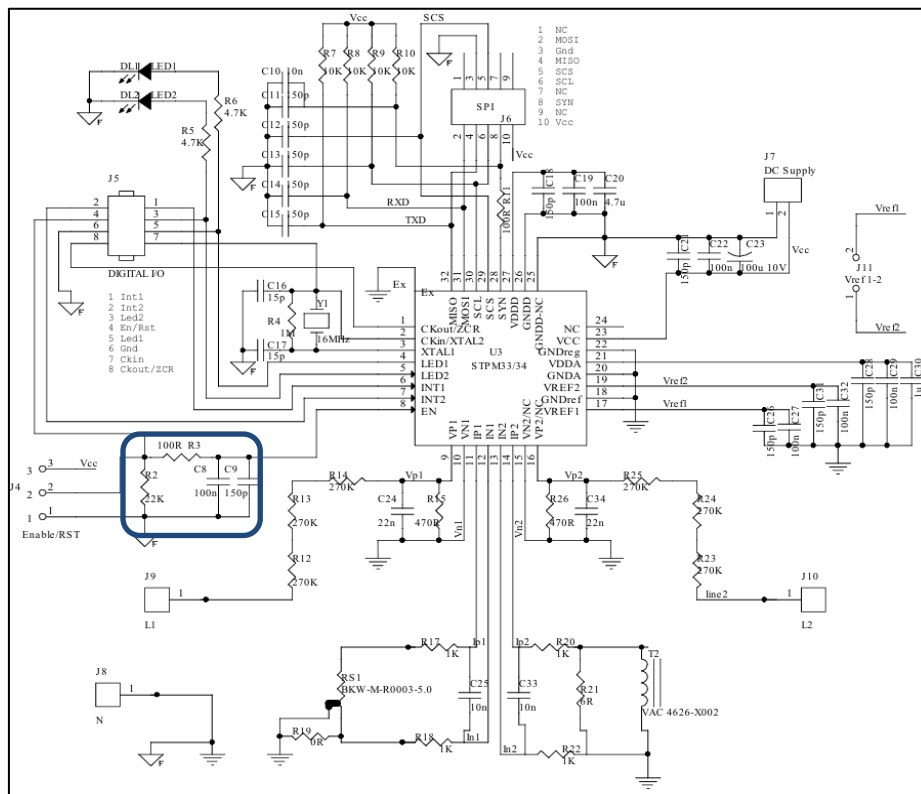


Figure 2. STPM3x typical application (anti-burst filter highlighted)

Note that a filter is already connected to the EN pin (in the blue rectangle) to protect the device from high-frequency bursts (in accordance with the IEC 61000-4-4 standard). This design tip suggests adding a 6.8 kΩ resistor and 150 μF capacitor between the driving line (or VCC connection, when EN is not driven separately) and the anti-burst filter. Figure 3 below shows the changed circuit, with the additional filter in the red rectangle.

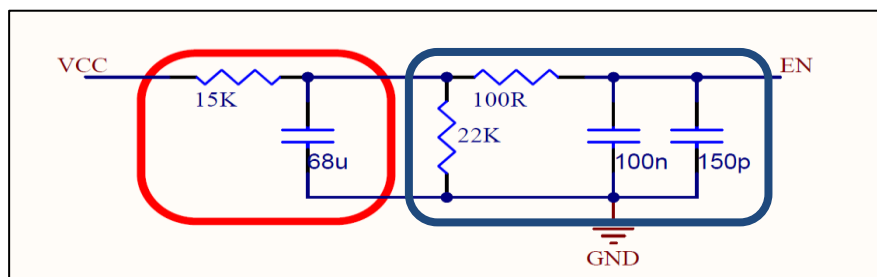


Figure 3. Modified anti-burst filter

The table below reports an example of suitable capacitor, with small SMT dimensions:

Manufacturer	Part Number	Value	Size
KYOCERA	LJA157M006R0900	150 μ F 6.3 V	1206

Tip #3. Replacing the voltage reference bypass capacitors

Error! Reference source not found. and 5 below show the recommended STPM3x application schematics with, in the red rectangles, the reference output capacitors on VREF1 and VREF2 (C29 and C32, by default 100nF each) that can be replaced with 2.2 μ F ones.

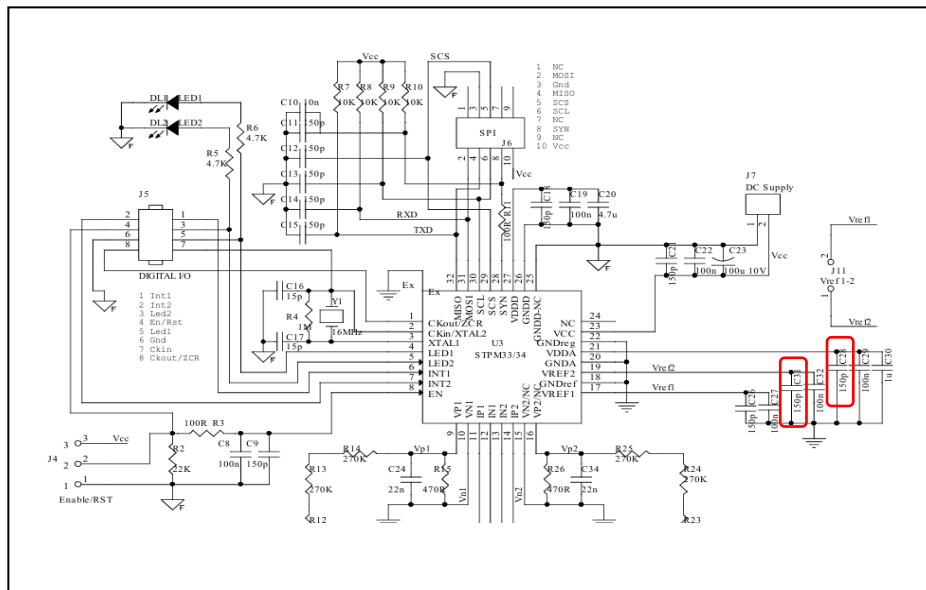


Figure 4. STPM3X typical application (reference output capacitors highlighted)

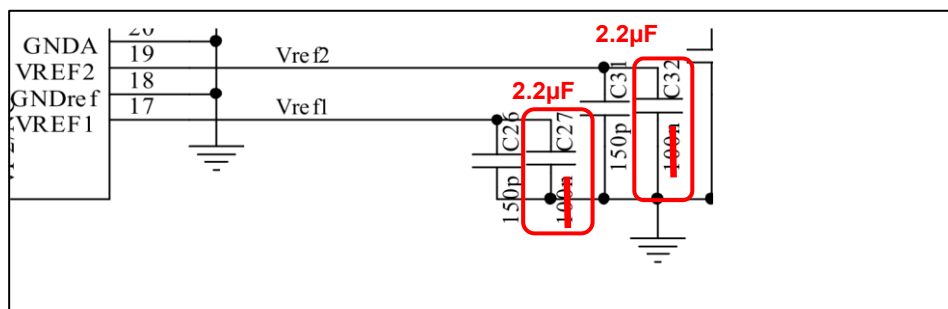


Figure 5. VREF modified capacitors (detail)

Support material

Related design support material
Evaluation board – optional changes, not strictly necessary, unless under the above-described operating conditions
Development kit – none
Gerber files – no changes
PCB layout, bill of materials and schematics files - optional changes, not strictly necessary, unless under the above-described operating conditions
Documentation
STPM3x datasheet - ASSP for metering applications with up to four independent 24-bit 2nd order sigma-delta ADCs, 4 MHz OSF and 2 embedded PGLNA

Revision history

Date	Version	Changes
24-Jul-2026	1	Initial release

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