DT0149
Design tip

Power over Ethernet application circuits, line surge analysis and treatment

Main components

List of ST components involved in the analysis.

Main components	
PM8803	High-efficiency, IEEE 802.3at compliant integrated PoE-PD interface and PWM controller
PM8805	IEEE 802.3bt PoE-PD interface with embedded dual active bridge

Purpose and benefits

The objects of this document are:
the effects of electrical Surge applied to an electronic circuit;
the cure of the effects along the electrical circuitry.

This paper can help application designers using ST interfaces, to design an application circuit able to pass line Surge occurrence.

The achievement of this objective allows applications to pass any certification tests, but especially to become more reliable and enduring.

The document provides a guideline to the voltage Surge test.

ST demo boards using main components are tested and their behavior is analyzed and improved as necessary.

The analysis provides the ability to tackle the technical activity.

Introduction

After an initial overview to explain subject, objective and other fundamental aspects of the matter, the paper gives a summary of the results, to give a complete vision, before illustrating the electrical analysis performed to obtain the results.

The following analysis is conducted on demo boards, which implement simple circuits dedicated to a Power over Ethernet application field.
Even though the research is focused on few cases of a specific type, it is useful for suggesting a valid approach for wider investigation into more complex circuitry.

The first five chapters contain some basic concepts and can be skipped by experienced technicians.

Chapter “PoE application circuits and ST devices” is necessary for a better understanding of the “Analysis results summary”.

“Analysis results summary” and “Additional design notes” report the analysis results and technical proposals for problem solving.

“Surge effects analysis” contains the investigation conducted on the boards under test;
it includes electrical test and technical analysis and it is aimed at those who want to tackle the issue from an engineering point of view.

Surge definition

From a technical point of view, a Surge consists of a transient wave of electrical current, voltage or power propagating along a line or a circuit and characterized by a rapid increase followed by a slower decrease.

Surges are real phenomena, that can be present on electrical lines; these can be both power supply lines and data transport lines, consequently any electric circuit, electrically connected to lines, becomes involved in Surge events.

Surges considered in this document, can be generated by electrical switching or lightning strikes (not direct injection) and are carriers of high energy to the devices connected to the interested lines; energy propagation influences device behavior and can result in circuit failures.

This reality necessitates the application circuit designers to consider Surges and to cure circuitry to guarantee product reliability.

The only effective way to solve the problem is to test the final circuits, subjecting them to the electrical Surge or performing an equivalent accurate simulation.

Standards and test

National or international bodies study and issue proper Standards, for matter regulation, some of those are:

IEC, the International Electrotechnical Commission which leads global organization that prepares and publishes International Standards for all electrical, electronic and related technologies;

ITU, the International Telecommunication Union which is the United Nations specialized agency in the field of telecommunications, information and communication technologies.

The scope of agencies is to guarantee the interoperability, reliability and the safety of infrastructures and equipment.

Standard specifies all aspects of the test procedure:
Equipment Under Test (EUT) type and classification;
EUT working environment classification;
Test type and waveform;
Test equipment and calibration method;
Test set-up and condition;
Test level;
Test results classification;
Mathematical modelling for simulated test.

Following the method and procedure present in the Standard, it is possible to establish the correct test for the specified EUT.

The Manufacturer and the product Designer, in compliance with current regulations and norms, choose to follow the most representative and most convenient Standard for product certification.

It is necessary to evaluate which Standard to follow, for defining tests to perform, considering:
a national or international Normative regulating product family;
general application field;
real application environment and working condition;
costs and benefits ratio resulting on the final product subjected to the selected Standard.

It should be taken into account that by satisfying a more severe Recommendation, other than just complying to the minimum mandatory requirements, it is possible to reach a high level of product performance, reliability and prestige.

A real Surge could not comply to Normative and Standard. (See Note1)

✎ *Note1. During its lifetime, an electronic product could be subject to various abnormal phenomena. Some of these can cause the same electrical effect on the circuit, even if they are very different to each other.*
An example of that are line surge and line short-circuit on PoE applications, the care of which is similar and shared.

Surge types

Since we are considering PoE application circuits, we must refer to test specifications related to communication lines.

There are two types of surge pulses foreseen for testing, named according to the time duration of the rising/falling voltage waveform:
the 10/700 µs, used to test ports intended for connection to outdoor symmetrical communication lines, which typically have cable lengths in excess of 300 m;
the 1,2/50 µs, used in all other cases.

Tests reported in this Design tip are conducted using the 1.2/50 µs surge, which is relative to the most common PoE application circuits.

Line classification

For communication lines the classification is as follows:

Shielded:
line where conductors are covered by a continuous metallic sheath, to reduce the penetration of an electric, magnetic or electromagnetic field into a given region.

Unshielded:
line where conductors are not shielded.

Symmetrical line:
pair of symmetrically driven conductors with a conversion loss from differential to common mode of greater than 20 dB (IEC 61000-4-5);
but also,
transmission media consisting of a pair of twisted wires balanced with respect to earth, usually assembled in groups in order to form a telecommunication cable (ITU-T K.xx).

This is the classification of Ethernet lines, where the eight conductors are divided in four pairs and every pair carries the signal in differential mode;

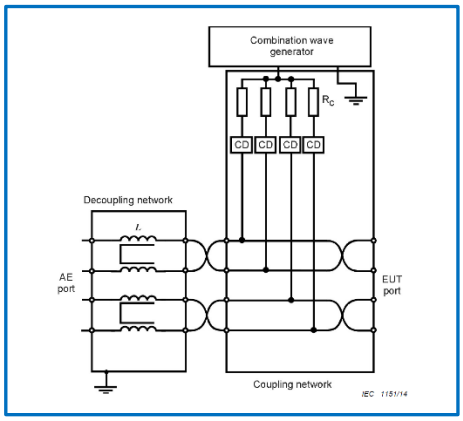
Unsymmetrical line:
line where conductors are not coupled and balanced with respect to earth.

PoE lines are frequently classified as Unshielded and Symmetrical, but it is possible to encounter a real working condition of Shielded (with shield connected to both ends) and Symmetrical lines.

Coupling and decoupling networks

We use unshielded symmetrical line set-up, for topic study in this paper, therefore the proper Coupling and Decoupling Network (CDN) is the following, as recommended by the IEC 61000-4-5 standard:

Figure 1. Coupling and decoupling networks for four wires line.



On Ethernet lines there are eight wires, the surge is split using the Coupling network.

The coupling resistor Rc is calculated to have a total equivalent resistance of 40 Ω, as required by the standard.

Rc = 40 x 8 = 320 Ω.

The coupling capacitor CD is chosen to meet the waveform parameters of the selected pulse (1.2/50 µ).

CD = 68 nF.

PoE application circuits and ST devices

Looking at ST PoE PD interfaces, it is possible to select two fundamental integrated circuits:

PM8803, which performs the PoE interface and the DC-DC converter for PD supply, but it has not the active bridge driving for the input line rectification;
demo board STEVAL-TSP004V2 is used as Device Under Test (DUT) (5 V – 4 A, synchronous flyback converter, see Data Brief DB2569 for electrical schematic viewing).

PM8805, which performs the PoE interface, with internally two complete active bridges, to get high efficiency input line rectification;
demo board STEVAL-POE002V1 is used as DUT (5 V – 8 A, synchronous flyback converter, see Data Brief DB3628 for electrical schematic viewing);
on the board, the DC-DC converter for PD supply is performed using the PM8804 controller.

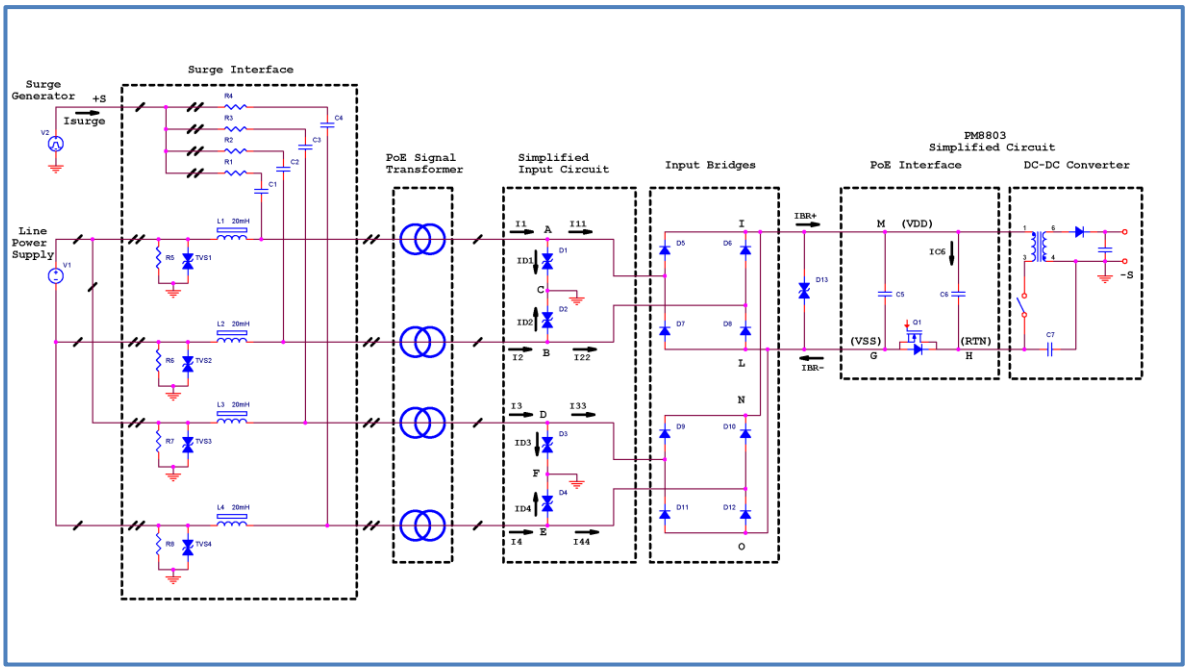
The significant difference between the two devices, for the Surge treatment, is the presence or not of the active bridges.

It is necessary to draw a simplified electrical diagram of the basic application circuit, to analyze the basic behavior during surge.

PM8803

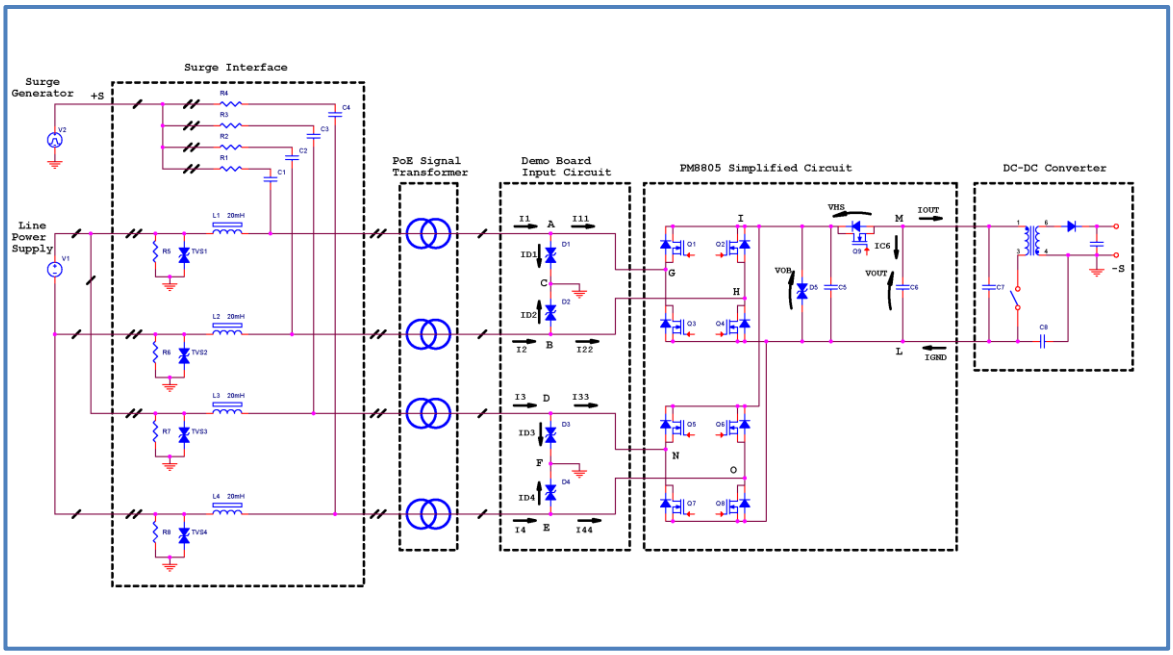
Using the STEVAL-TSP004V2, the following electrical diagram can be used to present the study; it contains a simplified circuit, which describes the significant parts of the demo board under test.

Figure 2. PM8803 electrical diagram for Surge analysis.



Using the STEVAL-POE002V1, the following electrical diagram can be used to present the study; it contains a simplified circuit, that describes the significant parts of the demo board under test.

Figure 3. PM8805 electrical diagram for Surge analysis.



In the previous diagrams, the block relative to the Surge Interface is sketched as a four-wire circuit, instead of an eight-wire one;
it is however valid, because on an Ethernet line, the wires of each pair are crossed by the same current and we consider the sum of those.

Line Power Supply

The demo boards under test are supplied by the Line Power Supply V1, with 48 Vdc.

Two pairs are connected in parallel to the positive output and two pairs are connected to the negative output.

Even if on the real condition, the voltages present on the four pairs of an Ethernet line are supplied by two different power supplies, the adopted set-up is valid;
that is because the Surge Interface contains four coupled inductors as Decoupling device, with 20 mH value, which are able to separate the four pairs.

Surge application points

The test equipment Surge Generator V2, is connected between the Surge Coupling Interface (+S) and the output of the DC-DC converter of the demo board under test (-S). Points C and F are connected to –S through demo board p.c.b. tracks.

The internal ground connections of the Surge Interface are connected to –S point with an external dedicated wire.

Methods of analysis

Due to the characteristic of the electrical phenomena under investigation, in particular for the timing of transients, it is possible to conduct the electrical analysis with three different approaches.

Theoretical analysis on the equivalent electrical circuit

This is the method requiring less tools.

It is necessary to be able to conduct correct analysis, studying the electrical circuit.

It is very important to draw the most significant electrical circuit, because the presence of various components on the real application circuit can deeply influence the Surge effect.

This method should be used for simple application circuit only, to not forget fundamental components during analysis.

Simulating the electrical circuit

This method requires a personal computer and a simulation software.

It allows to get results very similar to the real situation, because the timing of the signals under analysis is not very fast and the parasitic elements of the real circuit don’t influence results significantly.

It is necessary to be able to use the simulation method and tool correctly.

It is possible to implement and test changes very quickly.

Performing electrical test and measurement

This method requires proper instruments and an equipped laboratory.

It returns complete results on the real application circuit in a short time, but it could be difficult to implement changes to test.

For valid results, it is necessary to use a sample having all the functionality of the final product.

Analysis results summary

The following Surge analysis provides some fundamental dictates, to foresee circuitry behavior during Surge application, useful for designing application circuits.

Surge is applied between input lines and reference ground.
In a PoE application circuit, with functional isolation grade between primary and secondary side, the DC-DC converter transformer is not designed to sustain high voltage.
If no one protection is foreseen, the Surge can perforate the insulation of the components subjected to the Surge voltage.

In these working conditions, it is mandatory to limit the voltage applied to the input lines, using proper components placed between lines and reference ground.
The right choice is the Transient Voltage Suppressors, which limit the lines voltage to their clamping threshold, see Fig.2 and Fig.3, D1, D2, D3 and D4 components.

Other kinds of protectors exist, which act like a short-circuit after their threshold triggering: those components are not recommended, because they create input multiple short-circuits, with consequent circuitry stopping and possible failure during board capacitor discharge.

Even with TVS presence, the input lines are subjected to fast voltage transition and the behavior of the whole system depends on the electrical circuit under test.

Considering Fig.2 circuitry, in which the input bridges are made by diodes and the electrical circuit is quite simple, the behavior during Surge is good and the D.U.T. does not suffer the Surge.

A major part of the Surge current is split into equal quantities through the four TVS, D1, D2, D3 and D4.
The residual current flowing through the circuit is very low and it is not a risk.

The last forethought is to insert D13 TVS, which protects the circuitry against differential overvoltage of the input lines and can dissipate the energy stored by the four decoupling inductors L1, L2, L3 an L4, during Surge test.

Bill of material for Surge treatment depends on maximum voltage of applied surge, because it is necessary to consider the maximum value of the current flowing through the four TVS.

For 6 kV surge (1.2/50 µs), D1=D2=D3=D4=D13=SM15T68CA (ST Transient Voltage Suppressor).

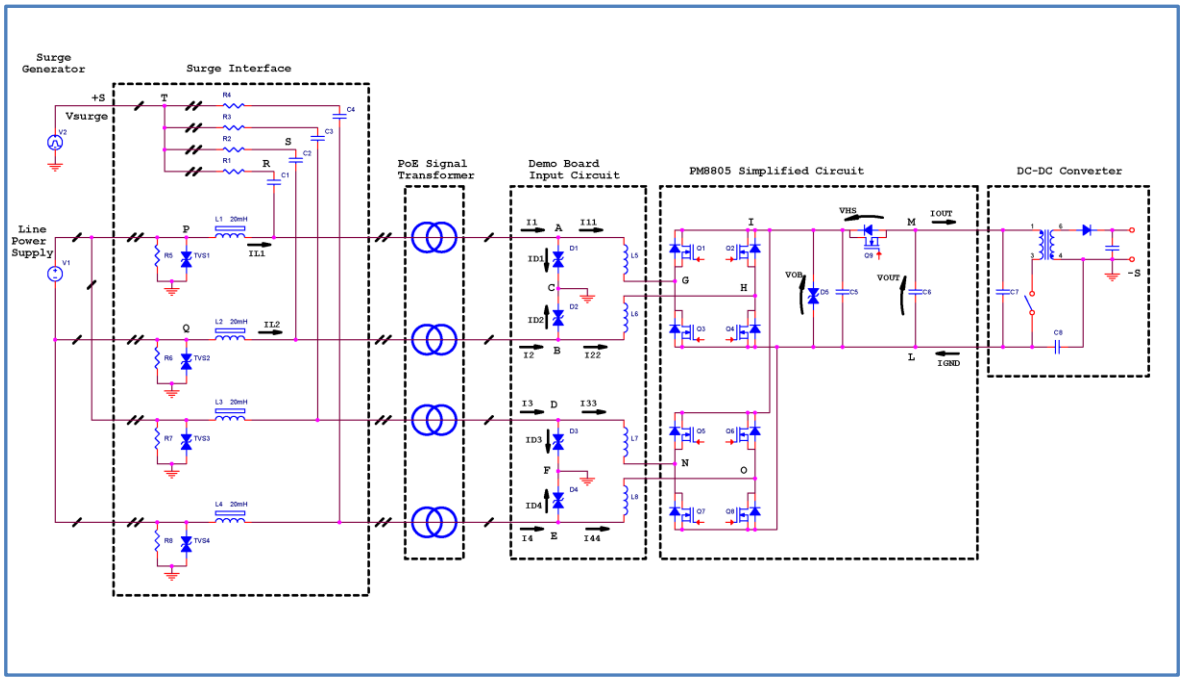
Considering Fig.3 circuitry, in which the input bridges are composed by MOSFETs, the Surge generates high currents flowing through the interested electrical circuit.
These currents can generate circuitry stopping, but if the value exceeds the components' absolute maximum rating, it can also lead to failure.

The problem is generated by the driving time of the bridge MOSFETs.
The driving circuit reacts to the reverse current flowing through the transistors, with a delay, that is sufficient to allow the Surge current flowing through the circuit, instead of into the four input TVS.

The Surge treatment consists in decoupling the input bridges from the input line, inserting four inductors in series, see Fig.4, L5, L6, L7 and L8.
The four inductors allow the most part of the Surge current to flow immediately through the four TVS.
The remaining current flowing though the circuitry remains in a safe range and it allows input bridges to open.

It is necessary to insert the TVS D5 (similar to D13 in Fig.2), for the same reason previously explained.

Figure 4. PM8805 electrical diagram with Surge treatment.



Bill of material used for 6 kV (1.2/50 µs) surge treatment is the following:

D1=D2=D3=D4=D5=SM15T68CA (ST Transient Voltage Suppressor)

L5=L6=L7=L8=SD54-103ML Coilcraft, or equivalent.

Important design notes are reported in the next chapter.

Additional design notes

Previous analysis points out that one of the basic principles for the treatment of Surge effects is to have very fast input bridge components in order to react to the inverse current.

A diodes bridge has the necessary speed, but it has the disadvantage of high-power losses.

The internal active bridges of the PM8805 perform a high efficiency input circuit, but lead to the necessity to add some inductors for the control of the Surge currents.

In general, if an active bridge is necessary for obtaining high efficiency, it is important to get a driving circuit with fast sensing of the current polarity into MOSFETs.
Reducing the time to open the bridge branch, it is possible to reduce the dimension of the four inductors added to reduce Surge current flowing through the application circuit.

It is possible to use input bridges made with diodes and MOSFETs together, for merging the good properties of both components.
Diodes are fast and improve the voltage transitions during Surge, MOSFETs improve bridge efficiency.
Diodes can be used as high-side rectifiers, N channel MOSFETs can be used as low-side components.
Using this kind of solution, the four inductors can be avoided or not, depending on the whole circuit configuration.

Fig.5 shows an example of a circuit in which it is necessary to use the four inductors.

Figure 5. PM8803 application circuit example.

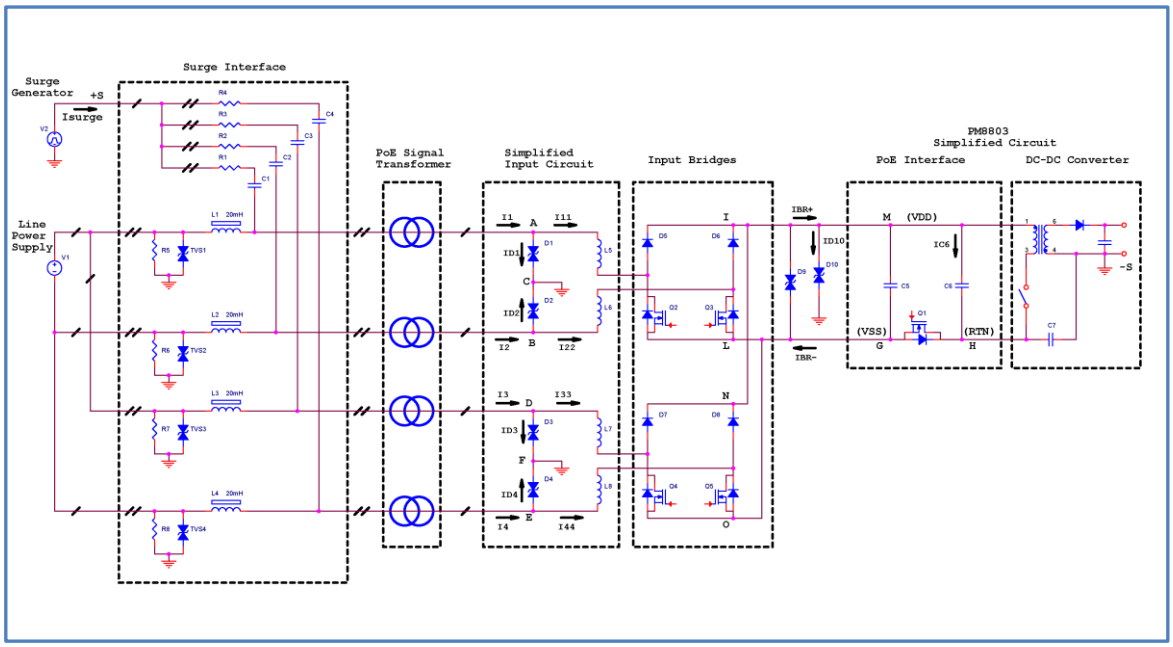
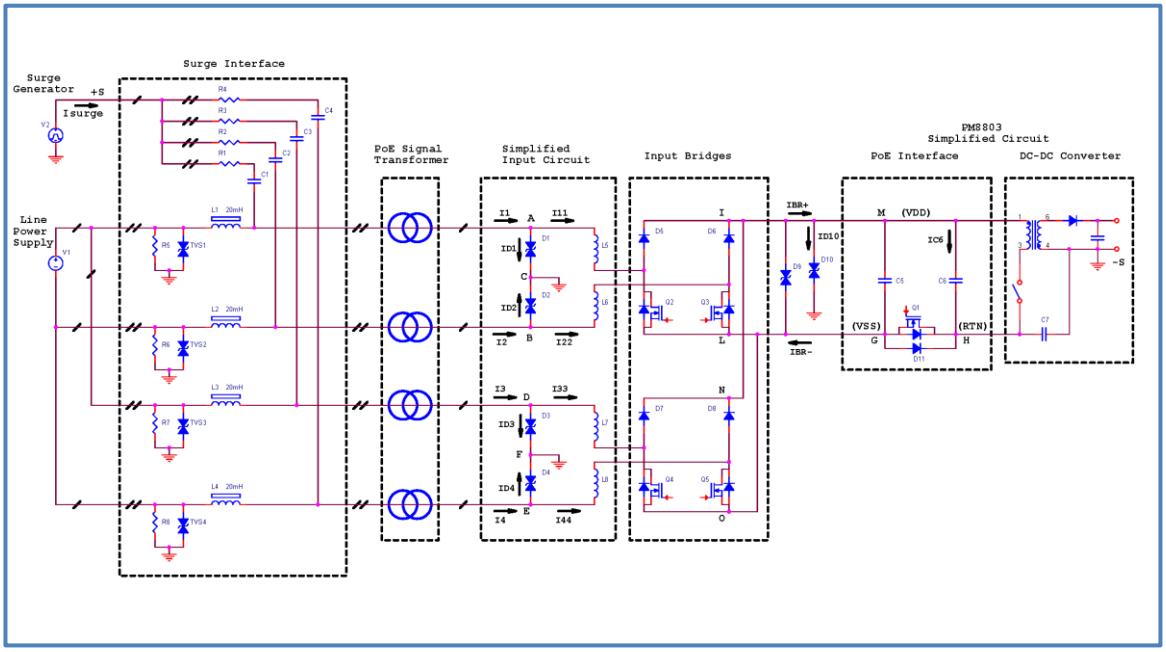


Fig.5 is a very simplified circuit of a real application, the presence of the TVS D10, creates a new path for the Surge current.
To limit the circulation of ID10, it is necessary to insert the four inductors L5, L6, L7 and L8, even if the two input bridges have the diodes D5, D6, D7 and D8 as high-side rectifier.

Fig.6 shows an additional protection applicable to PoE interfaces similar to the PM8803.

Figure 6. PM8803 electrical diagram with additional protection.



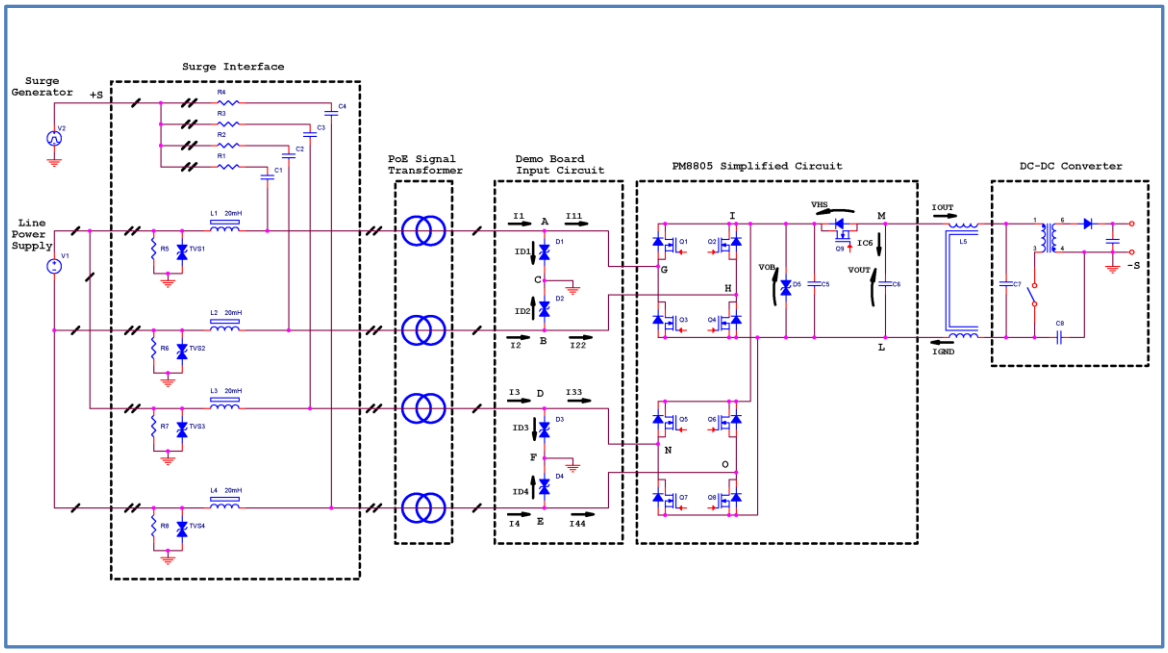
In Fig.6, the diode D11 is added in parallel to the hot swap MOSFET Q1.

The purpose of the diode is to shunt the peak current generated by the Surge, but its presence is useful to avoid high current flowing through Q1 during possible short-circuit on the board circuitry or on the Ethernet line.

D11= STPS2H100 (ST 2A 100 V Schottky diode), or better.

Fig.7 shows an important design note that should be taken into account when using the PM8805 device and similar PoE interfaces.

Figure 7. PM8805 electrical diagram with common mode inductor.



It is quite common to insert a common mode inductor upstream of the DC-DC converter, to reduce the conducted noise generated by the circuit, see Fig.7 L5.
The leakage inductance of L5 can create a voltage dump of V_ML and VOB, during the circulation of Surge current.
The current peak on IOUT and IGND path (see currents in Fig.16 and Fig.24), can create a drop of VOB and a consequent reset of the PM8805.

To avoid this, it is necessary to use a C6 with a sufficient capacitance, to allow the circulation of the Surge current through it.
It is possible to split the value of capacitor C7, between C6 and C7.

Surge effects analysis

To reach the goal it is necessary to analyze the electrical phenomena and look for proper corrective action for reducing detrimental effects of the Surge.

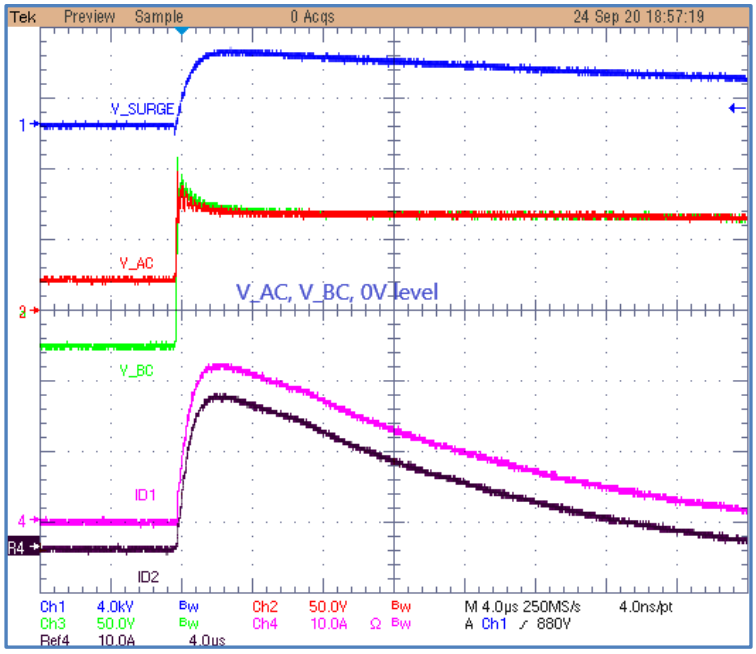
The following section of the document reports a detailed investigation into three circuital conditions, to focus on fundamental concepts.

The analysis is conducted using a positive voltage of the Surge, but the results are always valid for a negative one.

Diodes bridges

The following images show the effect of a 4 kV surge applied to the STEVAL-TSP004V2, see Fig.2 as reference.

Figure 8. 4 kV surge on STEVAL-TSP004V2.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_AC voltage;
Ch3 green trace, 50V/div, V_DC voltage;
Ch4 purple trace, 10A/div, ID1 current;
R4 brown trace, 10A/div, ID2 current.

In Fig.8 it is possible to see the following behavior:
at the Surge injection, the voltage on D1 and D2 (SM15T68CA) rises immediately and reaches the TVS threshold;
the current inside D1 and D2 increases following V_SURGE rise time;
both ID1 and ID2 reach the same maximum value, ID1=ID2≈23A.

The theoretical value of the Surge current peak is Isurge = V_SURGE/Rsurge = 4000/42≈95A, where Rsurge is the sum of the internal 2 Ω resistor of the Surge Generator and the internal 40 Ω of the Surge Interface.

Considering the presence of D3 and D4 also, the Isurge is split into four similar currents flowing into the four TVS and bypassing the other parts of the circuit.

Figure 9. 4 kV surge on STEVAL-TSP004V2.

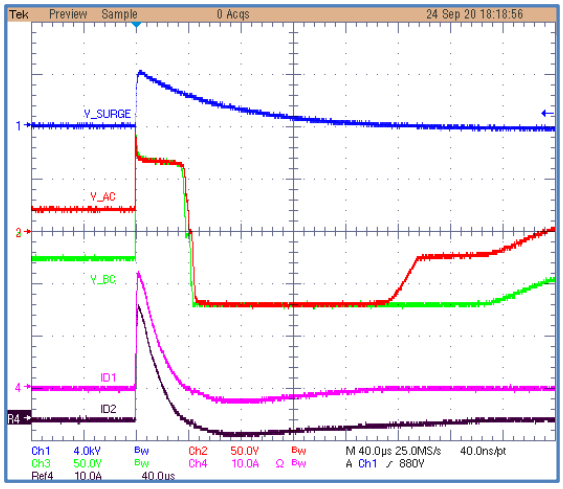


Fig.9 shows the same event as Fig.8, but in a longer time window.

It is possible to identify the following behavior:

even if the pulse generated by the Surge Generator is always positive during the event, the surge applied to the DUT has a first positive part and a second negative one; this is due to the coupling capacitors C1, C2, C3, and C4.

Figure 10. 4 kV surge on STEVAL-TSP004V2.

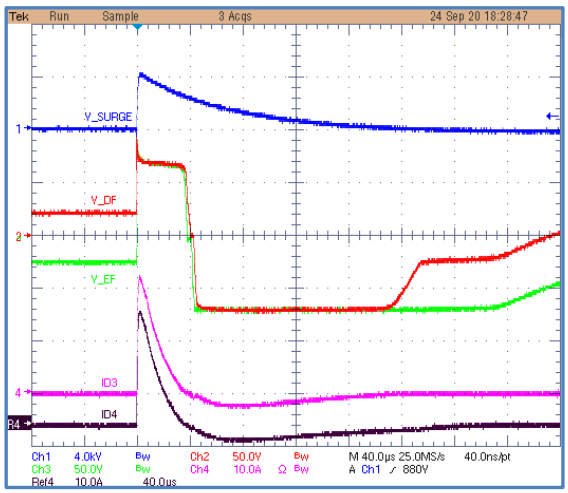
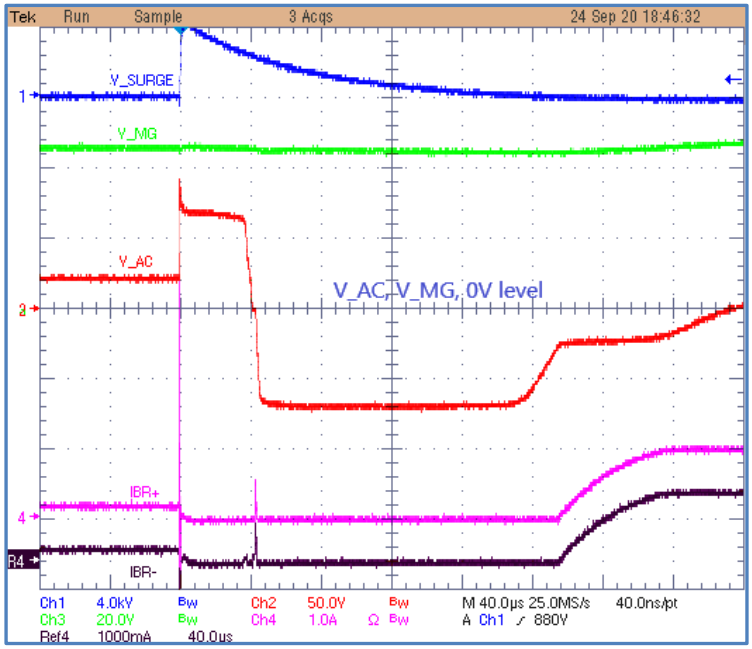


Fig.10 shows the behavior of ID3 and ID4, demonstrating that the Surge current is split into four similar parts.

Figure 11. 4 kV surge on STEVAL-TSP004V2.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_AC voltage;
Ch3 green trace, 20V/div, V_MG voltage;
Ch4 purple trace, 1A/div, IBR+ current;
R4 brown trace, 1A/div, IBR- current.

Fig.11 shows the behavior of three different signals:
V_MG, the voltage on the bridges output;
IBR+, the current on the positive output of the bridges;
IBR-, the current on the negative output of the bridges.

The V_MG voltage has little variation; this means the DC-DC converter does not suffer the Surge.

IBR+ and IBR- go to zero during the Surge, because the voltage at the bridges inputs is nulled.

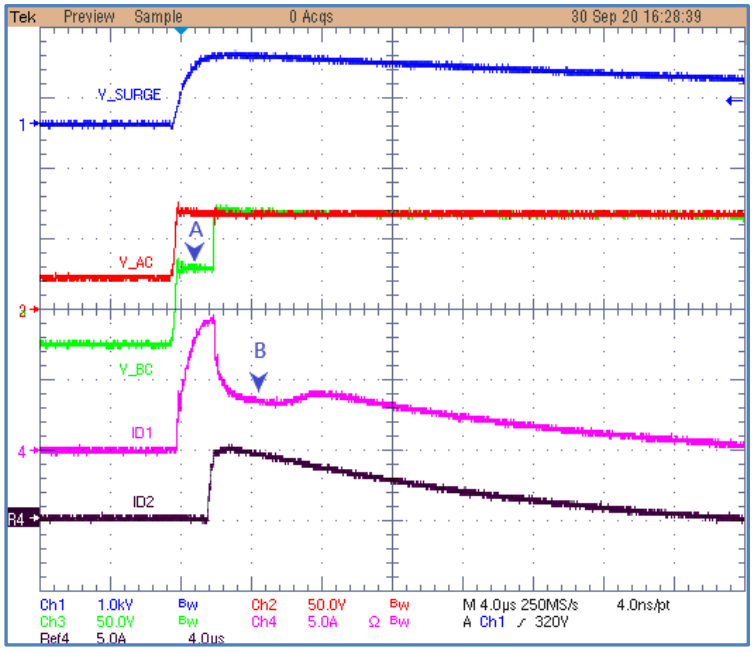
A very fast current spike at the Surge rising edge is noticeable, due to the current flowing through the DC-DC converter board capacitor C7 and through parasitic capacitance of the transformer. The board does not suffer the Surge for the current flowing through the circuit.

After Surge expiration, it is possible to see IBR+ and IBR- rising, due to the energy stored in the decoupling inductors L1, L2, L3 and L4, during the surge;
the energy is supplied to the board capacitors C5 and C6; the voltage V_MG rises until all energy is transferred.
If the board capacitors are not big enough, the voltage could rise to a not proper value; the TVS D13 is foreseen to avoid this risk.

A more detailed analysis about this last surge effect is comprised in the paragraph “Analysis of the entire Surge event”, on page 27.

The following images show the effect of a 1 kV surge applied to the STEVAL-POE002V1, see Fig.3 as reference.

Figure 12. 1 kV surge on STEVAL-POE002V1.

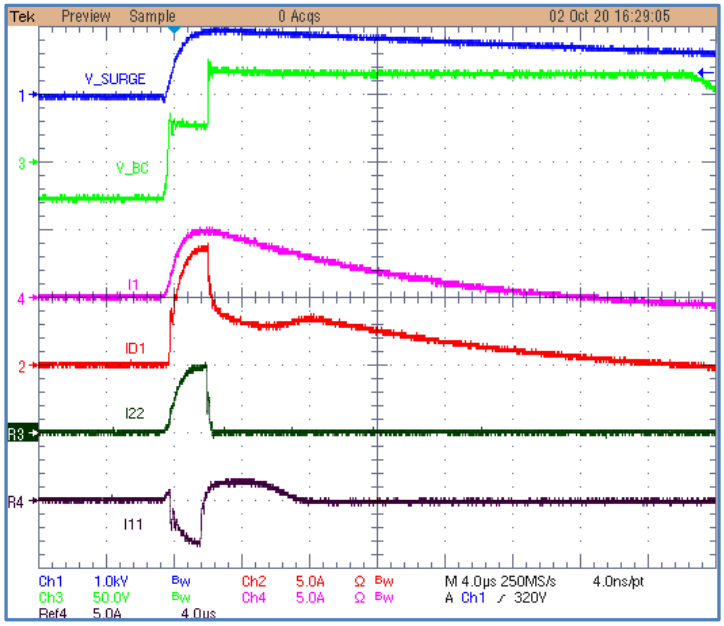


Ch1 blue trace, 1kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_AC voltage;
Ch3 green trace, 50V/div, V_BC voltage;
Ch4 purple trace, 5A/div, ID1 current;
R4 brown trace, 5A/div, ID2 current.

Fig.12 shows the following behavior:
At the Surge injection, during the first 2 µs (Fig.12_A), the D2 TVS does not conduct;
this is because the transistor Q1 and Q4 (Fig.3) are closed and board capacitors C5, C6, C7 fix the voltage V_ML=VOB=V_IH=V_AB=48 V;
this is visible on Fig.12_A point.

During this first time lapse, the current I2=I22 flows through Q4, through the board capacitors C5, C6, C7, through Q1 and into D1.
It is possible to see this behavior in Fig.13.

Figure 13. 1 kV surge on STEVAL-POE002V1.



Ch1 blue trace, 1kV/div, V2 surge voltage;
Ch2 red trace, 5A/div, ID1 current;
Ch3 green trace, 50V/div, V_BC voltage;
Ch4 purple trace, 5A/div, I1 current;
R3 dark green trace, 5A/div, I22 current;
R4 brown trace, 5A/div, I11 current.

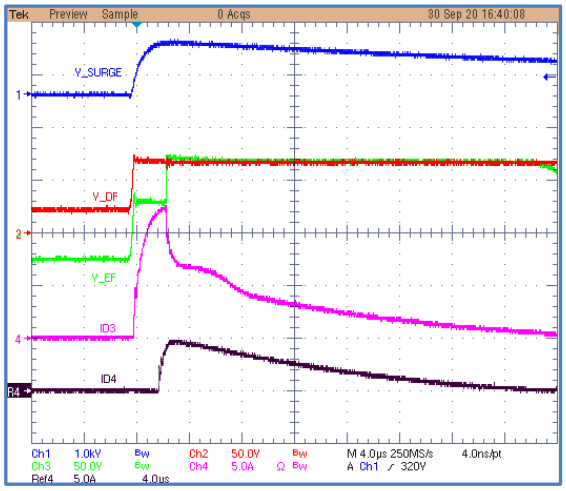
It is remarkable that during this first period of time, the I22 current is less than I11 current;
this is because I22 flows partly into D1 and partly into D3;
it is possible to verify ID1=I1+(-I11).

After the first 2 µs, the transistors Q4 and Q8 open, because the input bridge section senses the reverse current flowing through those;
at that point, Fig.12 shows the voltage V_BC rising to the D2 TVS threshold and the current I2=ID2 flowing through D2;
Fig.13 shows I22 going to zero and, at the same time, I11 flowing through Q1;
since ID1=I1-I11, the shape of ID1 and I11 point out the behavior of I11 at point B (Fig.12_B);
during Fig.12_B time lapse, the current I11 flows through Q1 and Q5, going into D3;
this passage is possible because the high-side MOSFETs Q1 and Q5 open with higher delay, if compared to the low-side Q4 and Q8.

After the opening of Q1 and Q5, the four Surge currents I1, I2, I3 and I4 flow into the respective TVS D1, D2, D3, D4.

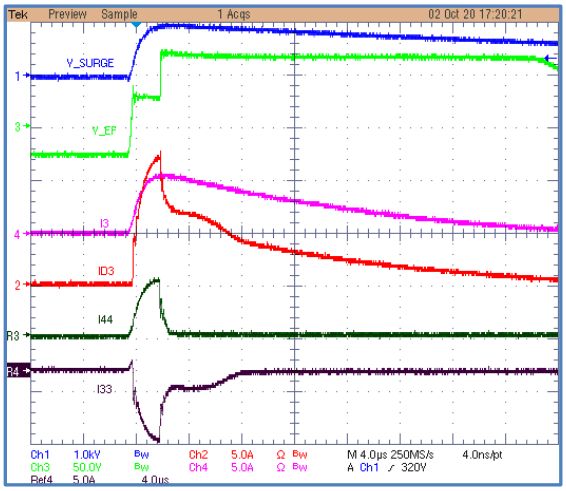
See also Fig.14 and 15 for comprehension of the transient.

Figure 14. 1 kV surge on STEVAL-POE002V1.



Ch1 blue trace, 1kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_DF voltage;
Ch3 green trace, 50V/div, V_EF voltage;
Ch4 purple trace, 5A/div, ID3 current;
R4 brown trace, 5A/div, ID4 current.

Figure 15. 1 kV surge on STEVAL-POE002V1.



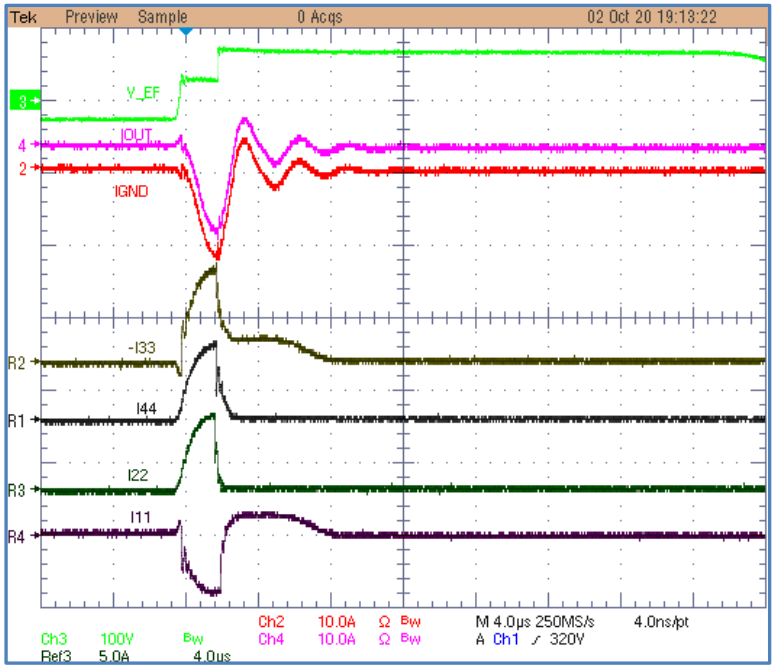
Ch1 blue trace, 1kV/div, V2 surge voltage;
Ch2 red trace, 5A/div, ID3 current;
Ch3 green trace, 50V/div, V_EF voltage;
Ch4 purple trace, 5A/div, I3 current;
R3 dark green trace, 5A/div, I44 current;
R4 brown trace, 5A/div, I33 current.

The delay relative to Fig.12_A point, is generated by the delay of the input bridges to open; during this time lapse there are two currents, I22 and I44, flowing through the PM8805 and through the application circuit.

These two currents are a risk for the circuit reliability, because they can reach high value and generate a circuit failure.

Fig.16 shows the current situation.

Figure 16. 1 kV surge on STEVAL-POE002V1.



Ch1 blue trace OFF, 1kV/div, V2 surge voltage;
Ch2 red trace, 10A/div, IGND current;
Ch3 green trace, 100V/div, V_EF voltage;
Ch4 purple trace, 10A/div, IOUT current;

R1 black trace, 5A/div, I44 current;
R2 dark trace, 5A/div, -I33 current;
R3 dark green trace, 5A/div, I22 current;
R4 brown trace, 5A/div, I11 current.

As previously explained, I22 and I44, during Fig.12_A time lapse, flow through Q4 and Q8, through board capacitors C5, C6, C7, coming back through the hot swap MOSFET Q9 and through Q1 and Q5.
The sum of I22 and I44 is IGND=IOUT.

The peak current flowing through the PM8805 is IOUT=IGND=12A.
This value is not a problem, because the input Surge level is 1 kV, but applying 4 kV the current should be around 48 A.

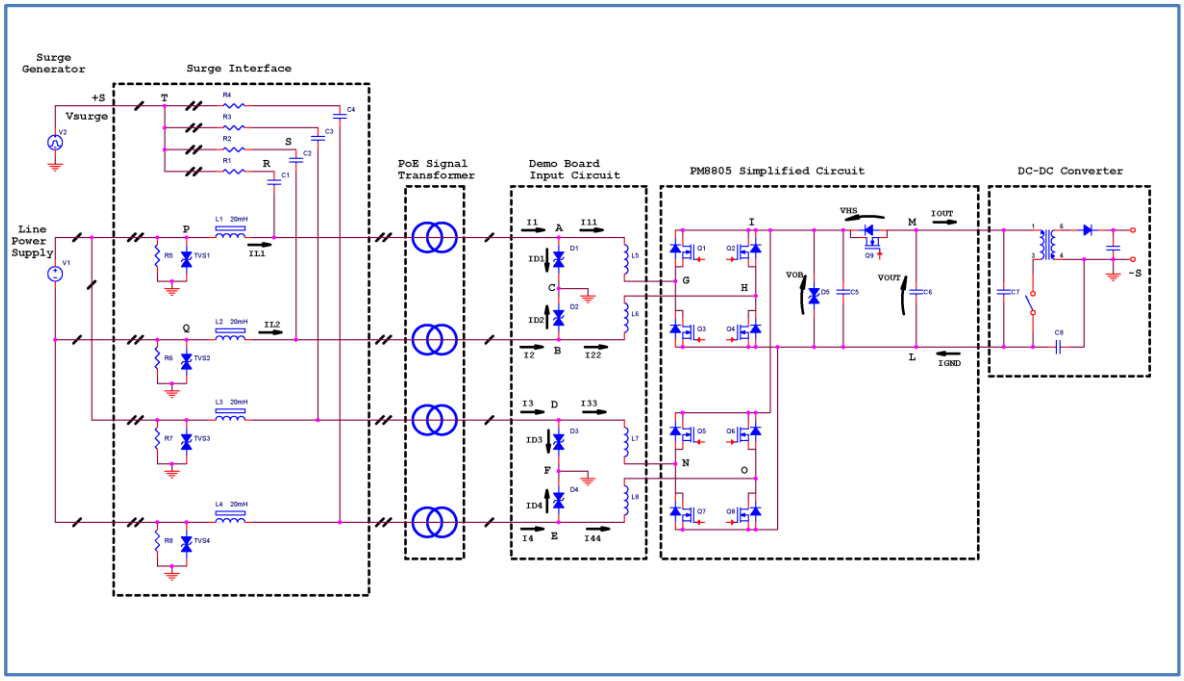
It is necessary to avoid these current peaks.

The current flows through the integrated circuit, because the bridge transistors Q4 and Q8 are not very fast to open;
using previous demo board STEVAL-TSP004V2, that has input bridges made with diodes, the problem is not present.

Adding inductors

To solve this problem, it is necessary to allow the fast transition of nodes B and E (see Fig.17). Adding four inductors on the four input lines, it is possible to insert an electrical decoupling valid for the fast transition of the Surge.

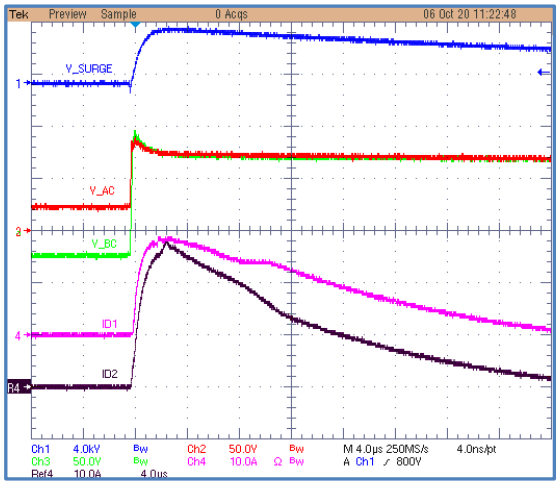
Figure 17. PM8805 electrical diagram with Surge treatment.



Inductors L5, L6, L7, L8 perform the following:
limit the currents I11, I22, I33 and I44;
allow the voltages V_BC and V_EF to reach the voltage threshold of D2 and D4;
allow the currents ID2 and ID4 to flow immediately at the Surge injection.

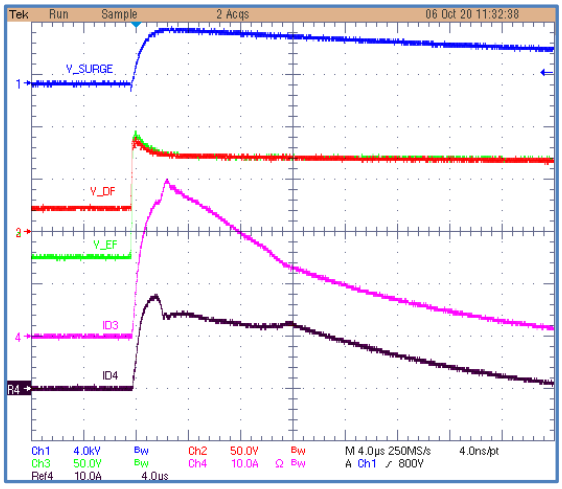
The following figures show the circuit behavior, when adding the four inductors.
The circuit is subject to a 4 kV surge.

Figure 18. STEVAL-POE002V1 with inductors.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_AC voltage;
Ch3 green trace, 50V/div, V_BC voltage;
Ch4 purple trace, 10A/div, ID1 current;
R4 brown trace, 10A/div, ID2 current.

Figure 19. STEVAL-POE002V1 with inductors.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_DF voltage;
Ch3 green trace, 50V/div, V_EF voltage;
Ch4 purple trace, 10A/div, ID3 current;
R4 brown trace, 10A/div, ID4 current.

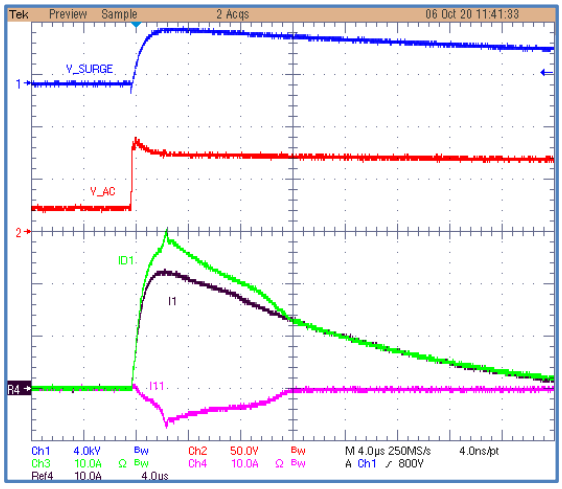
Fig.18 and Fig.19 show the effect of the inductors' presence:
V_AC, V_BC, V_DF and V_EF go immediately to the voltage threshold of the four TVS D1, D2, D3 and D4;
ID1, ID2, ID3 and ID4 flow immediately through the respective TVS.

This behavior is similar to the one obtained with the demo board STEVAL-TSP004V2, see Fig.8, Fig.9 and Fig.10.

Comparing the behavior of the two demo boards, it is possible notice some differences between the currents shape;
this is due to the difference of the input bridges;
STEVAL-TSP004V2 has diodes bridges, STEVAL-POE002V1 has MOSFET bridges;
as shown before, the four MOSFETs are driven with a delay, that allows the circulation of I11, I22, I33 and I44.

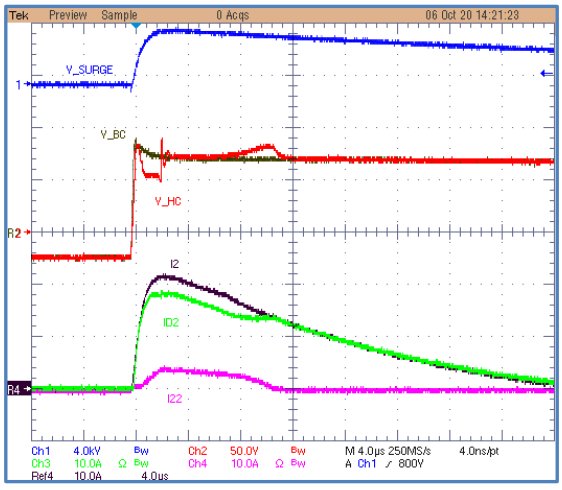
The following Fig.20, Fig.21, Fig.22 and Fig.23 point out the four currents.

Figure 20. STEVAL-POE002V1 with inductors.



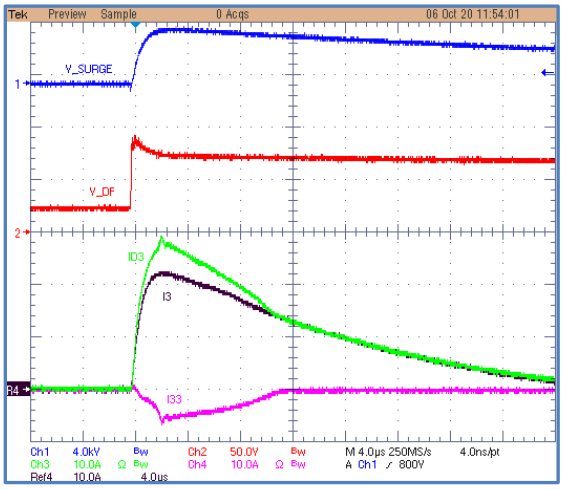
Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_AC voltage;
Ch3 green trace, 10A/div, ID1 current;
Ch4 purple trace, 10A/div, I11 current;
R4 brown trace, 10A/div, I1 current.

Figure 21. STEVAL-POE002V1 with inductors.



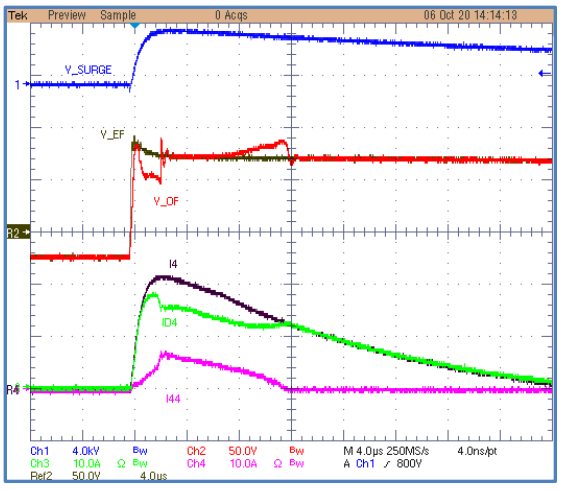
Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_HC voltage;
Ch3 green trace, 10A/div, ID2 current;
Ch4 purple trace, 10A/div, I22 current;
R2 dark green trace, 50V/div, V_BC voltage;
R4 brown trace, 10A/div, I2 current.

Figure 22. STEVAL-POE002V1 with inductors.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_DF voltage;
Ch3 green trace, 10A/div, ID3 current;
Ch4 purple trace, 10A/div, I33 current;
R4 brown trace, 10A/div, I3 current.

Figure 23. STEVAL-POE002V1 with inductors.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_OF voltage;
Ch3 green trace, 10A/div, ID4 current;
Ch4 purple trace, 10A/div, I44 current;
R2 light brown trace, 50V/div, V_EF voltage;
R4 brown trace, 10A/div, I4 current.

Analyzing the previous four images, it is possible to verify the following.

Since the four images are snapped in different surge events, it is not possible to have a perfect comparison of the currents shape, but it is possible to make the correct considerations.

During the first 2 µs of the Surge, Q4 and Q8 remain closed, but then open while Q1 and Q5 are still closed;
during the first 12 µs of the Surge, Q1 and Q5 remain closed, but then open.

During the first 2 µs:

ID1=I1-I11 and ID3=I3-I33;
I11+I33=IOUT;

IOUT=IGND, because the board main capacitors (C7) act like a short-circuit for alternate currents;
IGND=-I22-I44;

I11=-I33+IOUT=-I33+IGND=-I33-I22-I44;

the same is valid for I33=-I11-I22-I44.

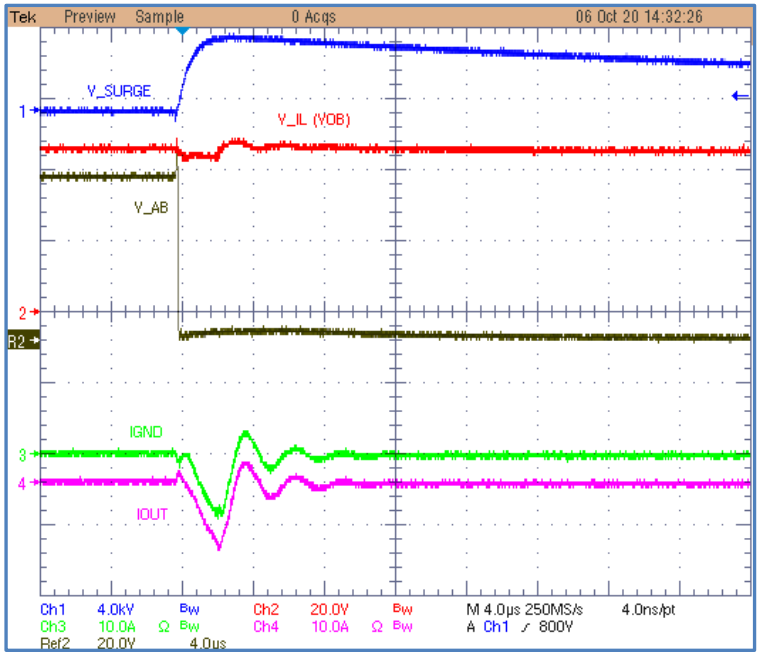
After the first 2 µs, Q4 and Q8 are open;
after the first 2 µs, Q1 and Q5 remain closed, but then open after the first 12µs;
since Q2 and Q6 have a diode in parallel, they can be considered closed, depending on their voltage condition.

After the first 2 µs, but before the first 12 µs, considering the node I:
I11=-I22-I33-I44;
I33=-I11-I22-I44.

Looking at the previous figures, it is very important to note that resulting currents I11, I22, I33 and I44 have an amplitude lower than 10A, even if the peak current is around Isurge=Vsurge/42Ω=4000/42=95A.

Fig.24 shows IOUT and IGND, plus the voltage V_IL=VOB.

Figure 24. STEVAL-POE002V1 with inductors.



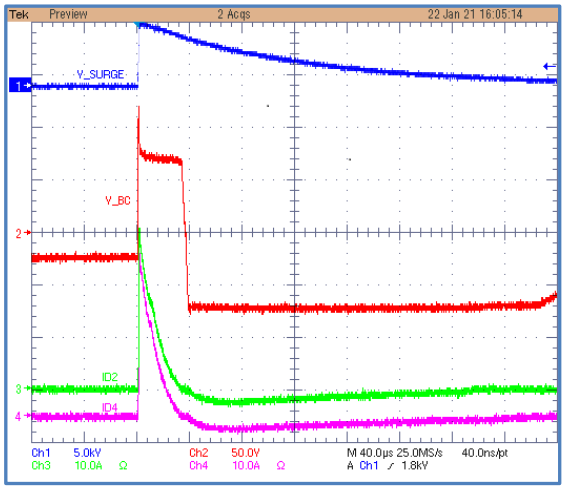
Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 20V/div, V_IL voltage;
Ch3 green trace, 10A/div, IGND current;
Ch4 purple trace, 10A/div, IOUT current;
R4 brown trace, 20V/div, V_AB voltage.

Fig.24 reports that IOUT=IGND<10A and VOB has a variation ΔVOB<10V.

The four inductors I5=I6=I7=I8=10µH are effective for Surge treatment, because the current flowing through the board is acceptable for the devices and the voltage of the main component is stable enough to guarantee the proper working.
Even if not reported, other parts of the application circuit present on the demo board remain in their normal working condition.

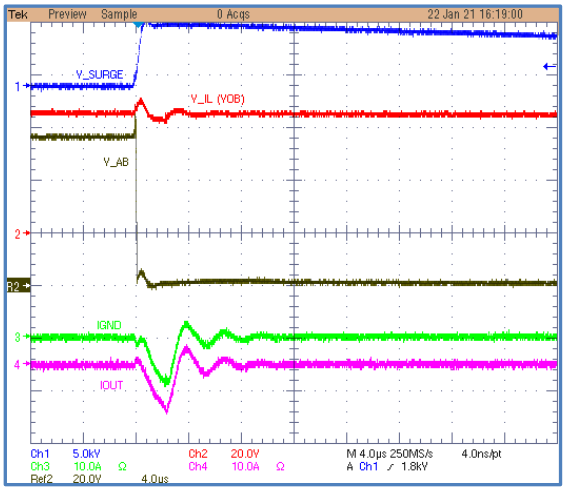
The following Fig.25 and Fig.26 report the circuit behavior when subjected to a 6 kV surge.

Figure 25. STEVAL-POE002V1 at 6 kV surge.



Ch1 blue trace, 5kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_BC voltage;
Ch3 green trace, 10A/div, ID2 current;
Ch4 purple trace, 10A/div, ID4 current.

Figure 26. STEVAL-POE002V1 at 6 kV surge.



Ch1 blue trace, 5kV/div, V2 surge voltage;
Ch2 red trace, 20V/div, V_IL voltage;
Ch3 green trace, 10A/div, IGND current;
Ch4 purple trace, 10A/div, IOUT current;
R4 brown trace, 20V/div, V_AB voltage.

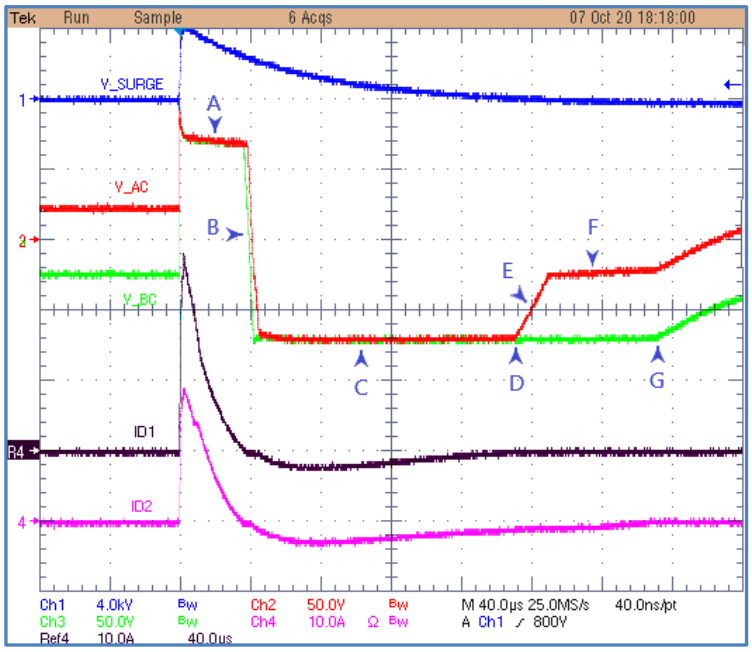
Fig.25 and Fig 26 demonstrate that the four inductors applied are effective with a 6 kV surge also.
ID2=ID4≈32A flow into the relative TVS at the Surge injection, see Fig.25.
V_IL (VOB) has a variation less than 10 V and IOUT=IGND has a peak value of 10 A, remaining inside the absolute maximum rating of the device.

The four TVS must be chosen taking into account the maximum peak current, flowing through them during surge:
ID1=ID2=ID3=ID4=Isurge/4=Vsurge/42Ω/4=6000/42/4=35.7A.

The four inductors must be chosen considering the delay of the input bridges to open, when the reverse current flows, during Surge injection:
lower delay means less inductance and smaller dimensions;
the inductors must be dimensioned taking into account the current flowing on the lines, at the maximum application load.

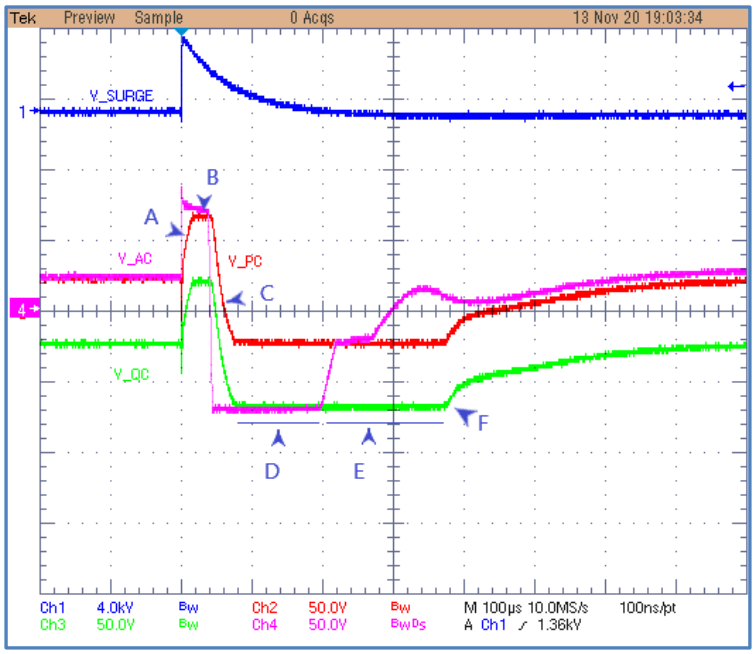
Fig.27 and Fig.28 show the behavior of the circuit during the 4 kV Surge, along the time following the Surge.

Figure 27. 4 kV surge on STEVAL-POE002V1.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_AC voltage;
Ch3 green trace, 50V/div, V_BC voltage;
Ch4 purple trace, 10A/div, ID2 current;
R4 brown trace, 10A/div, ID1 current.

Figure 28. 4 kV surge on STEVAL-POE002V1.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 50V/div, V_PC voltage;
Ch3 green trace, 50V/div, V_QC voltage;
Ch4 purple trace, 50V/div, V_AC voltage.

Looking at Fig.27, Fig.28 and Fig.17, it is possible to analyze the following events:

before the Surge injection, capacitors C1 and C2 (C3 and C4 also) are charged to a voltage V_AR=(V1)/2=48/2=24V and V_BS=-(V1)/2=-24V, while V2=V_SURGE=V_ST=V_RT=0V;
C1 and C2 have a voltage difference (V_AR)-(V_BS)=V_AB=48V;

during the first part of the Surge (Fig.27_A), along the previously explained currents course, it is necessary to consider that inductors L1 and L2 (L3 and L4 also) are subject to a voltage V_AP and V_BQ;
TVS1, TVS2, TVS3, TVS4, D1, D2, D3, D4 threshold voltage is 68 V;

during the Fig.27_A time lapse, TVS1, D1 and D2 (TVS3, D3, D4 also) go into conduction, after an initial transition (see Fig.28_A);
after that transition (see Fig.28_B), the voltage V_AP=(V_AC)-(V_PC) is very low;
but V_BQ=(V_BC)-(V_QC) is higher than 50 V, because V_AB=0 (points A and B are to the same potential);

during the Fig.27_A time lapse, IL1 and IL2 increase, both flowing through TVS1, but IL2>IL1 because V_BQ>V_AP;
since V_AB=0, C1 and C2 equalize a part of their voltage difference, through R1 and R2;

the voltage transition in Fig.27_B, is due to the voltage reached by capacitors C1 and C2, that are charged by the two Surge currents flowing through R1 and R2, during the Fig.27_A time lapse;
after the voltage transition the two capacitors are discharged, because V_SURGE turns lower than capacitors voltage;
the transition of V_BC is systematically earlier than the transition of V_AC, because the voltage on capacitor C2 is higher than the voltage on capacitor C1, so V_SC is higher than V_RC;
the little delay between V_BC and V_AC transition is the time necessary for V_SURGE to reach V_RC level;

during the Fig.27_C time lapse, capacitors C1 and C2 discharge following V_SURGE fall;
TVS1 opens, TVS2 reaches its -68 V voltage threshold, ID1 and ID2 change direction;

along the same time, after the transition of Fig.28_C, inductor L1 is subjected to V_PQ=(V_PC)-(V_QC)=48V, for the Fig.28_D time lapse;
L1 reverses its current and increases it through some paths, TVS2, L2, D1 and D2;
the currents flowing through L2 remain constant, flowing through several paths L1, D1 and D2;

since V_AB=0V again, C2 and C1 continue to equalize their voltage, through D1 and D2;

ID2 is systematically higher and longer than ID1;
ID2 is higher and longer because IL1, IL2 and the equalization current of C1 and C2 are summed into D2 and subtracted into D1;

at Fig.27_D point, IL1 becomes higher than the current flowing through C1 and ID1=0;
IL1 discharges C1 during the Fig.27_E time lapse and the voltage V_AB reaches V1=48V;

during Fig.27_F time lapse, a part of IL1 switches from C1 to the board input bridge, IL2 switches from D2 to the board input bridge, ID2 decrease to zero until Fig.27_G point;

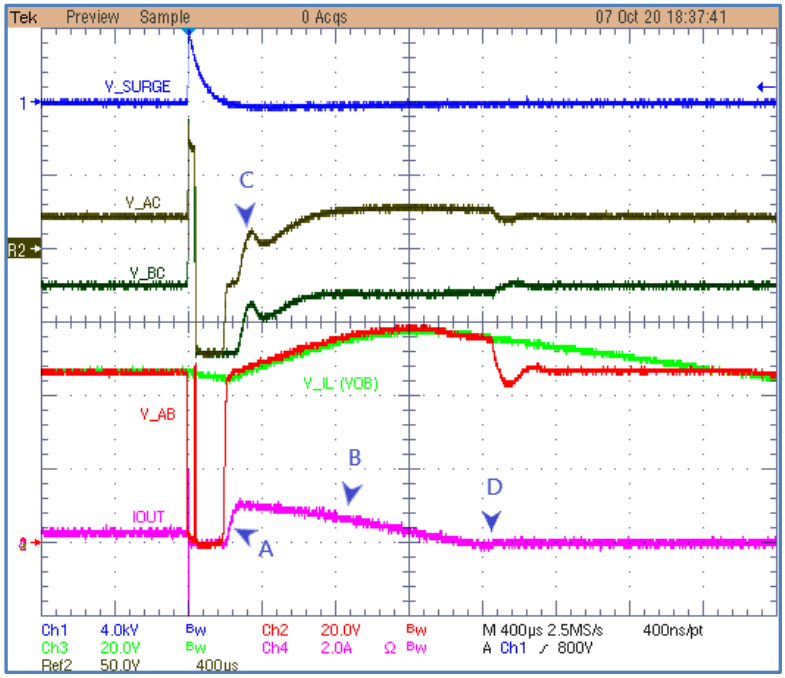
during the Fig.28_E time lapse, the TVS2 still conducts a part of IL1, through C1, until Fig.28_F point (IL1>IL2 because L1 was subjected to V_PQ=48V for Fig.28_D time lapse);

at Fig.28_F point, IL1=IL2 and flows to the board capacitor discharging the energy stored by L1 and L2;

after Fig.28_F point, C1 and C2 finish their stabilization through R5 and R6.

Looking at Fig.29, it is possible to see the complete Surge event.

Figure 29. 4kV surge on STEVAL-POE002V1.



Ch1 blue trace, 4kV/div, V2 surge voltage;
Ch2 red trace, 20V/div, V_AB voltage;
Ch3 green trace, 20V/div, V_IL (VOB) voltage;
Ch4 purple trace, 2A/div, IOUT current;
R2 brown trace, 50V/div, V_AC voltage;
R4 dark green trace, 50V/div, V_BC voltage.

The voltages at the bridge input V_AB and on the output (VOB) are displayed;
the output current IOUT is also present.

VOB decreases when the input voltage is zero, during the Fig.27_A and Fig.27_C time lapses;

at Fig.29_A point, the switching of IL1 and IL2 (IL3 and IL4 also) from the other paths to the input bridges is shown;

during the Fig.29_B time lapse, L1 and L2 give their energy to the board capacitors C6 and C7;

the elongation of V_AC and V_BC at Fig.29_C point, is due to the presence of L5 and L6, that react to the current variation of point A;

at the Fig.29_D point, the energy of Inductor L1 and L2 is finished;
after that, the voltage VOB decreases to its normal value and the Surge effects are completed.

Since during the Fig.29_B time lapse, the VOB voltage increases depending on the board output load, it is necessary to foresee D5 TVS, to avoid possible overvoltage on the PM8805 input and output pins.

Support material

Related design support material
Evaluation board – STEVAL-TSP004V2, 5 V/4 A, synchronous flyback converter, Power Over Ethernet (PoE) – IEEE 802.3at compliant reference design
Evaluation board – STEVAL-POE002V1, 5 V/8A, synchronous flyback converter, Power over Ethernet (PoE) IEEE 802.3bt compliant reference design
Documentation
Datasheet DS7139, High-efficiency, IEEE 802.3at compliant integrated PoE-PD interface and PWM controller
Datasheet DS12813, IEEE 802.3bt PoE-PD interface with embedded dual active bridge
Data brief DB2569, 5 V/4 A, synchronous flyback converter, Power over Ethernet (PoE) – IEEE 802.3at compliant reference design
Data brief DB3628, 5V/8A, synchronous flyback converter, Power over Ethernet (PoE) IEEE 802.3bt compliant reference design

Revision history

Date	Version	Changes
11-Feb-2022	1	Initial release

Contents index

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