DT0121
Design tip

How to configure the BlueNRG-1 and BlueNRG-2 devices in network coprocessor mode

Main components	
BlueNRG-1	Bluetooth Low Energy wireless system-on-chip
BlueNRG-2	Bluetooth Low Energy wireless system-on-chip

Purpose and benefits

The BlueNRG-1 and BlueNRG-2 are very low power Bluetooth low energy (BLE) single-mode system-on-chip (SoC), compliant with Bluetooth specification. They extend the features of award-winning BlueNRG network processor, enabling the usage of the embedded ARM Cortex-M0 for running the user application code.

The BlueNRG-1 and BlueNRG-2 devices can be also configured as a network coprocessor. In this scenario the device will be connected to an external host processor (e.g. STM32 microcontrollers). User application will run on the host processor, while the BlueNRG-1 and BlueNRG-2 devices will handle the Bluetooth low energy connectivity.

A specific application, named DTM (direct test mode), allows to configure the BlueNRG-1 and BlueNRG-2 devices as a network coprocessor.

Two options are available for the transport layer: SPI or UART interface.

The DTM application source code and documentation is available in the BlueNRG-1 and BlueNRG-2 software development kit (SDK) for a specific hardware configuration that matches the official products evaluation platforms, i.e. STEVAL-IDB008V2 and STEVAL-IDB007V2.

In the documentation section of the device SDK developers can also find the details related to the SPI protocol for communicating with the BlueNRG-2 device using this specific network coprocessor mode.

The purpose of this design tip is to provide customers with guidelines on how to modify the reference DTM application for running on a custom printed circuit board (PCB).

The entire content of this design tip applies both to BlueNRG-1 and to BlueNRG-2 devices with no modifications. For simplicity, we will refer to the BlueNRG-2 device in the following sections of the document.

Description

In order to configure the BlueNRG-2 device as a network coprocessor, the device shall be programmed with a specific application, named DTM (Direct Test Mode).

In the device SDK the source code for this application can be found in the path “\Project\BLE_Examples\DTM”.

Two different transport layers are available to configure BlueNRG-2 device as a network coprocessor: UART and SPI.

The reference application project supports both these transport layers with dedicated project configurations.

SPI interface

The default DTM application for the SPI interface makes use of the following pins:

SPI CLOCK	IO0
SPI MOSI	IO3
SPI MISO	IO2
SPI CS	IO11
SPI IRQ	IO7
BLUENRG-2 BOOT (1)	IO7
BLUENRG-2 RESETN	RESETN

Note (1): BLUENRG-2 BOOT pin to be connected only for bootloader mode

Developers can reconfigure these pins (except for the BOOT and RESETN pins) depending on the specific PCB electrical schematics. The mapping of the SPI interface on the BlueNRG-2 device pins can be found in the datasheet in the Table 128 “IO functional map”.

In the source code, these pins are defined in the header file *hw_config.h*.

UART interface

The default DTM application for the UART interface makes use of the following pins:

UART RX	IO11
UART TX	IO8
UART RTS	IO6
UART CTS	IO13
BLUENRG-2 BOOT (1)	IO7
BLUENRG-2 RESETN	RESETN

Note (1): BLUENRG-2 BOOT pin to be connected only for bootloader mode

Developers can reconfigure these pins (except for the BOOT and RESETN pins) depending on the specific PCB electrical schematic. The mapping of the UART interface on the BlueNRG-2 device pins can be found in the datasheet in the Table 128 “IO functional map”.

In the source code, these pins are defined in the header file *hw_config.h*.

Note that 2 different configurations are available for the UART interface: UART_16MHz and UART_32MHz. Developers should select the proper configuration corresponding to the High Speed Crystal Clock frequency selected on the PCB (the BlueNRG-2 device supports either 16 or 32 MHz clocks).

UART Bootloader

The BlueNRG-2 device embeds a pre-programmed bootloader accessible over a UART interface. The bootloader is an application stored on the BlueNRG-2 internal ROM at manufacturing time by STMicroelectronics.

The Application Note AN4872 contains the specifications of the BlueNRG-2 UART bootloader protocol.

The UART bootloader HW interface is briefly described here below.

The bootloader is accessible from a UART interface ONLY on the device pins IO8 and IO11 (refer to the device Datasheet).

The UART bootloader is activated by hardware forcing high IO7 pin at device reset. Once the bootloader is activated, the code starts a procedure to auto-detect the host processor UART baud rate and begins to scan the UART RX line pin.

If the user needs to configure the BlueNRG-2 device as a network coprocessor over the UART interface, it is then recommended that the UART interface selected for the network coprocessor mode is aligned to the UART bootloader interface, i.e. IO8 and IO9 as UART TX and UART RX lines (TX and RX functionalities from the BlueNRG-2 perspective). Also it is recommended that the Boot pin (IO7) to be connected to the external host processor. Note that the developer’s application must ensure that IO7 is forced low during power up in order not to boot the device in updater mode.

Sleep mode with the DTM application

The reference DTM application allows the BlueNRG-2 core to enter sleep mode through the following API call:

BlueNRG_Sleep(sleepMode, gpioWakeBitMask, gpioWakeLevelMask)

where

- *sleepMode* is the selected device sleep mode (for more details refer to AN4820)

- *gpioWakeBitMask* is a bit mask of the IO pins that are allowed to wake the device from deep sleep. A high bit in the mask will enable waking the device if the corresponding IO pin changes state.
- *gpioWakeLevelMask* is a mask used to setup the active wakeup level:
    - 0: the BlueNRG-2 core wakes up when IO is low
    - 1: the BlueNRG-2 core wakes up when IO is high

The default wakeup pin is IO11 for the SPI interface (CS line) and IO13 for the UART interface (CTS).

For both the options the wakeup level is the low level (the BlueNRG-2 core wakes up from deep sleep mode when the selected wakeup line is at low level).

If the developer wants to change the CS or CTS default pin configuration, care must be taken in selecting a valid pin among the device's wakeup pins. As a consequence, the sleep management API input parameter *gpioWakeBitMask* and *gpioWakeLevelMask* should be modified accordingly to the hardware platform requirements. Note that the wakeup pins of the device are IO9, IO10, IO11, IO12, and IO13.

Host Processor reference applications

Refer to the BlueNRG-2 SDK for source code applications running on an external host processor. The reference host processor device is a STM32L1xx microcontroller.

Four reference applications are available in the BlueNRG-2 SDK:

- "BLE Beacon": configures a beacon device
- "BLE Chat Master & Slave": allows to implement a BLE Chat application scenario
- "Sensor Demo": emulated acceleration and environmental sensors values
- "DTM": allows to use the BlueNRG GUI tool

Connecting the BlueNRG Graphical User Interface (GUI)

The STSW-BNRGUI software package (BlueNRG GUI) consists of a graphical user interface PC application that can be used to interact and evaluate the capabilities of both BlueNRG-2 and BlueNRG-1 devices.

The GUI PC application can send standard and vendor-specific HCI commands to the selected device and receive events from it. Commands and events can also be sent and received with scripts executed through the GUI script window.

When using the BlueNRG-2 device in network coprocessor mode, in order to use the BlueNRG GUI also the host processor device shall be programmed with a specific

application. This application implements a pass-through from a UART interface on the host processor (which is connected to the PC) to the blueNRG-2 device (over either UART or SPI interface between the host processor and the BlueNRG-2 device).

The source code for this host processor application example is available in the BlueNRG-2 SDK. The application is named DTM and it is the companion application of the DTM application running on the BlueNRG-2 device.

The default DTM host processor application runs on the STM32L1xx microcontroller. If the developer selects a different microcontroller, this application needs to be ported over the different host processor architecture.

BlueNRG-2 ST Eval kits

The official evaluation platforms for the BlueNRG-2 device are named STEVAL-IDB008V2 or STEVAL-IDB008V1, while for the BlueNRG-1 device the official evaluation platforms are named STEVAL-IDB007V2 or STEVAL-IDB007V1.

When the BlueNRG-2 or BlueNRG-1 device are configured in network coprocessor mode, the reference platform is Nucleo-L152RE and STEVAL-IDB008V2 (or IDB008V1) for the BlueNRG-2 device or Nucleo-L152RE and STEVAL-IDB007V2 (or IDB007V1) for the BlueNRG-1 device.

Within the device SDK specific documentation is available for describing the connections between the Nucleo-L152RE microcontroller board and the BlueNRG-2 (or BlueNRG-1) evaluation platforms.

Both the UART protocol implementation and SPI protocol implementation details are described.

Support material

Documentation
Datasheets: BlueNRG-1 BlueNRG-2 Programming Manual: PM0257: BLE stack programming guidelines Application Notes: AN4820: BlueNRG-1 and BlueNRG-2 low power modes AN4872: BlueNRG-1 and BlueNRG-2 UART bootloader protocol
Embedded Software: STSW-BLUENRG1-DK: BlueNRG-1, BlueNRG-2 DK SW package STSW-BNRG_V1-DK: BlueNRG-1 DK SW package for BLE stack family v1.x STSW-BNRGUI: BLUENRG family GUI

Revision history

Date	Version	Changes
27-Sep-2018	1	Initial release

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