DT0039
Design tip

Improving measuring accuracy and EFT immunity for STPM3x applications

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Main components	
STPM32	ASSP for metering applications with up to four independent 24-bit 2nd order sigma-delta ADCs, 4 MHz OSF and 2 embedded PGLNA
STPM33	
STPM34	

Purpose and benefits

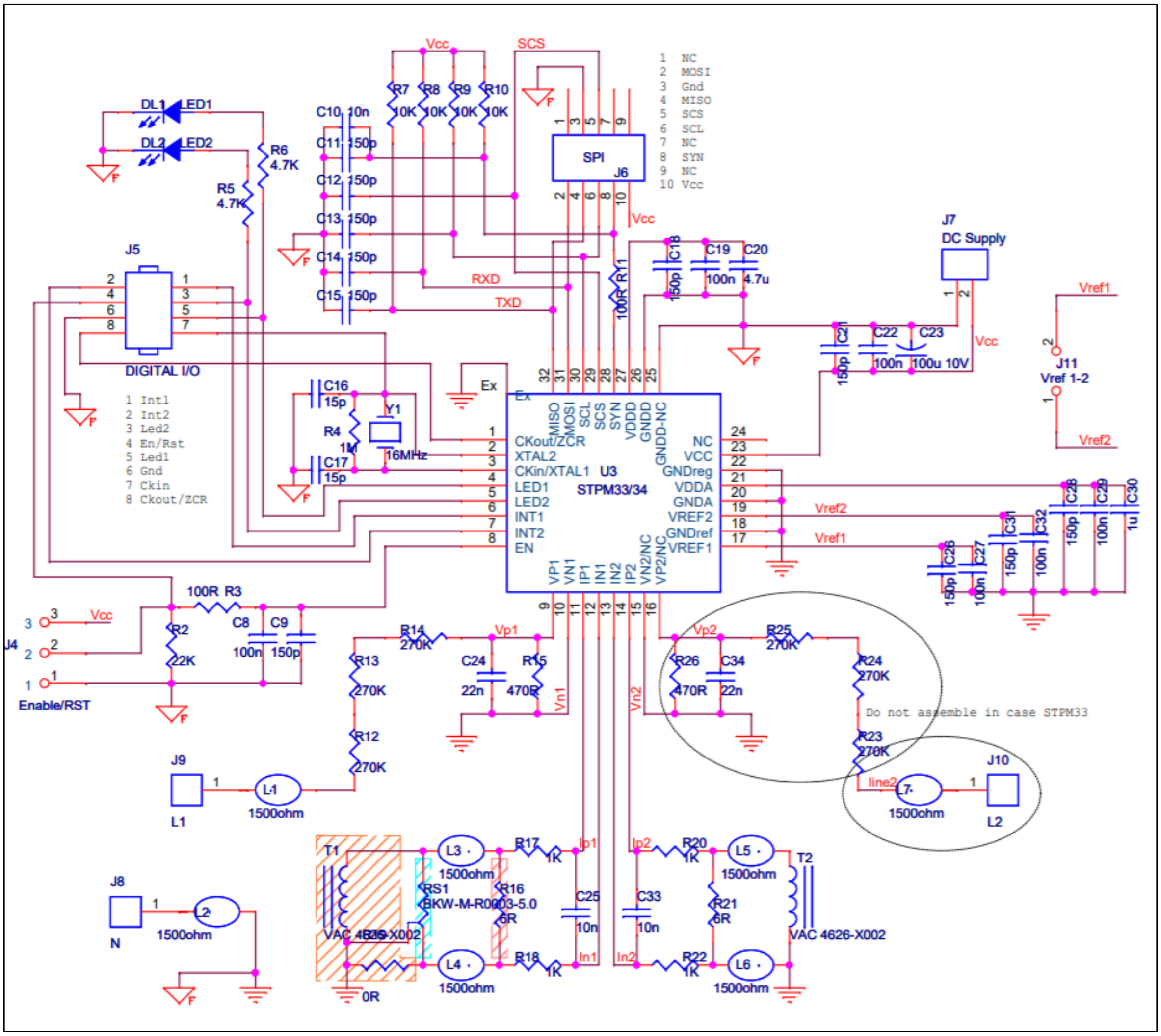
STPM3x devices have been designed for energy metering application. Their application boards usually works in harsh environments: they are connected to the AC electric energy distribution utility from one side and to the home appliances to the other side. For this reason they are subjected to huge electrical fast transient (EFT) spikes. In addition, due to the architecture of the measuring circuitry they have to measure very low amplitude signals with a very good accuracy in a continuous dynamic signal change.

Therefore, good PCB rules have to be followed in order to guarantee measuring accuracy and to keep the application operation working in the presence of EFT disturbances.

PCB tips help to keep a good measuring accuracy

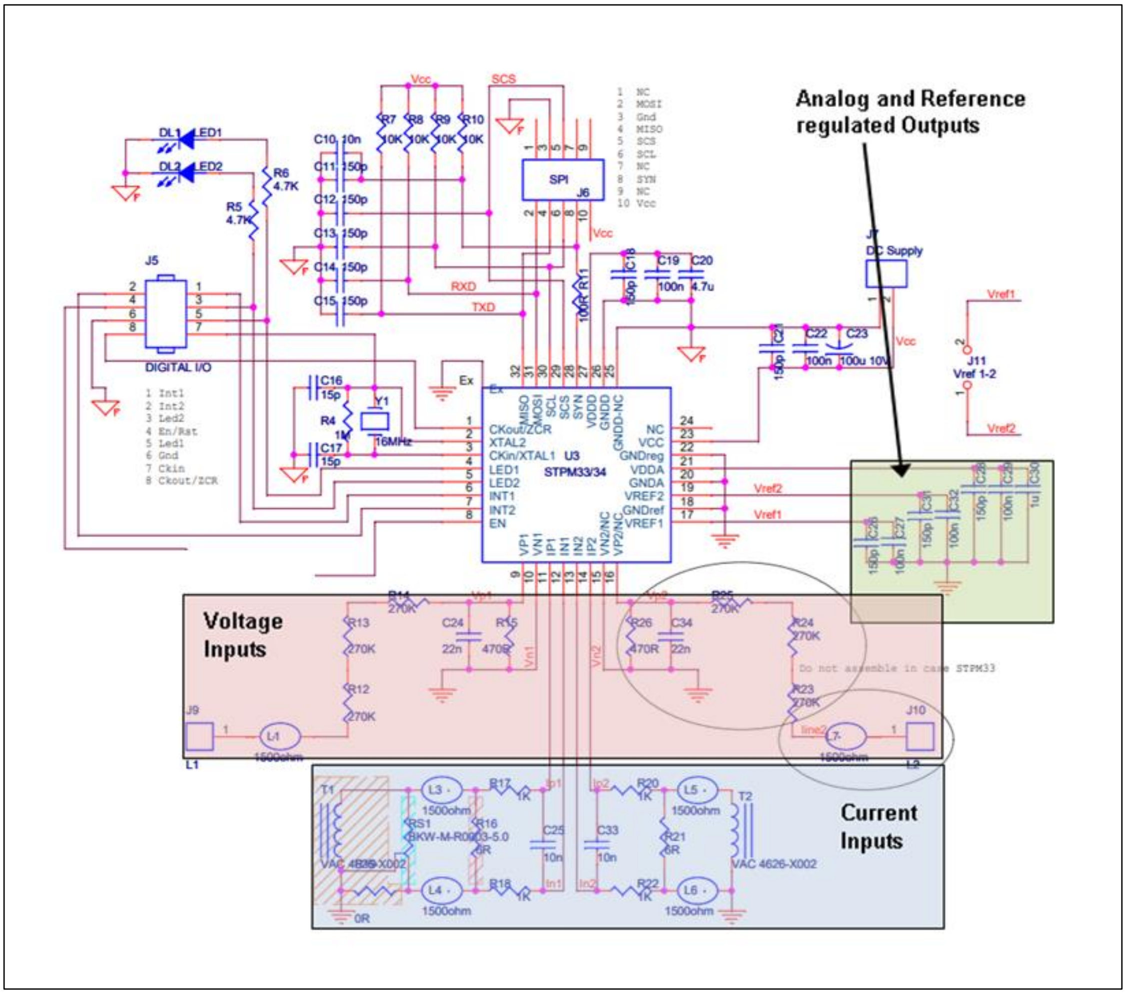
As a typical example of an application with the STPM3x devices, let’s consider the schematic of our evaluation boards:

Figure 1. Typical circuit diagram



It is possible to identify its main critical blocks:

Figure 2. Circuit critical blocks



The highlighted blocks are:

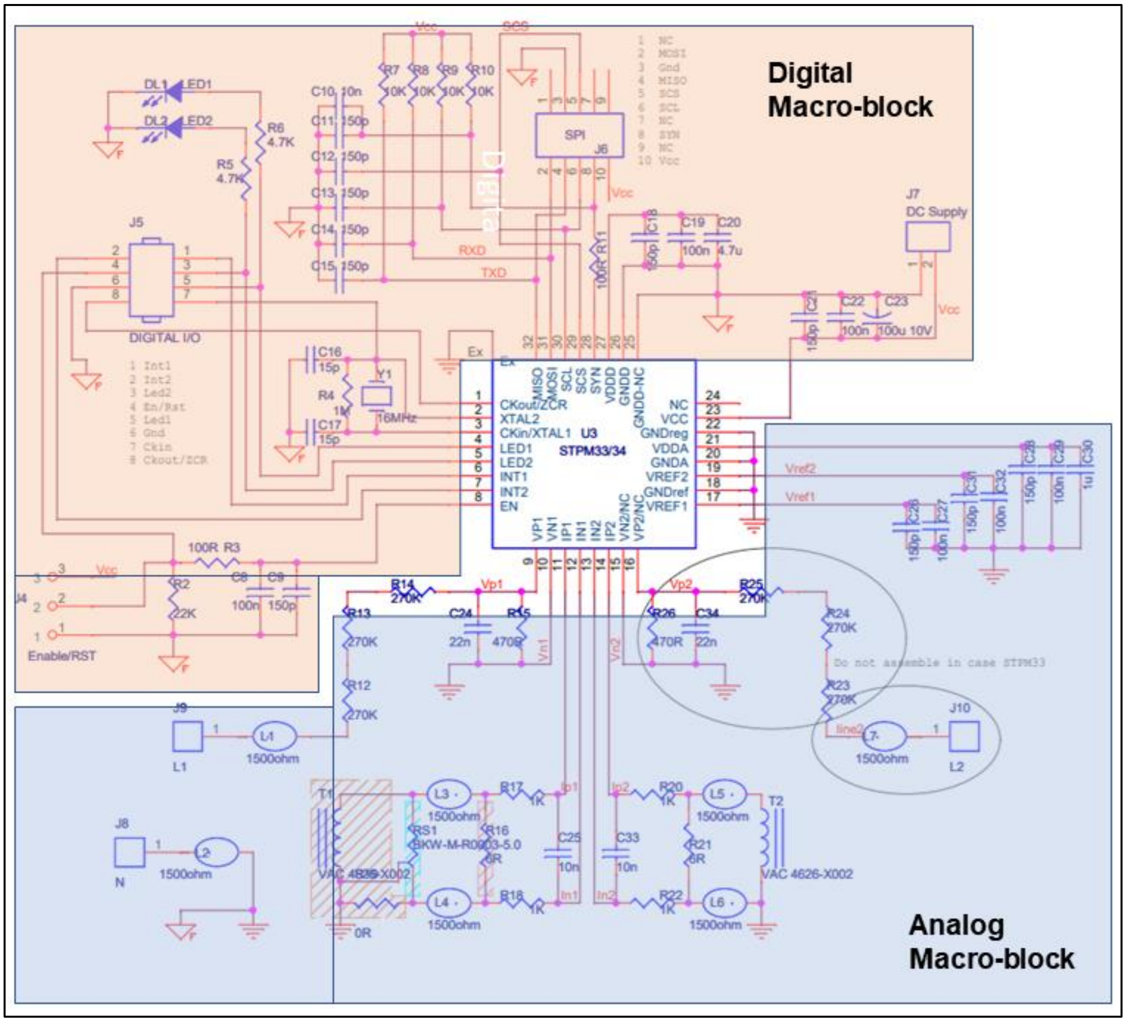
The current measuring block: it includes the current sensors (shunts CTs, RoCoils) and the ADC anti-aliasing filters. The AC current consumed by the appliances is transduced into a voltage signal and applied to the STPM3x ADC current inputs.

The voltage measuring block: it includes the voltage divider resistors and the ADC anti-aliasing filtering capacitor. The voltage provided by the utility network is scaled down to a safe and lower voltage signal and applied to the STPM3x ADC voltage inputs.

The analog and reference regulated outputs block: the STPM3x internal analog section is supplied by a low-drop voltage regulator (VDDA), whose output needs an external filtering capacitor. The ADC references can be selected as internal or external, for each primary and secondary channel; in the case of external selected, the reference voltage can be fed through the Vref1 and/or Vref2 input. In the case of internal selected, the Vref1 and/or Vref2 are outputs for external filtering capacitor(s).

All these three blocks can be grouped into one single macro-block, called Analog Block. The rest of the schematic contains other functional blocks, like oscillator, communication interface, main supply voltage, etc…, that can be grouped into a Digital macro-block.

Figure 3. Circuit Macro-blocks



The most important actions to keep an overall good accuracy have to be applied to the analog macro block. They are:

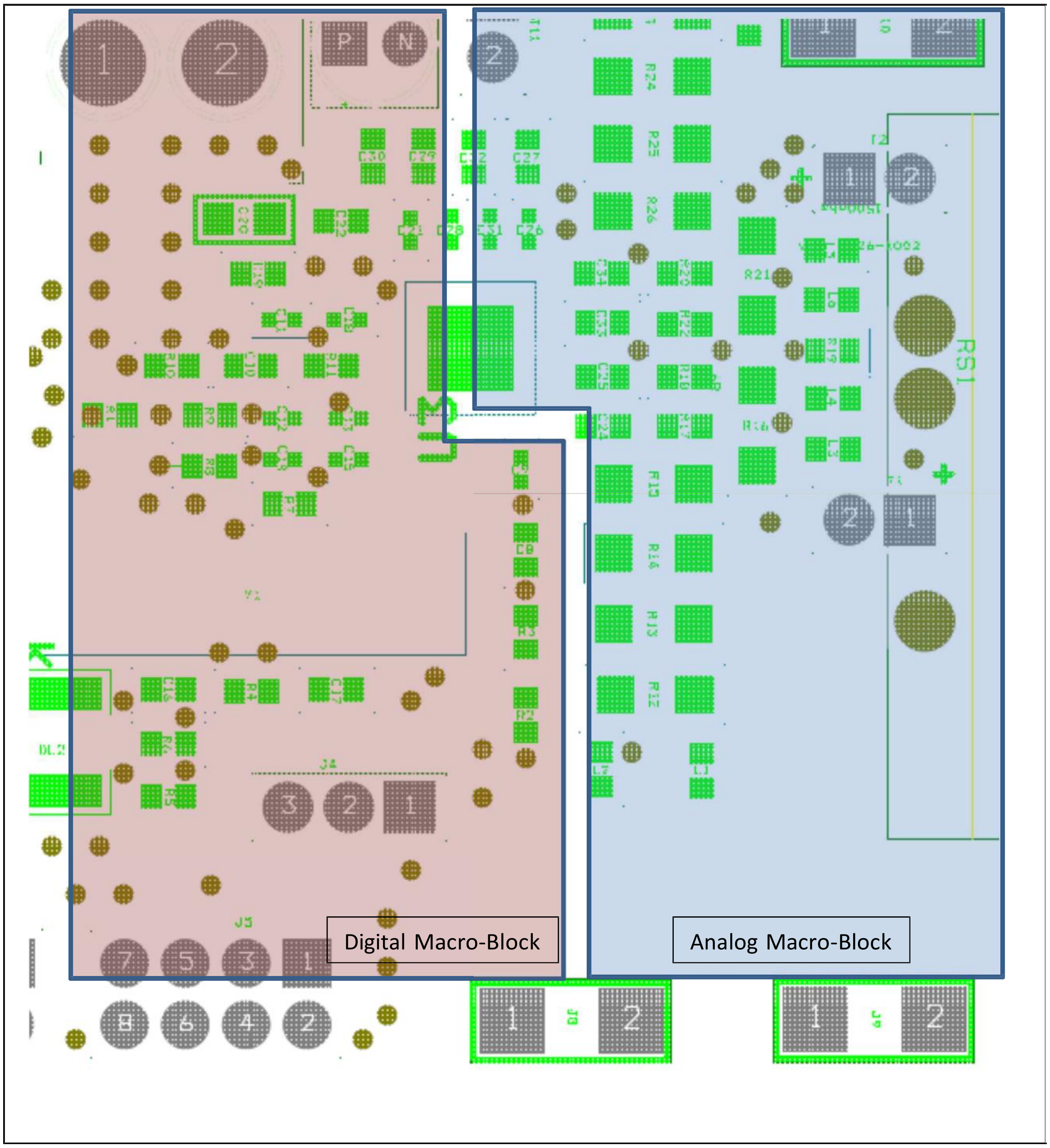
- To keep all the sensors and components as close as possible to the STPM3x analog measuring inputs, as well as the filtering capacitors to each regulated/reference pin. Maybe, the upper branch of each voltage divider (that consists of three or four resistors) requires more room due to high voltage constraints. In this case, to keep the lower resistors (R5 and R19 in the schematic) closer to the input pins is sufficient.

- To keep sufficient room between the analog and digital macro-blocks.

Another optimal improvement is the separation of the board ground into two PCB ground planes. The first surrounds and lays down the components of the analog macro-block, the second does the same for the components of the digital macro-block. Both ground planes have to be joined together in the correspondence of the STPM3x exposed pad (each STPM3x chip is enclosed in a QFN package which has a large square pad which lays exactly down the chip and is electrically connected to the device ground pins).

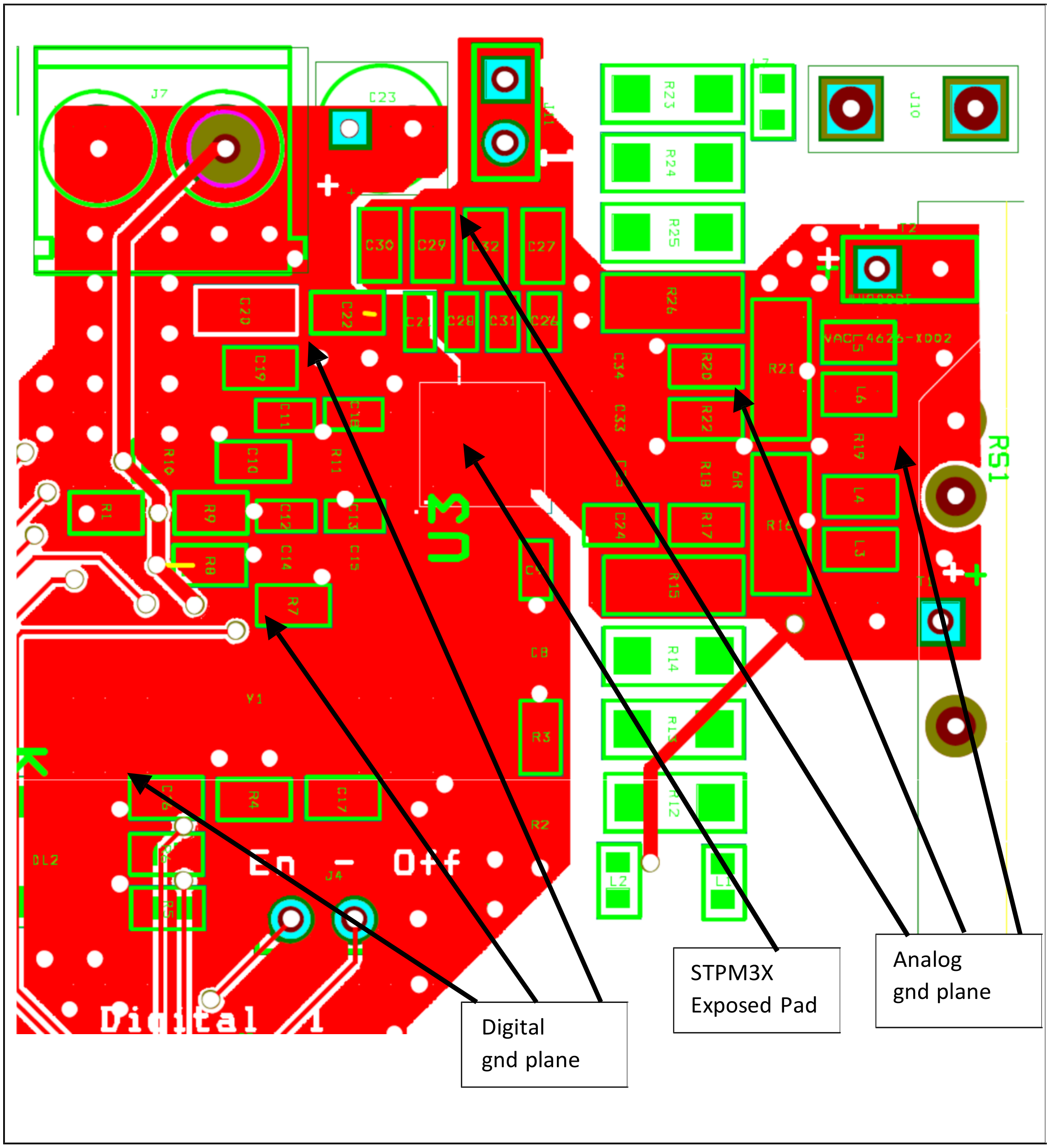
A good design tip could be to design the PCB layout following (as much as possible) the same placement of the components of the given schematic. The result is the creation of two “L” shaped regions and related gnd planes for the above macro-blocks. As an example, here below it is the PCB component placement for the STPM3x evaluation boards:

Figure 4. Macro-blocks in a STPM3x evaluation PCB



And below there is the PCB ground planes that lays in the bottom layer:

Figure 5. PCB ground planes



The digital ground plane (on the left) gets in contact with the analog ground plane just below the STPM3x, by means of its exposed pad.

PCB tips help to improve EFT immunity

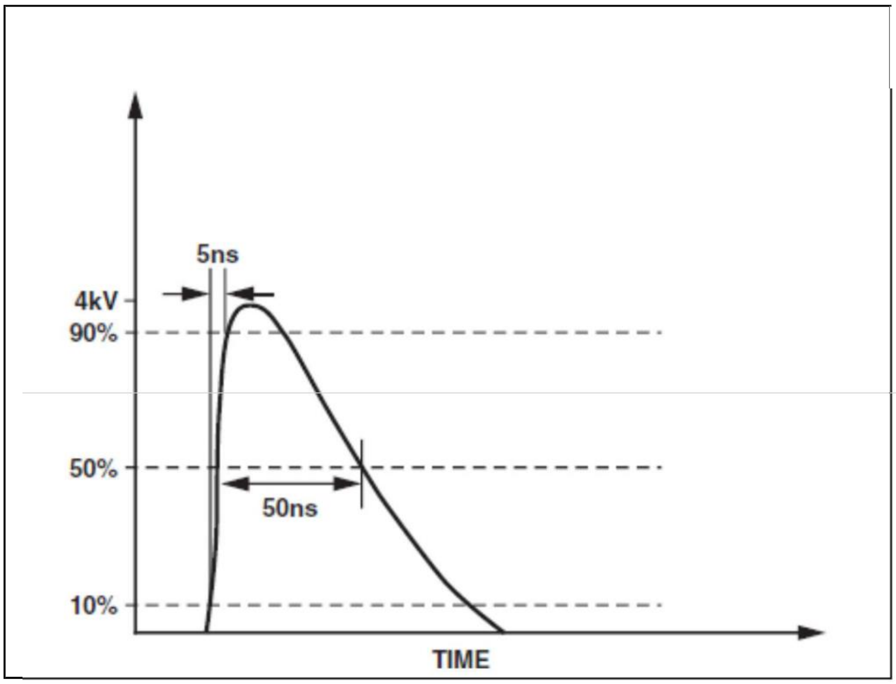
Due to the environment where energy meters operate, they often face with the problem of electrical fast transient (EFT) bursts. Such kind of disturbances, due to the high-frequency noise and high voltage amplitude can affect the normal operation and sometimes damage the electronic components. Energy meters must withstand EFT bursts without damage, loss of operation and/or loss of measurement accuracy.

In order to comply with these restrictions, energy meters are submitted to standard EFT tests, like the IEC-61000-4-4 test. The characteristics of this test are:

- Fast repetition of bursts of pulses
- Max. energy is 4mJ/pulse at 2KV (50ohm impedance)
- Pulse rise time is 5ns
- Pulse duration is 50ns (50% amplitude)

Here below, the amplitude vs time shape of a single pulse

Figure 6. Typical IEC61000-4-4 EFT pulse shape



The bursts are applied to the power lines with the energy meter connected to the energy utility and the current load. Therefore, the bursts enter the energy meter via the voltage and current sensing circuitry (the voltage divider and the current sensor, especially the shunt sensor which is a non-isolated transducer), but, the high-frequency content of each pulse allows them to couple to other parts of the application through stray capacitance; due to temporary voltage bounces, large differential signals can be generated by inductance of PCB tracks and signal ground. For the digital section of the application, which is responsible for programming and data transferring, this can lead to an undesirable loss of operation because of data corruption.

Like in the previous chapters, the actions that can be put in place against the EFT issue can be split into two separate groups for the analog and the digital blocks of the STPM3x applications:

Analog block: the easiest way is to reduce the bandwidth so that the high frequency content of the EFT can be arrested. The required bandwidth for the energy meters is quite low, it often does not exceed the 50th harmonics of the power line frequency (about 3KHz@60Hz line), then it can be limited without affecting the measurement performance. The anti-aliasing filters avoid the high-frequencies to reach the analog inputs. To increase the immunity, the internal analog voltage regulator and the voltage reference output pins have small capacitance capacitors in addition to the medium and high ones. Further protection could be added by putting SMD ferrite beads in series to each analog input, but several EFT tests performed on STPM3x show ferrite beads are not necessary.

The real improvement comes from an accurate PCB layout design that, basically, should follow the same rules and tips like for accuracy improvement: components very close to the inputs and separate analog ground plane surrounding all the sensitive components.

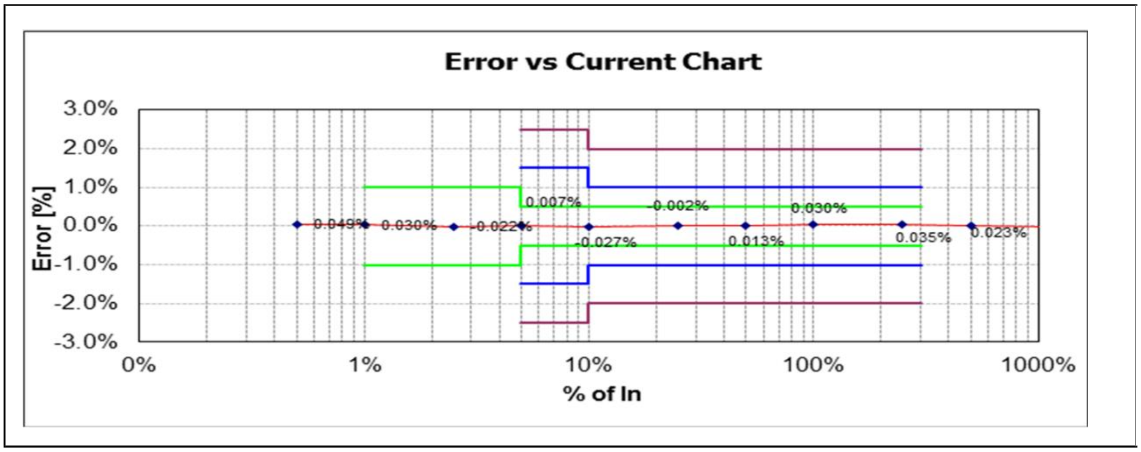
Digital block: since the EFT pulses can corrupt data information and can lead the Digital Signal Processing unit to an inoperative or unpredictable functional state, EFT tests performed on STPM3x boards show that the communication port terminals must be protected by filtering high-frequency spikes. This has been implemented by adding R-C filters to those terminals. Those filters should be placed close to the STPM3x input pins, rather than the port connectors (UART or SPI headers). Due to its specific function, the EN pin needs a stronger filter, so that EFT cannot cause accidental reset, with loss of configuration. Additional small capacitance capacitor ensures immunity also for the internal digital voltage regulator.

Also in this case, the separation of the digital and the analog blocks and the addition of a surrounding ground plane helps to prevent loss of operation, minimizing the cross-conduction of high-frequency noise across stray ground loops.

Conclusions

The PCB rules described above have been followed during the design of STPM3x demo-boards. After the implementation of those rules, accuracy tests and EFT immunity tests show excellent results. Here below a typical accuracy chart: X-axis is the % of the nominal current; Y-axis is the error between measured and supplied energy. Green, Blue and Brown shapes are the limits of the reference standards for 0.5, 1 and 2 accuracy classes:

Figure 7. Accuracy chart



EFT tests, in accordance with the IEC61000-4-4 standard show a correct device operation during and after the EFT injection up to and above 4KV pulse amplitude.

Support material

Related design support material
Product/ system Evaluation board – EVALSTPM32; EVALSTPM34; EVALSTPM35 http://www.st.com/st-web-ui/static/active/en/resource/technical/document/data_brief/DM00111800.pdf
Development kit –
Gerber files – EVALSTPM34_GERBER http://www.st.com/st-web-ui/static/active/en/resource/technical/layouts_and_diagrams/board_manufacturing_specification/EVAL-STPM34.zip
PCB layout, bill of materials and schematics files – EVALSTPM33/34_SCHEMATICS http://www.st.com/st-web-ui/static/active/en/resource/technical/layouts_and_diagrams/schematic_pack/33-34%20V2%20schematic.pdf EVALSTPM34_BOM http://www.st.com/st-web-ui/static/active/en/resource/technical/document/bill_of_materials/STPM34%20V2%20BOM.xls
Documentation
Datasheet STPM32, STPM33, STPM34 ASSP for metering applications with up to four independent 24-bit, 2nd order, sigma-delta ADCs, 4 MHz OSF and 2 embedded PGLNA

Related design support material
User manual, UM1719: The STPM3x evaluation software; UM1748: EVALSTPM34, EVALSTPM33, EVALSTPM32 evaluation board
Application note, AN4470: The STPM3x application calibration

Revision history

Date	Version	Changes
15-Sep-2014	1	Initial release
15-Nov-2021	2	Updated Figures 1, 2 and 3