DN0049
Design note

12 V 2 A not isolated buck converter, based on PM8803 PD controller, compliant to IEEE 802.3at PoE standard

Main components

List of ST components involved in the analysis.

Main components	
PM8803	High-efficiency, IEEE 802.3at compliant integrated PoE-PD interface and PWM controller
TL431AILT	Automotive adjustable voltage reference
STL30N10F7	N-channel 100 V, 8 A, STripFET Power MOSFET
STPS5H100SF	100 V, 5 A PSMC Power Schottky Rectifier

Specification

Parameter	Specs
VIN	32.5 V to 57 V
Auxiliary VIN AUXI	40 V to 60 V
Auxiliary VIN AUXII	40 V to 60 V
VOUT	12.00 V +/- 500 mV @ 2 A
Efficiency DC-DC only	91% typ. @ 12 V 2 A
Efficiency overall	90% typ. @ 12 V 2 A
Peak-To-Peak Output Ripple	250 mVpp
Switching Frequency	200 kHz typ. +/- 11%
Maximum Over/Undershoot	450 mV
Maximum Over/Undershoot Time Duration	200 µs
Dynamic Current Step	1 A to 2 A max. and back to 1 A
Ambient Operating Temperature Range	0 °o. to 30 °C

Application circuit description

This application circuit has been designed to demonstrate the capabilities of the PM8803, which is an interface compliant to the IEEE 802.3at PoE standard and it can be a smart controller for low cost, not isolated reverse buck converters.

This converter typology was selected to implement a simple driving method of the primary MOSFET, maintaining the ground reference as available in the PM8803.

In order to improve the overall efficiency, the classic diode bridges have been replaced with half active bridges, where N-channel power MOSFETS are used in place of low-side diodes.
The expected improvement is in the order of 1-2% on the overall efficiency, from mid to full output current.

The PM8803 does not embed the error amplifier, being designed for isolated applications; here a voltage reference TL431 is used as the external error amplifier.

The PM8803 embeds two drivers for MOSFET gates, but the first one (GAT1) is used only, as required by the reverse buck converter; the second driver (GAT2) is not used, and it is left open to avoid unjustified loss of power.

The application circuit implements two circuital workarounds useful to the best use of the PM8803.
The first one, relative to the classification process, avoids that the Powered Device (PD) logic is subject to a rare error condition, in the presence of very fast rising edges of the classification signal.
The second one, useful for type 2 PDs, guarantees the correct timing of the power sinking at the startup, in the case where the PD circuitry is not able to meet the 802.3at standard requirement.
A detailed description of each workaround can be found in two specific documents (design tips), see referenced docs listed in the support material section.

Figure 1. Application circuit diagram.

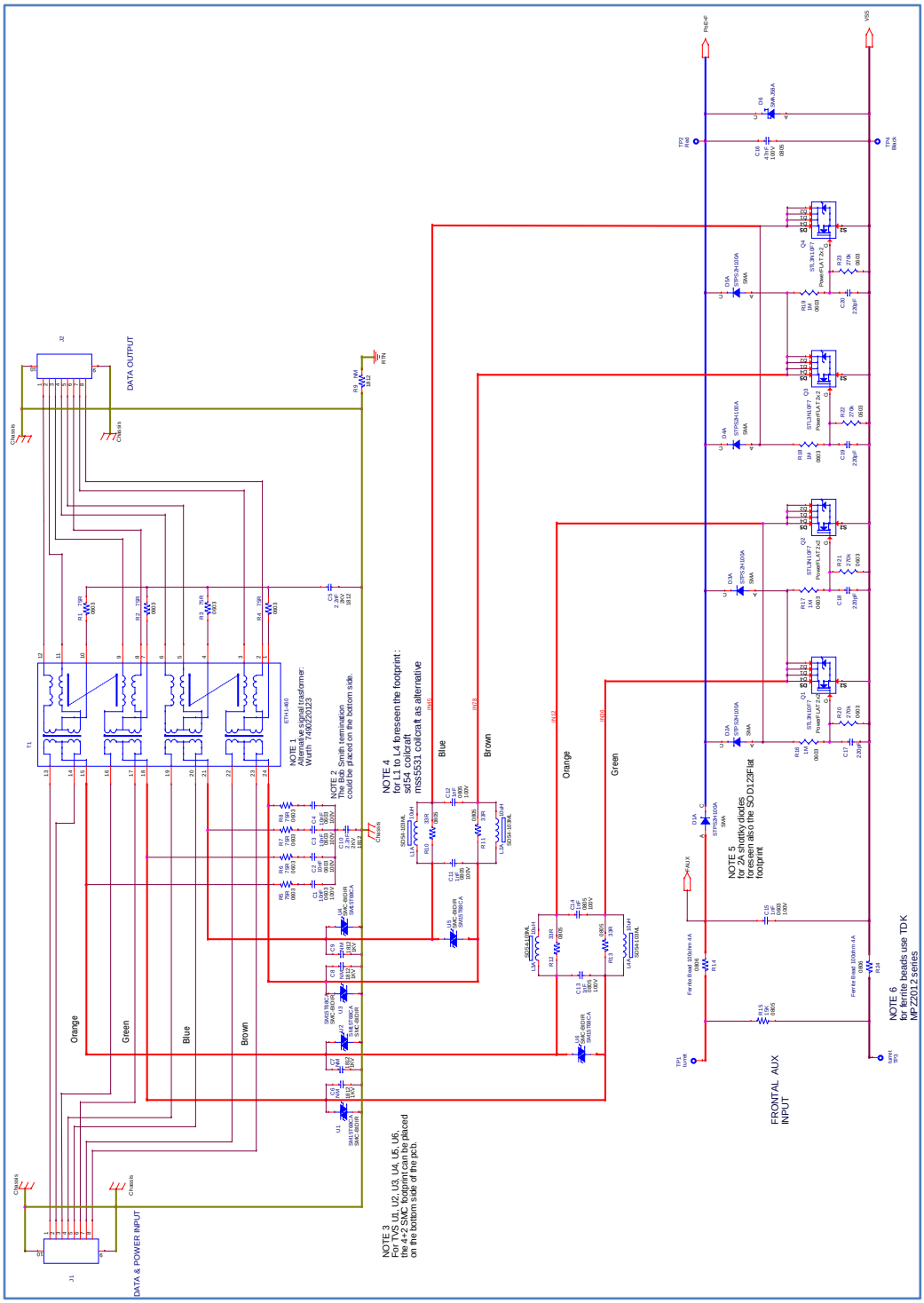
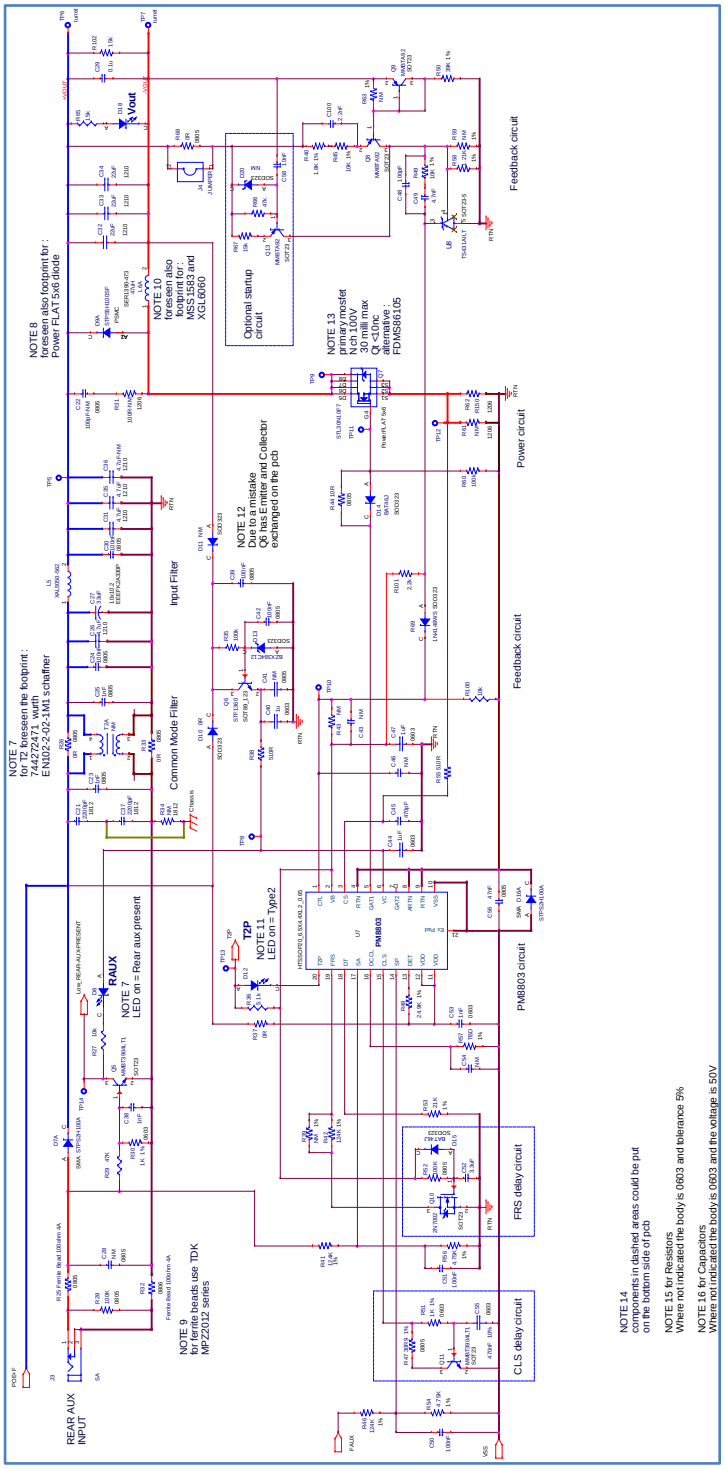


Figure 2. Application circuit diagram.



Prototype board

A dedicated prototype board was realized, for the purpose of testing the application circuit and to carry out the electrical measurements necessary to evaluate the circuit performances.

Following information regarding the board design, can be used as reference for other application circuit development.

Figure 3. Prototype board.

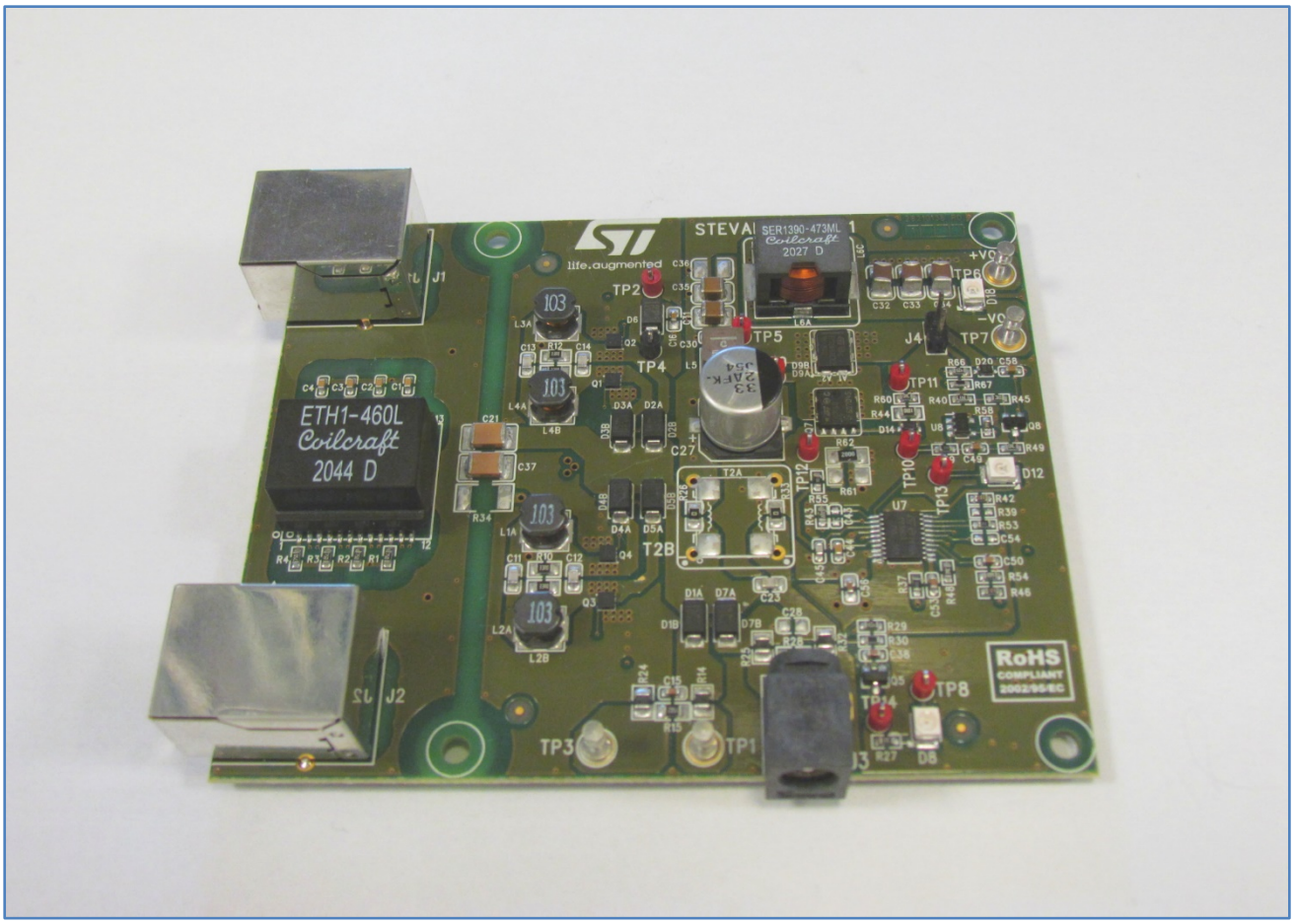
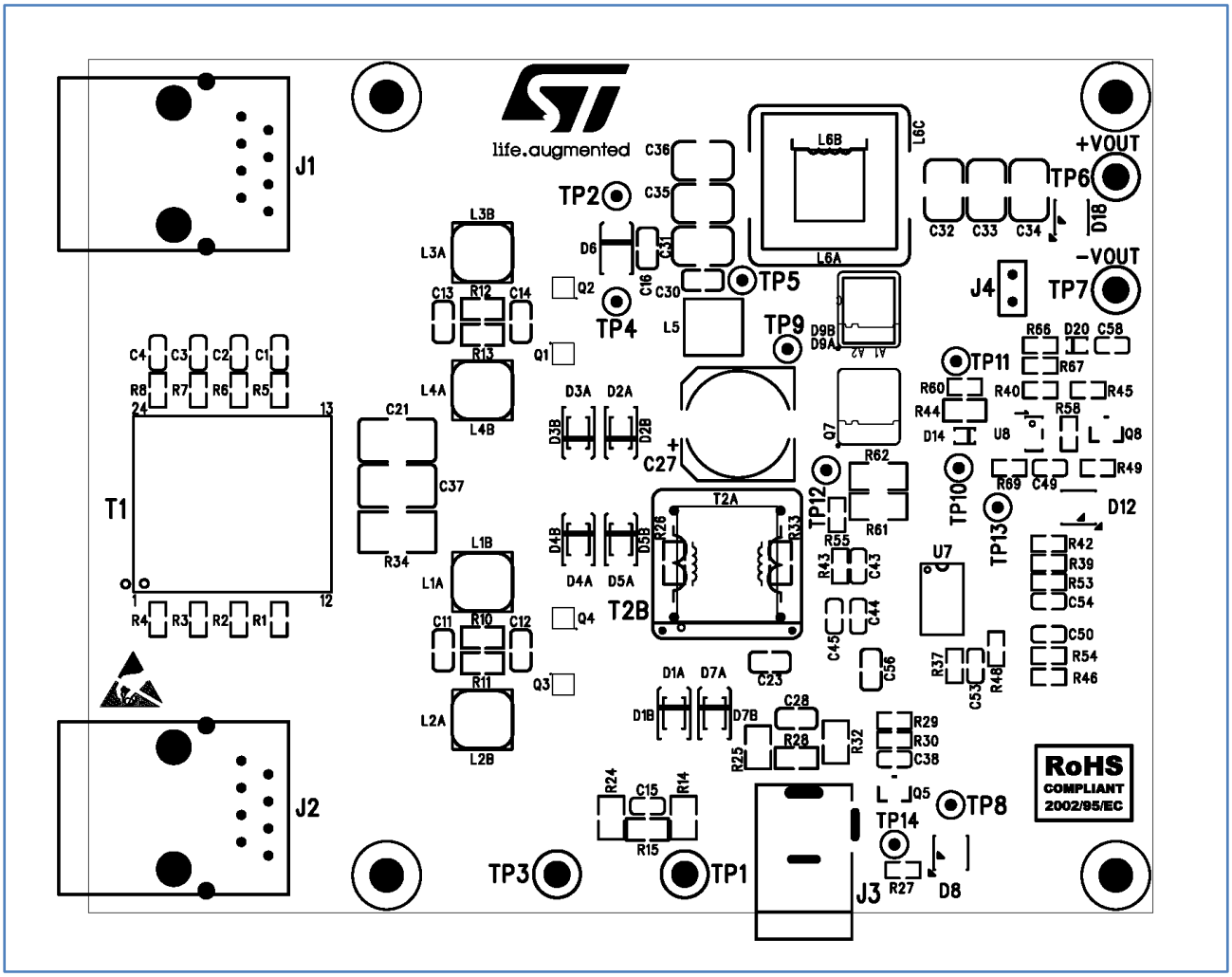


Figure 4. Prototype board top layer component layout.



Connection description

J1 is the RJ45 connector for PoE input, with data and power applied through the CAT5 cable.

J2 is the RJ45 data output connector.

TP1 + and TP3 – turrets are the input turrets for the Frontal Auxiliary input or AUXI.

J3 is the power jack for Rear Auxiliary input or AUXII.

TP6 + and TP7 – turrets are the board voltage output.

Figure 5. Prototype board bottom layer component layout.

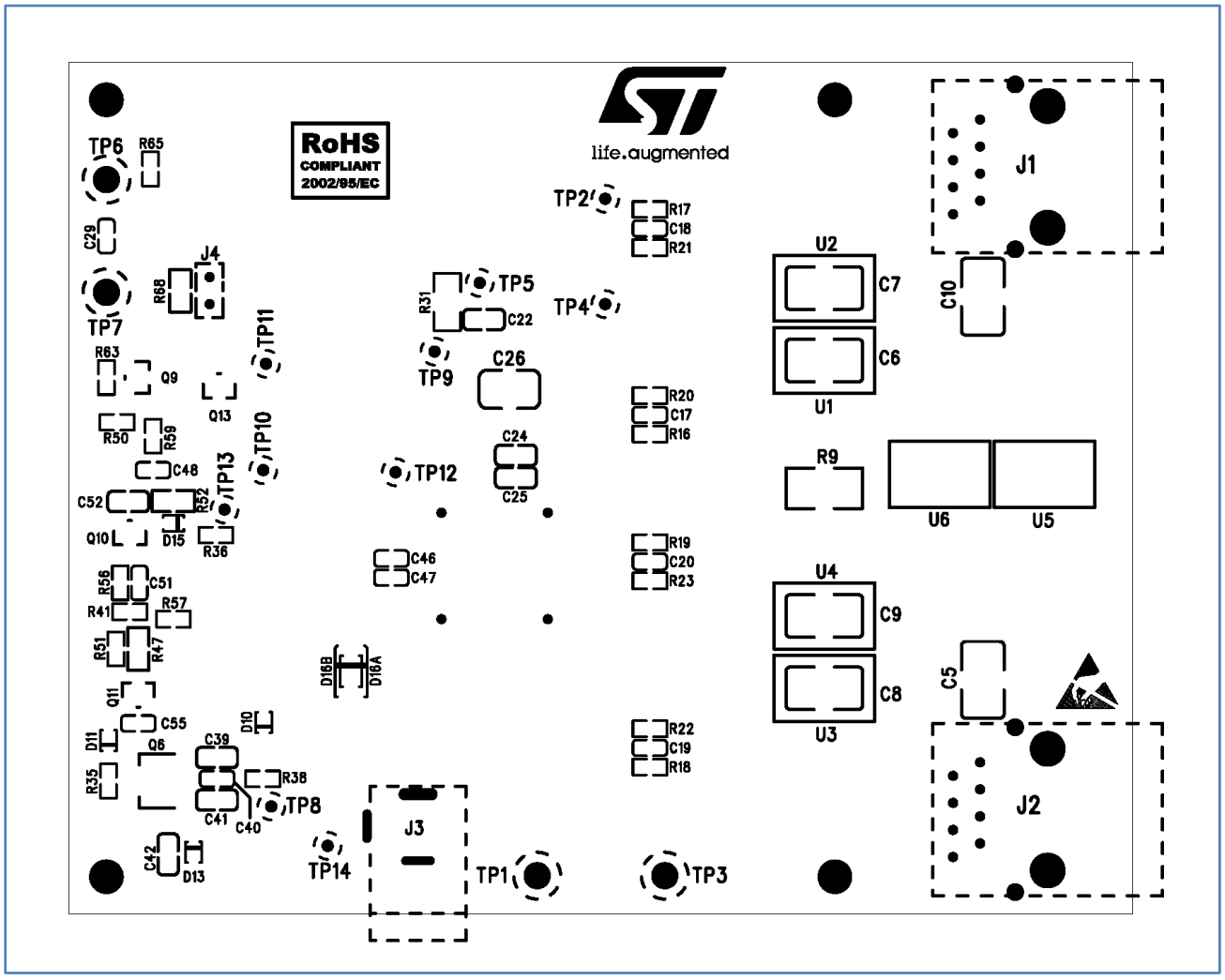


Table 1. Prototype board bill of material.

Q.ty	Reference	Value	Description	Package	Manuf. Code	Manufacturer
5	C1, C2, C3, C4, C58	10 mph 100 V	Ceramic Capacitor	0603	C0603C103K1RACTU	KEMET
4	C5, C10, C21, C37	2.2 nF 2 kV	Ceramic Capacitor	1812	C4532X7R3D222K130KA	TDK
4	C6, C7, C8, C9	NM		1812		
6	C11, C12, C13, C14, C23, C25	1 nF 100 V	Ceramic Capacitor	0805	GRM2195C2A102JA01D	MURATA
3	C15, C38, C53	1 nF 100 V	Ceramic Capacitor	0603	CGA3E2X8R2A102K080AD	TDK
2	C16, C56	47 nF 100 V	Ceramic Capacitor	0805	GRM21BR72A474KA73L	MURATA
4	C17, C18, C19, C20	220 pF	Ceramic Capacitor	0603	06031A221JAT2A	AVX
3	C22, C28, C41	NM		0805		
4	C24, C30, C39, C42	10 0nF	Ceramic Capacitor	0805	GCM21BR72A104KA37L	MURATA
3	C26, C31, C35	4.7 fun	Ceramic Capacitor	1210	C3225X7S2A475K200AB	TDK
1	C27	33 uF	ELCA	10x10.2	EEEFK2A330P	Panasonic
3	C29, C50, C51	100 nF	Ceramic Capacitor	0603	GRM188R72A104KA35D	MURATA
3	C32, C33, C34	22 uF	Ceramic Capacitor	1210	C3225X7R1C226K250AC	TDK
1	C36	NM		1210		
3	C40, C44, C47	1 uF	Ceramic Capacitor	0603	GRM188R71E105KA12D	MURATA
3	C43, C46, C54	NM				
1	C45	470 pF	Ceramic Capacitor	0603	GCM1885C2A471JA16D	MURATA
1	C48	100 pF	Ceramic Capacitor	0603	GRM1885C2A101JA01D	MURATA
1	C49	4.7 nF	Ceramic Capacitor	0603	CGA3E2X7R2A472K080AA	TDK
1	C52	3.3 uF	Ceramic Capacitor	0805	C2012X7R1C335K125AB	TDK
1	C55	470 nF 10%	Ceramic Capacitor	0603	Several	Several
1	C100	2.2 nF	Ceramic Capacitor	0805	Several	Several
7	D1A, D2A, D3A, D4A, D5A, D7A, D16A	STPS2H100A	**Schottky diode**	SMA	STPS2H100A	**STM**
7	D1B, D2B, D3B, D4B, D5B, D7B, D16B	NM		SOD-123		Alternative component
1	D6	SMAJ58A	**TVS diode**	SMC	SMAJ58A-TR	**STM**
6	U1, U2, U3, U4, U5, U6	SM15T68CA	**TVS diode**	SMC	SM15T68CA	**STM**
1	D9A	STPS5H100SF	**Schottky diode**	PSMC	STPS5H100SF	**STM**
1	D9B			POWERFLAT		Alternative component
1	D10	0R	Resistor	0603	ERJ-S120R00U	PANASONIC
2	D11, D20	NM				
2	D14, D15	BAT46J	**Signal diode**	SOD323	BAT46JFILM	**STM**
1	D13	BZX384C12	Zener diode	SOD323	BZX384-C12,115	NEXPERIA

Q.ty	Reference	Value	Description	Package	Manuf. Code	Manufacturer
2	J1, J2	RJ45	Connector		SS-7188S-A-NF	STEWART CONN
1	J3	SA	Power jack		RAPC722X	SWITCHCRAFT
1	J4	2 pin Jumper	Pin strip		M20-9990245	HARWIN
4	L1A, L2A, L3A, L4A	10 uH	Inductor 10 uH		SD54-103MLB	COILCRAFT
4	L1B, L2B, L3B, L4B	NM			MSS5131-103ML	Alternative component
1	L5	5.6 uH	Inductor	5.5x5.3x5.1 mm	XAL5050-562MEB	COILCRAFT
1	L6A	47 uH	Inductor	13.5x13.5x9 mm	SER1390-473MLD	COILCRAFT
1	L6B	NM			XLG6060	Alternative component
1	L6C	NM			MSS1583	Alternative component
4	Q1, Q2, Q3, Q4	STL3N10F7	Power MOSFET	PowerFLAT2x2	STL3N10F7	**STM**
2	Q5, Q11	MMBT3904LT1	NPN transistor	SOT23	MMBT3904-TP	Micro Commercial
1	Q6	STF1360	Power NPN transistor	SOT89	2STF1360	**STM**
1	Q7	STL30N10F7	Power MOSFET	PowerFLAT5x6	STL30N10F7	**STM**
3	Q8, Q9, Q13	MMBTA92	PNP transistor	SOT23	MMBTA92,215	NEXPERIA
1	Q10	2N7002	Signal MOSFET	SOT23	2N7002,215	NEXPERIA
8	R1, R2, R3, R4, R5, R6, R7, R8	75R	Resistor	0603	MC0063W0603175R	MULTICOMP
1	R9	NM		1812		
4	R10, R11, R12, R13	33R	Resistor	0805	RC0805FR-0733RL	YAGEO
4	R14, R24, R25, R32	F. Bead 100 ohm 4 A	Ferrite Bead	0805	NFZ2MSM101SN10L	MURATA
1	R15	15 K	Resistor	0805	RC0805FR-0715KL	YAGEO
4	R16, R17, R18, R19	1 M	Resistor	0603	CRG0603F1M0	TE Connectivity
4	R20, R21, R22, R23	270 k	Resistor	0603	RC0603FR-07270KL	YAGEO
3	R26, R33, R68	0R	Resistor	0805	RC0805JR-070RL	YAGEO
4	R27, R45, R49, R100	10 k	Resistor	0603	RC0603FR-0710KL	YAGEO
2	R28, R52	100 K	Resistor	0805	RC0805FR-07100KL	YAGEO
2	R29, R66	47 K	Resistor	0603	RC0603FR-0747KL	YAGEO
2	R30, R51	1 K 1%	Resistor	0603	RC0603FR-071KL	YAGEO
1	R31	NM		1206		
1	R34	NM		1812		
2	R35, R60	100 k	Resistor	0603	RC0603FR-07100KL	YAGEO
2	R65, R67, R102	15 k	Resistor	0603	RC0603FR-0715KL	YAGEO
2	R36,	5.1 k	Resistor	0603	RC0603FR-075K1L	YAGEO
1	R37	0R	Resistor	0603	RC0603JR-070RL	YAGEO
3	R6, R39, R43	NM				
1	R40	1.8 k 1%	Resistor	0603	RC0603FR-071K8L	YAGEO
3	R41, R42, R46	124 K	Resistor	0603	CPF0603F124KC1	TE Connectivity
1	R101	2.2 k	Resistor	0603	RC0603FR-072K2L	YAGEO
1	R44	10 R	Resistor	0805	RC0805FR-0710RL	YAGEO
1	R47	30R9 1%	Resistor	0805	RP73D2A30R9BTG	TE Connectivity

Q.ty	Reference	Value	Description	Package	Manuf. Code	Manufacturer
1	R48	24.9 K	Resistor	0603	RC0603FR-0724K9L	YAGEO
1	R50	39k 1%	Resistor	0603	RC0603FR-0739KL	YAGEO
		51 K	Resistor	0805	RC0805FR-0751KL	YAGEO
1	R53	21 K	Resistor	0603	CRCW060321K0FKEAHP	VISHAY
2	R54, R56	4.75 K	Resistor	0603	RC0603FR-074K75L	YAGEO
2	R38, R55	510 R	Resistor	0603	CRCW0603510RFKEA	VISHAY
1	R57	NM				
1	R58	1.21 k 1%	Resistor	0603	RMCF0603FT1K21	STACKPOLE
2	R59, R63	NM		0603		
1	R61	NM		1206		
1	R62	R150	Resistor	1206	CRCW1206150RFKEA	VISHAY
1	R69	1N4148WS	Signal diode	SOD323	Several	Several
4	TP1, TP3, TP6, TP7		Turret		2501-2-00-80-00-00-07-0	Mill-Max Manuf.
9	TP2, TP5, TP8, TP9, TP10, TP11, TP12, TP13, TP14	Red	Test Point		5000	KEYSTONE
1	TP4	Black	Test Point		5001	KEYSTONE
1	T1	ETH1-460	Data Tarof		ETH1-460LD	COILCRAFT
2	T2B, T2A	NM				Alternative component
3	D8, D12, D18	LED	Led		AA3528CGSK	KINGBRIGHT
1	U7	PM8803	PoE PWM controller	HTSSOP20	PM8803TR	**STM**
1	U8	TS431AILT	Voltage Reference	SOT23-5	TS431AILT	**STM**

Printed Circuit Board specification

PCB has been manufactured with the following Cu layer thickness:

Top and Bottom layers (1 and 4): 35 µm (1 oz)

Inner 2 and 3 layers: 16 µm (1/2 oz)

Layout guideline

Electrical return paths

There are four different return paths on the board, Chassis, VSS, RTN and -VOUT.

The Chassis is the first return path and it is used to connect the metallic body of the RJ45 and the return of the TVS devices used as protection against surge events.
This kind of common return can be connected to the Ground or the Protective Earth of the line.
The Chassis plane must be designed with proper isolation distance (creepage and clearance) from the other circuit electrical signals.
On this reference board, which implements a not isolated PD from the Ethernet line, a creepage of 60 mils (1.5 mm) is maintained.
This condition guarantees a functional isolation of 1500 Vdc.
Design copper areas for Chassis at least on both sides of the PCB.
Do not place as possible other signals under the RJ45 and under the data transformer area.

VSS is the negative voltage coming out from the input bridges.
The exposed pad of PM8803 must be connected to VSS: design a filled area with at least 6 vias to VSS plane.
Create where possible multiple VSS copper planes connected together, at least below the PM8803 position, to improve its heat dissipation.

RTN is the return path after the hot swap MOSFET inside the PM8803, it is connected to VSS after a successful detection and classification phase of the PoE PD interface section of the PM8803.

Keep separated the electrical path of -VOUT, that is a floating ground, from the rest of the circuit and note that it is not possible to use not insulated probes connected at the same time to RTN and to -VOUT signals.

Component placing and routing

Place the component group including: input ceramic capacitors, input inductor, power MOSFET and sense resistors close to each other, in order to keep the interconnections as short as possible.

Place the component group including rectifier diode, output inductor, output ceramic capacitors close to each other, in order to keep the interconnections as short as possible.

Design the copper area around the power MOSFET and the rectifier Diodes with at least ten vias of connection, to the internal copper planes.
Create where possible multiple copper layers connected together, at least below the MOSFETs and Diodes position, to improve the heat dissipation.

Placement and routing details:

- Place the input TVSs near the input diode bridges.

- Place the PM8803 and all related components close to each other; use both PCB sides.
- Place the PM8803 in such a way to have a short path to the gate of the power MOSFET; use a 20-30 mils wide path for this signal.
- Place the components for FRS, CS and CTL pins in low noise area, as much as possible separated from other signals.
- Place the decoupling capacitors for VCC close to the relevant PM8803 pin.
- Place the 100-mph input capacitor close to the VSS and GND pins.
- Connect the PM8803 pins 4, 8, 9 directly to the RTN copper area.

- Place the components of the feedback net close to each other, use both PCB sides.
- Place the current sense resistors close to the power MOSFET, on the same side.

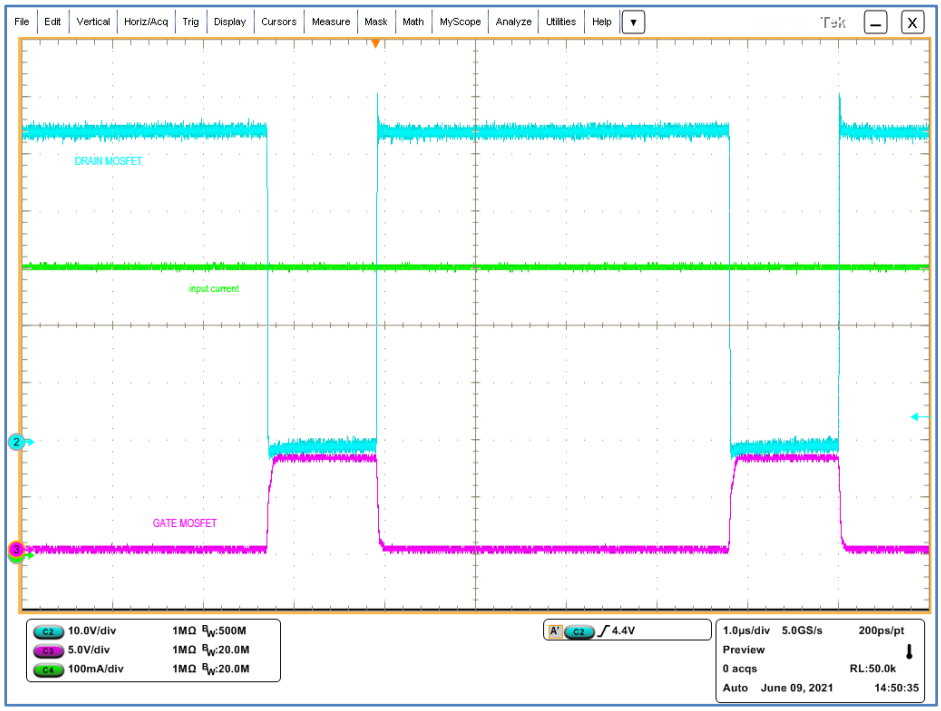
- Place the converter input ceramic capacitors close to the input side of the power inductor, preferably on the same side.
- Place the buck rectifier diode close to the power inductor, on the same side.
- Place the snubber net close to the power diode, on the bottom side.
- Place the output ceramic capacitors close to the rectifier diode, on the +VOUT copper area, top side.
- Place the last ceramic capacitors close to the output terminal of the power connector, bottom side.

Prototype board usage notes

- Note that TP1, TP3 and J3 auxiliary inputs have defined voltage polarity and value.
- Both passive and electronic loads can be used at the board output, it is necessary limit the output capacitance applied, to not impact on the loop compensation.
- The use of a DC power supply with 60 V and 3 A capability is recommended, as main PoE and Auxiliary inputs supply.

Main waveforms

Figure 6. MOSFET drain and gate voltage, input current.



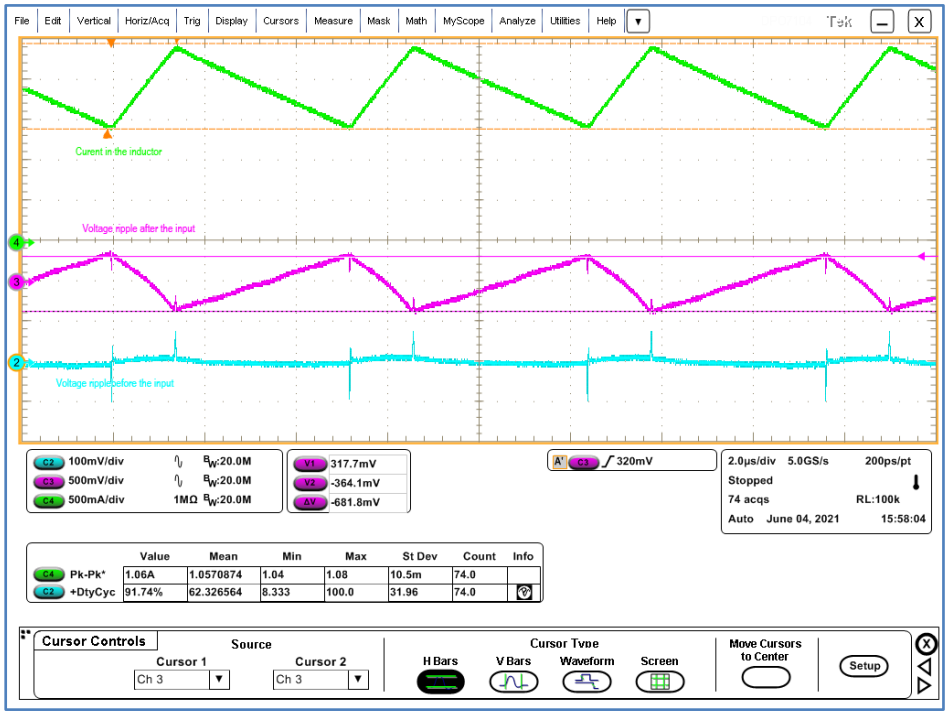
Blue trace,
MOSFET drain voltage.

Green trace,
Input current.

Purple trace,
MOSFET gate voltage.

Vin=54 V
Iout=2 A

Figure 7. Inductor current, input voltage ripple.



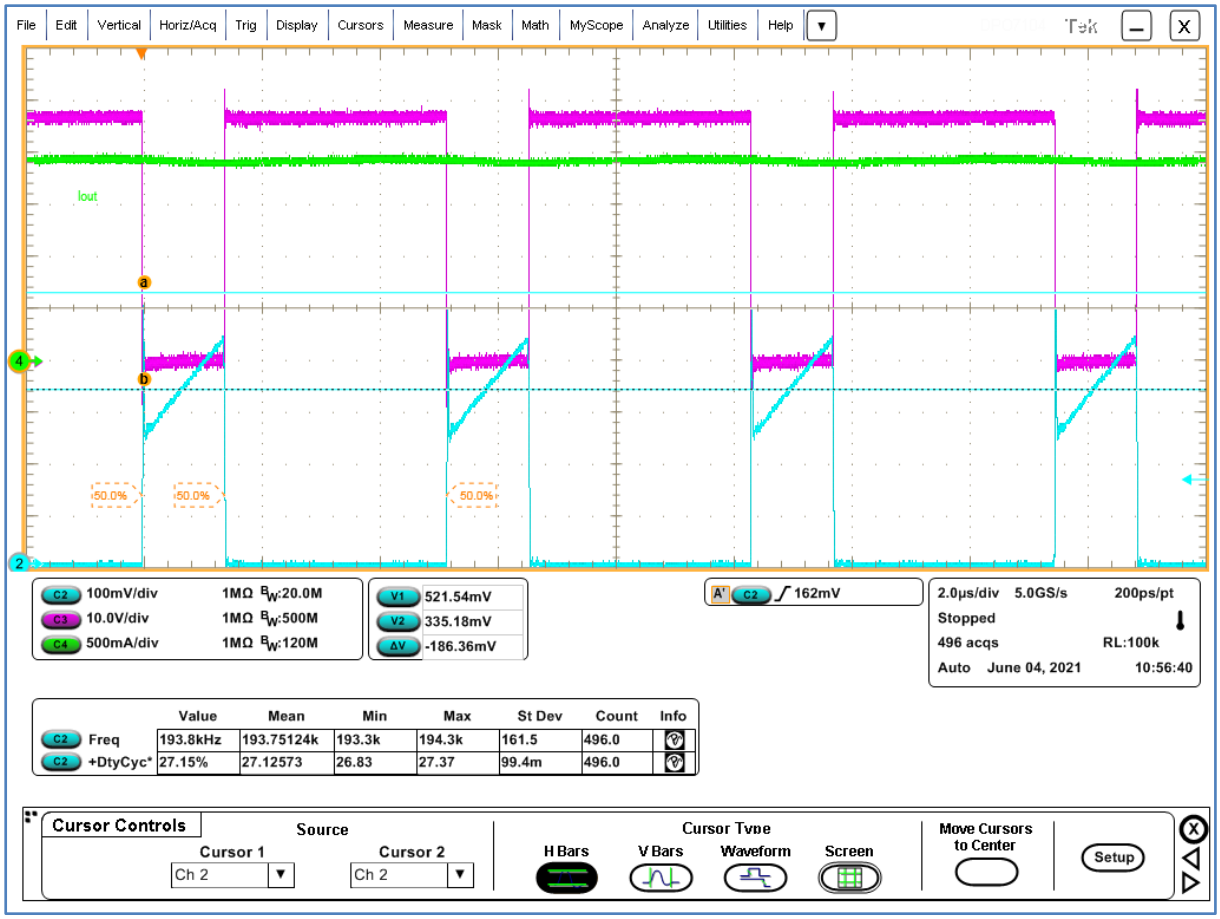
Green trace,
Inductor current.

Purple trace,
Voltage ripple after the input filter, V_TP5.

Blue trace,
Voltage ripple before the input filter, V_PoE+F.

Vin=48 V
Iout=2 A

Figure 8. MOSFET drain voltage, current sense voltage, output current.

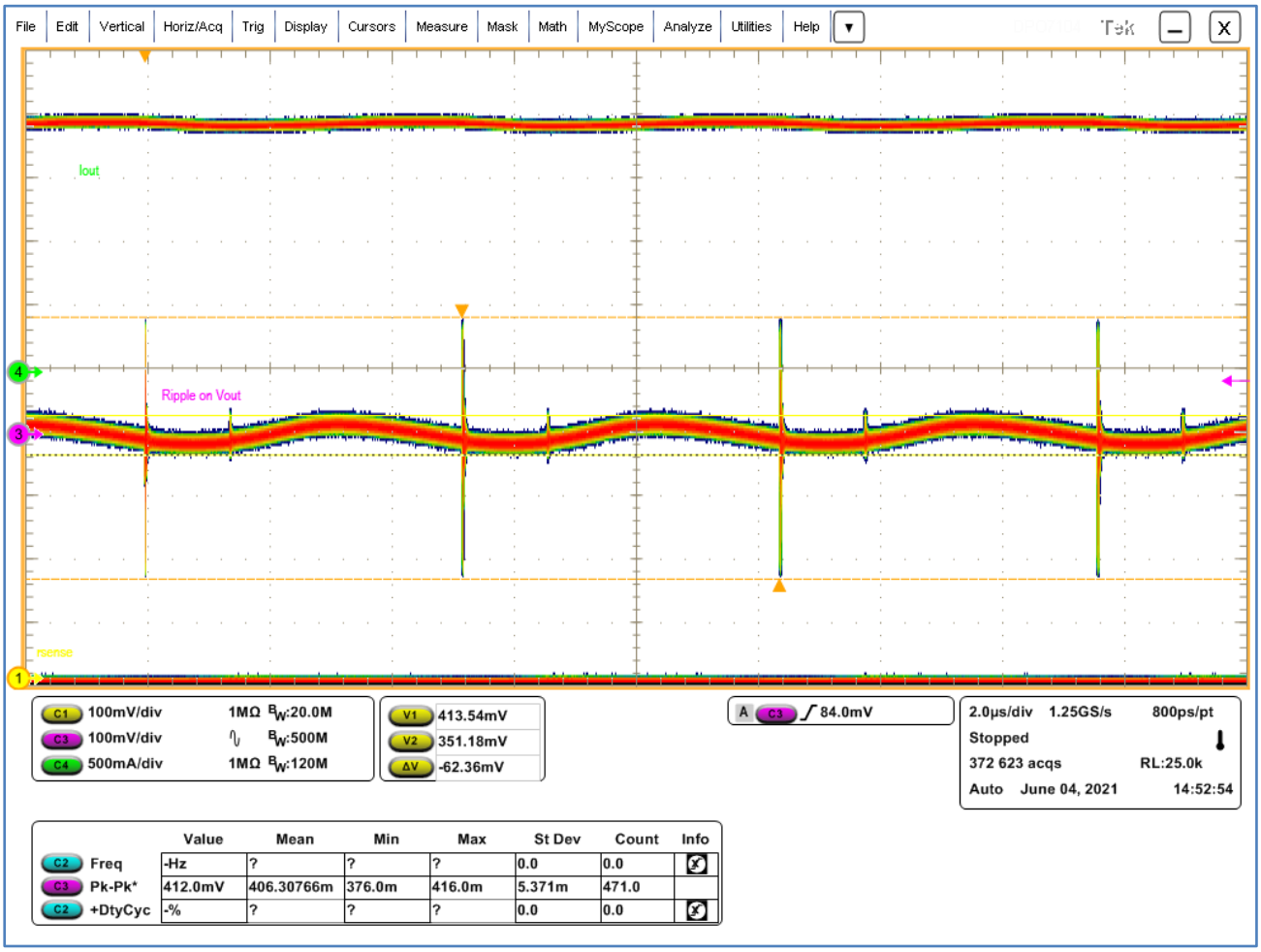


Vin=48 V, Iout=2 A

Purple trace, MOSFET drain.
Green trace, output current.
Blue trace, Sense voltage.

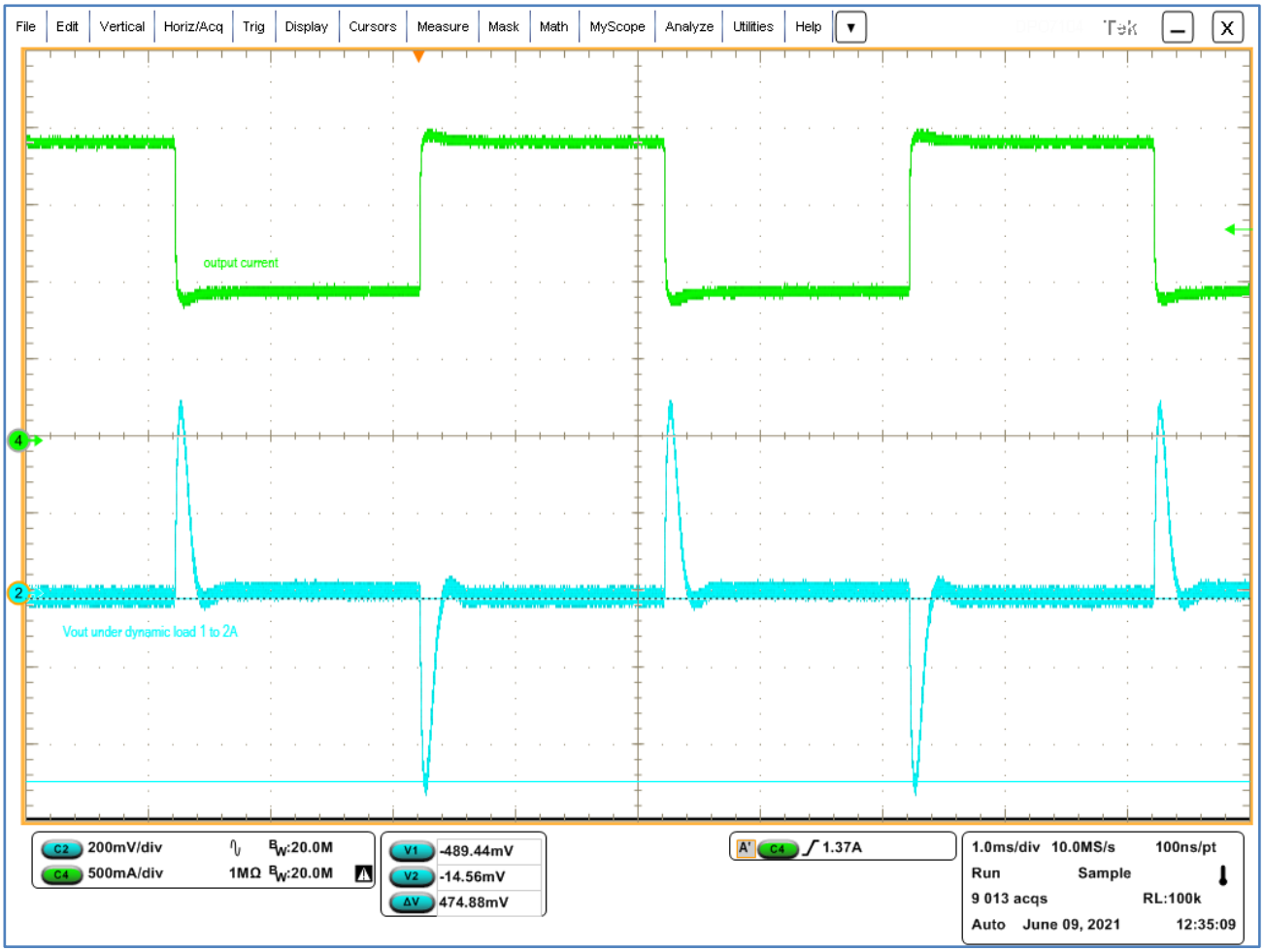
Output ripple and dynamic load

Figure 9. Output voltage ripple.



Iout=2 A. This acquisition was performed using a persistence of 1 sec.

Figure 10. Dynamic load response.



Dynamic load amplitude: Iout=1 to 2 A.

Startup transient

The board electrical circuit contains an optional startup circuitry (see Figure 2).
It is inserted in the feedback net and its purpose is to avoid possible voltage overshoots during startup transient.

The following figures show the different startup behavior depending on the presence of this dedicated circuit.
Measures are performed with two output current levels, Iout=100 mA and Iout=2 A (resistive loads).
Note the different Vout behavior at Iout=100 mA.

Figure 11. Startup without optional circuit, Iout=100 mA

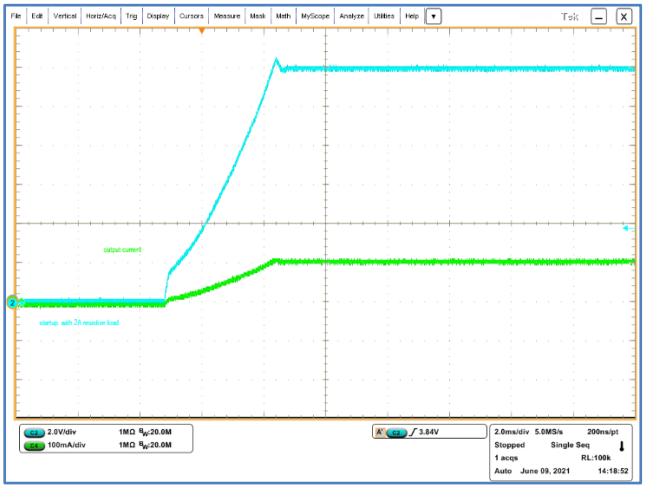
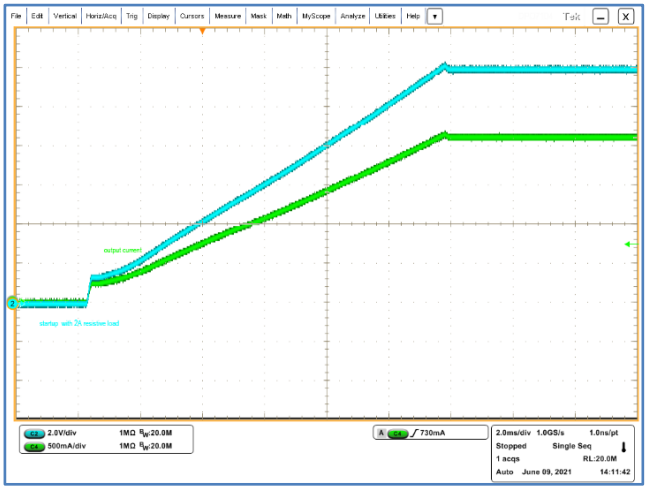


Figure 12. Startup without optional circuit, Iout=2 A



Blue trace, Vout.
Green trace, Iout.

Figure 13. Startup with optional circuit, Iout=100 mA.

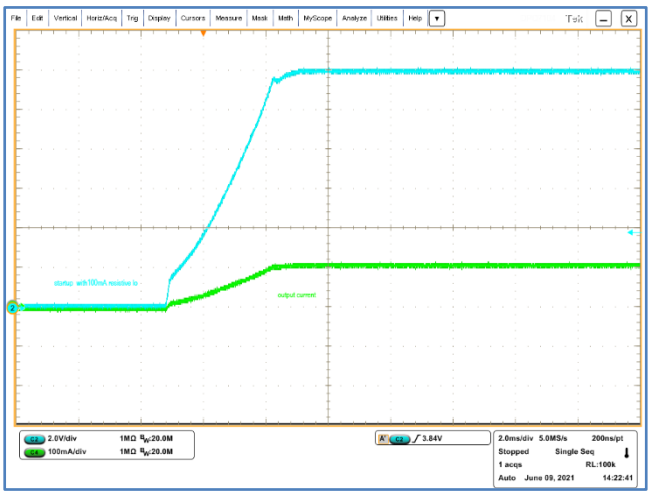
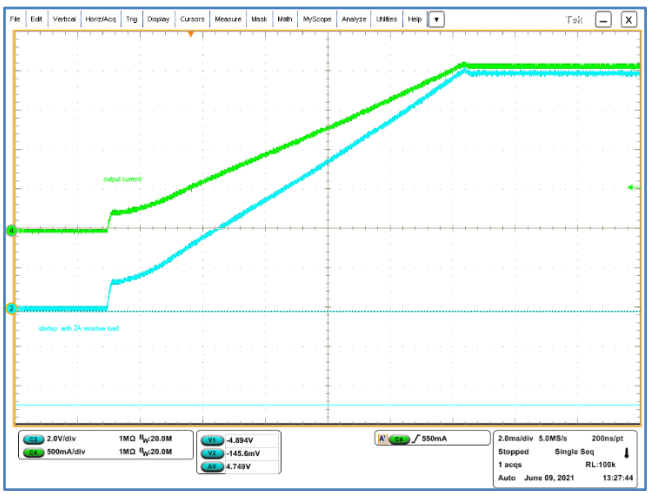


Figure 14. Startup with optional circuit, Iout=2 A.

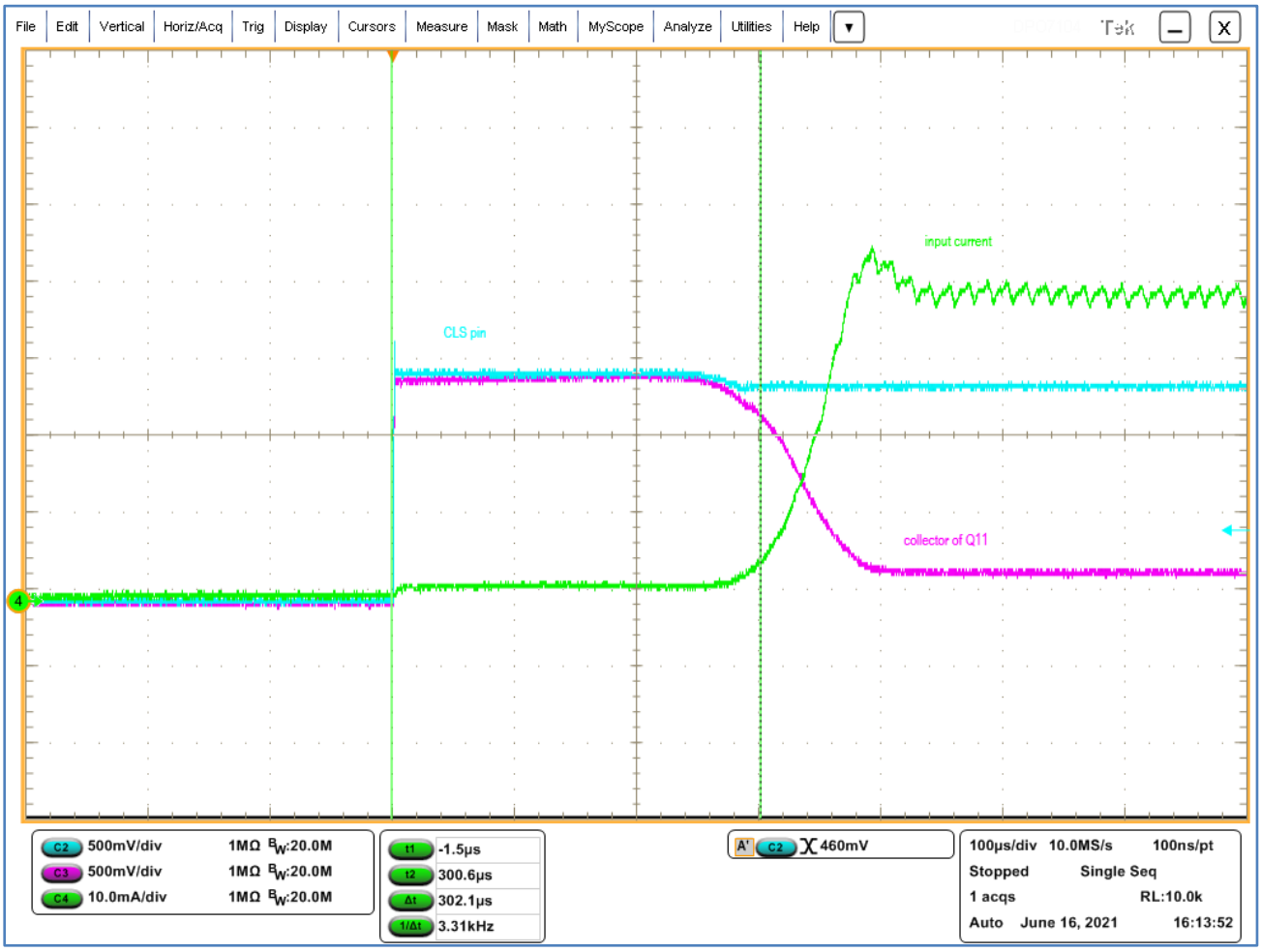


Additional delays

In the electrical diagram in Figure 2, there are two delay circuits:
the CLS delay with length 300 µs, to retard the current step of 40 mA during classification process;
the FRS delay with length 80 MS, to turn on the converter after the inrush current limitation phase.

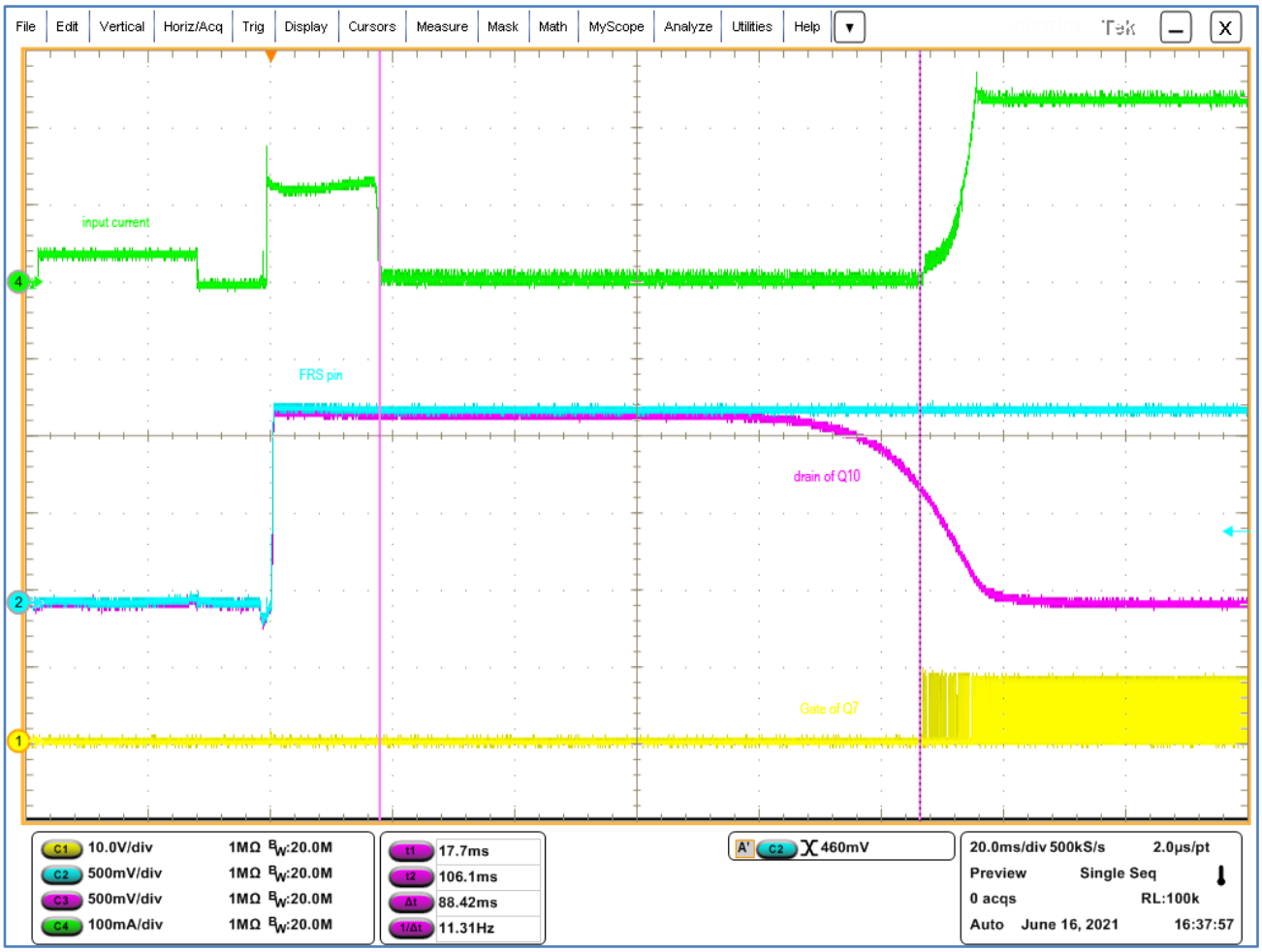
The following images show the behavior of those circuits.

Figure 15. CLS delay.



The connection delay of Rclass is about 300 µs, after this time the PSE is able to perform the right current limitation for the classification phase.

Figure 16. FRS delay.



The converter startup delay is around 80 MS, this solution guarantees the compliance of every PD circuit to the IEEE802.3 requirement.

DC-DC converter control loop analysis

The following measurements show the frequency response of the converter control loop, in terms of gain and phase. The measurements were made in closed loop condition, at the maximum load and with three different input voltages.

Figure 17. Control loop response, Vin=42 V Out=2 A.

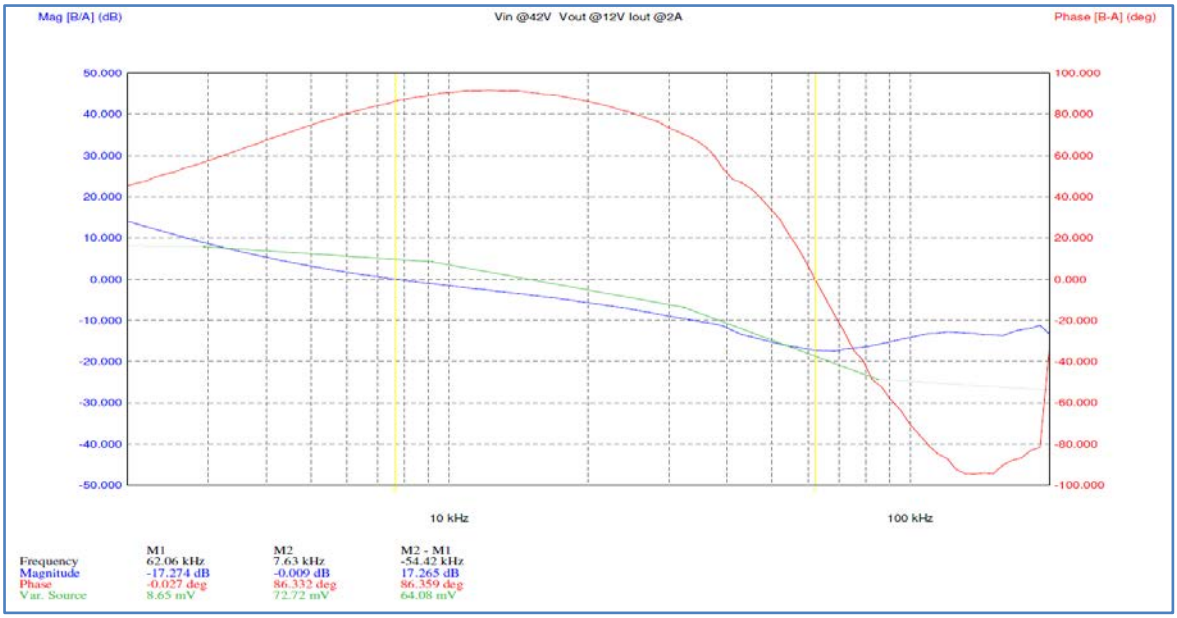


Figure 18. Control loop response, Vin=48 V Iout=2 A.

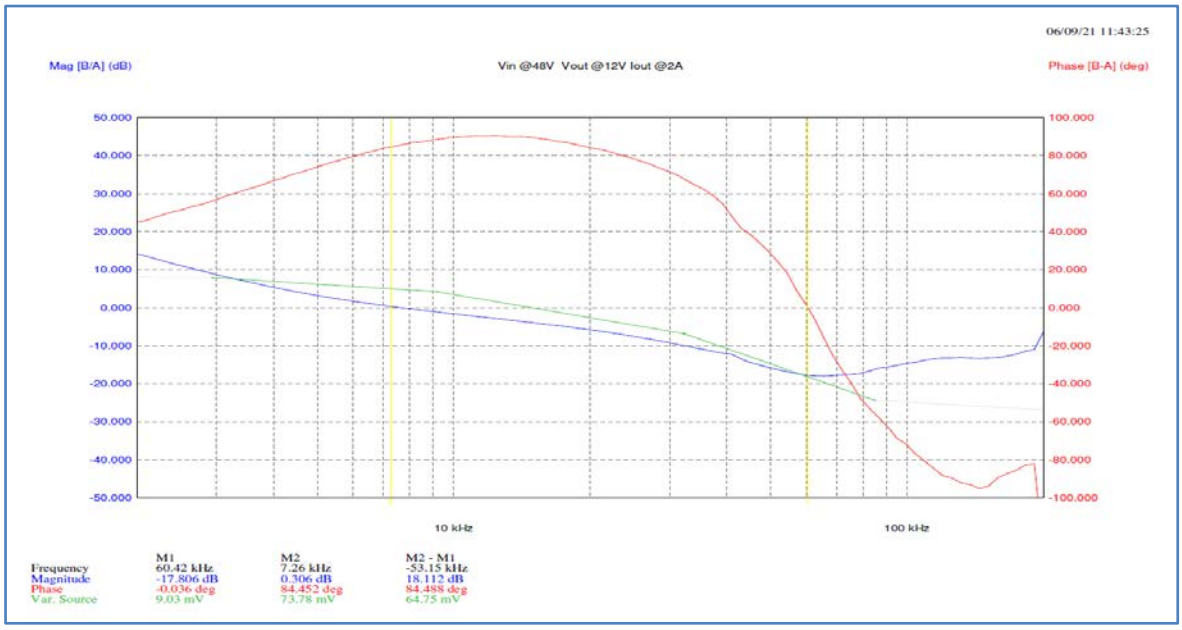
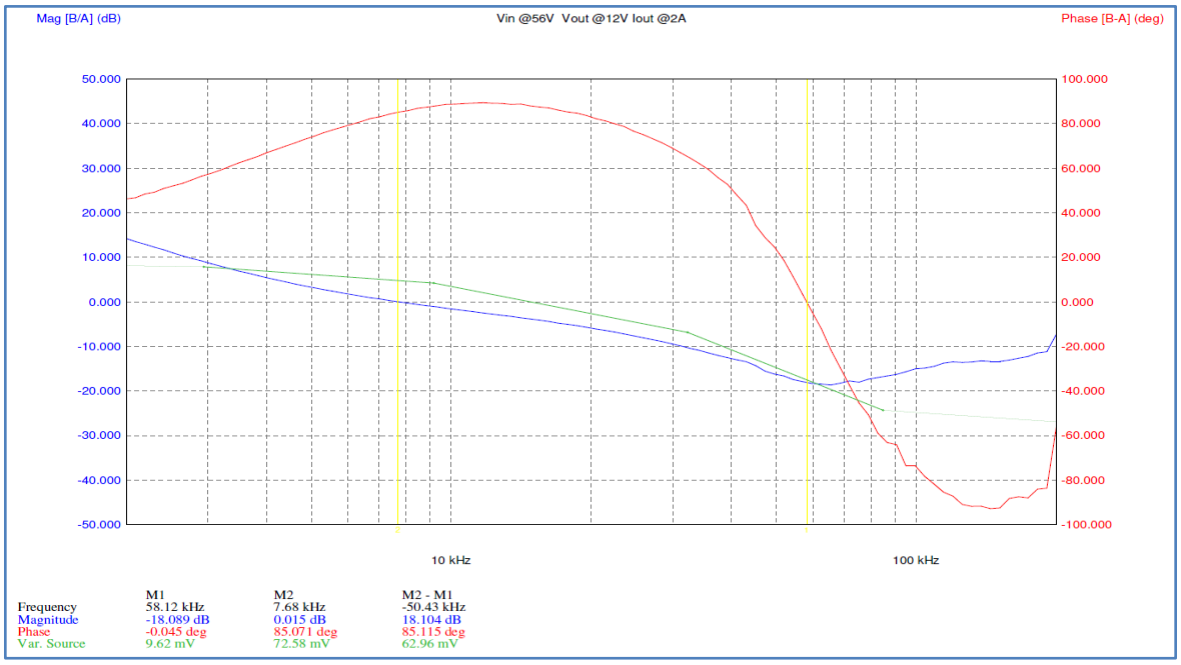


Figure 19. Control loop response, Vin=56 V Iout=2 A.



The following table shows the phase margin and the gain margin of the previous three measurements, note the minimum variation on the crossover frequency and on gain/phase margins.

Table 2. Control loop analysis results.

Vin=42 V, Iout=2 A	Vin=48 V, Iout=2 A	Vin=56 V, Iout=2 A
f=7.6 kHz / Phase M=86 deg	f=7.8 kHz / Phase M=84 deg	f=7.7 kHz / Phase M=85 deg
f=62 kHz / Gain M=17 dB	f=60 kHz / Gain M=18 dB	f=58 kHz / Gain M=18 dB

Prototype board efficiency

The system efficiency indicated as “Overall” was obtained measuring:
the input voltage at the RJ45 connector Tx and Rx pins (Pins 1,2 and 3,6);
the output voltage on the PCB module close to the output turrets (TP6 and TP7).

The “DC-DC converter” efficiency was obtained measuring:
the input voltage at the input filter level (TP2 and RTN);
the output voltage on the output turrets (TP6 and TP7);
in this measurement it is not considered the contribution of the data transformer, input bridges and the PM8803 hot swap MOSFET.

The “Bridge” efficiency was obtained measuring:
the input voltage at the bridge input (Q1 and Q2 drains);
the output voltage at the bridge output (TP2 and TP4).

Figure 20. Overall efficiency.

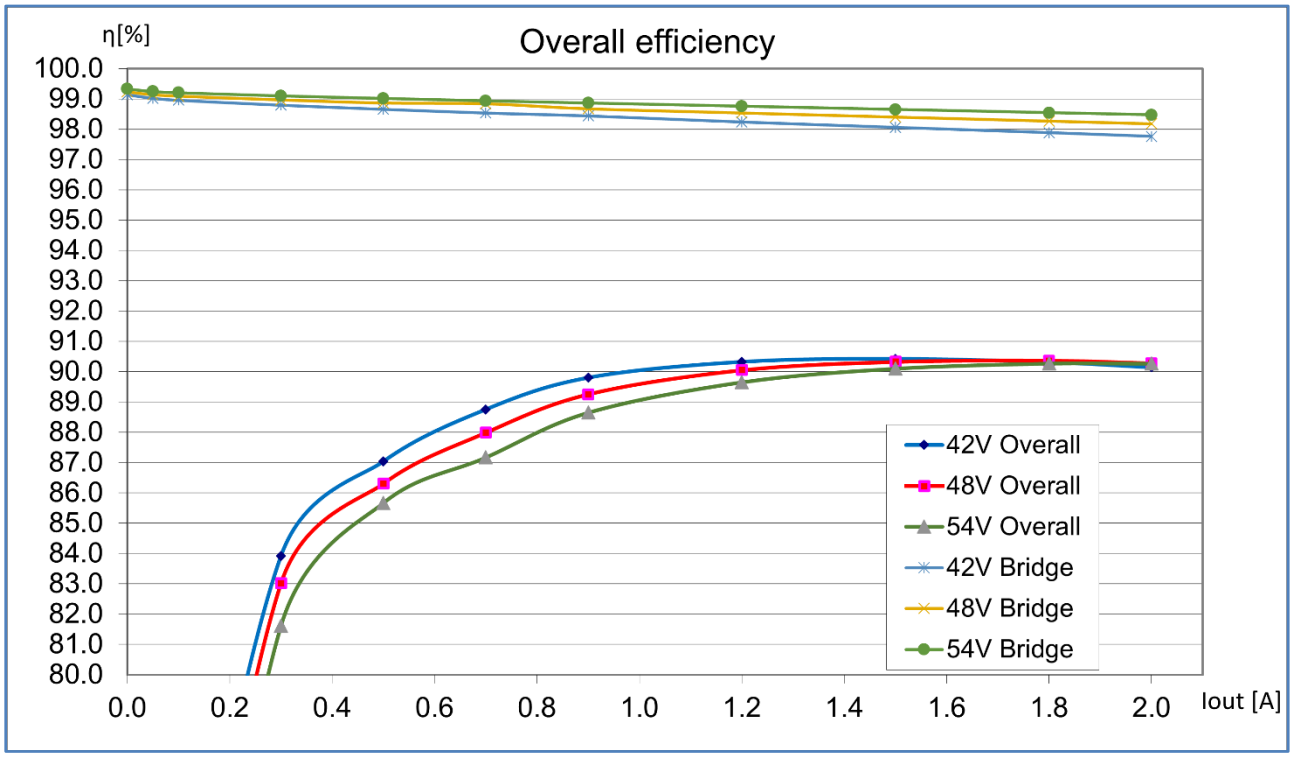
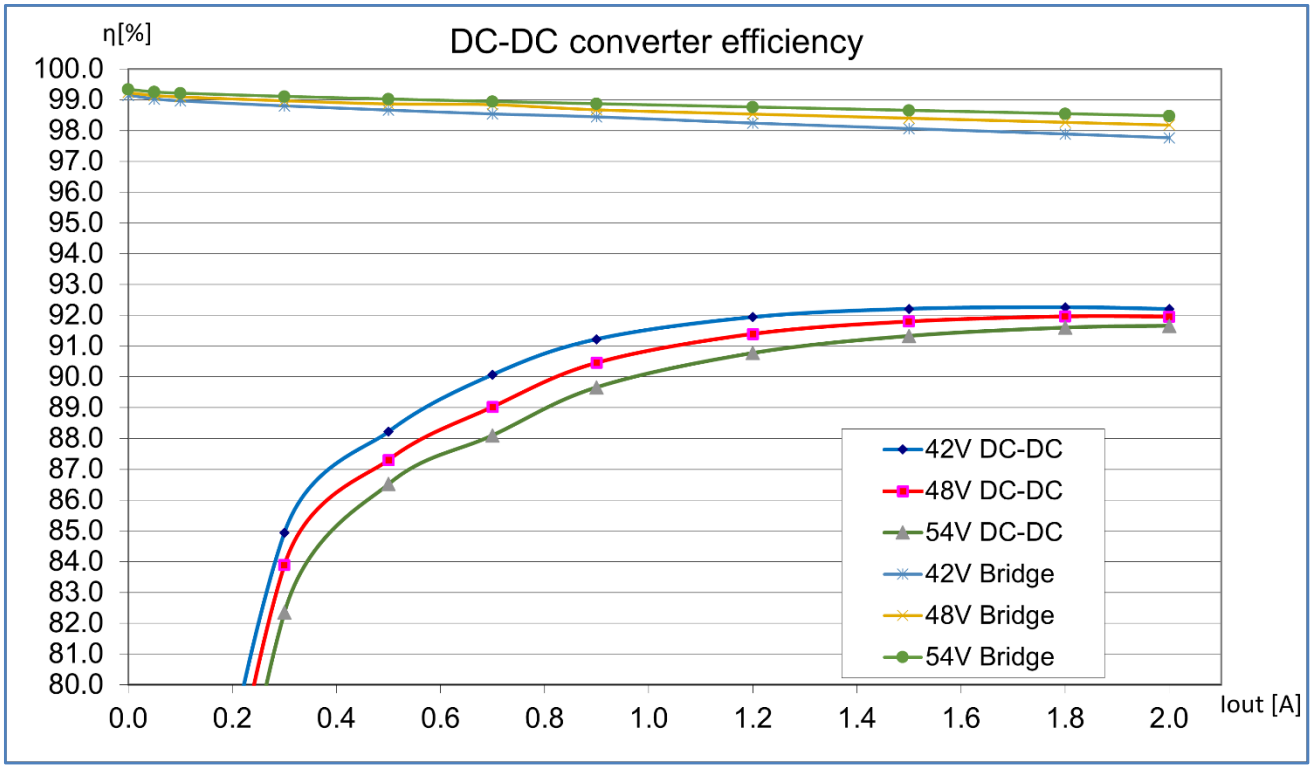


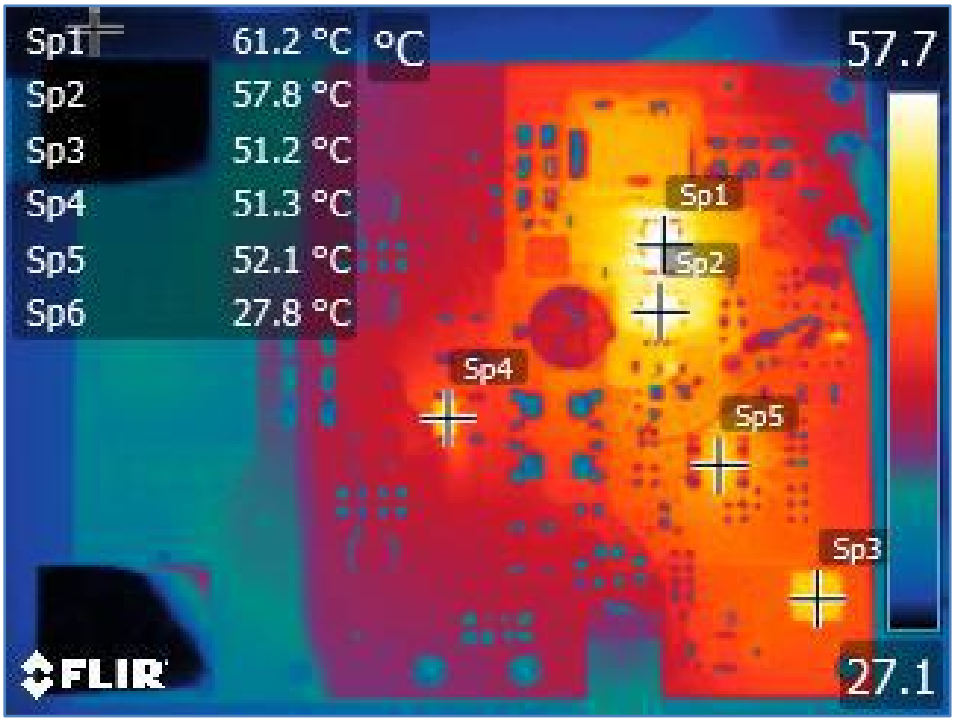
Figure 21. DC-DC converter efficiency.



Thermal measurement

The following image is a thermal map of the entire board, operating with the maximum load and after a warm up time of 1h, in free air.
The highest temp is reached by the main rectifier diode D9, which is the component with the highest power dissipation associated.

Figure 22. Prototype board thermal map.



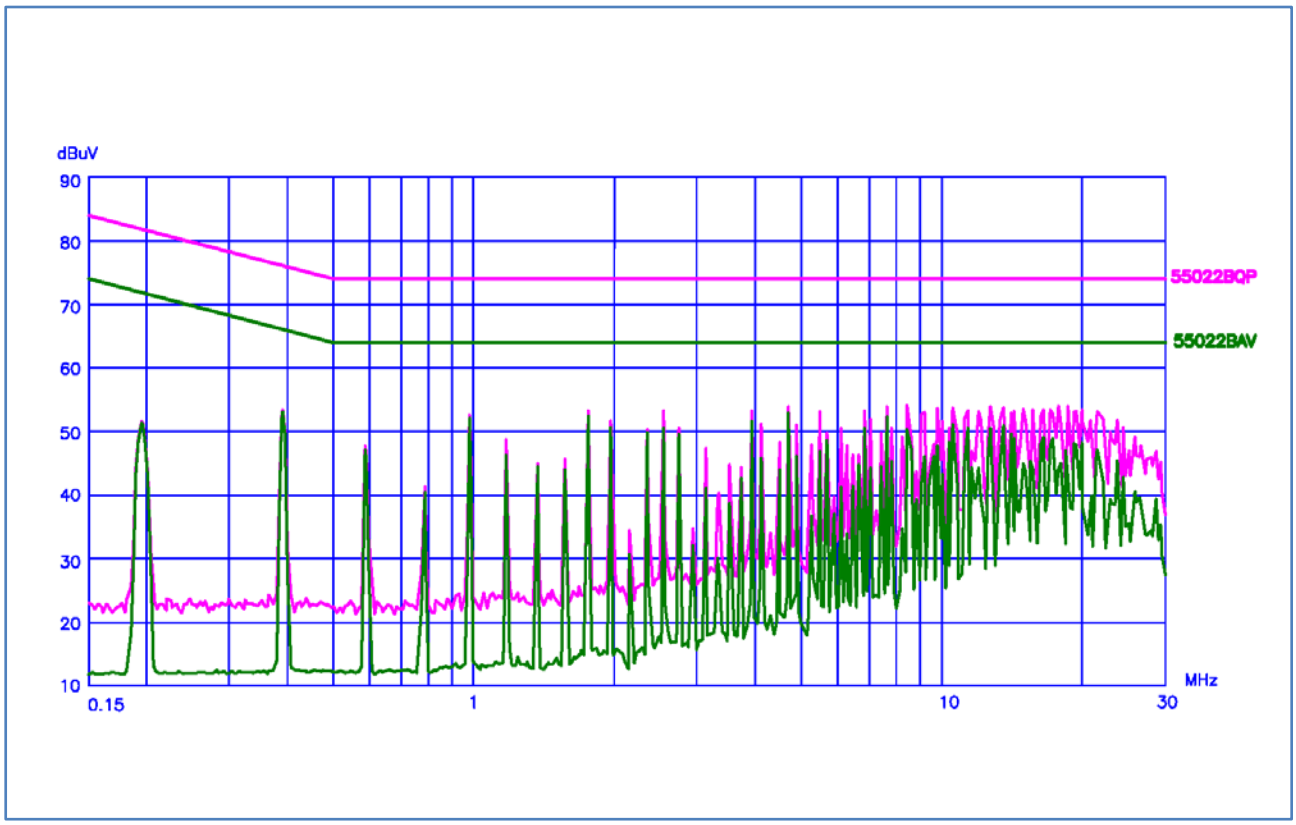
Vin=48 V Iout=2 A
Ta=27.1 °C, ambient temperature.

Electro-Magnetic Interferences

The following figure reports the measurement carried out on the board, relative to the conducted common mode (asymmetric mode) disturbance at telecommunication ports, in the frequency range 0.15 MHz to 30 MHz, for class B equipment.

The measurement is performed using a proper Impedance Stabilization Network (ISN), following the specification present in the CISPR 22: 2008 and EN 55022: 2010 standards.

Figure 23. Conducted common mode disturbance.



The previous measurement was performed using the following test condition:

Vin=48 V Iout=2 A

Electro-Magnetic Compatibility

The following section reports the measurement conducted on the board, relative to the voltage surge application.
Tests are performed using a proper Coupling and Decoupling Network (CDN), following the specification present in the IEC 61000-4-5 standard.

Tests reported in this design note are conducted using the 1.2/50 µs surge, which is relative to the most common PoE application circuits, that are connected to lines frequently classified as Unshielded and Symmetrical.

The scope of the test is to verify the presence of a failure risk, during the surge application.
Since the circuit foresees the presence of four TVS on the input lines (U1, U2, U3, U4), which limit the voltage transient amplitude on the board, a possible failure implies the presence of high currents flowing through the electrical paths.

It is very important to note that since the board output voltage is not isolated, there cannot be a ground connection of the output.
During the test, the ground connection was applied to the Chassis ground plane.

Considering the board circuitry, the most sensitive component is the PM8803, which can suffer high current flowing into its hot swap MOSFET.
To verify the amplitude of the current flowing through the PM8803, it is enough to measure the current flowing into the R26 resistor, that means the current flowing along the positive path POE+F.

The tests report a safe effect of ±6 kV surges, which show a maximum current peak I_R26=1.2 A, during the Surge injection.

The presence in the board circuit of input bridges composed by diodes and MOSFETs, guarantees a fast opening of the bridge itself.
That leads to having the same result during surge injection, independently by the presence of the four input inductors L1, L2, L3 and L4.
The four inductors presence is useful in case the board is used together with another external circuitry, that could change the current path during surge event.

The following four figures show the test results.

Notes:

- The presence of the four TVSs on the input lines, allows the injection of high voltage surge, even if the creepage distance maintained between input lines paths and the Chassis plane is 60 mils only.
- See design tip DT0149 “Power over Ethernet application circuits, line surge analysis and treatment”, to obtain more information on the subject.

Figure 24. +6 kV surge.

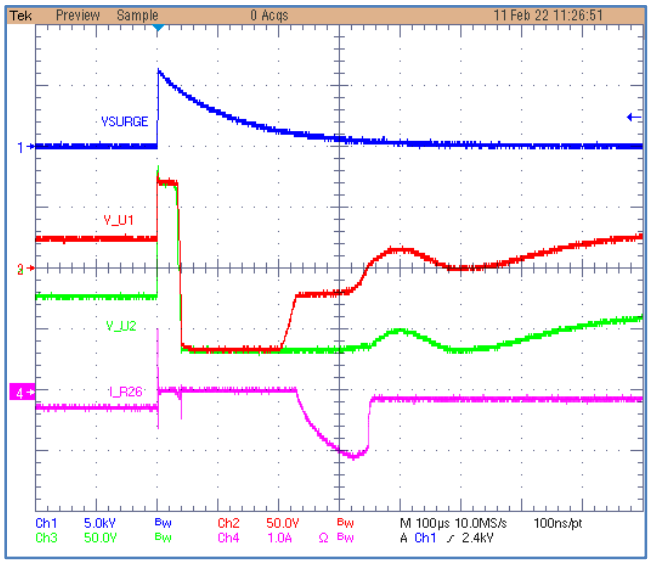


Figure 25. +6 kV surge.

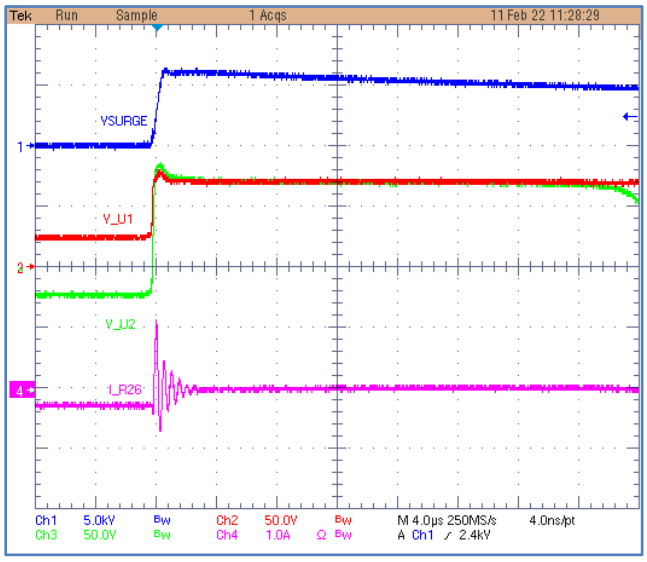


Figure 26. -6 kV surge.

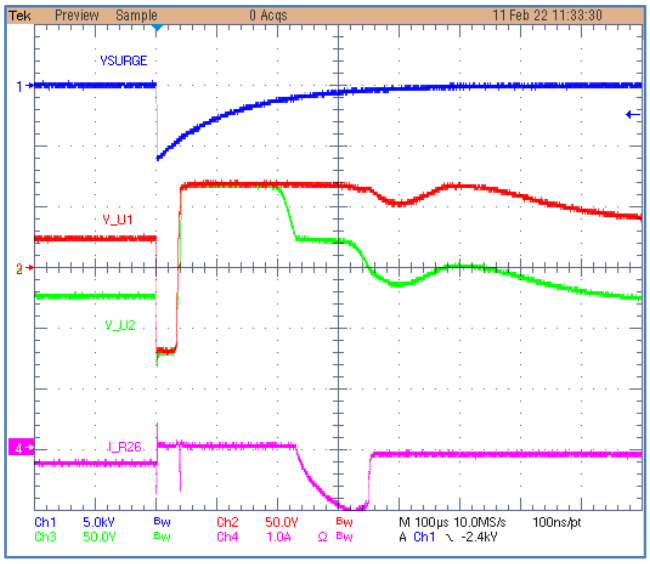
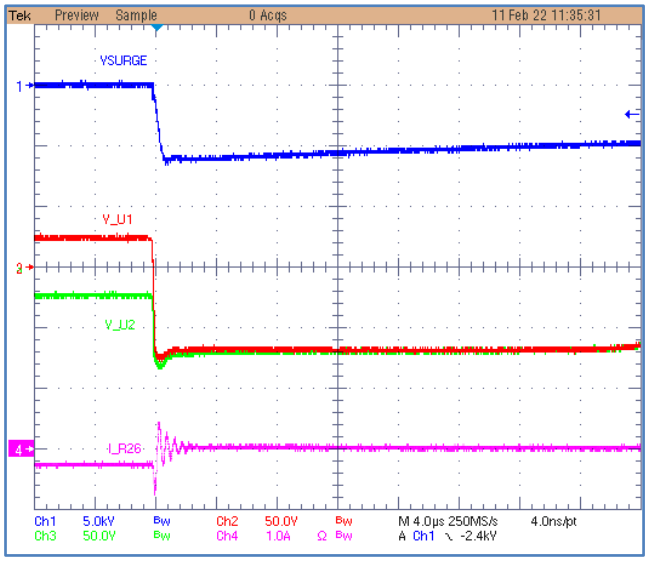


Figure 27. -6 kV surge.



Support material

Documentation
Design tip DT0145, PM8803/03C design tip: T2P issue with certain PSE.
Design tip DT0146, PM8803/03C design tip: how to solve a marginality of AT standard.
Design tip DT0149, Power over Ethernet application circuits, line surge analysis and treatment.

Revision history

Date	Version	Changes
05-Jul-2022	1	Initial release.

Contents index