

Dual current limit with STCC2540 / STCC5011 /
STCC5021

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Main components	
STCC2540	USB charging controller with integrated power switch
STCC5011, STCC5021	USB charging controller with integrated power switch and attach detector

Specification

The STCC2540, STCC5011 and STCC5021 are providing the charging capabilities based on the CTLx pin configuration. The CTL1 and CTL2 pins are typically driven by the Intel chipset SLP_S3# and SLP_S4# signals while the CTL3 pin typically toggles on/off the charging capabilities based on the battery state or BIOS/user setting. If CTL3 is driven low, the USB port is a standard USB port without battery charging support. If CTL3 is driven high, the charging capability is enabled.

This feature does not change the device output current limit; this relies on the fact the portable devices are properly handling charging negotiation. In order to increase the platform safety, it is possible to change the output current limit by adding only a few components.

Circuit description

The STCC2540 / 5011 / 5021 devices primarily offer one current limit set by external resistor R_{ILIM} connected between the ILIM and GND pins (Figure 1a). This is sufficient for 90% of applications.

✎ The current limit can be calculated using the formula $ILIM = 48000 / R_{ILIM} [mA, k\Omega]$.

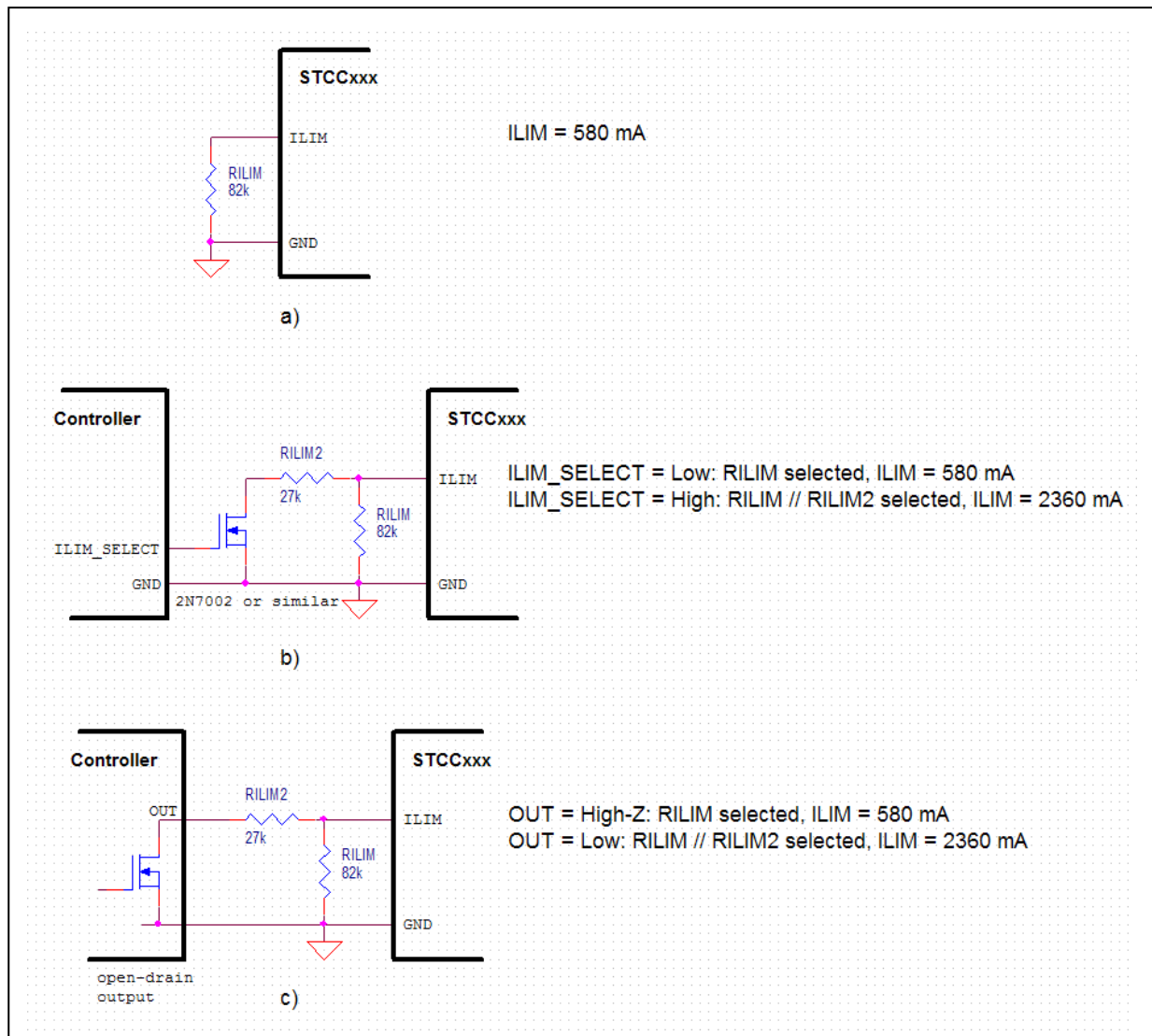
However in some cases it is fine to have the possibility to select the current limit based on operating mode (standard USB port allows lower current limit than charging USB port), power supply capability (AC network / battery) or battery charge level.

The solution is simple: The current limit can be set to a higher level by a second resistor R_{ILIM2} , connected in parallel to an existing R_{ILIM} through any small N-channel MOSFET (Figure 1b).

- If the MOSFET is turned off, only the R_{ILIM} resistor is setting the current limit (e.g. 580 mA for 82 k Ω).
- If the MOSFET is turned on, the current limit is set by the parallel combination of R_{ILIM} and R_{ILIM2} (e.g. 2360 mA for a parallel combination of 27 k Ω and 82 k Ω). Apparently the resulting current limit for MOSFET turned on is always higher than the current limit for MOSFET turned off.

Furthermore, if the controller output is of open-drain type without any pull-up, it can directly switch on/off the additional resistor (Figure 1c). In this case, extreme care should be taken to make all connections to ILIM and GND pins of STCC device as short as possible to avoid any noise which could affect the current limit precision. Excessive parasitic capacitance could also influence the stability of the current limit feedback loop.

Figure 1. Circuit diagram



Current limit control recommendation

The current limit should never be changed in SDP or CDP mode when USB device is attached. This could lead to data corruption in the case that insufficient current limit is selected and the STCC device enters the constant-current mode resulting into VBUS voltage falling below the valid range.

In order to provide data integrity over the USB connection, the capability change should occur only when the system is in the suspend mode.

From application point of view, the embedded controller should take care of the following conditions:

- we should not reduce the current limit in the S0 state (data transfer enabled, CTL1 = 1) (CTL1 is usually connected to the Intel chipset SLP_S3# signal)
- In S3, S4, S5 state (CTL1=0) we can toggle Vbus and change the current limit if no charging detected - $\overline{\text{CHARGING}} = 1$.

Revision history

Date	Version	Changes
06-Jun-2013	1	Initial release

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