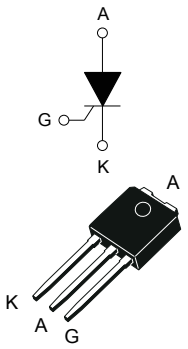
X0405MH

Datasheet

4 A Sensitive gate SCR in IPAK package



IPAK

Features

- 4 A SCR
- Sensitive SCR: I_{GT} = 50 µA
- V_{DRM} / V_{RRM} = 600 V and V_{DSM} / V_{RSM} = 750 V
- 125 °C maximum junction temperature T_j
- IPAK package
- Halogen-free molding, lead-free plating
- ECOPACK2 compliant

Applications

- Actuators
- Ignitors
- Inrush current limiting circuits

Product status link
X0405MH

Product summary	
$I_{T(RMS)}$	4 A
V_{DSM}/V_{RSM}	750 V
I_{GT}	50 µA
T_j max.	125 °C

Description

The X04 series is 4 A SCR housed in compact through hole IPAK package. This highly sensitive device is suited to home appliances or power tools and industrial systems and drives loads up to 4 A.

1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter		Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	T_c = 114 °C	4	A
$I_{T\ AV}$	RMS on-state average current (full sine wave)	T_c = 114 °C	2.5	A
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	t = 8.3 ms	33	A
		t = 10 ms	30	
I^2t	I^2t value for fusing	t_p = 10 ms	9	A^2s
dI/dt	Critical rate of rise of on-state current, I_G = 2 x I_{GT}, tr ≤ 100 ns, f = 60 Hz	T_j = 125 °C	50	A/µs
V_{DRM}/V_{RRM}	Repetitive peak off-state voltage	T_j = 125 °C	600	V
V_{DSM}/V_{RSM}	Non Repetitive peak off-state voltage, 10 ms		750	V
I_{GM}	Maximum peak gate current	t_p = 20 µs, T_j = 125 °C	1.2	A
P_{GM}	Maximum gate power dissipation		0.5	W
T_{stg}	Storage temperature range		-40 to +125	°C
T_j	Operating junction temperature range		-40 to +125	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Table 2. Electrical characteristics (T_j = 25 °C, unless otherwise specified)

Symbol	Test conditions			Value	Unit
I_{GT} (1)	V_D = 12 V, R_L = 140 Ω		Min.	20	µA
			Max.	50	
V_{GT}			Max.	0.8	V
V_{GD}	V_D = V_{DRM}, R_L = 3.3 kΩ	T_j = 125 °C	Min.	0.1	V
V_{RGM}	I_{RG} = 10 µA		Max.	8	V
I_L	I_G = 1.2 x I_{GT}		Max.	6	mA
I_H (2)	I_T = 500 mA, gate open		Max.	5	mA
dV/dt (2)	V_D = 67 % V_{DRM}, R_{GK} = 1 kΩ	T_j = 110 °C	Min.	15	V/µs

1. *For both polarities of OUT pin referenced to COM pin.*
2. *For both polarities of A2 referenced to A1.*

Table 3. Static characteristics

Symbol	Test conditions	T_j		Value	Unit
V_{TM} (1)	I_{TM} = 8 A, t_p = 380 µs	25 °C	Max.	1.8	V
V_{TO} (1)	Threshold voltage	125 °C	Max.	0.85	V
R_D (1)	Dynamic resistance	125 °C	Max.	100	mΩ
I_{DRM}/I_{RRM}	V_D = V_{DRM}; V_R = V_{RRM}; R_{GK} = 1 kΩ	25 °C	Max.	5	µA
		125°C		1	mA

1. *For both polarities of A2 referenced to A1.*

Table 4. Thermal resistance

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Max.	3	°C/W
$R_{th(j-a)}$	Junction to ambient	Typ.	70	°C/W

1.1 Characteristics (curves)

Figure 1. Maximum average power dissipation versus on-state RMS current

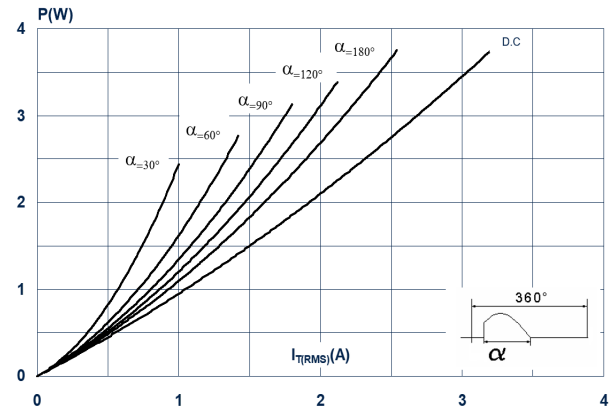


Figure 2. Average and DC on-state current versus case temperature

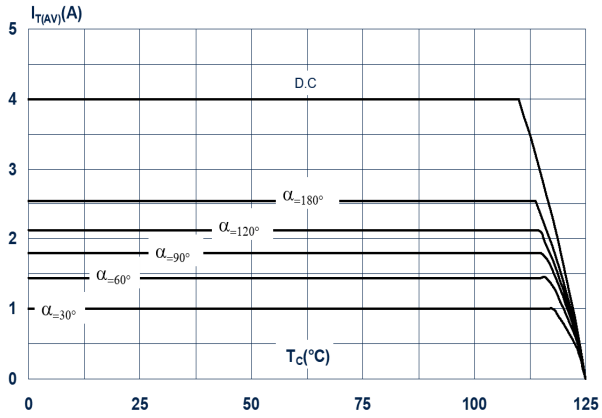


Figure 3. On-state RMS current versus ambient temperature (full cycle)

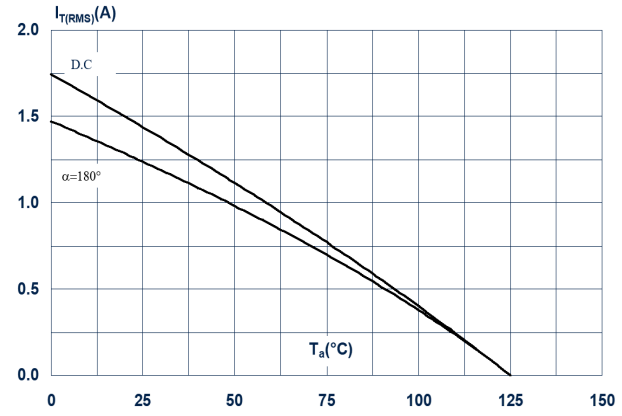


Figure 4. Relative variation of thermal impedance versus pulse duration

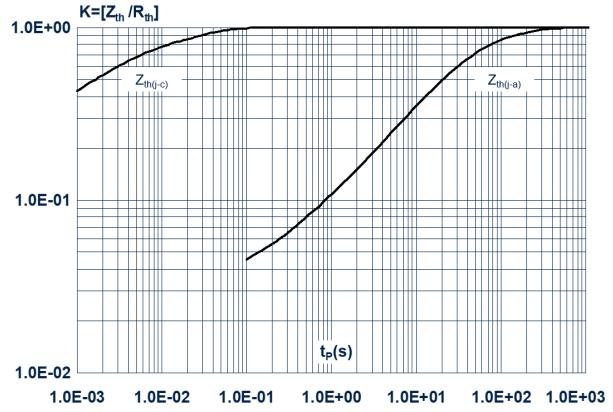


Figure 5. Relative variation of gate triggering current and voltage versus junction temperature (typical values)

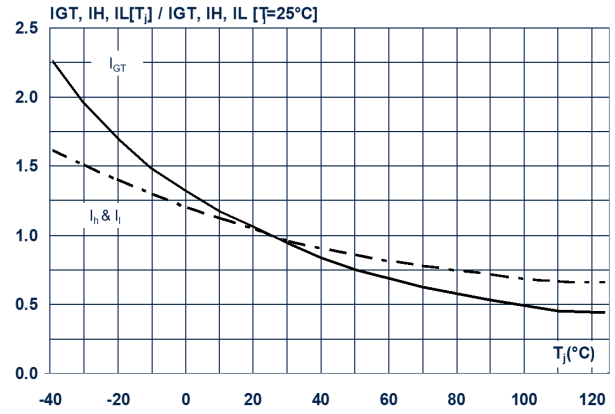


Figure 6. Surge peak on-state current versus number of cycles

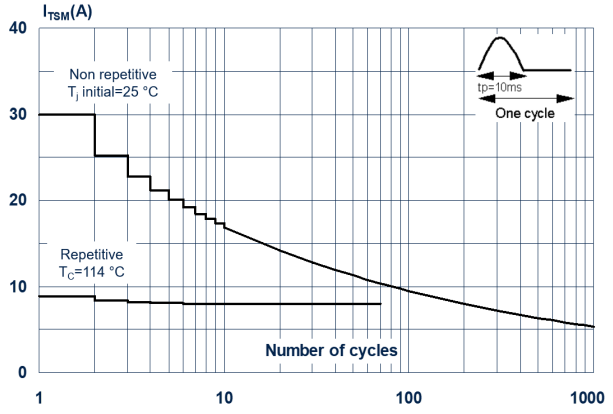


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms and corresponding value of I^2t

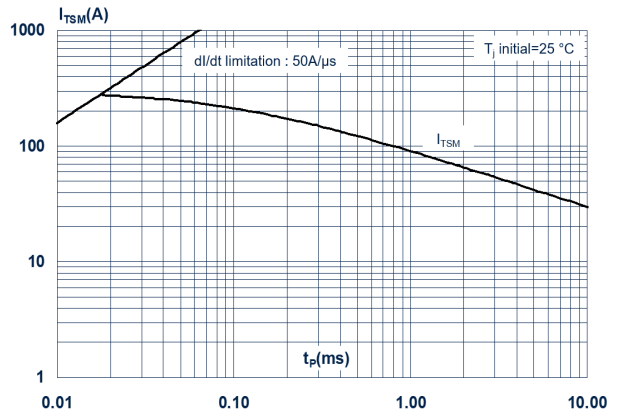


Figure 8. On-state characteristics (maximum values)

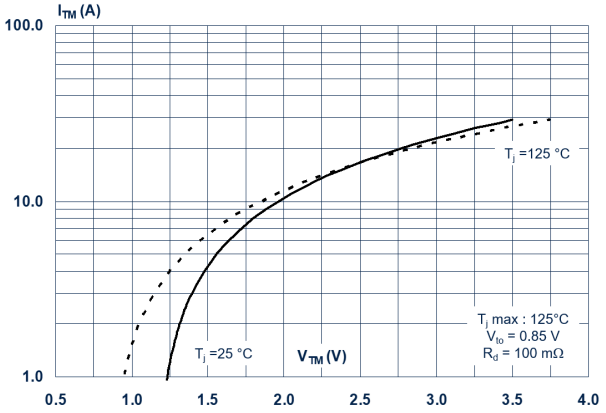


Figure 9. Relative variation of static dV/dt immunity versus gate-to-cathode resistance (typical values)

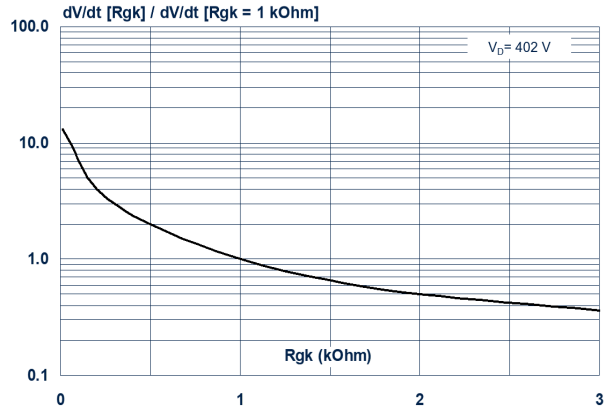


Figure 10. Relative variation of static dV/dt immunity versus gate-to-cathode capacitance (typical values)

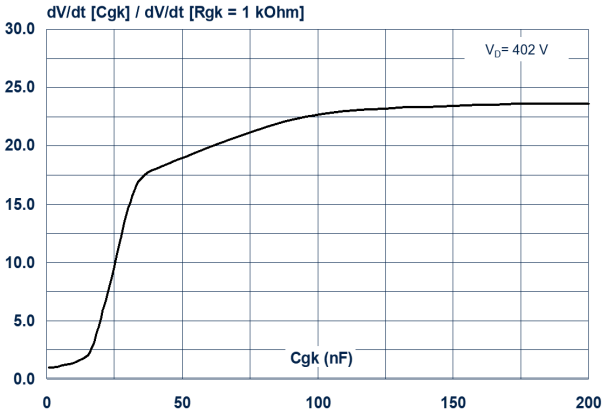
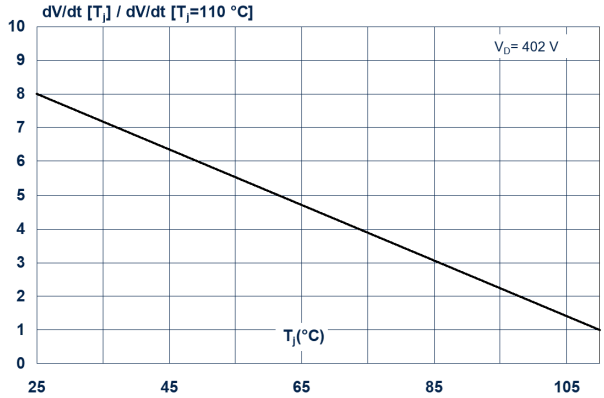


Figure 11. Relative variation of static dV/dt immunity versus junction temperature



2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 IPAK package information

- Molding compounded resin is halogen free and meets UL94 flammability standard, level V0
- Lead-free package leads plating

Figure 12. IPAK package outline

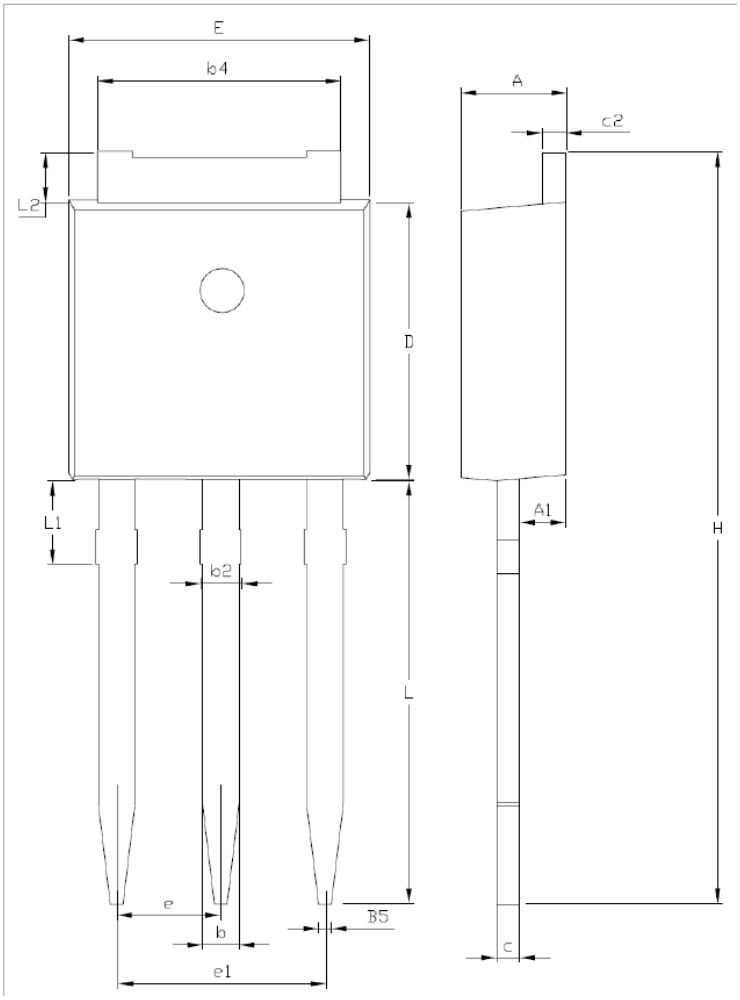


Table 5. **IPAK package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.086		0.094
A1	0.90		1.10			0.035
b	0.64		0.90	0.025		0.035
b2			0.95			0.037
b4	5.20		5.43			
B5		0.30			0.012	
c	0.45		0.60			
c2	0.46		0.60			
D	6		6.20			
E	6.40		6.65	0.252		0.262
e		2.28			0.090	
e1	4.40		4.60	0.173		0.181
H		16.10			0.634	
L	9		9.60	0.354		0.377
L1	0.8		1.20	0.031		0.047
L2		0.80	1.25		0.031	0.049
V1		10°			10°	

3 Ordering information

Figure 13. **Ordering information scheme**

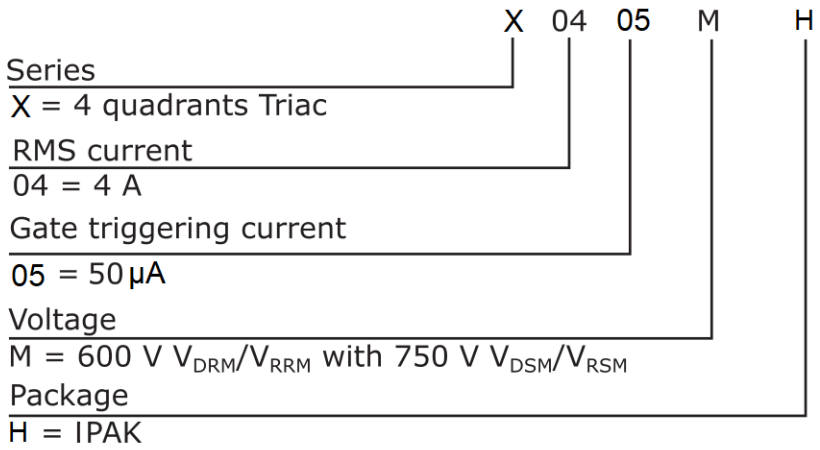


Table 6. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
X0405MH	X0405MH	IPAK	0.31 g	75	Tube

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
06-Sep-2022	1	Initial release.
10-Dec-2024	2	Updated Section IPAK package silhouette.

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