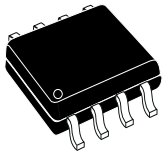
VNL5300S5-E

OMNIFET III
fully protected low-side driver

Datasheet - production data



SO-8

Features

Type	V_{clamp}	$R_{DS(on)}$	I_D
VNL5300S5-E	41 V	300 mΩ	2 A

- AEC-Q100 qualified
- Drain current: 2 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- Compliant with European directive 2002/95/EC
- Open drain status output

Description

The VNL5300S5-E is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery.

Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the device in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

Table 1. Devices summary

Package	Order codes (tape and reel)
SO-8	VNL5300S5TR-E

Contents

List of tables

List of figures

1 Block diagrams and pins configurations

Figure 1. Block diagram

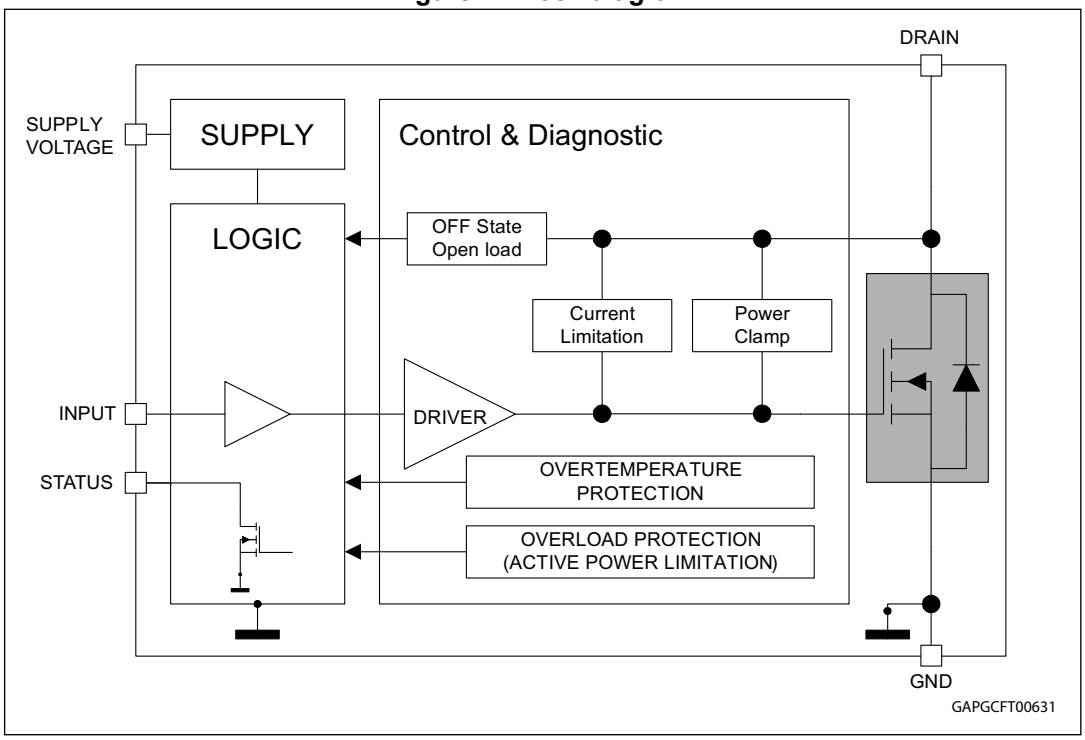


Table 2. Pin function

Name	Function
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. It Controls output switch state
DRAIN	PowerMOS drain
SOURCE	PowerMOS source and ground reference for the control section
SUPPLY VOLTAGE	Supply voltage connected to the signal part (5 V)
STATUS	Open drain digital diagnostic pin

Figure 2. Current and voltage conventions

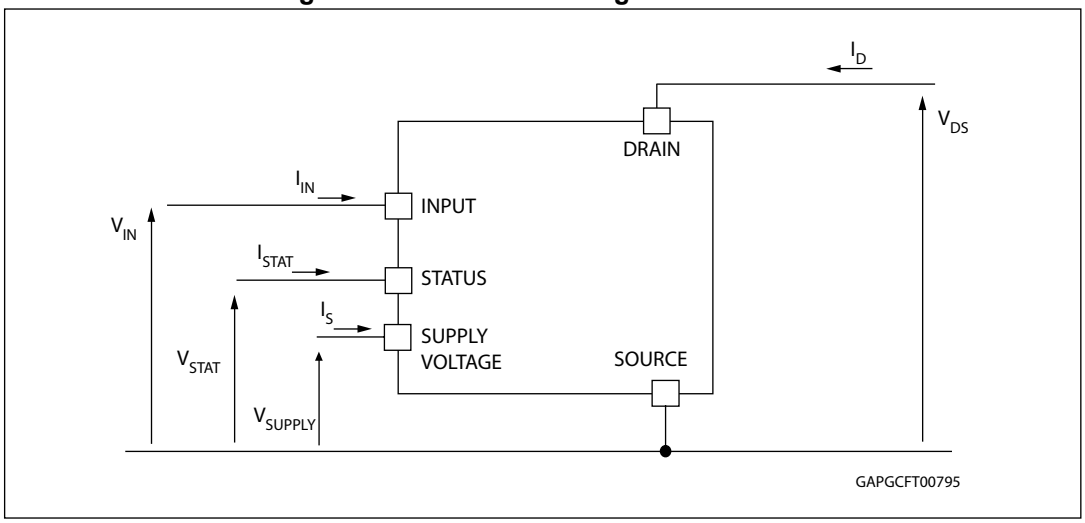
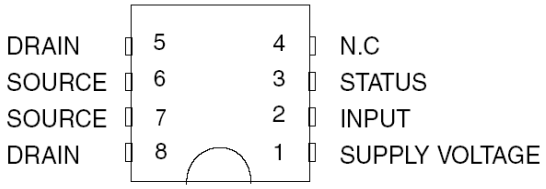


Figure 3. Configuration diagrams (top view)



SO-8

Table 3. Suggested connections for unused and N.C. pins

Connection / pin	STATUS	N.C.	INPUT
Floating	X(1)	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

1. X: do not care.

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 4* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{IN} = 0 V)	Internally clamped	V
I_D	DC drain current	Internally limited	A
$-I_D$	Reverse DC drain current	6	A
I_S	DC supply current	-1 to 10	mA
I_{IN}	DC input current	-1 to 10	mA
I_{STAT}	DC status current	-1 to 10	mA
V_{ESD1}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF) – DRAIN – SUPPLY, INPUT, STATUS	 5000 4000	V
V_{ESD2}	Electrostatic discharge on output pin only (R = 330 Ω, C = 150 pF)	2000	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C
E_{AS}	Single pulse avalanche energy (L = 19 mH, T_j = 150 °C, R_L = 0, I_{OUT} = I_{limL})	26	mJ

2.2 Thermal resistance data

Table 5. Thermal resistance

Symbol	Parameter	Typ.	Unit
$R_{thJ\text{-}Lead}$	Junction to lead	27.5(1)	°C/W
$\Psi_{J\text{-}Top}$	Thermal characterization parameter Junction to top	8(2)	°C/W
$R_{thJ\text{-}Amb}$	Junction to ambient on PCB 2 layers	See *Figure 9* (3)	°C/W
	Junction to ambient on PCB 4 layers	53.8	°C/W

1. T_{Lead} temperature measured with a thermocouple soldered on pin 8 according to Jedec JESD51-8.
2. T_{Top} temperature measured at the top center of the package using an infrared thermal camera according to Jedec HESD51-12.
3. Measured in still air condition according to Jedec JESD51-1, JESD51-2.

2.3 Electrical characteristics

Values specified in this section are for $V_{supply} = V_{IN}$ = 4.5 V to 5.5 V, -40°C < T_j < 150°C; unless otherwise stated.

Table 6. PowerMOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{supply}	Operating supply voltage	-	3.5	5	5.5	V
R_{ON}	ON-state resistance	I_D = 0.8 A; T_j = 25 °C, $V_{supply} = V_{IN}$ = 4.5 V		300		mΩ
		I_D = 0.8 A; T_j = 150°C, $V_{supply} = V_{IN}$ = 4.5 V			600	
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 0.8 A	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36			V
I_{DSS}	OFF-state output current	V_{IN} = 0 V; V_{DS} = 13 V; T_j = 25°C	0		3	µA
		V_{IN} = 0 V; V_{DS} = 13 V; T_j = 125°C	0		5	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	I_D = 0.8 A; V_{IN} = 0 V	—	0.8	—	V

Table 8. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation, V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation, V_{STAT} = 5 V			100	pF
V_{STCL}	Status clamp voltage	I_{STAT} = 1 mA	5.5		7	V
		I_{STAT} = -1 mA		-0.7		

Table 9. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.13			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		

Table 10. Openload detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Openload OFF-state voltage detection threshold	V_{IN} = 0 V	0.6	1.2	1.7	V
$t_{d(oloff)}$	Delay between INPUT falling edge and STATUS falling edge in openload condition	I_{OUT} = 0 A	45	425	1100	µs

Table 11. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Supply current	OFF-state; T_j = 25°C; V_{IN} = V_{DRAIN} = 0 V;		10	25	µA
		ON-state; V_{IN} = 5 V; V_{DS} = 0 V		25	65	
V_{SCL}	Supply clamp voltage	I_{SCL} = 1 mA	5.5		7	V
		I_{SCL} = -1 mA		-0.7		

Table 12. Switching characteristics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-on delay time	R_L = 16 Ω; V_{CC} = 13 V(2)	—	8	—	µs
$t_{d(OFF)}$	Turn-off delay time	R_L = 16 Ω; V_{CC} = 13 V(2)	—	12	—	µs
t_r	Rise time	R_L = 16 Ω; V_{CC} = 13 V(2)	—	11	—	µs
t_f	Fall time	R_L = 16 Ω; V_{CC} = 13 V(2)	—	7	—	µs
W_{ON}	Switching energy losses at turn-on	R_L = 16 Ω; V_{CC} = 13 V(2)	—	0.026	—	mJ
W_{OFF}	Switching energy losses at turn-off	R_L = 16 Ω; V_{CC} = 13 V(2)	—	0.016	—	mJ
Q_g	Total gate charge	V_{SUPPLY} = V_{IN} = 5 V	—	0.6	—	nC

1. See *Figure 5: Application schematic*
2. See *Figure 4: Switching characteristics*

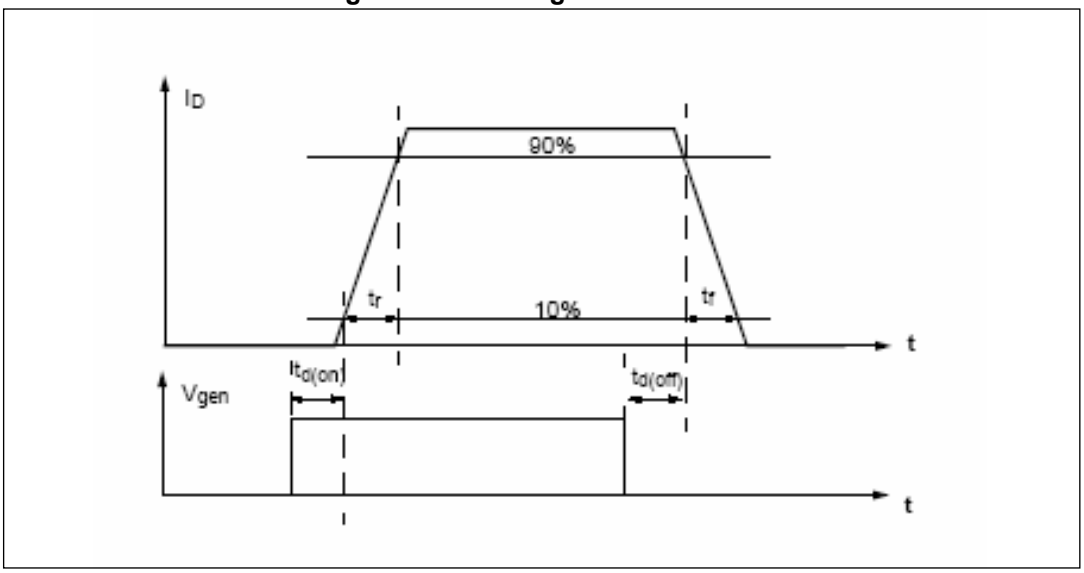
Table 13. Protection and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{DS} = 13 V; V_{supply} = V_{IN} = 5 V	2	2.8	3.8	A
I_{limL}	Short-circuit current during thermal cycling	V_{DS} = 13 V; $T_R < T_j < T_{TSD}$; V_{supply} = V_{IN} = 5 V		1.4		A
t_{dlimL}	Step response current limit	V_{DS} = 13 V; V_{input} = 5 V		7		µs
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C

Table 14. Truth table

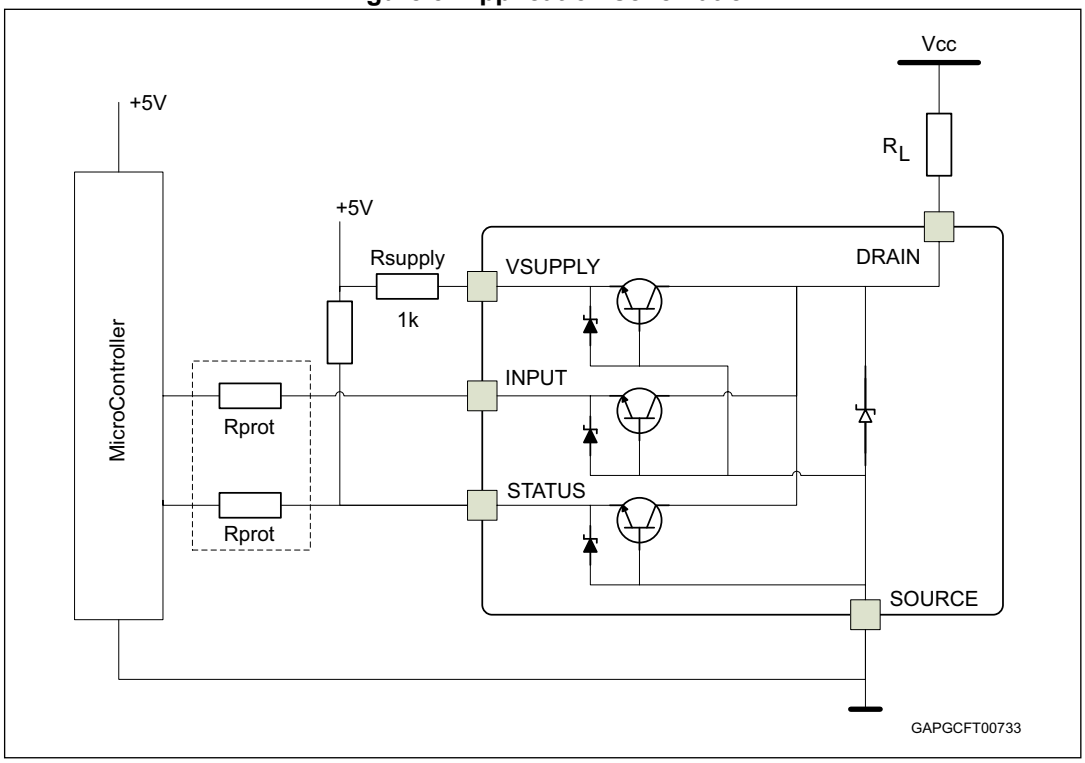
Conditions	INPUT	DRAIN	STATUS
Normal operation	L H	H L	H H
Current limitation	L H	H X	H H
Overtemperature	L H	H H	H L
Undervoltage	L H	H H	X X
Output voltage < V_{OL}	L H	L L	L H

Figure 4. Switching characteristics



3 Application information

Figure 5. Application schematic



3.1 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up[(a)]. The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1

$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH})}{I_{IH\ max}}$$

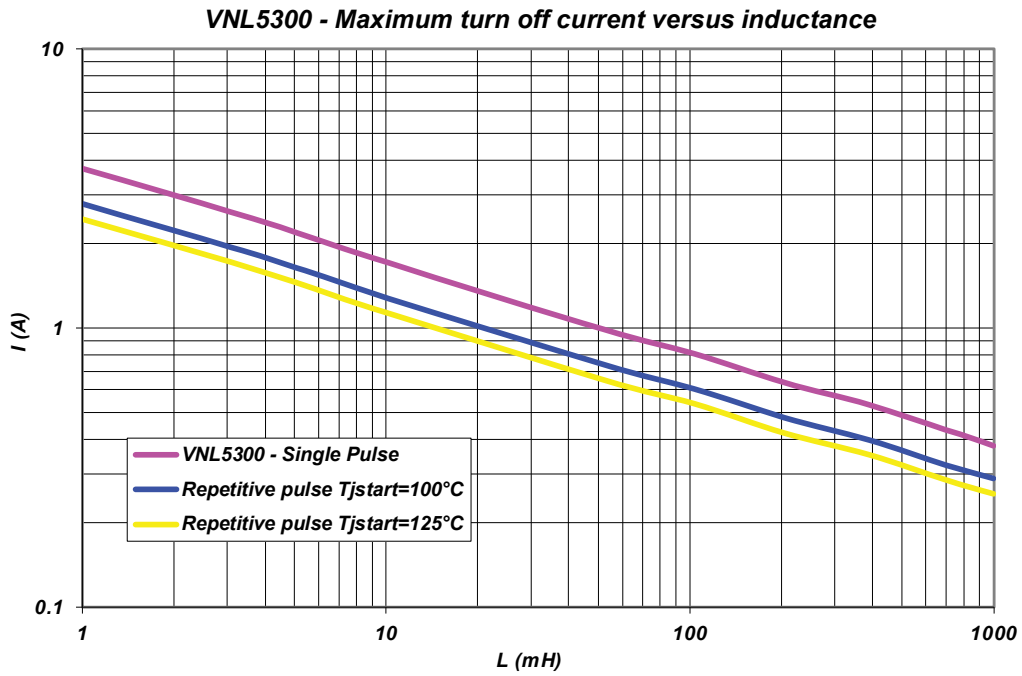
Let:

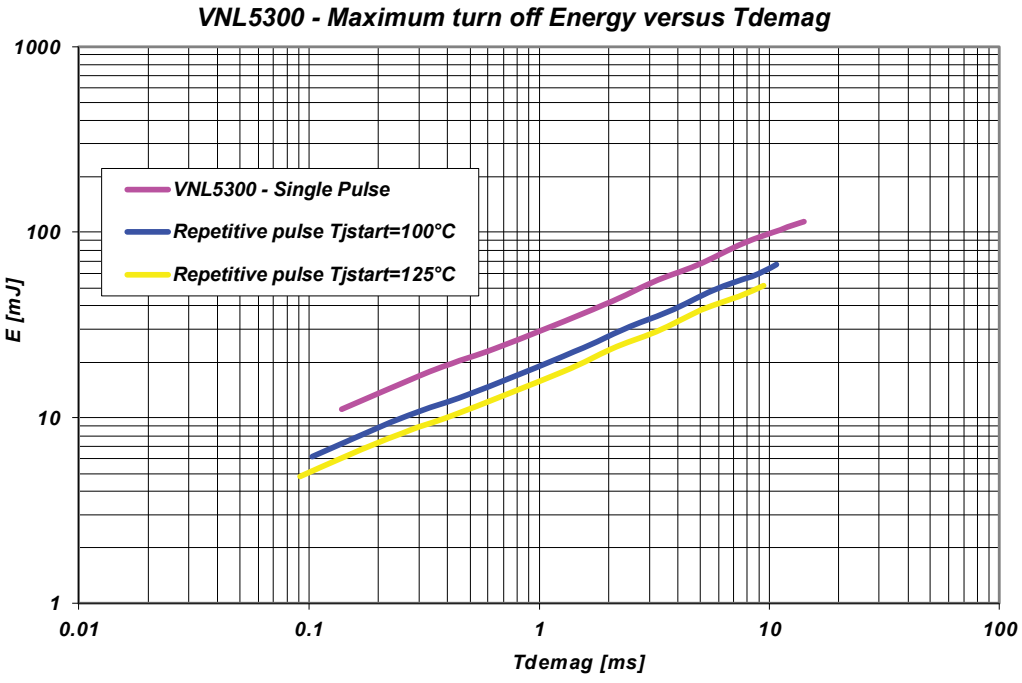
- $I_{latchup} \geq 20$ mA
- $V_{OH\mu C} \geq 4.5$ V
- $35\ \Omega \leq R_{prot} \leq 100\ K\Omega$

Then, the recommended value is $R_{prot} = 1\ K\Omega$

a. In case of negative transient on the drain pin.

Figure 6. Maximum demagnetization energy





GAPG1107131511CFT

1. Values are generated with $R_L = 0\Omega$.
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 SO-8 thermal PCB data

Figure 7. SO-8 PCB 2layers

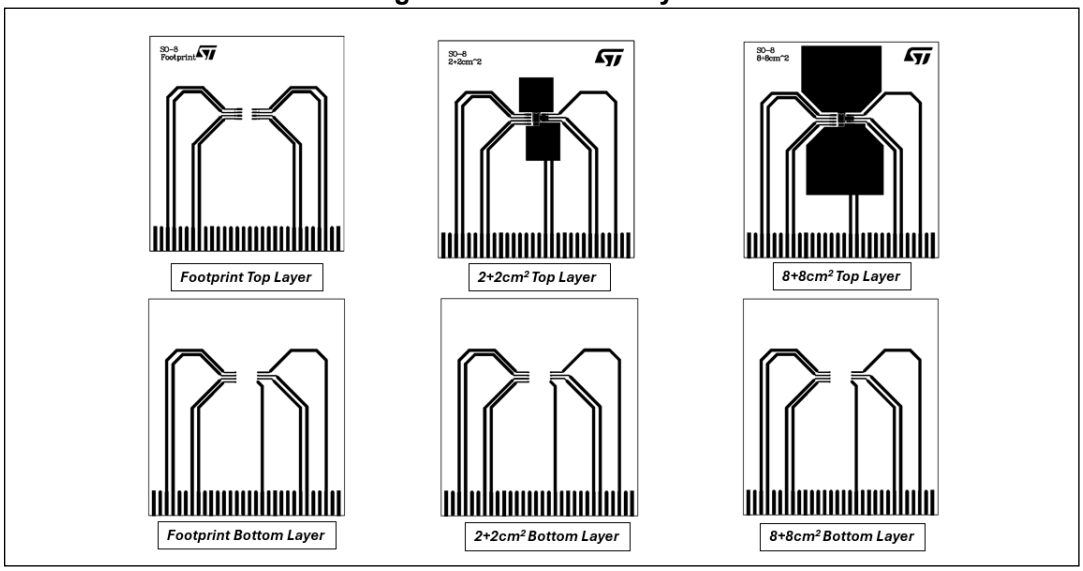


Figure 8. SO-8 PCB 4 layers

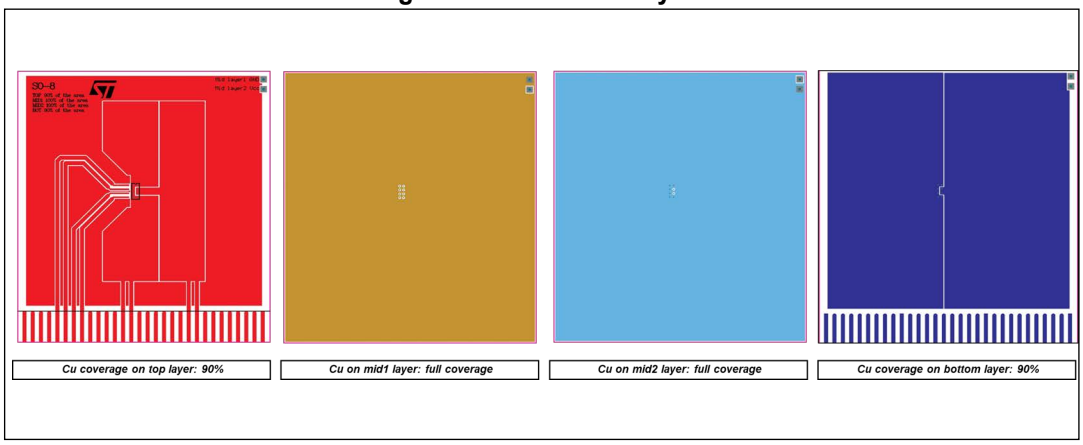


Table 15. 2-layer and 4-layer PCB characteristics

Dimension	Value
Board material	FR4
Board finish thickness	1.6 mm ± 10%
Board dimensions	77 x 86 mm
Outer layers CU thickness	70 µm
Inner layers CU thickness (4-layer PCB)	35 µm
Thermal vias separation	1.2 mm
Thermal via diameter	300 ± 80 µm
CU thickness on vias	25 µm

Figure 9. SO-8 $R_{thJ\text{-}Amb}$ vs. 2-layer PCB copper heatsink area

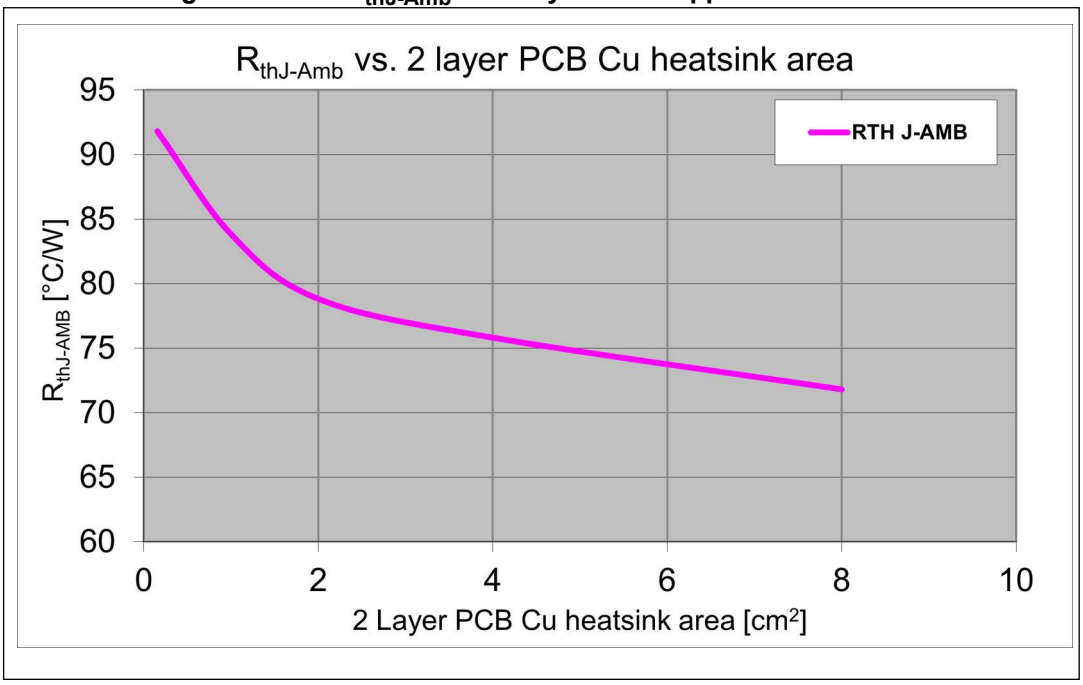


Figure 10. SO-8 thermal impedance junction ambient single pulse

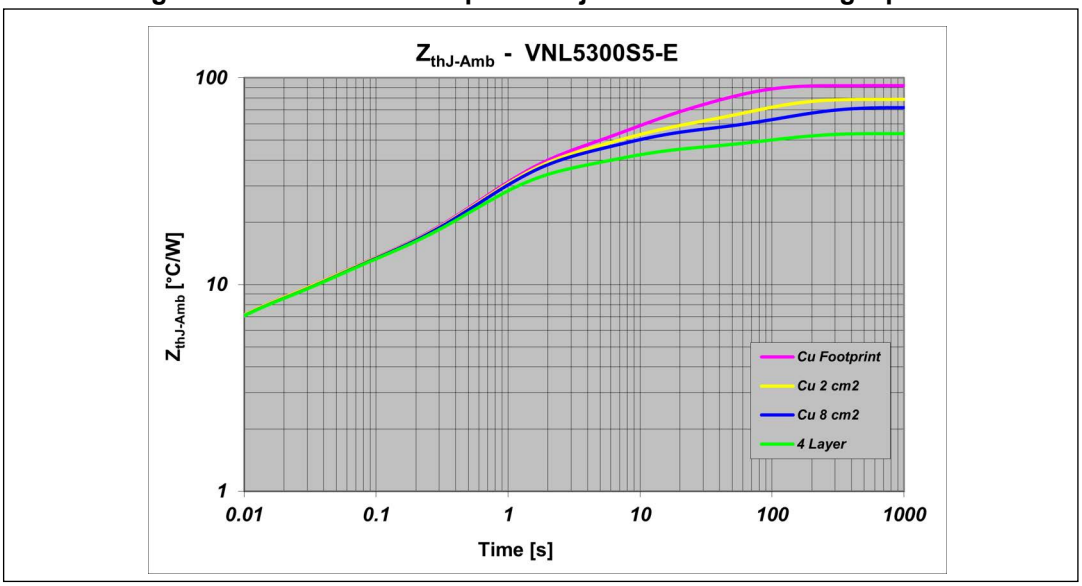
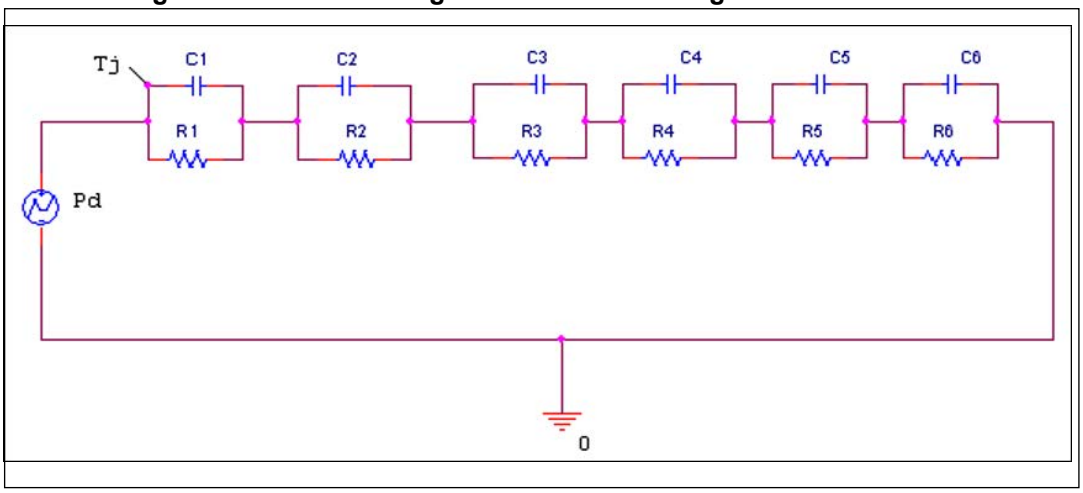


Figure 11. Thermal fitting model of an LSD single channel in SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. SO-8 thermal parameters

Thermal parameter	2-layer PCB Cu area			4-layer PCB
	FP	2 cm^2	8 cm^2	
R1 [°C/W]	1.7			
R2 [°C/W]	4.2			
R3 [°C/W]	4.6			
R4 [°C/W]	25	25	25	21
R5 [°C/W]	21	18	17	12
R6 [°C/W]	35	25	19	10
C1 [W.s/°C]	$0.2*10^{-3}$			
C2 [W.s/°C]	$1*10^{-3}$			
C3 [W.s/°C]	$8.2*10^{-3}$	$8.2*10^{-3}$	$8.7*10^{-3}$	$8.7*10^{-3}$
C4 [W.s/°C]	$35*10^{-3}$	$35*10^{-3}$	$35*10^{-3}$	$35*10^{-3}$
C5 [W.s/°C]	0.35	0.35	0.4	0.5
C6 [W.s/°C]	1.2	3	7	10

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SO-8 mechanical data

Figure 12. SO-8 package dimensions

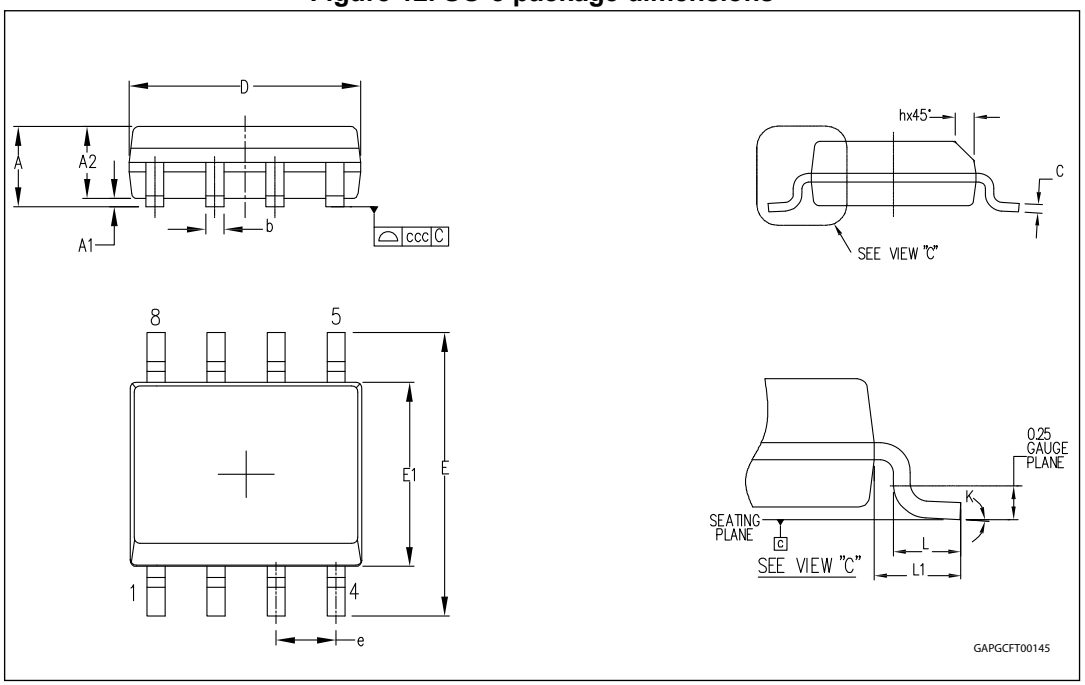


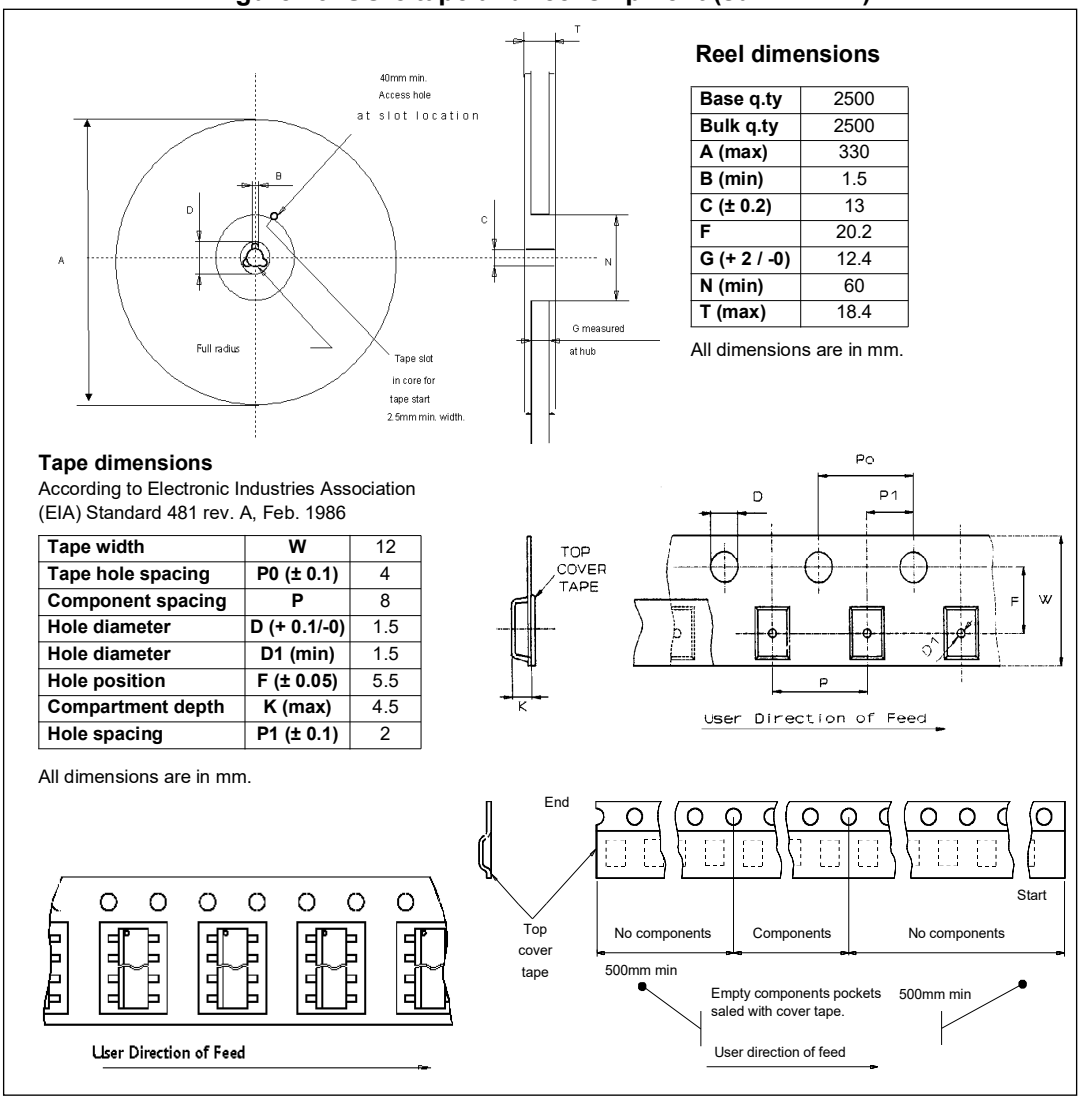
Table 17. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D(1)	4.80	4.90	5.00
E	5.80	6.00	6.20
E1(2)	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.3 SO-8 packing information

Figure 13. SO-8 tape and reel shipment (suffix “TR”)



6 Revision history

Table 18. Document revision history

Date	Revision	Changes
02-Jul-2012	1	Initial release.
23-May-2013	2	*Table 5: Thermal resistance*: – $R_{thj-amb}$: updated value *Table 6: PowerMOS section*: – R_{ON}: updated value *Table 11: Supply section*: – I_S: updated value *Table 12: Switching characteristics*: – $t_{d(ON)}$, $t_{d(OFF)}$, t_r, W_{ON}, W_{OFF}: updated values *Table 13: Protection and diagnostics*: – t_{dlimL}: updated value Updated *Figure 5: Application schematic* Updated *Section 3.1: MCU I/O protection* Updated *Chapter 4: Package and PC board thermal data*
18-Jul-2013	3	*Table 4: Absolute maximum ratings*: – $-I_D$: updated value – E_{AS}: updated parameter value *Table 12: Switching characteristics*: – $t_{d(ON)}$, t_r, W_{ON}, W_{OFF}: updated typical values Added *Figure 6: Maximum demagnetization energy*
18-Sep-2013	4	Updated disclaimer.
13-Dec-2013	5	*Table 6: PowerMOS section*: – R_{ON}: updated test conditions
12-Oct-2025	6	Updated *Table 1*: removed tube packing option Updated *Table 5*: revised thermal data Updated Figures and Tables in *Section 4*: - Changed *Figure 7: SO-8 PCB 2layers* - Added *Figure 8: SO-8 PCB 4 layers* - Added T*Table 15: 2-layer and 4-layer PCB characteristics* - Changed *Figure 9: SO-8 $R_{thJ-Amb}$ vs. 2-layer PCB copper heatsink area* - Changed *Figure 10: SO-8 thermal impedance junction ambient single pulse* - Removed equation 2 - Changed *Table 16: SO-8 thermal parameters*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com